LMZ31710, LMZ31707 and LMZ31704 Simple Switcher® Power Module Evaluation Module

The LMZ31710EVM-001, LMZ31707EVM-002 and LMZ31704EVM-003 evaluation modules are designed as an easy-to-use platform that facilitates an extensive evaluation of the features and performance of the Simple Switcher® power module. This guide provides information on the correct usage of the EVM and an explanation of the numerous test points on the board.

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1 Description

This EVM features the LMZ31710 (10-A), LMZ31707 (7-A), or LMZ31704 (4-A), synchronous buck power module configured for operation with typical 5-V and 12-V input bus applications. The output voltage can be set to one of seven popular values by using a configuration jumper. In similar fashion, the switching frequency can be set to one of seven values with a jumper. The full output current rating of the device can be supplied by the EVM. Input and output capacitors are included on the board to accommodate the entire range of input and output voltages. Monitoring test points are provided to allow measurement of efficiency, power dissipation, input ripple, output ripple, line and load regulation, and transient response. Control test points are provided for use of the PWRGD, Inhibit/UVLO, synchronization, and slow-start/tracking features of the LMZ317xx device. The EVM uses a recommended PCB layout that maximizes thermal performance and minimizes output ripple and noise.

2 Getting Started

Figure 1 highlights the user interface items associated with the EVM. The polarized *PVin Power* terminal block (TB1) is used for connection to the host input supply and the polarized *Vout Power* terminal block (TB2) is used for connection to the load. These terminal blocks can accept up to 16-AWG wire. The polarized Vbias terminal block (TB3) is used along with the Vin select jumper (P1) when optional split power supply operation is desired. Refer to the LMZ317xx datasheet for further information on split power supply operation.

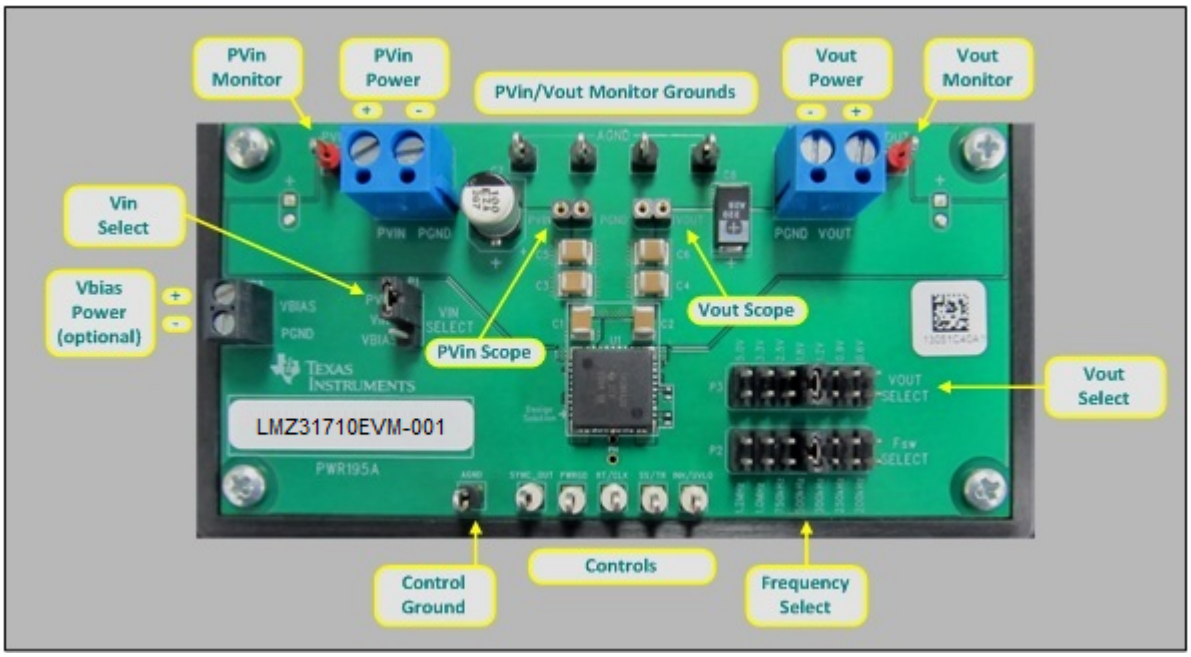

Figure 1. LMZ317xxEVM User Interface

The *PVin Monitor* and *Vout Monitor* test points located near the power terminal blocks are intended to be used as voltage monitoring points where voltmeters can be connected to measure PVin and Vout. The voltmeter references should be connected to any of the four *PVin/Vout Monitor Grounds* test points located between the power terminal blocks. Do *not* use these PVin and Vout monitoring test points as the input supply or output load connection points. The PCB traces connecting to these test points are not designed to support high currents.

The PVin Scope and Vout Scope test points can be used to monitor PVin and Vout waveforms with an oscilloscope. These test points are intended for use with un-hooded scope probes outfitted with a low-inductance ground lead (ground spring) mounted to the scope barrel. The two sockets of each test point are on 0.1 in centers. The scope probe tip should be connected to the socket labeled PVin or Vout, and the scope ground lead should be connected to the socket labeled PGND.

The Controls test points located directly below the device are made available to test the features of the device. Any external connections made to these test points should be referenced to the Control Ground test point located along the bottom of the EVM. Refer to the Test Points Descriptions section of this guide for more information on the individual control test points.

The *Vout Select* jumper (P3) and *Fsw Select* jumper (P2) are provided for selecting the desired output voltage and appropriate switching frequency. Before applying power to the EVM, ensure that the jumpers are present and properly positioned for the intended output voltage. Refer to Table 1 for the recommended jumper settings. Always remove input power before changing the jumper settings.

Once the jumper settings have been confirmed, configure the host input supply to apply the appropriate bus voltage listed in Table 1 and confirm that the selected output voltage is obtained.

Table 1. Output Voltage and Switching Frequency Jumper Settings

Vout Select	Fsw Select	PVin Bus Voltage
5.0 V	1 MHz	12 V
3.3 V	750 kHz	5 V or 12 V
2.5 V	750 kHz	5 V or 12 V
1.8 V	500 kHz	5 V or 12 V
1.2 V	300 kHz	5 V or 12 V
0.9 V	250 kHz	5 V or 12 V
0.6 V	200 kHz	5 V or 12 V

3 Test Point Descriptions

Twelve wire-loop test points and two scope probe test points have been provided as convenient connection points for digital voltmeters (DVM) or oscilloscope probes to aid in the evaluation of the device. A description of each test point follows:

Table 2. Test Point Descriptions(1)

PVIN	Input voltage monitor. Connect DVM to this point for measuring efficiency.
VOUT	Output voltage monitor. Connect DVM to this point for measuring efficiency, line regulation, and load regulation.
AGND	Input and output voltage monitor grounds (located between terminal blocks). Reference the above DVMs to any of these four analog ground points.
PVIN Scope (J1)	Input voltage scope monitor. Connect an oscilloscope to this set of points to measure input ripple voltage.
VOUT Scope (J2)	Output voltage scope monitor. Connect an oscilloscope to this set of points to measure output ripple voltage and transient response.
PWRGD	Monitors the power good signal of the device. This is an open drain signal that requires an external pullup resistor if monitoring is desired. A 10-kΩ to 100-kΩ pullup resistor is recommended. PWRGD is high if the output voltage is within 92% to 107% of its nominal value.
INH/UVLO	Connect this point to control ground to inhibit the device. Allow this point to float to enable the device. An external resistor divider can be connected between this point, control ground, and Vin to adjust the UVLO of the device.
RT/CLK	Connects to the RT/CLK pin of the device. An external clock signal can be applied to this point to synchronize the device to an appropriate frequency.
SS/TR	Connects to the internal slow-start capacitor of the device. An external capacitor can be connected from this point to control ground to increase the slow-start time of the device. This point can also be used as for tracking applications.
SYNC_OUT	This output provides a clock signal that is 180º out of phase with the PH node of the device and can be used to synchronize other devices.
AGND	Control ground (located along bottom of EVM). Reference any signals associated with the control test points to this analog ground point.

(1) Refer to the LMZ317xx datasheet for absolute maximum ratings associated with above features.

4 Operation Notes

In order to operate the EVM using a single power supply, the Vin Select jumper (P1) must be in the default PVIN-VIN position shown in Figure 1. In this position, the PVin and Vin pins of the device are connected together. The UVLO threshold of the EVM is approximately 4 V with 0.15 V of hysteresis. The input voltage must be above the UVLO threshold in order for the device to startup. After startup, the minimum input voltage to the device must be at least 4.5 V or (Vout + 0.7 V), whichever is greater. The maximum operating input voltage for the device is 17 V. Refer to the LMZ317xx datasheet for further information on the input voltage range, UVLO operation, and optional split power supply operation for operating with PVin as low as 2.95 V when using an external Vbias supply.

After application of the proper input voltage, the output voltage of the device will ramp to its final value in approximately 1.2 ms. If desired, this soft-start time can be increased by adding a capacitor to the SS/TR test point as described above. Refer to the LMZ317xx datasheet for further information on adjusting the soft-start time.

Table 1 lists the recommended switching frequencies for each of the Vout selections. These recommendations cover operation over a wide range of input voltage and output load conditions. Several factors such as duty cycle, minimum on-time, minimum off-time, and current limit influence selection of the appropriate switching frequency. In some applications, other switching frequencies might be used for particular output voltages, depending on the above factors. Refer to the LMZ317xx datasheet for further information on switching frequency selection, including synchronization.

The EVM includes input and output capacitors to accommodate the entire range of input and output voltage conditions. The actual capacitance required will depend on the input and output voltage conditions of the particular application, along with the desired transient response. In most cases, the required output capacitance will be less than that supplied on the EVM. Refer to the LMZ317xx datasheet for further information on the minimum required I/O capacitance and transient response.

The LMZ317xx operates in pulse skip mode at light currents to improve light load efficiency (LLE mode). At output voltages of less than 1.5 V, the pulse skipping may cause the output to rise when there is no load to discharge the energy. A minimum load of 600 µA or less, depending on Vout, is required to keep the output voltage within regulation. For the worst case condition of Vout = 0.6 V, a 1-kΩ resistor would provide a required minimum load of 600 µA. If the application requires an additional load to meet the minimum load requirement, the additional load could be connected external to the EVM or installed in the R16 position on the underside of the EVM. Refer to the LMZ317xx datasheet for further information on LLE mode and determining the required minimum load.

5 Performance Data

Figure 2 through Figure 9 demonstrate the LMZ31710EVM performance with Vout = 1.8 V and Fsw = 500 kHz. For data regarding the LMZ31707 and the LMZ31704 please see the product data sheet.

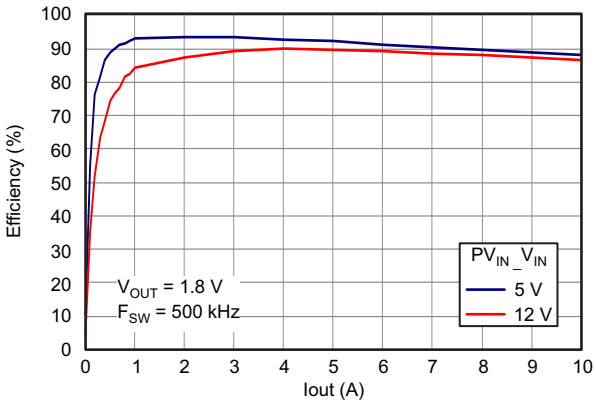

Figure 2. LMZ31710EVM Efficiency

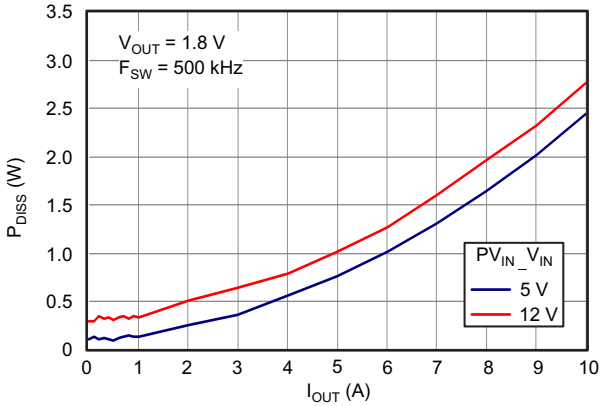

Figure 3. LMZ31710EVM Power Dissipation

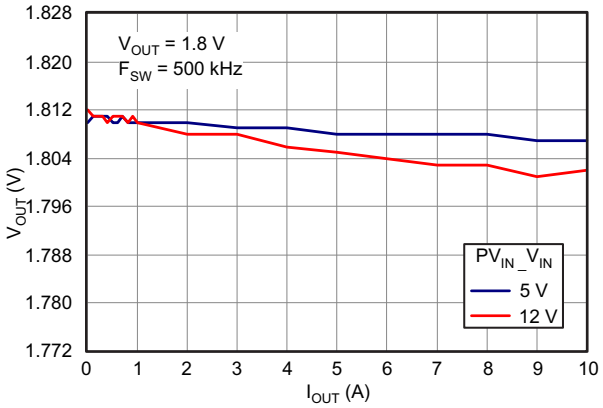

Figure 4. LMZ31710EVM Load Regulation

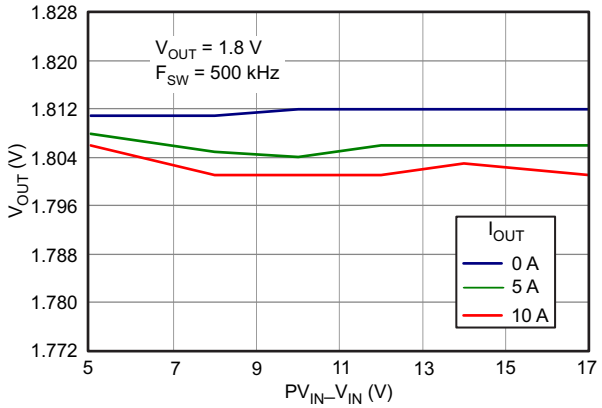

Figure 5. LMZ31710EVM Line Regulation

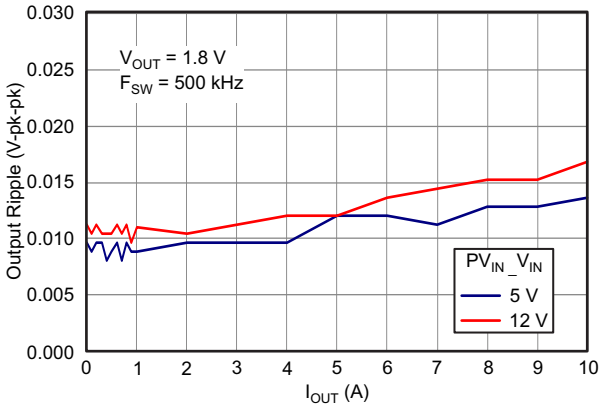

Figure 6. LMZ31710EVM Output Ripple

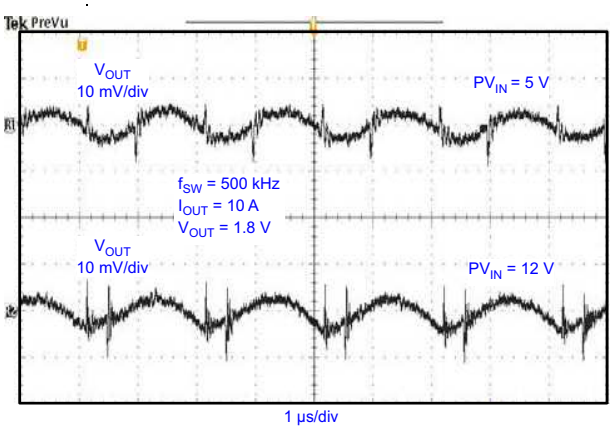

Figure 7. LMZ31710EVM Output Ripple Waveforms

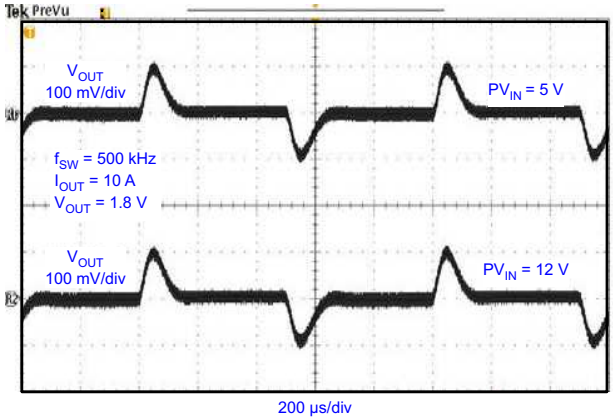

Figure 8. LMZ31710EVM Transient Response Waveforms

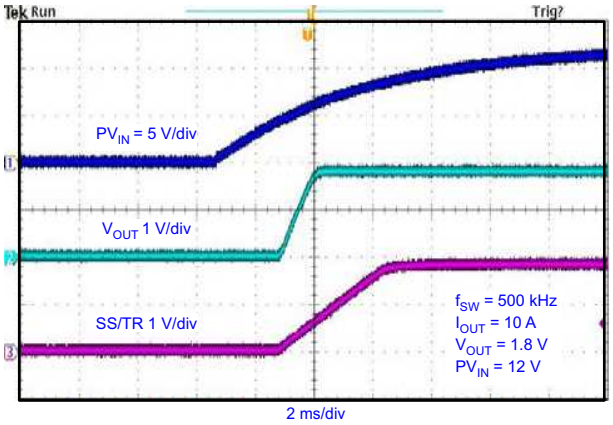

Figure 9. LMZ31710EVM Startup Waveforms

6 Schematic

Figure 10 is the schematic for this EVM.

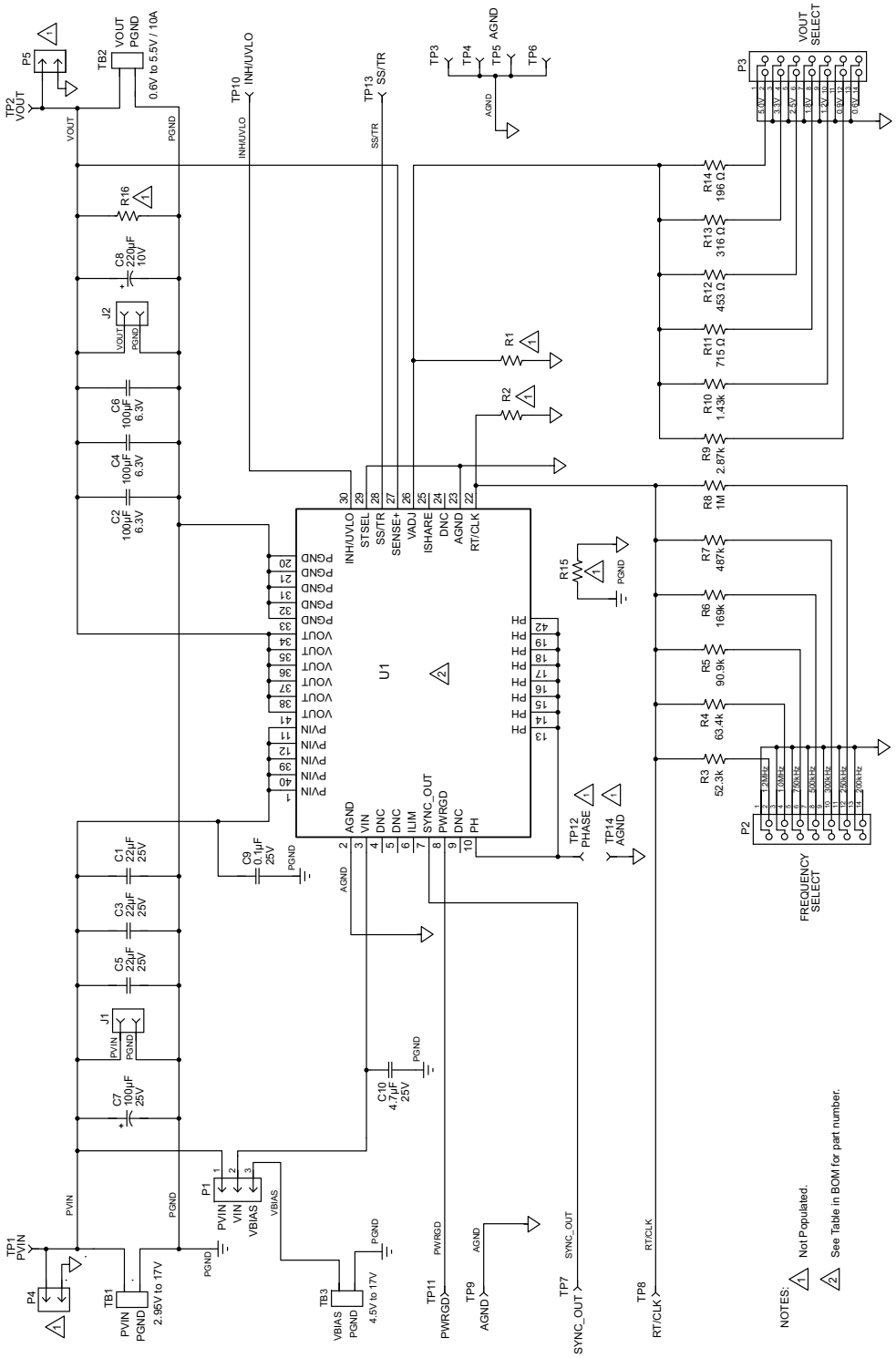

Figure 10. LMZ317xxEVM Schematic

7 Bill of Materials

Table 3 is the BOM for the EVM.

Table 3. LMZ317xxEVM Bill of Materials

-001	-002	-003	RefDes	Value	Description	Size	Part Number	Mfg
3	3	3	C1, C3, C5	22uF	Capacitor, Ceramic, 25V, X5R, 10%	1210	GRM32ER61E226K	Murata
3	3	3	C2, C4, C6	100uF	Capacitor, Ceramic, 6.3V, X5R, 20%	1210	GRM32ER60J107M	Murata
1	1	1	C7	100uF	Capacitor, Polymer, 25V, 20%	6.3mm	EEH-ZA1E101XP	Panasonic
1	1	1	C8	220uF	Capacitor, Polymer, 10V, 20%	D3L	10TPE220ML	Sanyo
1	1	1	C9	0.1uF	Capacitor, Ceramic, 25V, X7R, 10%	0805	Std	Std
1	1	1	C10	4.7uF	Capacitor, Ceramic, 25V, X5R, 10%	0805	GRM21BR61E475K	Murata
2	2	2	J1,J2	310-43-102-41-001000	Header, Female, 1x2 socket, 0.1" centers	0.100 inch x 1 x 2	310-43-102-41-001000	Mill-Max
1	1	1	P1	PEC03SAAN	Header, Male, 1x3 pin, 0.1" centers	0.100 inch x 1 x 3	PEC03SAAN	Sullins
2	2	2	P2, P3	PEC07DAAN	Header, Male, 2x7 pin, 0.1" centers	0.100 inch x 2 x 7	PEC07DAAN	Sullins
0	0	0	P4, P5	PEC02SAAN (not populated)	Header, Male, 1x2 pin, 0.1" centers	0.100 inch x 1 x 2	PEC02SAAN	Sullins
0	0	0	R1	optional (user-defined)	Resistor, Chip, 1/16W, 1%	0402	Std	Std
0	0	0	R2	optional (user-defined)	Resistor, Chip, 1/16W, 1%	0402	Std	Std
1	1	1	R3	52.3k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	1	R4	63.4k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	1	R5	90.9k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	1	R6	169k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	1	R7	487k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	1	R8	1M	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	1	R9	2.87k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	1	R10	1.43k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	1	R11	715	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	1	R12	453	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	1	R13	316	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	1	1	R14	196	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	0	0	R15	0 (not populated)	Resistor, Chip, 1/10W, 1%	0805	Std	Std
0	0	0	R16	1k (not populated)	Resistor, Chip, 1/10W, 1%	0805	Std	Std
2	2	2	TB1,TB2	ED120/2DS	Terminal Block, 2-pin, 15A, 5.1mm	0.40 x 0.35 inch	ED120/2DS	OST
1	1	1	TB3	ED555/2DS	Terminal Block, 2-pin, 6A, 3.5mm	0.27 x 0.25 inch	ED555/2DS	OST
2	2	2	TP1,TP2	5010	Test Point, Red, Wire Loop, Thru Hole	0.125 x 0.125 inch	5010	Keystone
5	5	5	TP3, TP4, TP5, TP6, TP9	5011	Test Point, Black, Wire Loop, Thru Hole	0.125 x 0.125 inch	5011	Keystone
5	5	5	TP7, TP8, TP10, TP11, TP13	5012	Test Point, White, Wire Loop, Thru Hole	0.125 x 0.125 inch	5012	Keystone
0	0	0	TP12, TP14	---	Test Point, Internal	---	---	---
1	0	0	U1	LMZ31710RVQ	Sync Buck, 2.95V to 17V Input, 10A Output	10x10x4.3 mm QFN	LMZ31710RVQ	TI
0	1	0	U1	LMZ31707RVQ	Sync Buck, 2.95V to 17V Input, 7A Output	10x10x4.3 mm QFN	LMZ31707RVQ	TI
0	0	1	U1	LMZ31704RVQ	Sync Buck, 2.95V to 17V Input, 4A Output	10x10x4.3 mm QFN	LMZ31704RVQ	TI
3	3	3	---	---	Shunt, Black	0.100 inch x 1 x 2	929950-00	3M
4	4	4	---	---	Bumpon, Hemisphere, Black	0.44 Dia. x 0.20 inch	SJ-5003	3M

Table 3. LMZ317xxEVM Bill of Materials (continued)

-001	-002	-003	RefDes	Value	Description	Size	Part Number	Mfg
1	1	1	---	---	PCB, 2" x 4" x 0.062"	2 x 4 x 0.062 inch	PWR195	Any
1	1	1	---	---	Label	1.25 x 0.25 inch	THT-13-457-10	Brady

8 PCB Layout

Figure 11 through Figure 16 show the PCB layouts of the EVM.

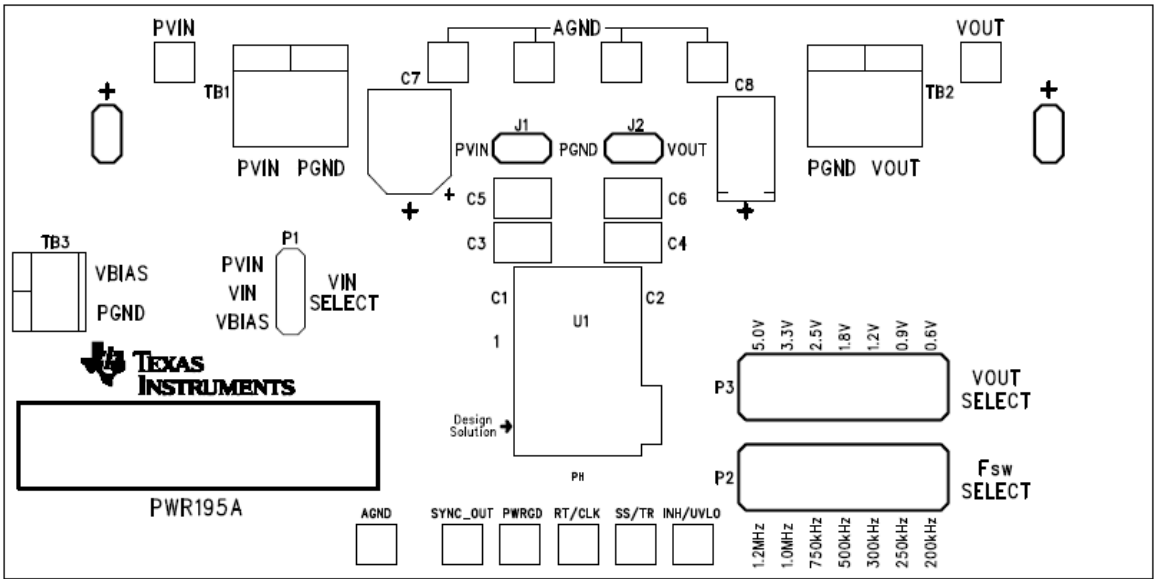

Figure 11. LMZ317xxEVM Topside Component Layout

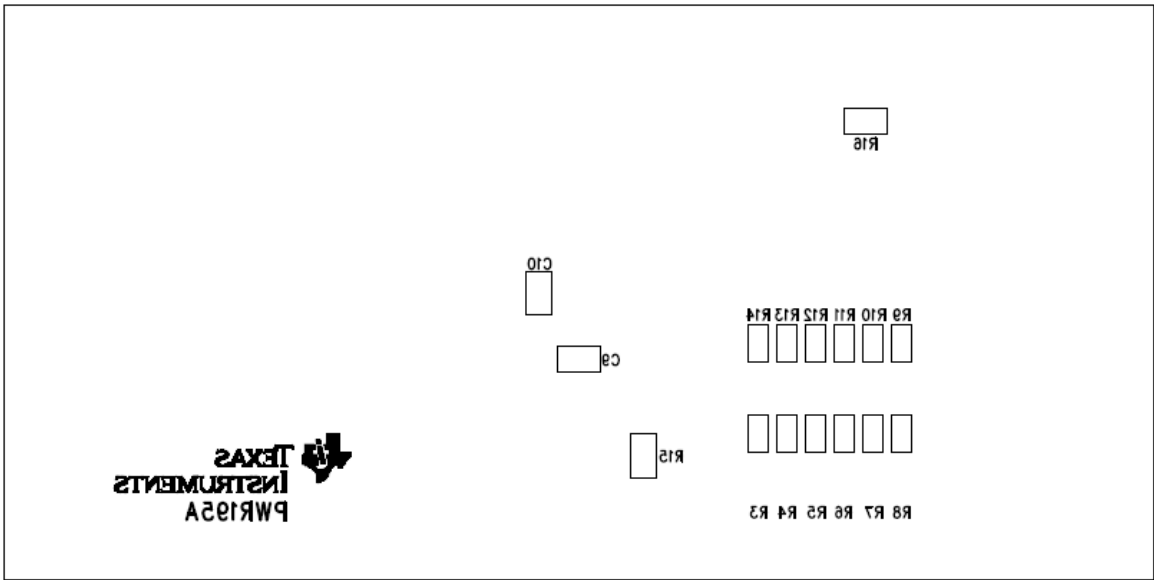

Figure 12. LMZ317xxEVM Bottom-Side Component Layout

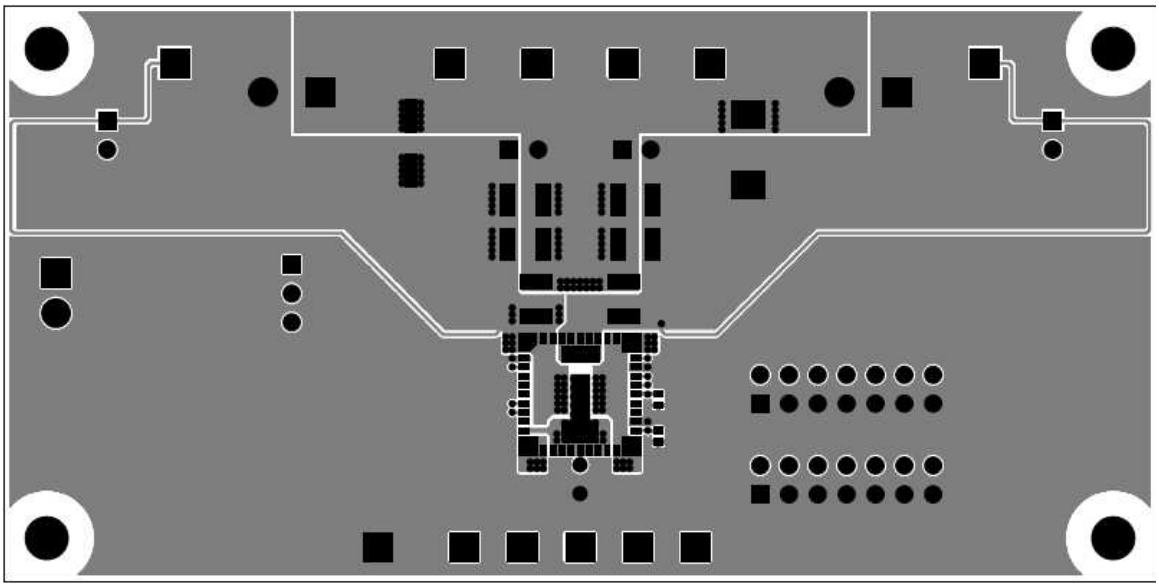

Figure 13. LMZ317xxEVM Layer 1 Copper

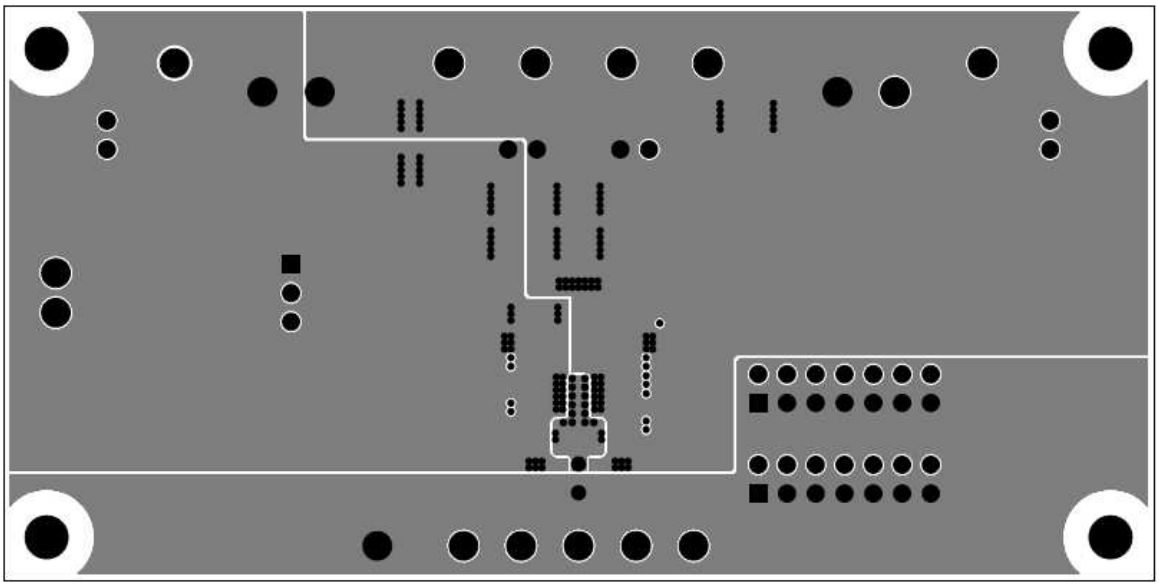

Figure 14. LMZ317xxEVM Layer 2 Copper

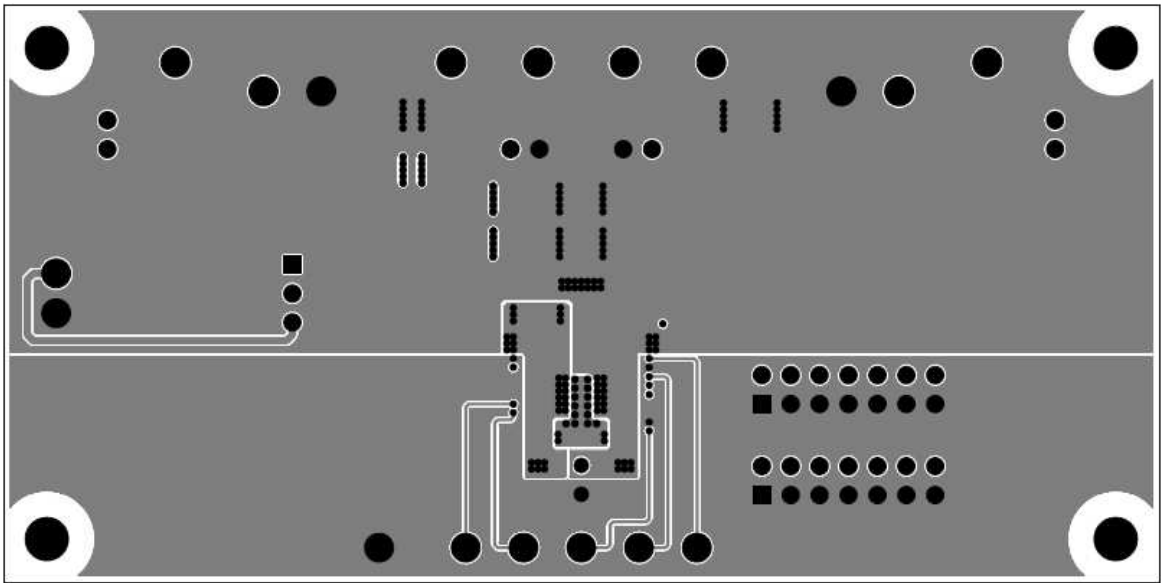

Figure 15. LMZ317xxEVM Layer 3 Copper

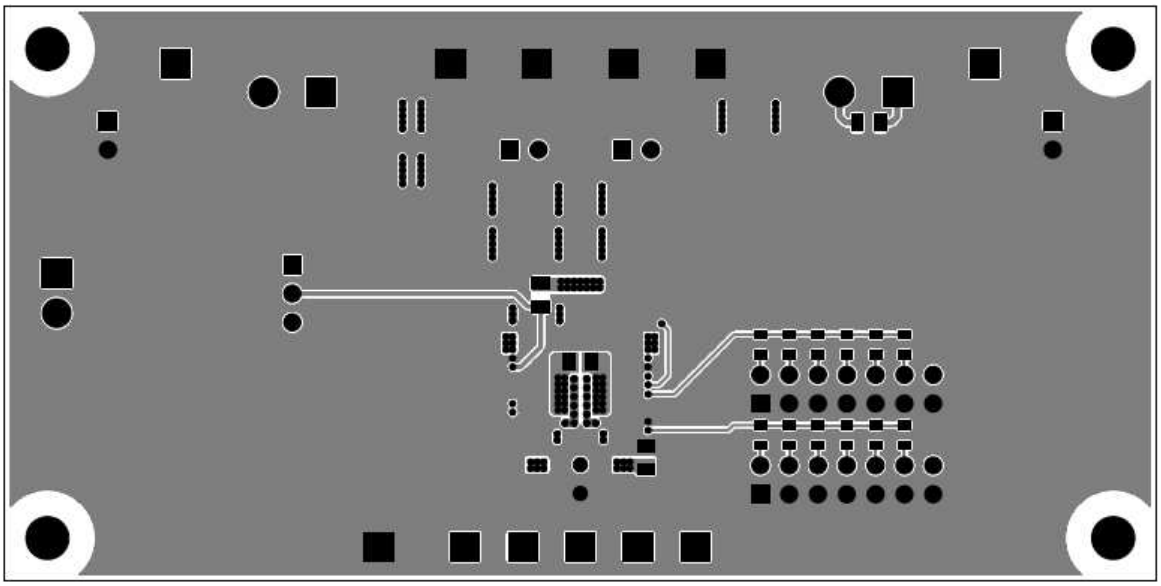

Figure 16. LMZ317xxEVM Layer 4 Copper

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