SM72480 SolarMagic 1.6V, WSON-6 Factory Preset Temperature Switch and Temperature Sensor

Check for Samples: SM72480

FEATURES

- **Renewable Energy Grade**
- **Low 1.6V Operation**
- **Latching Function: Device Can Latch the Over Temperature Condition**
- **Push-pull and Open-Drain Temperature Switch Outputs**
- **Very Linear Analog V_{TEMP} Temperature Sensor Output**
- **V_{TEMP} Output Short-circuit Protected**
- **2.2 mm by 2.5 mm (typ) WSON-6 Package**
- **Excellent Power Supply Noise Rejection**

APPLICATIONS

- **PV Power Optimizers**
- **Wireless Transceivers**
- **Battery Management**
- **Automotive**
- **Disk Drives**

KEY SPECIFICATIONS

- **Supply Voltage 1.6V to 5.5V**
- **Supply Current 8 μA (typ)**
- **Accuracy, Trip Point Temperature 0°C to 150°C ±2.2°C**
- **Accuracy, VTEMP 0°C to 150°C ±2.3°C**
- **VTEMP Output Drive ±100 μA**
- **Operating Temperature −50°C to 150°C**
- **Hysteresis Temperature 4.5°C to 5.5°C**

DESCRIPTION

The SM72480 is a low-voltage, precision, dual-output, low-power temperature switch and temperature sensor. The temperature trip point (T_{TRIP}) is set at the factory to be 120°C. Built-in temperature hysteresis (T_{HYST}) keeps the output stable in an environment of temperature instability.

In normal operation the SM72480 temperature switch outputs assert when the die temperature exceeds T_{TRIP}. The temperature switch outputs will reset when the temperature falls below a temperature equal to (T_{TRIP} − T_{HYST}). The OVERTEMP digital output, is active-high with a push-pull structure, while the $\overline{\text{OVERTEMP}}$ digital output, is active-low with an open-drain structure.

The analog output, V_{TEMP}, delivers an analog output voltage with Negative Temperature Coefficient — NTC.

Driving the TRIP TEST input high: (1) causes the digital outputs to be asserted for in-situ verification and, (2) causes the threshold voltage to appear at the V_{TEMP} output pin, which could be used to verify the temperature trip point.

The SM72480's low minimum supply voltage makes it ideal for 1.8 volt system designs. Its wide operating range, low supply current , and excellent accuracy provide a temperature switch solution for a wide range of commercial and industrial applications.

Connection Diagram

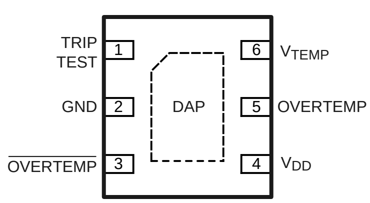
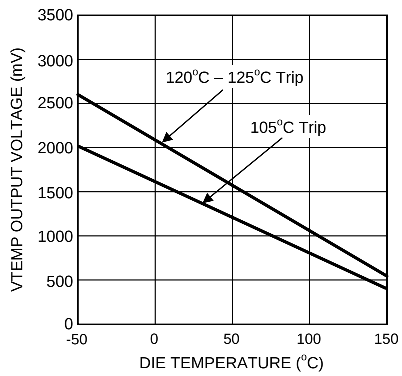


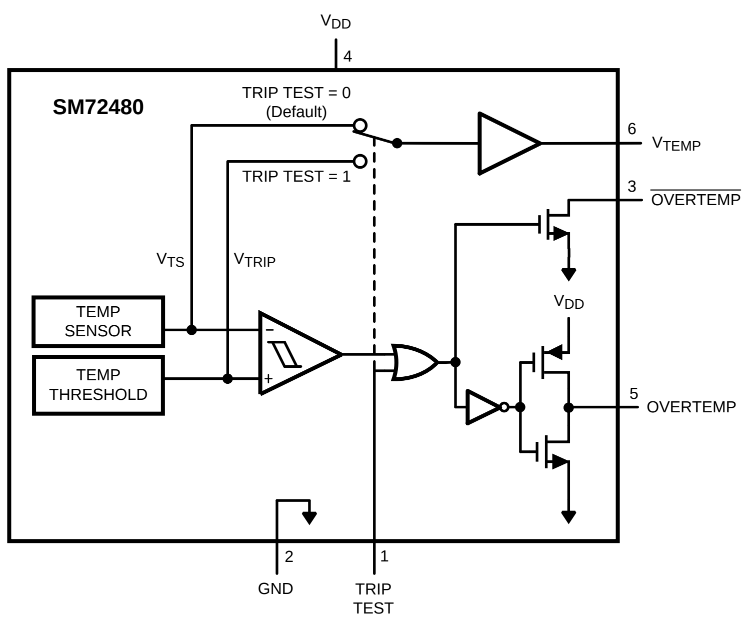
Figure 1. WSON-6 - Top View
See Package Number NGF0006A

Typical Transfer Characteristic

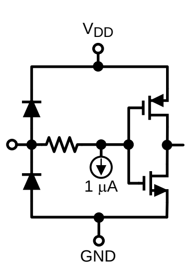
Figure 2. V_{TEMP} Analog Voltage vs Die Temperature



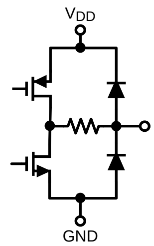
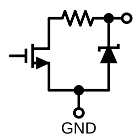
Block Diagram

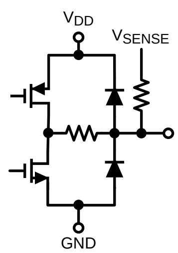


PIN DESCRIPTIONS

Pin No.	Name	Type	Equivalent Circuit	Description
1	TRIP TEST	Digital Input		TRIP TEST pin. Active High input. If TRIP TEST = 0 (Default) then: $V_{TEMP} = V_{TS}$, Temperature Sensor Output Voltage If TRIP TEST = 1 then: OVERTEMP and $\overline{\text{OVERTEMP}}$ outputs are asserted and $V_{TEMP} = V_{TRIP}$, Temperature Trip Voltage. This pin may be left open if not used.

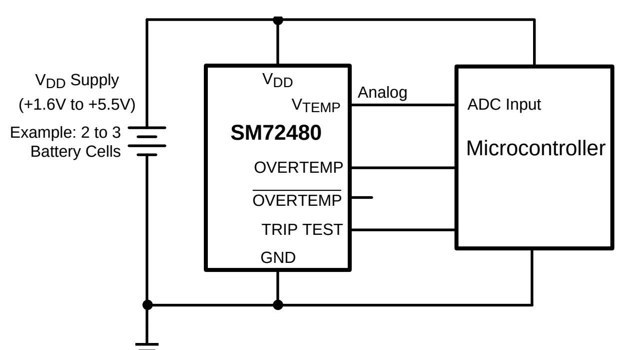
PIN DESCRIPTIONS (continued)

Pin No.	Name	Type	Equivalent Circuit	Description
5	OVERTEMP	Digital Output		Over Temperature Switch output Active High, Push-Pull Asserted when the measured temperature exceeds the Trip Point Temperature or if TRIP TEST = 1 This pin may be left open if not used.
3	$\overline{\text{OVERTEMP}}$	Digital Output		Over Temperature Switch output Active Low, Open-drain (See $\overline{\text{OVERTEMP}}$ OPEN-DRAIN DIGITAL OUTPUT regarding required pull-up resistor.) Asserted when the measured temperature exceeds the Trip Point Temperature or if TRIP TEST = 1 This pin may be left open if not used.

6	V_{TEMP}	Analog Output		V_{TEMP} Analog Voltage Output
				If TRIP TEST = 0 then
				$V_{TEMP} = V_{TS}$, Temperature Sensor Output Voltage
				If TRIP TEST = 1 then
				$V_{TEMP} = V_{TRIP}$, Temperature Trip Voltage
				This pin may be left open if not used.

4	V_{DD}	Power		Positive Supply Voltage
2	GND	Ground		Power Supply Ground
DAP	Die Attach Pad			The best thermal conductivity between the device and the PCB is achieved by soldering the DAP of the package to the thermal pad on the PCB. The thermal pad can be a floating node. However, for improved noise immunity the thermal pad should be connected to the circuit GND node, preferably directly to pin 2 (GND) of the device.

Typical Application



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1]

Supply Voltage		−0.3V to +6.0V
Voltage at $\overline{\text{OVERTEMP}}$ pin		−0.3V to +6.0V
Voltage at OVERTEMP and V_{TEMP} pins		−0.3V to (V_{DD} + 0.5V)
TRIP TEST Input Voltage		−0.3V to (V_{DD} + 0.5V)
Output Current, any output pin		±7 mA
Input Current at any pin[2]		5 mA
Storage Temperature		−65°C to +150°C
Maximum Junction Temperature	$T_{J(MAX)}$	+155°C
ESD Susceptibility[3]	Human Body Model	4500V
	Machine Model	300V
	Charged Device Model	1000V
For soldering specifications: see www.ti.com/lit/SNOA549		

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) When the input voltage (V_I) at any pin exceeds power supplies (V_I < GND or V_I > V_{DD}), the current at that pin should be limited to 5 mA.
(3) The Human Body Model (HBM) is a 100 pF capacitor charged to the specified voltage then discharged through a 1.5 kΩ resistor into each pin. The Machine Model (MM) is a 200 pF capacitor charged to the specified voltage then discharged directly into each pin. The Charged Device Model (CDM) is a specified circuit characterizing an ESD event that occurs when a device acquires charge through some triboelectric (frictional) or electrostatic induction processes and then abruptly touches a grounded object or surface.

Operating Ratings[1]

Specified Temperature Range		**$T_{MIN} \le T_A \le T_{MAX}$**
SM72480		−50°C ≤ T_A ≤ +150°C
Supply Voltage Range (V_{DD})		+1.6 V to +5.5 V
Thermal Resistance (θ_{JA})[2][3]	WSON-6 (Package SDB06A)	152 °C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) The junction to ambient temperature resistance (θ_{JA}) is specified without a heat sink in still air.
(3) Changes in output due to self heating can be computed by multiplying the internal dissipation by the temperature resistance.

Accuracy Characteristics Trip Point Accuracy

Parameter	Conditions		Limits[1]	Units (Limit)
Trip Point Accuracy[2]	0°C − 150°C	V_{DD} = 5.0 V	**±2.2**	°C (max)

(1) Limits are ensured to AOQL (Average Outgoing Quality Level).
(2) Accuracy is defined as the error between the measured and reference output voltages, tabulated in the Conversion Table at the specified conditions of supply gain setting, voltage, and temperature (expressed in °C). Accuracy limits include line regulation within the specified conditions. Accuracy limits do not include load regulation; they assume no DC load.

Accuracy Characteristics V_{TEMP} Analog Temperature Sensor Output Accuracy

The limits do not include DC load regulation. The stated accuracy limits are with reference to the values in the SM72480 Conversion Table.

Parameter	Conditions			Limits [1]	Units (Limit)
V_{TEMP} Temperature Accuracy [2]	Trip Point 125°C or 120°C	T_A = 20°C to 40°C	V_{DD} = 2.3 to 5.5 V	**±1.8**	°C (max) [2]
		T_A = 0°C to 70°C	V_{DD} = 2.5 to 5.5 V	**±2.0**	
		T_A = 0°C to 90°C	V_{DD} = 2.5 to 5.5 V	**±2.1**	
		T_A = 0°C to 120°C	V_{DD} = 2.5 to 5.5 V	**±2.2**	
		T_A = 0°C to 150°C	V_{DD} = 2.5 to 5.5 V	**±2.3**	
		T_A = –50°C to 0°C	V_{DD} = 3.0 to 5.5 V	**±1.7**	
V_{TEMP} Temperature Accuracy	Trip Point 105°C	T_A = 20°C to 40°C	V_{DD} = 1.8 to 5.5 V	**±1.8**	°C (max)
		T_A = 0°C to 70°C	V_{DD} = 1.9 to 5.5 V	**±2.0**	
		T_A = 0°C to 90°C	V_{DD} = 1.9 to 5.5 V	**±2.1**	
		T_A = 0°C to 120°C	V_{DD} = 1.9 to 5.5 V	**±2.2**	
		T_A = 0°C to 150°C	V_{DD} = 1.9 to 5.5 V	**±2.3**	
		T_A = −50°C to 0°C	V_{DD} = 2.3 to 5.5 V	**±1.7**	

(1) Limits are ensured to AOQL (Average Outgoing Quality Level).
(2) Accuracy is defined as the error between the measured and reference output voltages, tabulated in the Conversion Table at the specified conditions of supply gain setting, voltage, and temperature (expressed in °C). Accuracy limits include line regulation within the specified conditions. Accuracy limits do not include load regulation; they assume no DC load.

Electrical Characteristics

Unless otherwise noted, these specifications apply for $+V_{DD}$ = +1.6V to +5.5V. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions		Typical [1]	Limits [2]	Units (Limit)
GENERAL SPECIFICATIONS						
I_S	Quiescent Power Supply Current			8	**16**	µA (max)
	Hysteresis			5	**5.5**	°C (max)
					4.5	°C (Min)
OVERTEMP DIGITAL OUTPUT		**ACTIVE HIGH, PUSH-PULL**				
V_{OH}	Logic "1" Output Voltage	V_{DD} ≥ 1.6V	Source ≤ 340 µA		**V_{DD} − 0.2V**	V (min)
		V_{DD} ≥ 2.0V	Source ≤ 498 µA			
		V_{DD} ≥ 3.3V	Source ≤ 780 µA			
		V_{DD} ≥ 1.6V	Source ≤ 600 µA		**V_{DD} − 0.45V**	V (min)
		V_{DD} ≥ 2.0V	Source ≤ 980 µA			
		V_{DD} ≥ 3.3V	Source ≤ 1.6 mA			
BOTH OVERTEMP and $\overline{\text{OVERTEMP}}$ DIGITAL OUTPUTS						
V_{OL}	Logic "0" Output Voltage	V_{DD} ≥ 1.6V	Sink ≤ 385 µA		**0.2**	V (max)
		V_{DD} ≥ 2.0V	Sink ≤ 500 µA			
		V_{DD} ≥ 3.3V	Sink ≤ 730 µA			
		V_{DD} ≥ 1.6V	Sink ≤ 690 µA		**0.45**	
		V_{DD} ≥ 2.0V	Sink ≤ 1.05 mA			
		V_{DD} ≥ 3.3V	Sink ≤ 1.62 mA			

(1) Typicals are at $T_J = T_A$ = 25°C and represent most likely parametric norm.
(2) Limits are ensured to AOQL (Average Outgoing Quality Level).

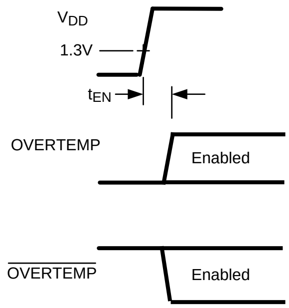
Electrical Characteristics (continued)

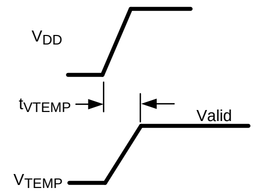
Unless otherwise noted, these specifications apply for $+V_{DD}$ = +1.6V to +5.5V. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions		Typical (1)	Limits (2)	Units (Limit)
$\overline{OVERTEMP}$ DIGITAL OUTPUT		**ACTIVE LOW, OPEN DRAIN**				
I_{OH}	Logic "1" Output Leakage Current (3)	T_A = 30 °C		0.001	1	µA (max)
		T_A = 150 °C		0.025		
V_{TEMP} ANALOG TEMPERATURE SENSOR OUTPUT						
	V_{TEMP} Sensor Gain	Trip Point = 105°C		-7.7		mV/°C
		Trip Point = 125°C or 120°C		−10.3		mV/°C
	V_{TEMP} Load Regulation (4)	1.6V ≤ V_{DD} < 1.8V	Source ≤ 90 µA ($V_{DD} − V_{TEMP}$) ≥ 200 mV	−0.1	**−1**	mV (max)
			Sink ≤ 100 µA V_{TEMP} ≥ 260 mV	0.1	**1**	mV (max)
		V_{DD} ≥ 1.8V	Source ≤ 120 µA ($V_{DD} − V_{TEMP}$) ≥ 200 mV	−0.1	**−1**	mV (max)
			Sink ≤ 200 µA V_{TEMP} ≥ 260 mV	0.1	**1**	mV (max)
		Source or Sink = 100 µA		1		Ohm
	V_{DD} Supply- to-V_{TEMP} DC Line Regulation (5)	V_{DD} = +1.6V to +5.5V		0.29		mV
				74		µV/V
				−82		dB
C_L	V_{TEMP} Output Load Capacitance	Without series resistor. See CAPACITIVE LOADS.		1100		pF (max)
TRIP TEST DIGITAL INPUT						
V_{IH}	Logic "1" Threshold Voltage				**V_{DD}− 0.5**	V (min)
V_{IL}	Logic "0" Threshold Voltage				**0.5**	V (max)
I_{IH}	Logic "1" Input Current			1.5	**2.5**	µA (max)
I_{IL}	Logic "0" Input Current (3)			0.001	**1**	µA (max)
TIMING						
t_{EN}	Time from Power On to Digital Output Enabled. See definition below.			1.1	**2.3**	ms (max)
t_V	Time from Power On to Analog Temperature Valid. See definition below.	V_{TEMP} C_L = 0 pF to 1100 pF		1.0	**2.9**	ms (max)

(3) The 1 µA limit is based on a testing limitation and does not reflect the actual performance of the part. Expect to see a doubling of the current for every 15°C increase in temperature. For example, the 1 nA typical current at 25°C would increase to 16 nA at 85°C.
(4) Source currents are flowing out of the SM72480. Sink currents are flowing into the SM72480.
(5) Line regulation (DC) is calculated by subtracting the output voltage at the highest supply voltage from the output voltage at the lowest supply voltage. The typical DC line regulation specification does not include the output voltage shift discussed in VOLTAGE SHIFT.

Definitions of t_{EN} and t_V





The curves shown represent typical performance under worst-case conditions. Performance improves with larger overhead (V_{DD} − V_{TEMP}), larger V_{DD}, and lower temperatures.

The curves shown represent typical performance under worst-case conditions. Performance improves with larger V_{TEMP}, larger V_{DD} and lower temperatures.

Typical Performance Characteristics

V_{TEMP} Output Temperature Error vs. Temperature

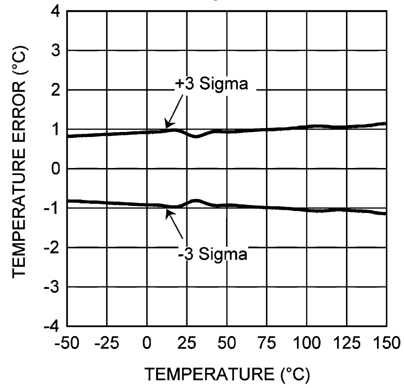


Figure 3.

Minimum Operating Temperature vs. Supply Voltage

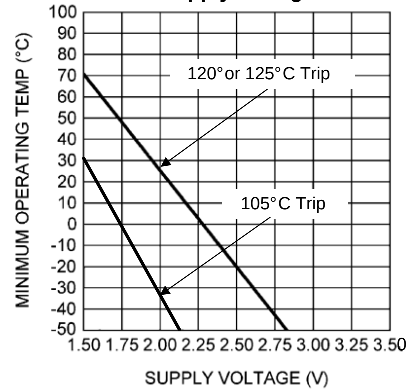


Figure 4.

Supply Current vs. Temperature

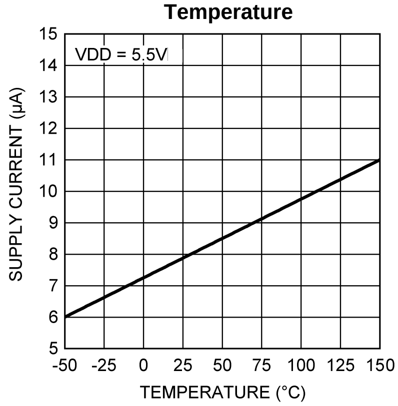


Figure 5.

Supply Current vs. Supply Voltage

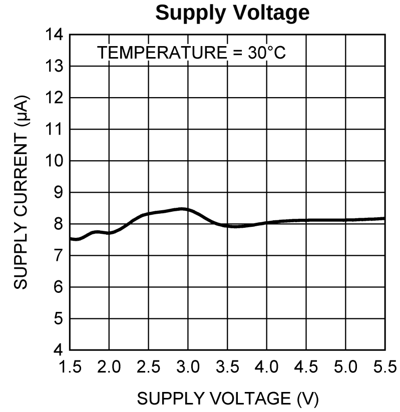


Figure 6.

V_{TEMP} Supply-Noise Rejection vs. Frequency

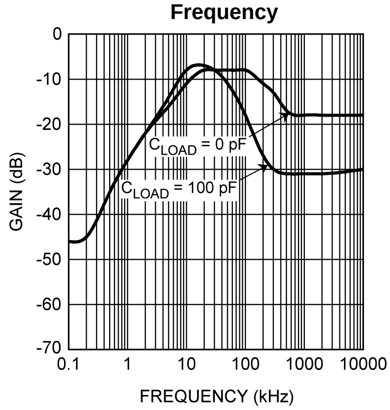


Figure 7.

Line Regulation V_{TEMP} vs. Supply Voltage Trip Points 120°C

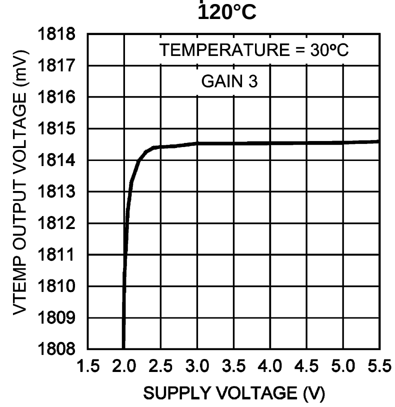


Figure 8.

SM72480 V_{TEMP} VS DIE TEMPERATURE CONVERSION TABLE

The SM72480 has a factory-set gain, which is dependent on the Temperature Trip Point. The V_{TEMP} temperature sensor voltage, in millivolts, at each discrete die temperature over the complete operating range is shown in the conversion table below.

Table 1. V_{TEMP} Temperature Sensor Output Voltage vs Die Temperature Conversion Table(1)

Die Temp., °C	V_{TEMP}, Analog Output Voltage, mV	
	T_{TRIP} = 125 or 120°C	T_{TRIP} = 105°C
−50	2623	1967
−49	2613	1960
−48	2603	1952
−47	2593	1945
−46	2583	1937
−45	2573	1930
−44	2563	1922
−43	2553	1915
−42	2543	1908
−41	2533	1900
−40	2523	1893
−39	2513	1885
−38	2503	1878
−37	2493	1870
−36	2483	1863
−35	2473	1855
−34	2463	1848
−33	2453	1840
−32	2443	1833
−31	2433	1825
−30	2423	1818
−29	2413	1810
−28	2403	1803
−27	2393	1795
−26	2383	1788
−25	2373	1780
−24	2363	1773
−23	2353	1765
−22	2343	1757
−21	2333	1750
−20	2323	1742
−19	2313	1735
−18	2303	1727
−17	2293	1720
−16	2283	1712
−15	2272	1705
−14	2262	1697
−13	2252	1690
−12	2242	1682

(1) The V_{TEMP} temperature sensor output voltage, in mV, vs Die Temperature, in °C for the gain corresponding to the temperature trip point. V_{DD} = 5.0V.

Table 1. V_{TEMP} Temperature Sensor Output Voltage vs Die Temperature Conversion Table(1) (continued)

Die Temp., °C	V_{TEMP}, Analog Output Voltage, mV	
	T_{TRIP} = 125 or 120°C	T_{TRIP} = 105°C
−11	2232	1674
−10	2222	1667
−9	2212	1659
−8	2202	1652
−7	2192	1644
−6	2182	1637
−5	2171	1629
−4	2161	1621
−3	2151	1614
−2	2141	1606
−1	2131	1599
0	2121	1591
1	2111	1583
2	2101	1576
3	2090	1568
4	2080	1561
5	2070	1553
6	2060	1545
7	2050	1538
8	2040	1530
9	2029	1522
10	2019	1515
11	2009	1507
12	1999	1499
13	1989	1492
14	1978	1484
15	1968	1477
16	1958	1469
17	1948	1461
18	1938	1454
19	1927	1446
20	1917	1438
21	1907	1431
22	1897	1423
23	1886	1415
24	1876	1407
25	1866	1400
26	1856	1392
27	1845	1384
28	1835	1377
29	1825	1369
30	1815	1361
31	1804	1354
32	1794	1346
33	1784	1338
34	1774	1331

Table 1. V_{TEMP} Temperature Sensor Output Voltage vs Die Temperature Conversion Table[(1)] (continued)

Die Temp., °C	V_{TEMP}, Analog Output Voltage, mV	
	T_{TRIP} = 125 or 120°C	T_{TRIP} = 105°C
35	1763	1323
36	1753	1315
37	1743	1307
38	1732	1300
39	1722	1292
40	1712	1284
41	1701	1276
42	1691	1269
43	1681	1261
44	1670	1253
45	1660	1245
46	1650	1238
47	1639	1230
48	1629	1222
49	1619	1214
50	1608	1207
51	1598	1199
52	1588	1191
53	1577	1183
54	1567	1176
55	1557	1168
56	1546	1160
57	1536	1152
58	1525	1144
59	1515	1137
60	1505	1129
61	1494	1121
62	1484	1113
63	1473	1105
64	1463	1098
65	1453	1090
66	1442	1082
67	1432	1074
68	1421	1066
69	1411	1059
70	1400	1051
71	1390	1043
72	1380	1035
73	1369	1027
74	1359	1019
75	1348	1012
76	1338	1004
77	1327	996
78	1317	988
79	1306	980
80	1296	972

Table 1. V_{TEMP} Temperature Sensor Output Voltage vs Die Temperature Conversion Table(1) (continued)

Die Temp., °C	V_{TEMP}, Analog Output Voltage, mV	
	T_{TRIP} = 125 or 120°C	T_{TRIP} = 105°C
81	1285	964
82	1275	957
83	1264	949
84	1254	941
85	1243	933
86	1233	925
87	1222	917
88	1212	909
89	1201	901
90	1191	894
91	1180	886
92	1170	878
93	1159	870
94	1149	862
95	1138	854
96	1128	846
97	1117	838
98	1106	830
99	1096	822
100	1085	814
101	1075	807
102	1064	799
103	1054	791
104	1043	783
105	1032	775
106	1022	767
107	1011	759
108	1001	751
109	990	743
110	**979**	735
111	**969**	727
112	**958**	719
113	**948**	711
114	**937**	703
115	**926**	695
116	**916**	687
117	**905**	679
118	**894**	671
119	**884**	663
120	**873**	655
121	**862**	647
122	**852**	639
123	**841**	631
124	**831**	623
125	**820**	615
126	**809**	607

Table 1. V_{TEMP} Temperature Sensor Output Voltage vs Die Temperature Conversion Table(1) (continued)

Die Temp., °C	V_{TEMP}, Analog Output Voltage, mV	
	T_{TRIP} = 125 or 120°C	T_{TRIP} = 105°C
127	**798**	599
128	**788**	591
129	**777**	583
130	766	575
131	756	567
132	745	559
133	734	551
134	724	543
135	713	535
136	702	527
137	691	519
138	681	511
139	670	503
140	659	495
141	649	487
142	638	479
143	627	471
144	616	463
145	606	455
146	595	447
147	584	438
148	573	430
149	562	422
150	552	414

V_{TEMP} vs DIE TEMPERATURE APPROXIMATIONS

The SM72480's V_{TEMP} analog temperature output is very linear. The Conversion Table above and the equation in The Second-Order Equation (Parabolic) represent the most accurate typical performance of the V_{TEMP} voltage output vs Temperature.

The Second-Order Equation (Parabolic)

The data from the Conversion Table, or the equation below, when plotted, has an umbrella-shaped parabolic curve. V_{TEMP} is in mV.

$$V_{(TEMP=120\ or\ 125)} = 1814.6 - 10.270 \times (T_{DIE} - 30°C) - 2.12e\text{-}3 \times (T_{DIE} - 30°C)^2$$
$$V_{(TEMP=105)} = 1361.4 - 7.701 \times (T_{DIE} - 30°C) - 1.60e\text{-}3 \times (T_{DIE} - 30°C)^2 \quad (1)$$

The First-Order Approximation (Linear)

For a quicker approximation, although less accurate than the second-order, over the full operating temperature range the linear formula below can be used. Using this formula, with the constant and slope in the following set of equations, the best-fit V_{TEMP} vs Die Temperature performance can be calculated with an approximation error less than 18 mV. V_{TEMP} is in mV.

$$V_{(TEMP=120\ or\ 125)} = 2119 - 10.36 \times T_{DIE}$$
$$V_{(TEMP=105)} = 1590 - 7.77 \times T_{DIE} \quad (2)$$

First-Order Approximation (Linear) over Small Temperature Range

For a linear approximation, a line can easily be calculated over the desired temperature range from the Conversion Table using the two-point equation:

$$V - V_1 = \left(\frac{V_2 - V_1}{T_2 - T_1}\right) \times (T - T_1) \tag{3}$$

Where V is in mV, T is in °C, T_1 and V_1 are the coordinates of the lowest temperature, T_2 and V_2 are the coordinates of the highest temperature.

$$V - 2396\text{ mV} = (-12.8\text{ mV/°C}) \times (T - 20°C) \tag{4}$$

$$V = (-12.8\text{ mV/°C}) \times (T - 20°C) + 2396\text{ mV} \tag{5}$$

Using this method of linear approximation, the transfer function can be approximated for one or more temperature ranges of interest.

OVERTEMP and $\overline{\text{OVERTEMP}}$ Digital Outputs

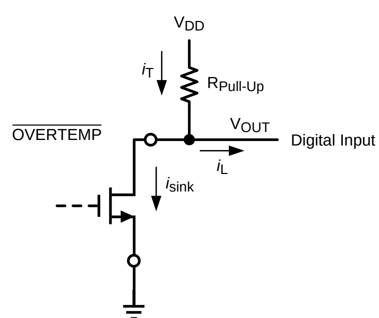
The OVERTEMP Active High, Push-Pull Output and the $\overline{\text{OVERTEMP}}$ Active Low, Open-Drain Output both assert at the same time whenever the Die Temperature reaches the factory preset Temperature Trip Point. They also assert simultaneously whenever the TRIP TEST pin is set high. Both outputs de-assert when the die temperature goes below the Temperature Trip Point - Hysteresis. These two types of digital outputs enable the user the flexibility to choose the type of output that is most suitable for his design.

Either the OVERTEMP or the $\overline{\text{OVERTEMP}}$ Digital Output pins can be left open if not used.

$\overline{\text{OVERTEMP}}$ OPEN-DRAIN DIGITAL OUTPUT

The $\overline{\text{OVERTEMP}}$ Active Low, Open-Drain Digital Output, if used, requires a pull-up resistor between this pin and V_{DD}. The following section shows how to determine the pull-up resistor value.

Figure 9. Determining the Pull-up Resistor Value



The Pull-up resistor value is calculated at the condition of maximum total current, i_T, through the resistor. The total current is:

$$i_T = i_L + i_{sink}$$

where

- i_T is the maximum total current through the Pull-up Resistor at V_{OL}.
- i_L is the load current, which is very low for typical digital inputs.
- V_{OUT} is the Voltage at the $\overline{\text{OVERTEMP}}$ pin. Use V_{OL} for calculating the Pull-up resistor.
- $V_{DD(Max)}$ is the maximum power supply voltage to be used in the customer's system. (6)

The pull-up resistor maximum value can be found by using the following formula:

$$R_{pull\text{-}up} = \frac{V_{DD\,(Max)} - V_{OL}}{i_T} \tag{7}$$

EXAMPLE CALCULATION

Suppose we have, for our example, a V_{DD} of 3.3 V ± 0.3V, a CMOS digital input as a load, a V_{OL} of 0.2 V.

1. We see that for V_{OL} of 0.2 V the electrical specification for $\overline{OVERTEMP}$ shows a maximim i_{sink} of 385 µA.
2. Let i_L= 1 µA, then i_T is about 386 µA max. If we select 35 µA as the current limit then i_T for the calculation becomes 35 µA
3. We notice that $V_{DD(Max)}$ is 3.3V + 0.3V = 3.6V and then calculate the pull-up resistor as $R_{Pull\text{-}up}$ = (3.6 − 0.2)/35 µA = 97k
4. Based on this calculated value, we select the closest resistor value in the tolerance family we are using.

In our example, if we are using 5% resistor values, then the next closest value is 100 kΩ.

NOISE IMMUNITY

The SM72480 is virtually immune from false triggers on the OVERTEMP and $\overline{OVERTEMP}$ digital outputs due to noise on the power supply. Test have been conducted showing that, with the die temperature within 0.5°C of the temperature trip point, and the severe test of a 3 Vpp square wave "noise" signal injected on the V_{DD} line, over the V_{DD} range of 2V to 5V, there were no false triggers.

TRIP TEST Digital Input

The TRIP TEST pin simply provides a means to test the OVERTEMP and $\overline{OVERTEMP}$ digital outputs electronically by causing them to assert, at any operating temperature, as a result of forcing the TRIP TEST pin high.

When the TRIP TEST pin is pulled high the V_{TEMP} pin will be at the V_{TRIP} voltage.

If not used, the TRIP TEST pin may either be left open or grounded.

V_{TEMP} Analog Temperature Sensor Output

The V_{TEMP} push-pull output provides the ability to sink and source significant current. This is beneficial when, for example, driving dynamic loads like an input stage on an analog-to-digital converter (ADC). In these applications the source current is required to quickly charge the input capacitor of the ADC. See the Applications Circuits section for more discussion of this topic. The SM72480 is ideal for this and other applications which require strong source or sink current.

NOISE CONSIDERATIONS

The SM72480's supply-noise rejection (the ratio of the AC signal on V_{TEMP} to the AC signal on V_{DD}) was measured during bench tests. It's typical attenuation is shown in the Typical Performance Characteristics section. A load capacitor on the output can help to filter noise.

For operation in very noisy environments, some bypass capacitance should be present on the supply within approximately 2 inches of the SM72480.

CAPACITIVE LOADS

The V_{TEMP} Output handles capacitive loading well. In an extremely noisy environment, or when driving a switched sampling input on an ADC, it may be necessary to add some filtering to minimize noise coupling. Without any precautions, the V_{TEMP} can drive a capacitive load less than or equal to 1100 pF as shown in Figure 10. For capacitive loads greater than 1100 pF, a series resistor is required on the output, as shown in Figure 11, to maintain stable conditions.

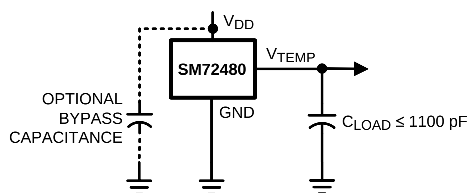


Figure 10. SM72480 No Decoupling Required for Capacitive Loads Less than 1100 pF.

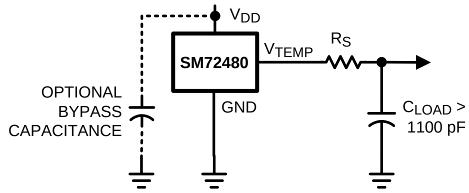


Figure 11.

C_{LOAD}	Minimum R_S
1.1 nF to 99 nF	3 kΩ
100 nF to 999 nF	1.5 kΩ
1 µF	800 Ω

VOLTAGE SHIFT

The SM72480 is very linear over temperature and supply voltage range. Due to the intrinsic behavior of an NMOS/PMOS rail-to-rail buffer, a slight shift in the output can occur when the supply voltage is ramped over the operating range of the device. The location of the shift is determined by the relative levels of V_{DD} and V_{TEMP}. The shift typically occurs when $V_{DD} - V_{TEMP} = 1.0V$.

This slight shift (a few millivolts) takes place over a wide change (approximately 200 mV) in V_{DD} or V_{TEMP}. Since the shift takes place over a wide temperature change of 5°C to 20°C, V_{TEMP} is always monotonic. The accuracy specifications in the Electrical Characteristics table already includes this possible shift.

Mounting and Temperature Conductivity

The SM72480 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface.

The best thermal conductivity between the device and the PCB is achieved by soldering the DAP of the package to the thermal pad on the PCB. The temperatures of the lands and traces to the other leads of the SM72480 will also affect the temperature reading.

Alternatively, the SM72480 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the SM72480 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. If moisture creates a short circuit from the V_{TEMP} output to ground or V_{DD}, the V_{TEMP} output from the SM72480 will not be correct. Printed-circuit coatings are often used to ensure that moisture cannot corrode the leads or circuit traces.

The thermal resistance junction-to-ambient (θ_{JA}) is the parameter used to calculate the rise of a device junction temperature due to its power dissipation. The equation used to calculate the rise in the SM72480's die temperature is

$$T_J = T_A + \theta_{JA}\left[(V_{DD} I_Q) + (V_{DD} - V_{TEMP})\ \ I_L \right] \quad (8)$$

where T_A is the ambient temperature, I_Q is the quiescent current, I_L is the load current on the output, and V_O is the output voltage. For example, in an application where T_A = 30 °C, V_{DD} = 5 V, I_{DD} = 9 µA, Gain 4, V_{TEMP} = 2231 mV, and I_L = 2 µA, the junction temperature would be 30.021 °C, showing a self-heating error of only 0.021°C. Since the SM72480's junction temperature is the actual temperature being measured, care should be taken to minimize the load current that the V_{TEMP} output is required to drive. If The $\overline{\text{OVERTEMP}}$ output is used with a 100 k pull-up resistor, and this output is asserted (low), then for this example the additional contribution is [(152° C/W)x$(5V)^2$/100k] = 0.038°C for a total self-heating error of 0.059°C. Table 2 shows the thermal resistance of the SM72480.

Table 2. SM72480 Thermal Resistance

Device Number	Package Number	Thermal Resistance (θ_{JA})
SM72480SD	SDB06A	152° C/W

Applications Circuits

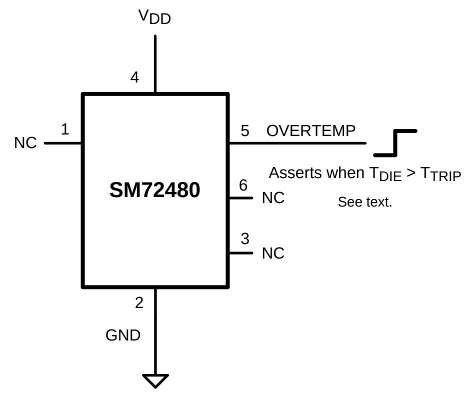


Figure 12. Temperature Switch Using Push-Pull Output

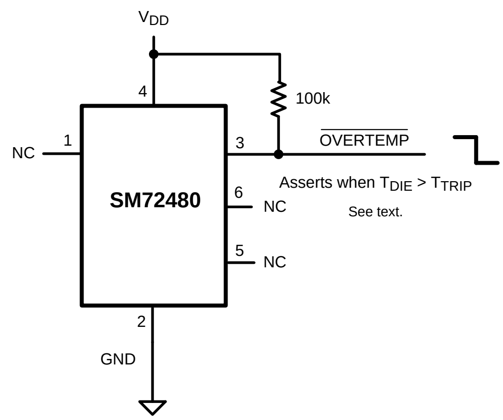


Figure 13. Temperature Switch Using Open-Drain Output

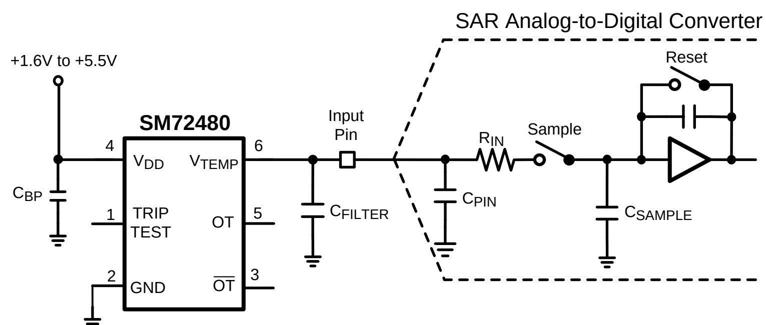


Figure 14. Suggested Connection to a Sampling Analog-to-Digital Converter Input Stage

Most CMOS ADCs found in microcontrollers and ASICs have a sampled data comparator input structure. When the ADC charges the sampling cap, it requires instantaneous charge from the output of the analog source such as the SM72480 temperature sensor and many op amps. This requirement is easily accommodated by the addition of a capacitor (C_{FILTER}). The size of C_{FILTER} depends on the size of the sampling capacitor and the sampling frequency. Since not all ADCs have identical input stages, the charge requirements will vary. This general ADC application is shown as an example only.

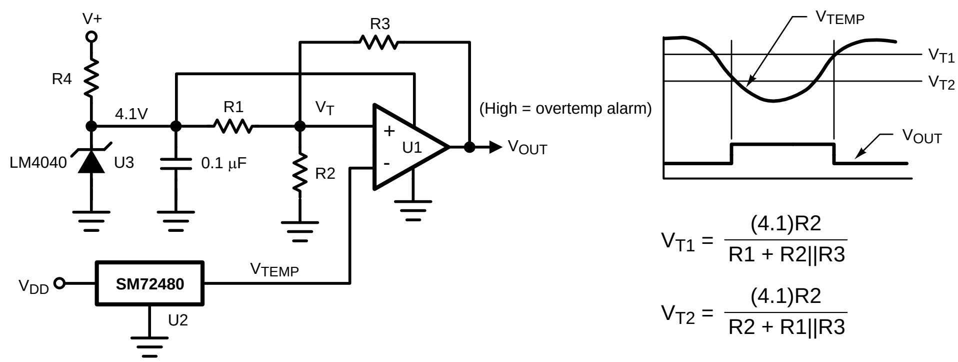


Figure 15. Celsius Temperature Switch

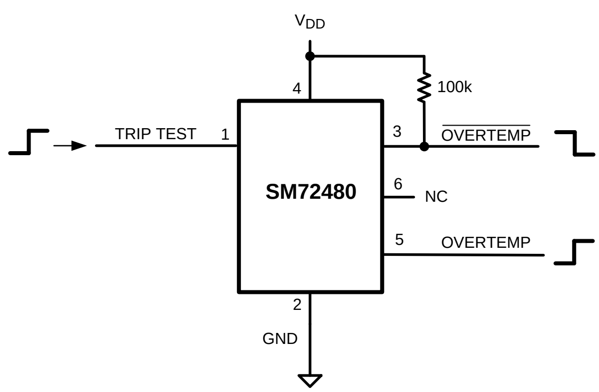


Figure 16. TRIP TEST Digital Output Test Circuit

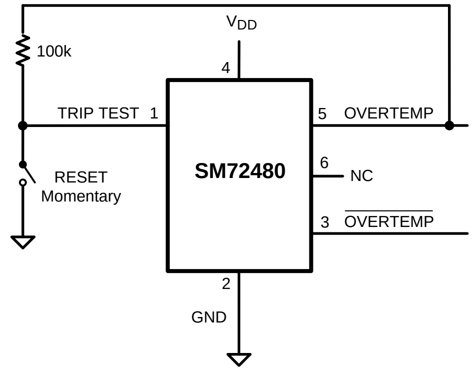


Figure 17. Latch Circuit using OVERTEMP Output

The TRIP TEST pin, normally used to check the operation of the OVERTEMP and $\overline{\text{OVERTEMP}}$ pins, may be used to latch the outputs whenever the temperature exceeds the programmed limit and causes the digital outputs to assert. As shown in the figure, when OVERTEMP goes high the TRIP TEST input is also pulled high and causes OVERTEMP output to latch high and the $\overline{\text{OVERTEMP}}$ output to latch low. The latch can be released by either momentarily pulling the TRIP TEST pin low (GND), or by toggling the power supply to the device. The resistor limits the current out of the OVERTEMP output pin.

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	19

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SM72480SD-105/NOPB	NRND	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-50 to 150	701	
SM72480SD-120/NOPB	NRND	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-50 to 150	S80	
SM72480SD-125/NOPB	NRND	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-50 to 150	299	
SM72480SDE-105/NOPB	NRND	WSON	NGF	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-50 to 150	701	
SM72480SDE-120/NOPB	ACTIVE	WSON	NGF	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-50 to 150	S80	Samples
SM72480SDE-125/NOPB	NRND	WSON	NGF	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-50 to 150	299	
SM72480SDX-105/NOPB	NRND	WSON	NGF	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-50 to 150	701	
SM72480SDX-120/NOPB	NRND	WSON	NGF	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-50 to 150	S80	
SM72480SDX-125/NOPB	NRND	WSON	NGF	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-50 to 150	299	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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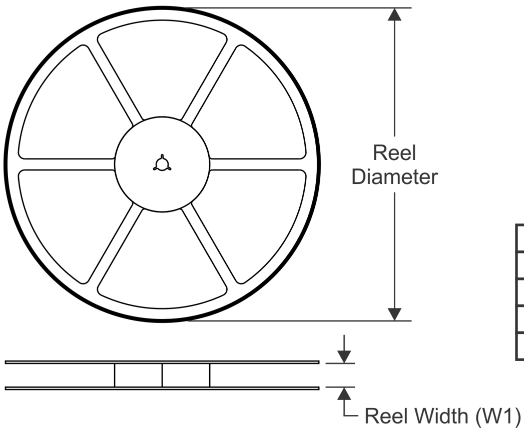
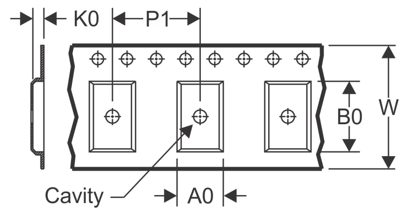
TAPE AND REEL INFORMATION

REEL DIMENSIONS

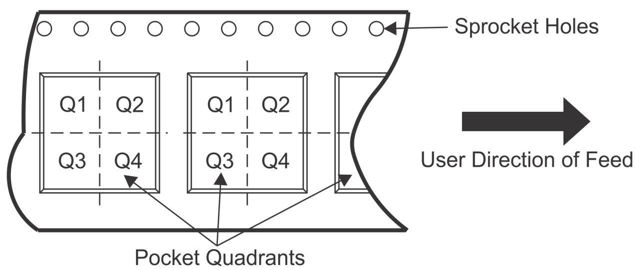


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

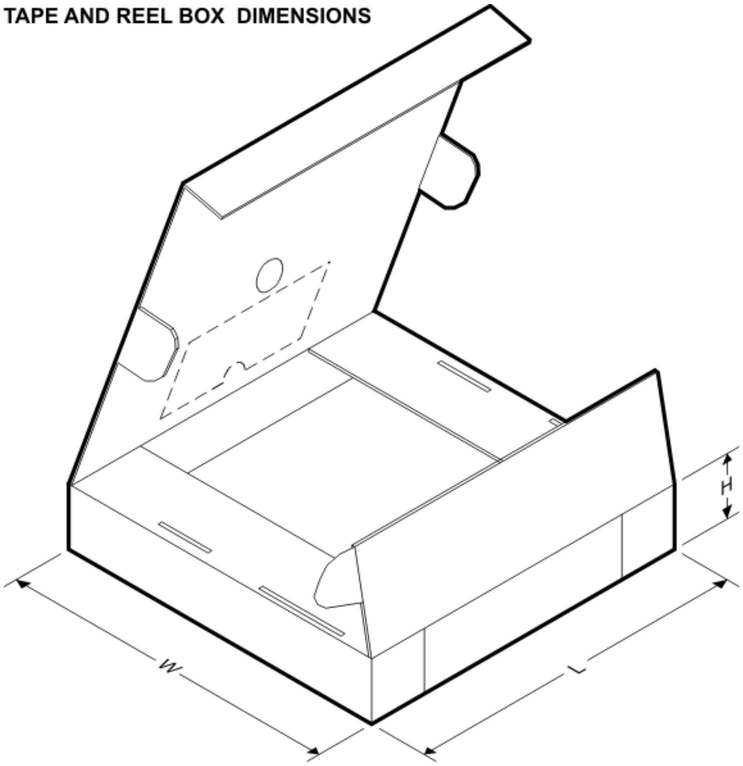
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SM72480SD-105/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
SM72480SD-120/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
SM72480SD-125/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
SM72480SDE-105/NOPB	WSON	NGF	6	250	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
SM72480SDE-120/NOPB	WSON	NGF	6	250	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
SM72480SDE-125/NOPB	WSON	NGF	6	250	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
SM72480SDX-105/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
SM72480SDX-120/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
SM72480SDX-125/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1

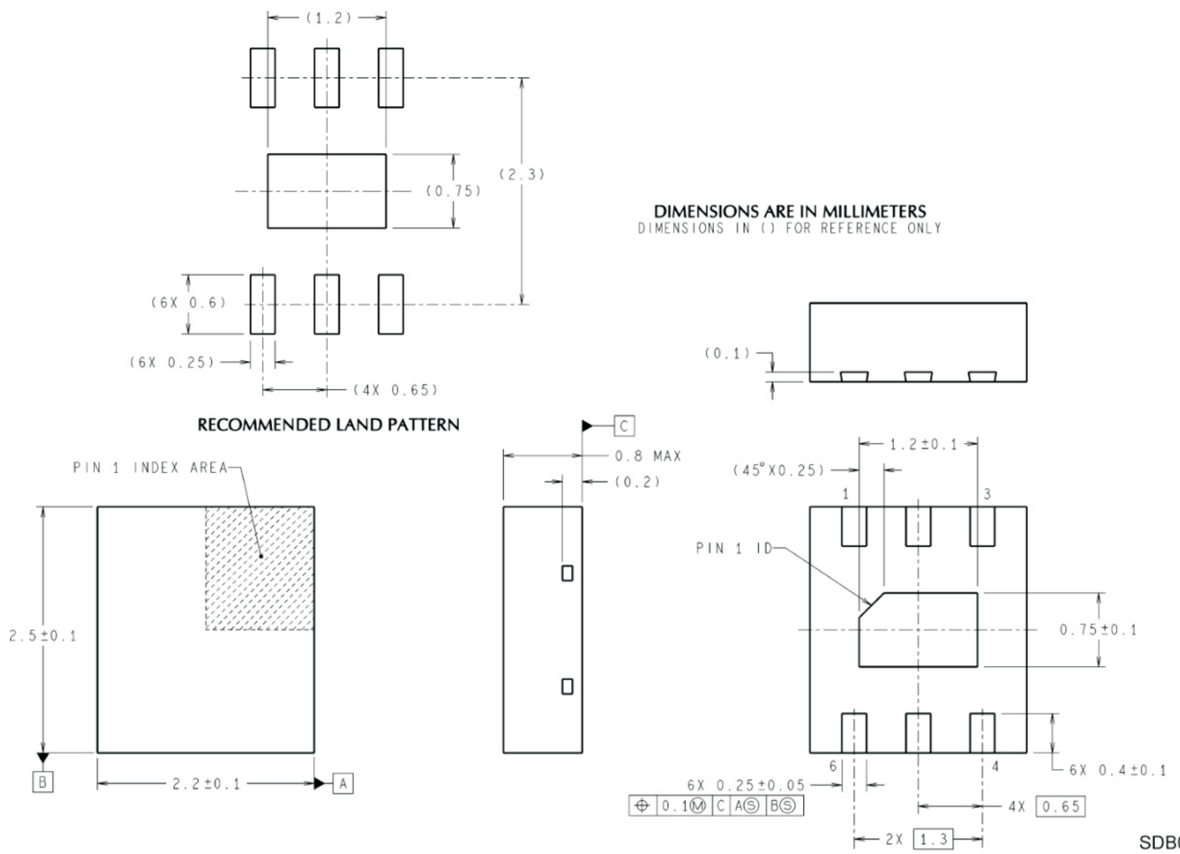
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SM72480SD-105/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
SM72480SD-120/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
SM72480SD-125/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
SM72480SDE-105/NOPB	WSON	NGF	6	250	210.0	185.0	35.0
SM72480SDE-120/NOPB	WSON	NGF	6	250	210.0	185.0	35.0
SM72480SDE-125/NOPB	WSON	NGF	6	250	210.0	185.0	35.0
SM72480SDX-105/NOPB	WSON	NGF	6	4500	367.0	367.0	35.0
SM72480SDX-120/NOPB	WSON	NGF	6	4500	367.0	367.0	35.0
SM72480SDX-125/NOPB	WSON	NGF	6	4500	367.0	367.0	35.0

NGF0006A



SDB06A (Rev A)

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265