Dual Precision, 17 MHz, Low Noise, CMOS Input Amplifier

Check for Samples: SM73307

FEATURES

- **Unless Otherwise Noted, Typical Values at V_S = 5V.**
- **Renewable Energy Grade**
- **Input Offset Voltage ±150 µV (max)**
- **Input Bias Current 100 fA**
- **Input Voltage Noise 5.8 nV/√Hz**
- **Gain Bandwidth Product 17 MHz**
- **Supply Current 1.30 mA**
- **Supply Voltage Range 1.8V to 5.5V**
- **THD+N @ f = 1 kHz 0.001%**
- **Operating Temperature Range −40°C to 125°C**
- **Rail-to-rail Output Swing**
- **8-Pin VSSOP Package**

APPLICATIONS

- **Photovoltaic Electronics**
- **Active Filters and Buffers**
- **Sensor Interface Applications**
- **Transimpedance Amplifiers**
- **Automotive**

DESCRIPTION

The SM73307 is a dual, low noise, low offset, CMOS input, rail-to-rail output precision amplifier with a high gain bandwidth product. The SM73307 is ideal for a variety of instrumentation applications including solar photovoltaic.

Utilizing a CMOS input stage, the SM73307 achieves an input bias current of 100 fA, an input referred voltage noise of 5.8 nV/√Hz, and an input offset voltage of less than ±150 µV. These features make the SM73307 a superior choice for precision applications.

Consuming only 1.30 mA of supply current per channel, the SM73307 offers a high gain bandwidth product of 17 MHz, enabling accurate amplification at high closed loop gains.

The SM73307 has a supply voltage range of 1.8V to 5.5V, which makes it an ideal choice for portable low power applications with low supply voltage requirements.

The SM73307 is built with TI’s advanced VIP50 process technology and is offered in an 8-pin VSSOP package.

The SM73307 incorporates enhanced manufacturing and support processes for the photovoltaic and automotive market, including defect detection methodologies. Reliability qualification is compliant with the requirements and temperature grades defined in the Renewable Energy Grade and AEC-Q100 standards.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance(3)	Human Body Model	2000V
	Machine Model	200V
	Charge-Device Model	1000V
V_{IN} Differential		±0.3V
Supply Voltage ($V_S = V^+ – V^–$)		6.0V
Voltage on Input/Output Pins		V^+ +0.3V, $V^–$ −0.3V
Storage Temperature Range		−65°C to 150°C
Junction Temperature(4)		+150°C
Soldering Information	Infrared or Convection (20 sec)	235°C
	Wave Soldering Lead Temp. (10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional. For specifications and the test conditions, see the Electrical Characteristics Tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $θ_{JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/θ_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Operating Ratings(1)

Temperature Range(2)		−40°C to 125°C
Supply Voltage ($V_S = V^+ – V^–$)	$0°C ≤ T_A ≤ 125°C$	1.8V to 5.5V
	$−40°C ≤ T_A ≤ 125°C$	2.0V to 5.5V
Package Thermal Resistance ($θ_{JA}$(2))	8-Pin VSSOP	236°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional. For specifications and the test conditions, see the Electrical Characteristics Tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $θ_{JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/θ_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

2.5V Electrical Characteristics

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 2.5V, $V^–$ = 0V ,$V_O = V_{CM} = V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min(1)	Typ(2)	Max(1)	Units
V_{OS}	Input Offset Voltage	$−20°C ≤ T_A ≤ 85°C$			±20	±180 **±330**	μV
		$−40°C ≤ T_A ≤ 125°C$			±20	±180 **±430**	
TC V_{OS}	Input Offset Voltage Temperature Drift(3)(4)				–1.75	±4	μV/°C
I_B	Input Bias Current	V_{CM} = 1.0V(5)(4)	$−40°C ≤ T_A ≤ 85°C$		0.05	1 **25**	pA
			$−40°C ≤ T_A ≤ 125°C$		0.05	1 **100**	

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(3) Offset voltage average drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(4) This parameter is specified by design and/or characterization and is not tested in production.
(5) Positive current corresponds to current flowing into the device.

2.5V Electrical Characteristics (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 2.5V, V^- = 0V ,V_O = V_{CM} = V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
I_{OS}	Input Offset Current	V_{CM} = 1V (4)		0.006	0.5 **50**	pA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.4V	83 **80**	100		dB
PSRR	Power Supply Rejection Ratio	2.0V ≤ V^+ ≤ 5.5V V^- = 0V, V_{CM} = 0	85 **80**	100		dB
		1.8V ≤ V^+ ≤ 5.5V V^- = 0V, V_{CM} = 0	85	98		
CMVR	Common Mode Voltage Range	CMRR ≥ 80 dB CMRR ≥ 78 dB	−0.3 **−0.3**		1.5 **1.5**	V
A_{VOL}	Open Loop Voltage Gain	V_O = 0.15 to 2.2V R_L = 2 kΩ to V^+/2	84 **80**	92		dB
		V_O = 0.15 to 2.2V R_L = 10 kΩ to V^+/2	90 **86**	95		
V_{OUT}	Output Voltage Swing High	R_L = 2 kΩ to V^+/2		25	70 **77**	mV from either rail
		R_L = 10 kΩ to V^+/2		20	60 **66**	
	Output Voltage Swing Low	R_L = 2 kΩ to V^+/2		30	70 **73**	
		R_L = 10 kΩ to V^+/2		15	60 **62**	
I_{OUT}	Output Current	Sourcing to V^- V_{IN} = 200 mV (6)	36 **30**	52		mA
		Sinking to V^+ V_{IN} = −200 mV (6)	7.5 **5.0**	15		
I_S	Supply Current	Per Channel		1.10	1.50 **1.85**	mA
SR	Slew Rate	A_V = +1, Rising (10% to 90%)		8.3		V/µs
		A_V = +1, Falling (90% to 10%)		10.3		
GBW	Gain Bandwidth			14		MHz
e_n	Input Referred Voltage Noise Density	f = 400 Hz		6.8		nV/$\sqrt{Hz}$
		f = 1 kHz		5.8		
i_n	Input Referred Current Noise Density	f = 1 kHz		0.01		pA/$\sqrt{Hz}$
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, R_L = 100 kΩ V_O = 0.9 V_{PP}		0.003		%
		f = 1 kHz, A_V = 1, R_L = 600Ω V_O = 0.9 V_{PP}		0.004		

(6) The short circuit test is a momentary open loop test.

5V Electrical Characteristics

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min[(1)]	Typ[(2)]	Max[(1)]	Units
V_{OS}	Input Offset Voltage	−20°C ≤ T_A ≤ 85°C			±10	±150 **±300**	μV
		−40°C ≤ T_A ≤ 125°C			±10	±150 **±400**	
TC V_{OS}	Input Offset Voltage Temperature Drift[(3)(4)]				–1.75	±4	μV/°C
I_B	Input Bias Current	V_{CM} = 2.0V[(5)(4)]	−40°C ≤ T_A ≤ 85°C		0.1	1 **25**	pA
			−40°C ≤ T_A ≤ 125°C		0.1	1 **100**	
I_{OS}	Input Offset Current	V_{CM} = 2.0V[(4)]			0.01	0.5 **50**	pA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3.7V		85 **82**	100		dB
PSRR	Power Supply Rejection Ratio	2.0V ≤ V^+ ≤ 5.5V V^- = 0V, V_{CM} = 0		85 **80**	100		dB
		1.8V ≤ V^+ ≤ 5.5V V^- = 0V, V_{CM} = 0		85	98		
CMVR	Common Mode Voltage Range	CMRR ≥ 80 dB CMRR ≥ 78 dB		−0.3 **−0.3**		4 **4**	V
A_{VOL}	Open Loop Voltage Gain	V_O = 0.3 to 4.7V R_L = 2 kΩ to V^+/2		84 **80**	90		dB
		V_O = 0.3 to 4.7V R_L = 10 kΩ to V^+/2		90 **86**	95		
V_{OUT}	Output Voltage Swing High	R_L = 2 kΩ to V^+/2			32	70 **77**	mV from either rail
		R_L = 10 kΩ to V^+/2			22	60 **66**	
	Output Voltage Swing Low	R_L = 2 kΩ to V^+/2			45	75 **78**	
		R_L = 10 kΩ to V^+/2			20	60 **62**	
I_{OUT}	Output Current	Sourcing to V^- V_{IN} = 200 mV[(6)]		46 **38**	66		mA
		Sinking to V^+ V_{IN} = −200 mV[(6)]		10.5 **6.5**	23		
I_S	Supply Current	(per channel)			1.30	1.70 **2.05**	mA

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(3) Offset voltage average drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(4) This parameter is specified by design and/or characterization and is not tested in production.
(5) Positive current corresponds to current flowing into the device.
(6) The short circuit test is a momentary open loop test.

5V Electrical Characteristics (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min [1]	Typ [2]	Max [1]	Units
SR	Slew Rate	A_V = +1, Rising (10% to 90%)	6.0	9.5		V/μs
		A_V = +1, Falling (90% to 10%)	7.5	11.5		
GBW	Gain Bandwidth			17		MHz
e_n	Input Referred Voltage Noise Density	f = 400 Hz		7.0		nV/√Hz
		f = 1 kHz		5.8		
i_n	Input Referred Current Noise Density	f = 1 kHz		0.01		pA/√Hz
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, R_L = 100 kΩ V_O = 4 V_{PP}		0.001		%
		f = 1 kHz, A_V = 1, R_L = 600Ω V_O = 4 V_{PP}		0.004		

Connection Diagram

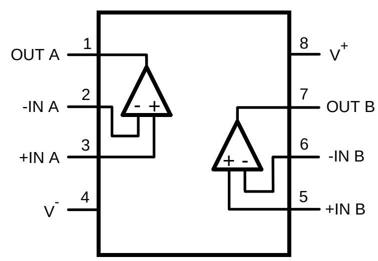


Figure 1. 8-Pin VSSOP – Top View
See Package Number DGK

Typical Performance Characteristics

Unless otherwise noted: T_A = 25°C, V_S = 5V, V_{CM} = V_S/2.

Offset Voltage Distribution

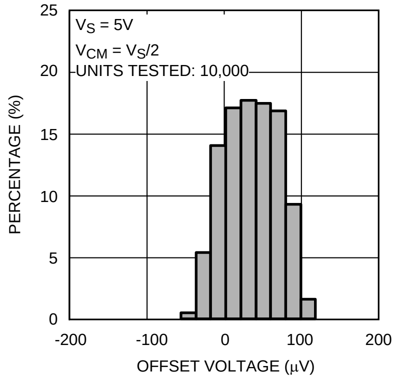


Figure 2.

Input Referred Voltage Noise

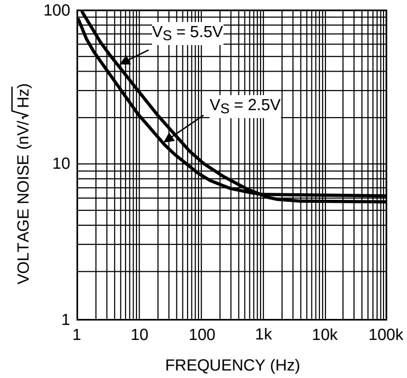


Figure 3.

Offset Voltage Distribution

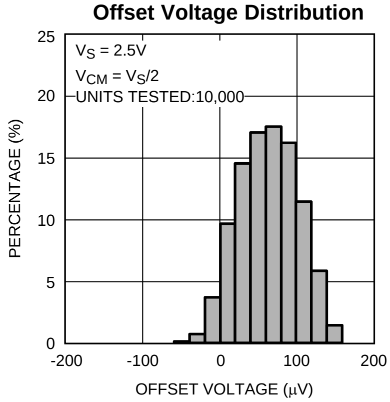


Figure 4.

Offset Voltage Distribution

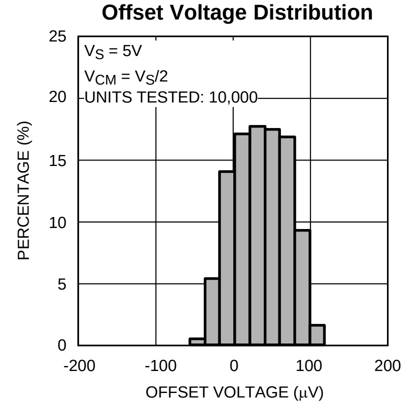


Figure 5.

TCV$_{OS}$ Distribution

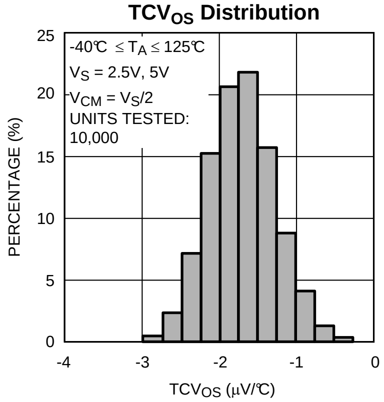


Figure 6.

Offset Voltage vs. V$_{CM}$

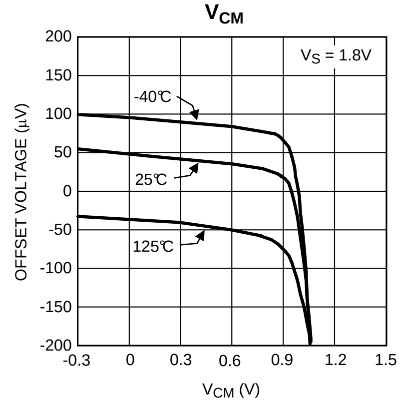


Figure 7.

Typical Performance Characteristics (continued)

Unless otherwise noted: T_A = 25°C, V_S = 5V, V_{CM} = V_S/2.

Offset Voltage vs. V_{CM}

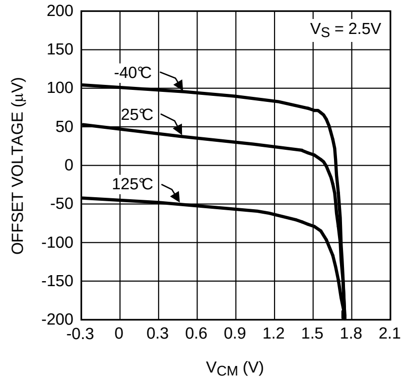


Figure 8.

Offset Voltage vs. V_{CM}

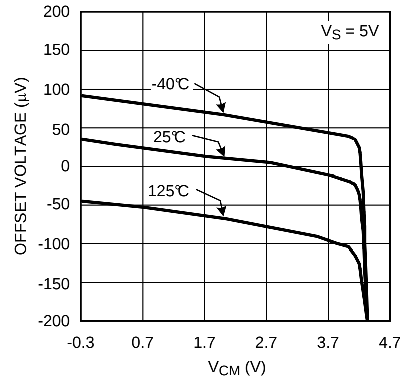


Figure 9.

Offset Voltage vs. Supply Voltage

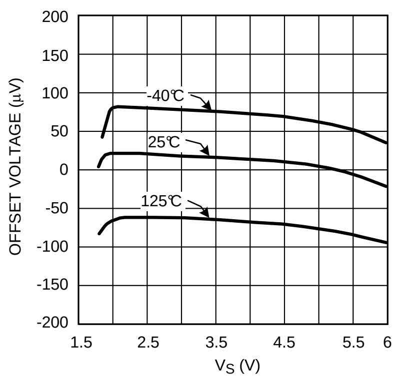


Figure 10.

CMRR vs. Frequency

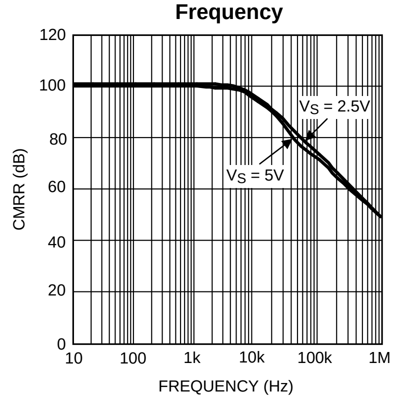


Figure 11.

Input Bias Current vs. V_{CM}

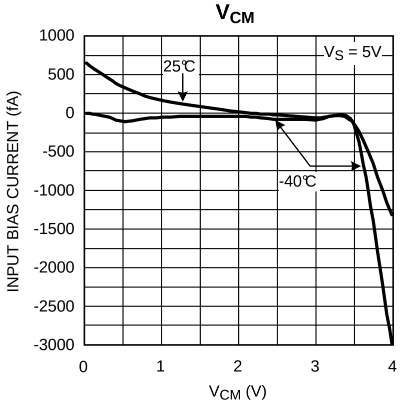


Figure 12.

Input Bias Current vs. V_{CM}

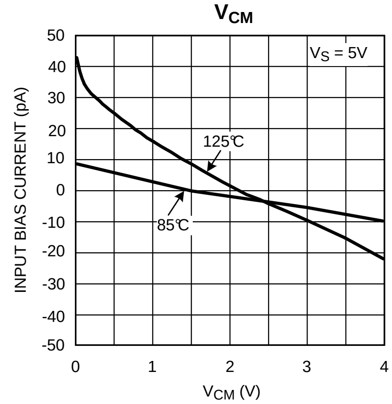


Figure 13.

Typical Performance Characteristics (continued)

Unless otherwise noted: T_A = 25°C, V_S = 5V, V_{CM} = V_S/2.

Supply Current vs. Supply Voltage

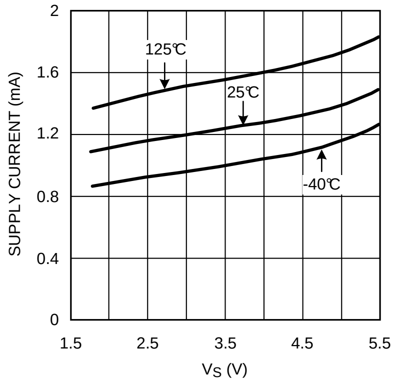


Figure 14.

Crosstalk Rejection Ratio

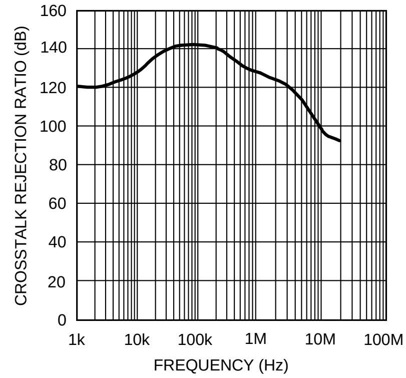


Figure 15.

Sourcing Current vs. Supply Voltage

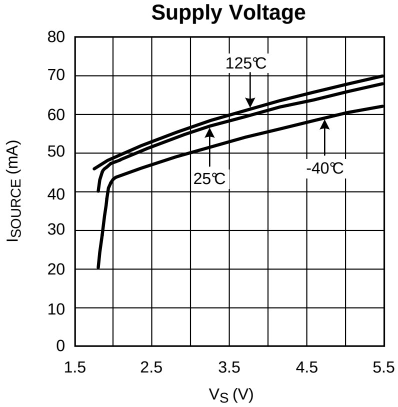


Figure 16.

Sinking Current vs. Supply Voltage

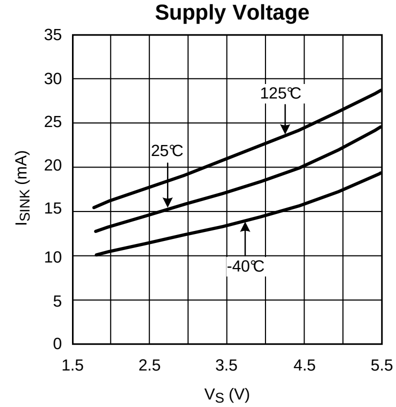


Figure 17.

Sourcing Current vs. Output Voltage

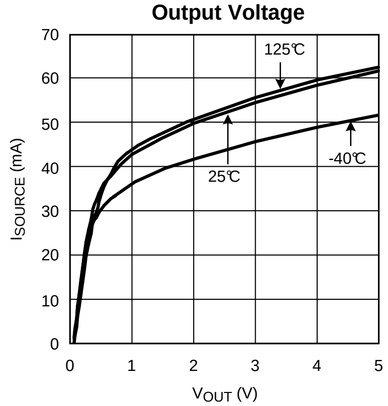


Figure 18.

Sinking Current vs. Output Voltage

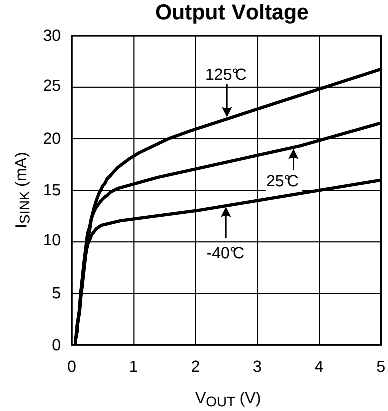


Figure 19.

Typical Performance Characteristics (continued)

Unless otherwise noted: T_A = 25°C, V_S = 5V, V_{CM} = V_S/2.

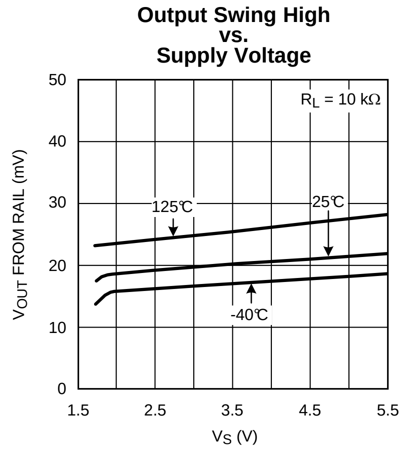


Figure 20.

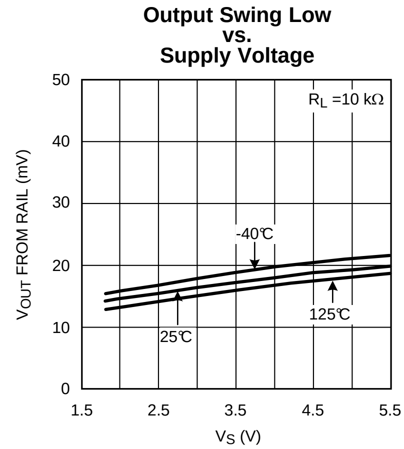


Figure 21.

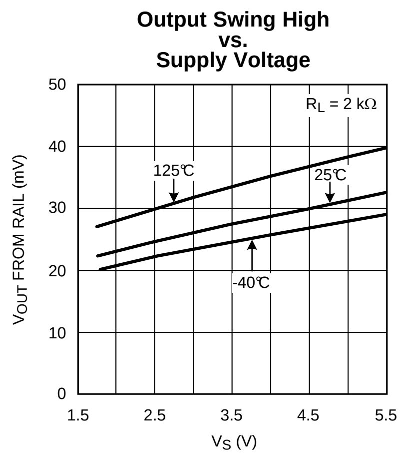


Figure 22.

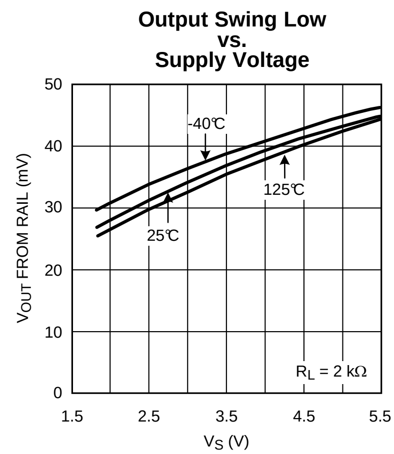


Figure 23.

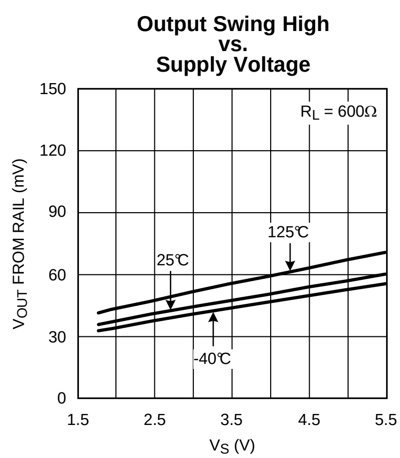


Figure 24.

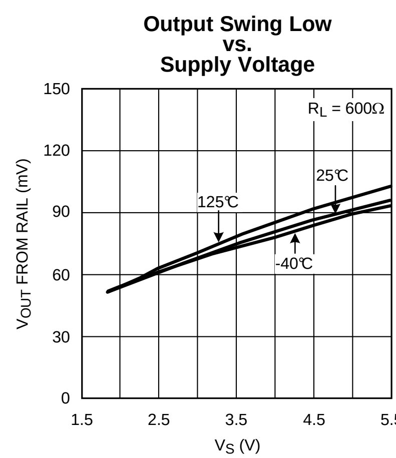


Figure 25.

Typical Performance Characteristics (continued)

Unless otherwise noted: $T_A = 25°C$, $V_S = 5V$, $V_{CM} = V_S/2$.

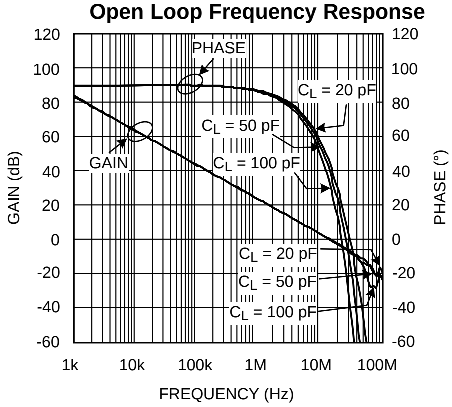


Figure 26.

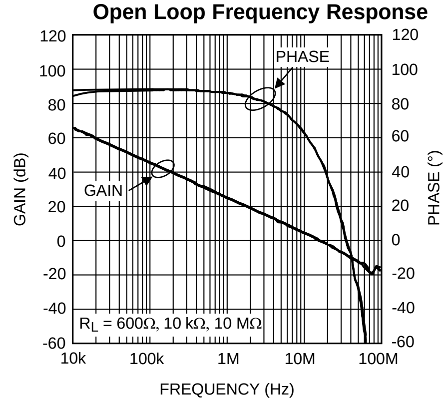


Figure 27.

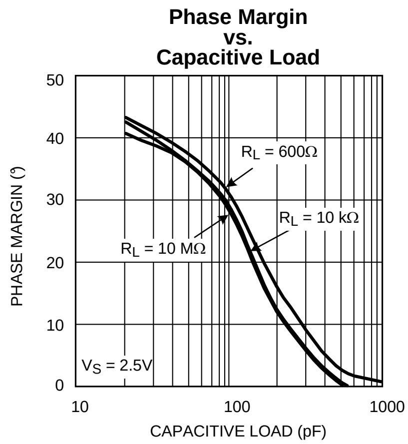


Figure 28.

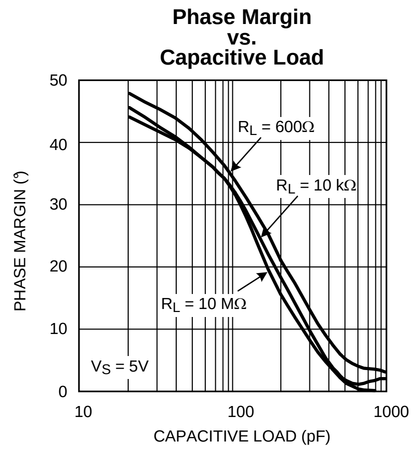


Figure 29.

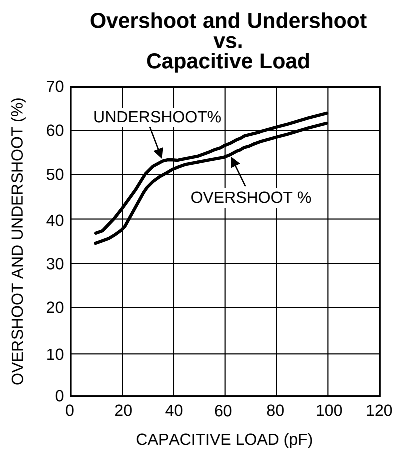


Figure 30.

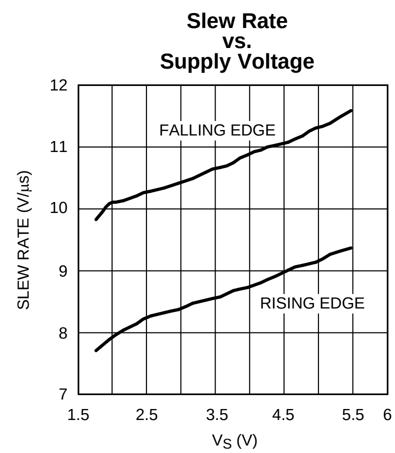


Figure 31.

Typical Performance Characteristics (continued)

Unless otherwise noted: T_A = 25°C, V_S = 5V, V_{CM} = V_S/2.

Small Signal Step Response

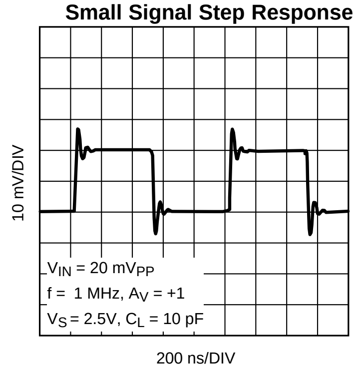


Figure 32.

Large Signal Step Response

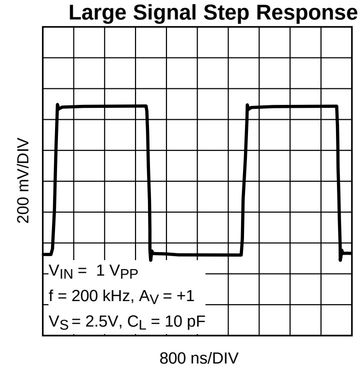


Figure 33.

Small Signal Step Response

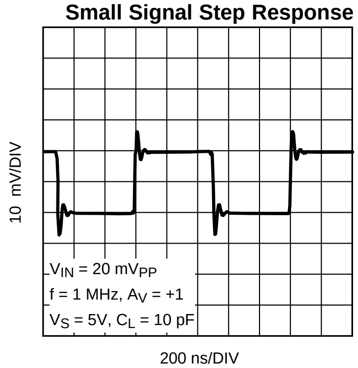


Figure 34.

Large Signal Step Response

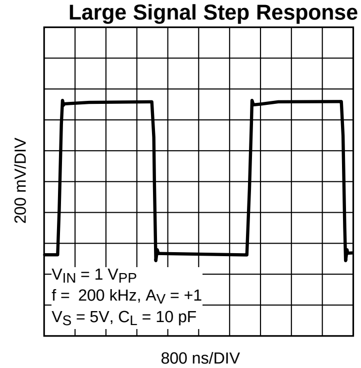


Figure 35.

THD+N vs. Output Voltage

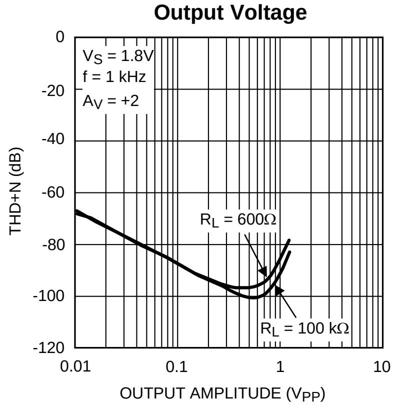


Figure 36.

THD+N vs. Output Voltage

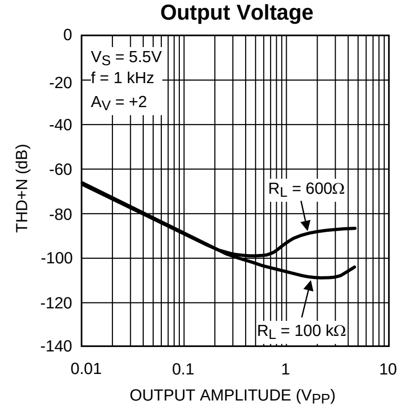


Figure 37.

Typical Performance Characteristics (continued)

Unless otherwise noted: T_A = 25°C, V_S = 5V, V_{CM} = V_S/2.

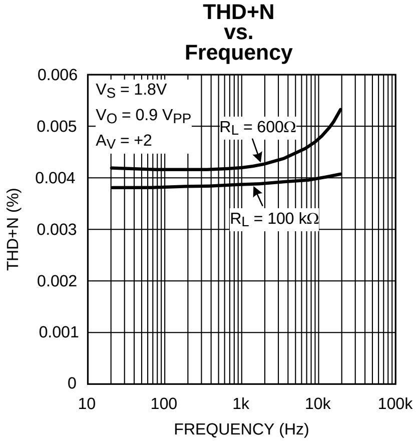


Figure 38.

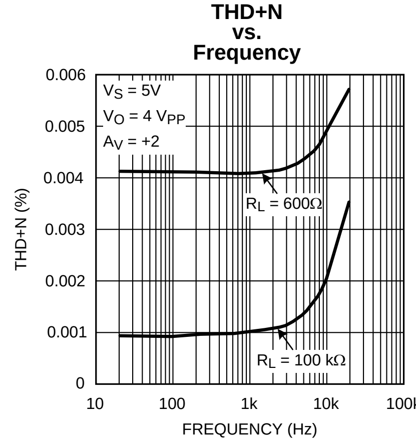


Figure 39.

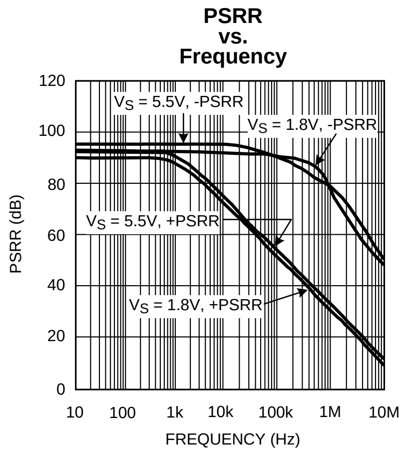


Figure 40.

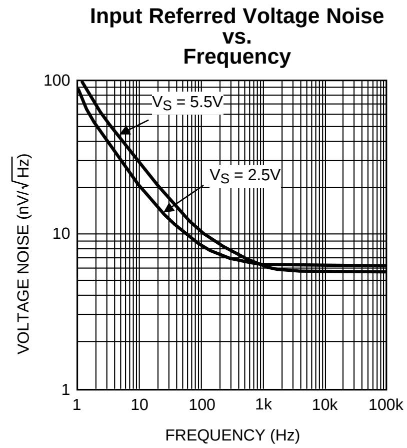


Figure 41.

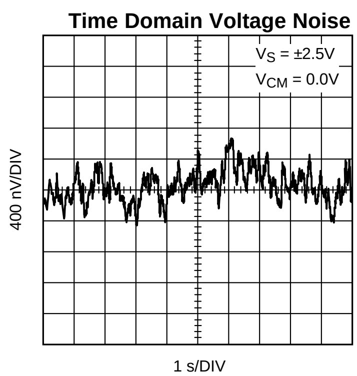


Figure 42.

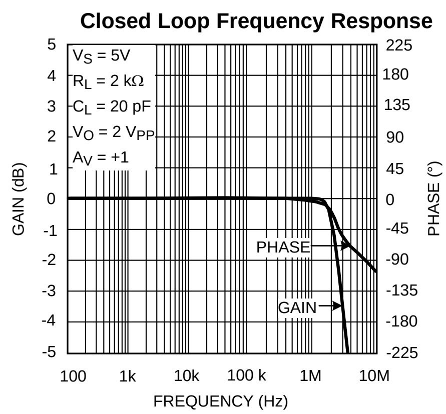


Figure 43.

Typical Performance Characteristics (continued)

Unless otherwise noted: T_A = 25°C, V_S = 5V, V_{CM} = V_S/2.

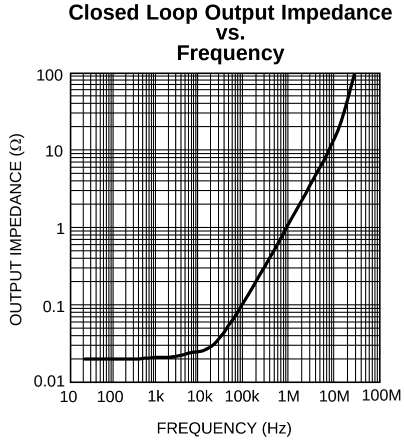


Figure 44.

APPLICATION INFORMATION

The SM73307 is a dual, low noise, low offset, rail-to-rail output precision amplifier with a wide gain bandwidth product of 17 MHz and low supply current. The wide bandwidth makes the SM73307 an ideal choice for wide-band amplification in photovoltaic and portable applications.

The SM73307 is superior for sensor applications. The very low input referred voltage noise of only 5.8 nV/$\sqrt{Hz}$ at 1 kHz and very low input referred current noise of only 10 fA/$\sqrt{Hz}$ mean more signal fidelity and higher signal-to-noise ratio.

The SM73307 has a supply voltage range of 1.8V to 5.5V over a wide temperature range of 0°C to 125°C. This is optimal for low voltage commercial applications. For applications where the ambient temperature might be less than 0°C, the SM73307 is fully operational at supply voltages of 2.0V to 5.5V over the temperature range of −40°C to 125°C.

The outputs of the SM73307 swing within 25 mV of either rail providing maximum dynamic range in applications requiring low supply voltage. The input common mode range of the SM73307 extends to 300 mV below ground. This feature enables users to utilize this device in single supply applications.

The use of a very innovative feedback topology has enhanced the current drive capability of the SM73307, resulting in sourcing currents of as much as 47 mA with a supply voltage of only 1.8V.

The SM73307 is offered in an 8-pin VSSOP package. This small package is an ideal solution for applications requiring minimum PC board footprint.

CAPACITIVE LOAD

The unity gain follower is the most sensitive configuration to capacitive loading. The combination of a capacitive load placed directly on the output of an amplifier along with the output impedance of the amplifier creates a phase lag which in turn reduces the phase margin of the amplifier. If phase margin is significantly reduced, the response will be either under-damped or the amplifier will oscillate.

The SM73307 can directly drive capacitive loads of up to 120 pF without oscillating. To drive heavier capacitive loads, an isolation resistor, R_{ISO} as shown in Figure 45, should be used. This resistor and C_L form a pole and hence delay the phase lag or increase the phase margin of the overall system. The larger the value of R_{ISO}, the more stable the output voltage will be. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive.

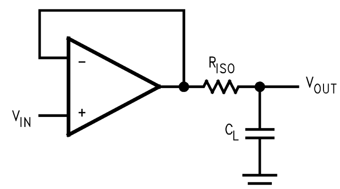


Figure 45. Isolating Capacitive Load

INPUT CAPACITANCE

CMOS input stages inherently have low input bias current and higher input referred voltage noise. The SM73307 enhances this performance by having the low input bias current of only 50 fA, as well as, a very low input referred voltage noise of 5.8 nV/$\sqrt{Hz}$. In order to achieve this a larger input stage has been used. This larger input stage increases the input capacitance of the SM73307. Figure 46 shows typical input common mode capacitance of the SM73307.

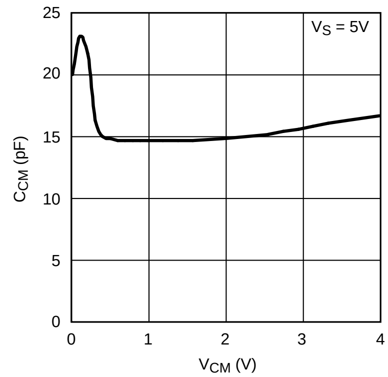
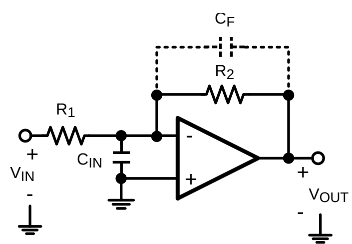


Figure 46. Input Common Mode Capacitance

This input capacitance will interact with other impedances, such as gain and feedback resistors which are seen on the inputs of the amplifier, to form a pole. This pole will have little or no effect on the output of the amplifier at low frequencies and under DC conditions, but will play a bigger role as the frequency increases. At higher frequencies, the presence of this pole will decrease phase margin and also cause gain peaking. In order to compensate for the input capacitance, care must be taken in choosing feedback resistors. In addition to being selective in picking values for the feedback resistor, a capacitor can be added to the feedback path to increase stability.

The DC gain of the circuit shown in Figure 47 is simply $-R_2/R_1$.



$$A_V = -\frac{V_{OUT}}{V_{IN}} = -\frac{R_2}{R_1}$$

Figure 47. Compensating for Input Capacitance

For the time being, ignore C_F. The AC gain of the circuit in Figure 47 can be calculated as follows:

$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-R_2/R_1}{\left[1 + \frac{s}{\left(\frac{A_0 R_1}{R_1 + R_2}\right)} + \frac{s^2}{\left(\frac{A_0}{C_{IN} R_2}\right)}\right]} \quad (1)$$

This equation is rearranged to find the location of the two poles:

$$P_{1,2} = \frac{-1}{2C_{IN}}\left[\frac{1}{R_1} + \frac{1}{R_2} \pm \sqrt{\left(\frac{1}{R_1} + \frac{1}{R_2}\right)^2 - \frac{4 A_0 C_{IN}}{R_2}}\right] \quad (2)$$

As shown in Equation 2, as the values of R_1 and R_2 are increased, the magnitude of the poles are reduced, which in turn decreases the bandwidth of the amplifier. Figure 48 shows the frequency response with different value resistors for R_1 and R_2. Whenever possible, it is best to choose smaller feedback resistors.

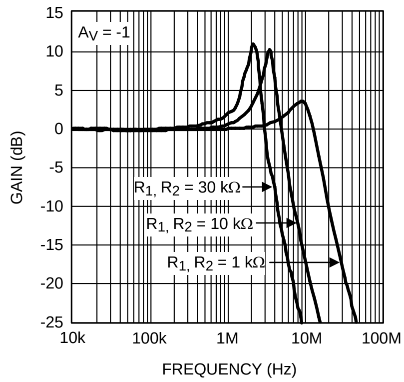


Figure 48. Closed Loop Frequency Response

As mentioned before, adding a capacitor to the feedback path will decrease the peaking. This is because C_F will form yet another pole in the system and will prevent pairs of poles, or complex conjugates from forming. It is the presence of pairs of poles that cause the peaking of gain. Figure 49 shows the frequency response of the schematic presented in Figure 47 with different values of C_F. As can be seen, using a small value capacitor significantly reduces or eliminates the peaking.

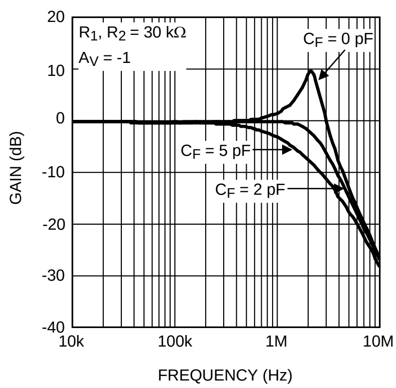
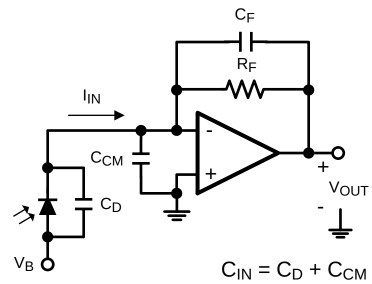


Figure 49. Closed Loop Frequency Response

TRANSIMPEDANCE AMPLIFIER

In many applications the signal of interest is a very small amount of current that needs to be detected. Current that is transmitted through a photodiode is a good example. Barcode scanners, light meters, fiber optic receivers, and industrial sensors are some typical applications utilizing photodiodes for current detection. This current needs to be amplified before it can be further processed. This amplification is performed using a current-to-voltage converter configuration or transimpedance amplifier. The signal of interest is fed to the inverting input of an op amp with a feedback resistor in the current path. The voltage at the output of this amplifier will be equal to the negative of the input current times the value of the feedback resistor. Figure 50 shows a transimpedance amplifier configuration. C_D represents the photodiode parasitic capacitance and C_{CM} denotes the common-mode capacitance of the amplifier. The presence of all of these capacitances at higher frequencies might lead to less stable topologies at higher frequencies. Care must be taken when designing a transimpedance amplifier to prevent the circuit from oscillating.

With a wide gain bandwidth product, low input bias current and low input voltage and current noise, the SM73307 is ideal for wideband transimpedance applications.



$$C_{IN} = C_D + C_{CM}$$

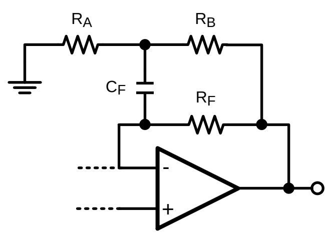
$$\frac{V_{OUT}}{I_{IN}} = -R_F$$

Figure 50. Transimpedance Amplifier

A feedback capacitance C_F is usually added in parallel with R_F to maintain circuit stability and to control the frequency response. To achieve a maximally flat, 2^{nd} order response, R_F and C_F should be chosen by using Equation 3:

$$C_F = \sqrt{\frac{C_{IN}}{GBWP * 2\pi R_F}} \quad (3)$$

Calculating C_F from Equation 3 can sometimes result in capacitor values which are less than 2 pF. This is especially the case for high speed applications. In these instances, it is often more practical to use the circuit shown in Figure 51 in order to allow more sensible choices for C_F. The new feedback capacitor, C_F', is $(1+ R_B/R_A)\ C_F$. This relationship holds as long as $R_A << R_F$.



IF $R_A << R_F$

$$C_F' = \left(1 + \frac{R_B}{R_A}\right) C_F$$

Figure 51. Modified Transimpedance Amplifier

SENSOR INTERFACE

The SM73307 has a low input bias current and low input referred noise, which makes it an ideal choice for sensor interfaces such as thermopiles, Infra Red (IR) thermometry, thermocouple amplifiers, and pH electrode buffers.

Thermopiles generate voltage in response to receiving radiation. These voltages are often only a few microvolts. As a result, the operational amplifier used for this application needs to have low offset voltage, low input voltage noise, and low input bias current. Figure 52 shows a thermopile application where the sensor detects radiation from a distance and generates a voltage that is proportional to the intensity of the radiation. The two resistors, R_A and R_B, are selected to provide high gain to amplify this signal, while C_F removes the high frequency noise.

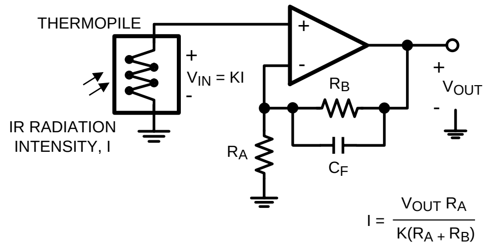


Figure 52. Thermopile Sensor Interface

PRECISION RECTIFIER

Rectifiers are electrical circuits used for converting AC signals to DC signals. Figure 53 shows a full-wave precision rectifier. Each operational amplifier used in this circuit has a diode on its output. This means for the diodes to conduct, the output of the amplifier needs to be positive with respect to ground. If V_{IN} is in its positive half cycle then only the output of the bottom amplifier will be positive. As a result, the diode on the output of the bottom amplifier will conduct and the signal will show at the output of the circuit. If V_{IN} is in its negative half cycle then the output of the top amplifier will be positive, resulting in the diode on the output of the top amplifier conducting and delivering the signal from the amplifier's output to the circuit's output.

For $R_2/ R_1 \geq 2$, the resistor values can be found by using the equation shown in Figure 53. If $R_2/ R_1 = 1$, then R_3 should be left open, no resistor needed, and R_4 should simply be shorted.

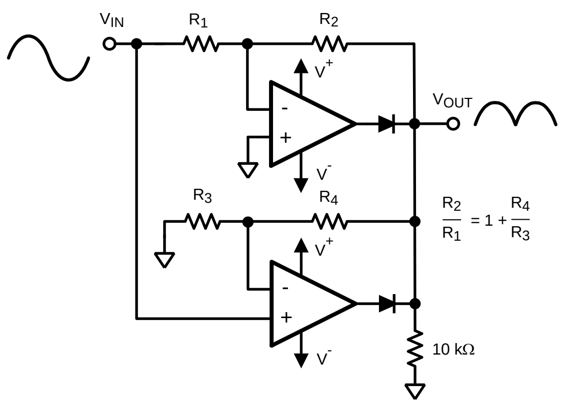


Figure 53. Precision Rectifier

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SM73307MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S307	Samples
SM73307MME/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S307	Samples
SM73307MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S307	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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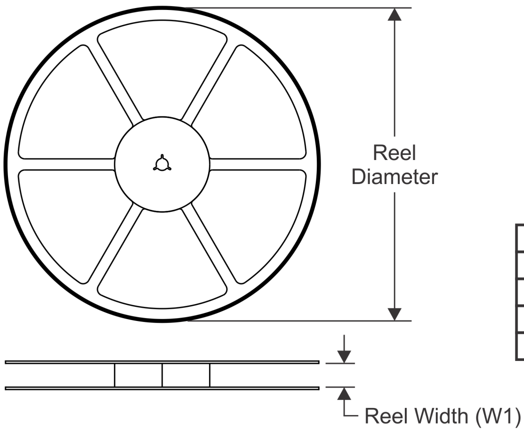
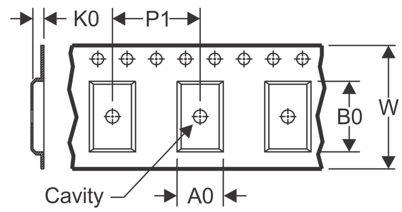
TAPE AND REEL INFORMATION

REEL DIMENSIONS

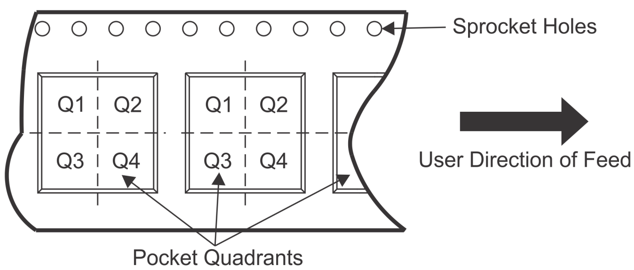


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

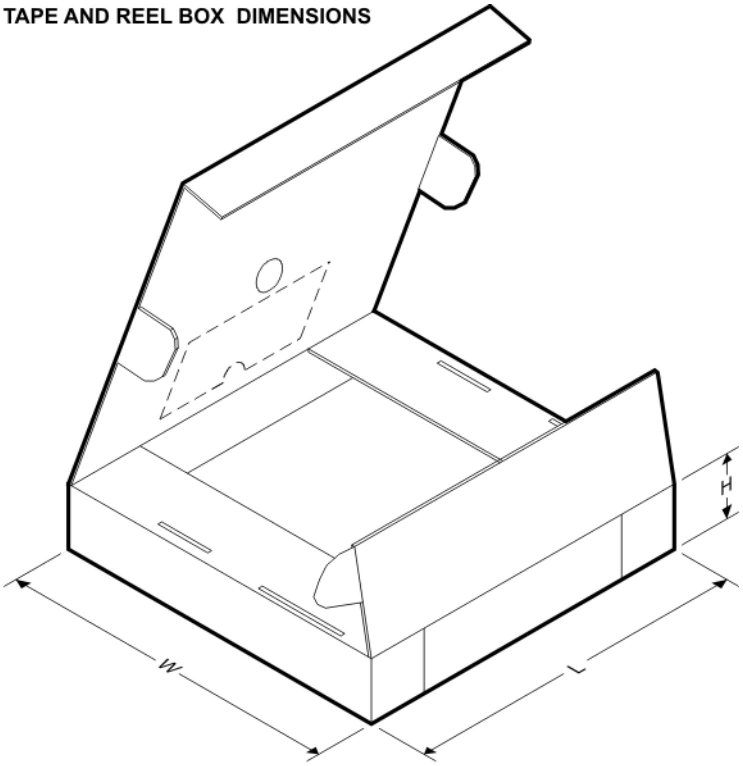
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SM73307MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SM73307MME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SM73307MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

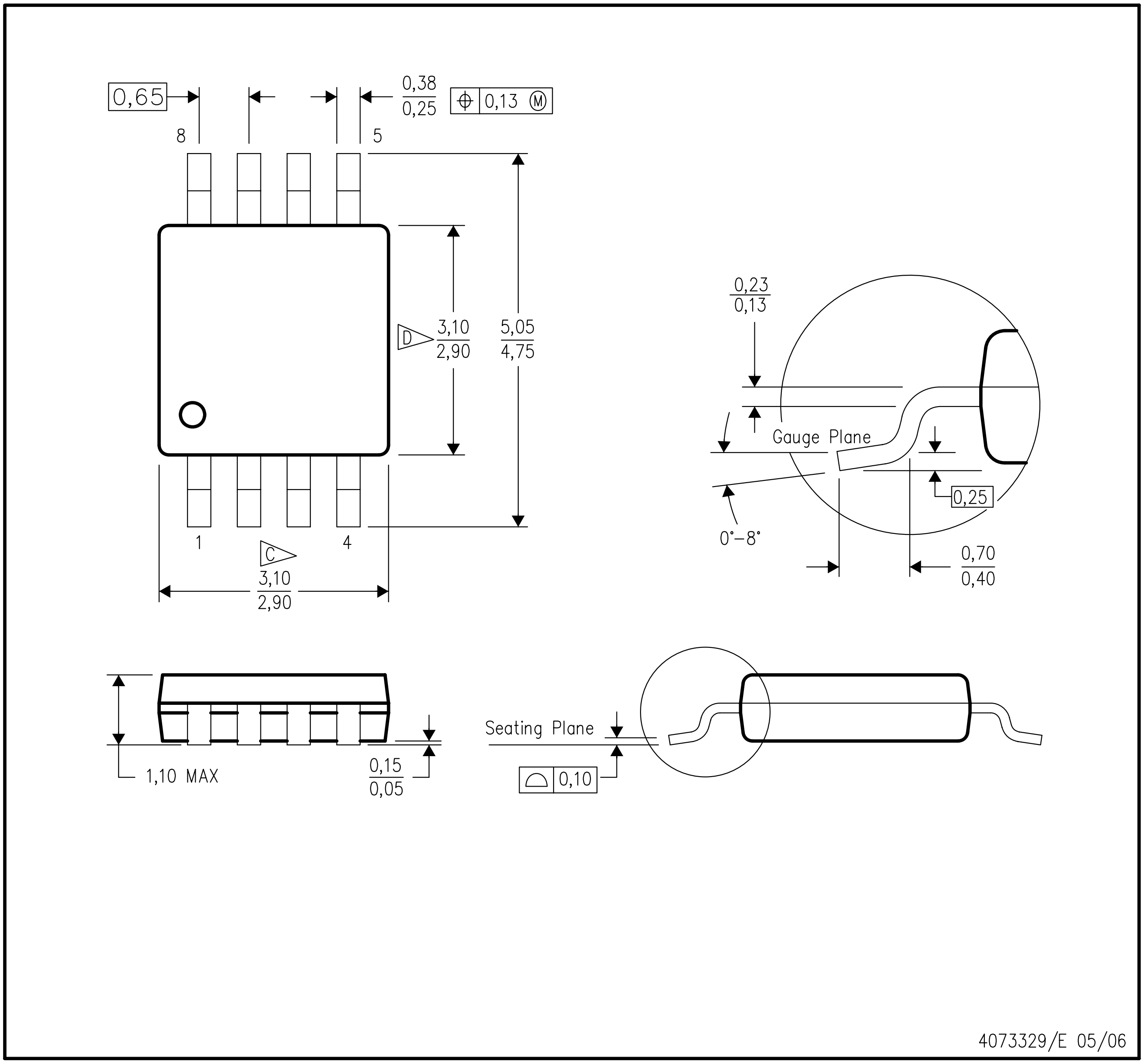
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SM73307MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
SM73307MME/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
SM73307MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

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