



## SM843251-156

### ClockWorks™ 10-Gigabit Ethernet, 156.25MHz, Ultra-Low Jitter LVPECL Clock Frequency Synthesizer

#### General Description

The SM843251-156 is a 10-Gigabit Ethernet, 156.25MHz LVPECL clock frequency synthesizer and a member of the ClockWorks™ family of devices from Micrel. It provides a low-noise timing solution for high-speed, high-accuracy synthesis of clock signals. It includes a patented RotaryWave® architecture that provides a very stable clock with very low noise.

Power supplies of either 2.5V or 3.3V are supported, with superior jitter and phase noise performance. The device synthesizes a 156.25MHz, low-noise, LVPECL output for Ethernet applications. The crystal reference frequency is 25MHz.

The SM843251-156 is an excellent replacement for IDT FemtoClocks®, with improved waveform integrity, and jitter.

Data sheets and support documentation can be found on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

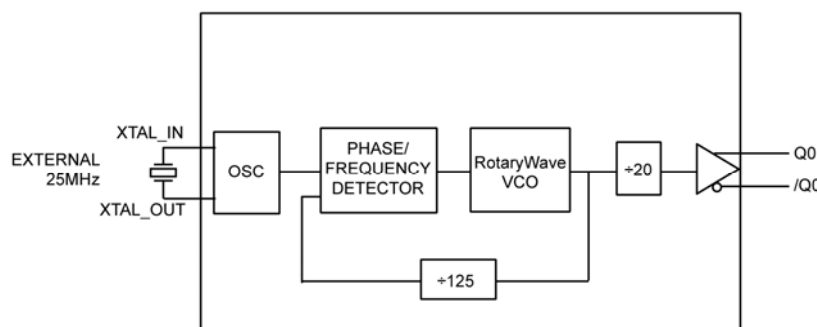
#### Features

- Generates a low-noise 156.25MHz LVPECL output
- 2.5V or 3.3V operating voltage
- Typical phase jitter @156.25MHz~110fs (1.875MHz – 20MHz)
- Crystal frequency: 25MHz
- 156.25MHz output frequency
- Phase Noise @ 156.25MHz:
  - 1kHz: –123dBc/Hz
  - 10kHz: –130dBc/Hz
  - 100kHz: –135dBc/Hz
  - 1MHz: –140dBc/Hz
  - 10MHz: –161dBc/Hz
  - 20MHz: –166/dBc/Hz
- Industrial temperature range
- Green-, RoHS-, and PFOS-compliant
- Available in 8-pin TSSOP

#### Applications

- Gigabit Ethernet
- 10-Gigabit Ethernet

#### Block Diagram



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RotaryWave is a registered trademark of Multigig, Inc.  
FemtoClocks is a registered trademark of IDT, Inc.

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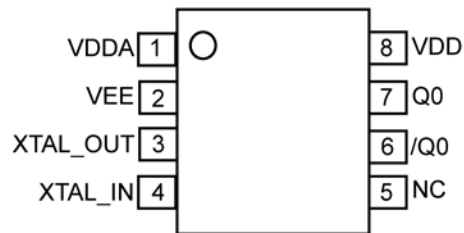
## Ordering Information<sup>(1)</sup>

Part Number	Package Type	Operating Range	Package Marking
SM843251-156KA	K-8	Industrial	843251-156
SM843251-156KA TR <sup>(2)</sup>	K-8	Industrial	843251-156

### Notes:

1. Devices are Green-, RoHS-, and PFOS-compliant.
2. Tape and Reel.

## Pin Configuration



8-Pin TSSOP (K-8)

## Pin Description

Pin Number	Pin Name	Type	Level	Pin Function
1	V <sub>DDA</sub>	PWR		Analog 2.5V or 3.3V Power Supply. No filter resistor needed.
2	V <sub>EE</sub>	PWR		Ground.
3	XTAL_OUT	O, (SE)	12pF crystal	Crystal Reference Output, no load caps needed.
4	XTAL_IN	I, (SE)	12pF crystal	Crystal Reference Input, no load caps needed.
5	NC	–		No Connect
6	/Q0	O, (DIF)	LVPECL	Differential Clock Output
7	Q0	O, (DIF)	LVPECL	Differential Clock Output
8	V <sub>DD</sub>	PWR		2.5V or 3.3V Power Supply

**Absolute Maximum Ratings<sup>(1)</sup>**

Supply Voltage ( $V_{DDA}$ , $V_{DD}$ )	+4.6V
Input Voltage ( $V_{IN}$ )	-0.50V to $V_{DD} + 0.5V$
LVPECL Output Current ( $I_{OUT}$ )	
Continuous	50mA
Surge	100mA
Lead Temperature (soldering, 20sec.)	260°C
Case Temperature	115°C
Storage Temperature ( $T_s$ )	-65°C to +150°C

**Operating Ratings<sup>(2)</sup>**

Supply Voltage ( $V_{DD}$ , $V_{DDA}$ )	+2.375 to +3.465
Ambient Temperature ( $T_A$ )	-40°C to +85°C
Junction Thermal Resistance	
TSSOP ( $\theta_{JA}$ )(Still Air)	141°C/W

**DC Electrical Characteristics<sup>(3)</sup>**

$V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{DD}$	Core Supply Voltage		3.135	3.30	3.465	V
$V_{DDA}$	Analog Supply Voltage		3.135	3.30	3.465	V
$I_{DDA}$	Analog Supply Current	Included in $I_{EE}$		50	60	mA
$I_{EE}$	Total Supply Current	No load		88	110	mA

$V_{DD} = V_{DDA} = 2.5V \pm 5\%$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{DD}$	Core Supply Voltage		2.375	2.50	2.625	V
$V_{DDA}$	Analog Supply Voltage		2.375	2.50	2.625	V
$I_{DDA}$	Analog Supply Current	Included in $I_{EE}$		50	60	mA
$I_{EE}$	Total Supply Current	No load		80	100	mA

**LVPECL DC Electrical Characteristics<sup>(3, 4)</sup>**

$V_{DD} = V_{DDA} = 2.5V \pm 5\%$  or  $3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{OH}$	Output High Voltage	$50\Omega$ to $V_{DD} - 2V$	$V_{DD} - 1.145$	$V_{DD} - 0.97$	$V_{DD} - 0.845$	V
$V_{OL}$	Output Low Voltage	$50\Omega$ to $V_{DD} - 2V$	$V_{DD} - 1.945$	$V_{DD} - 1.77$	$V_{DD} - 1.645$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6	0.8	1.0	V

**Notes:**

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established with a transverse airflow greater than 500 lfm.
4. See Figure 4 for load test circuit example.

## AC Electrical Characteristics<sup>(5)</sup>

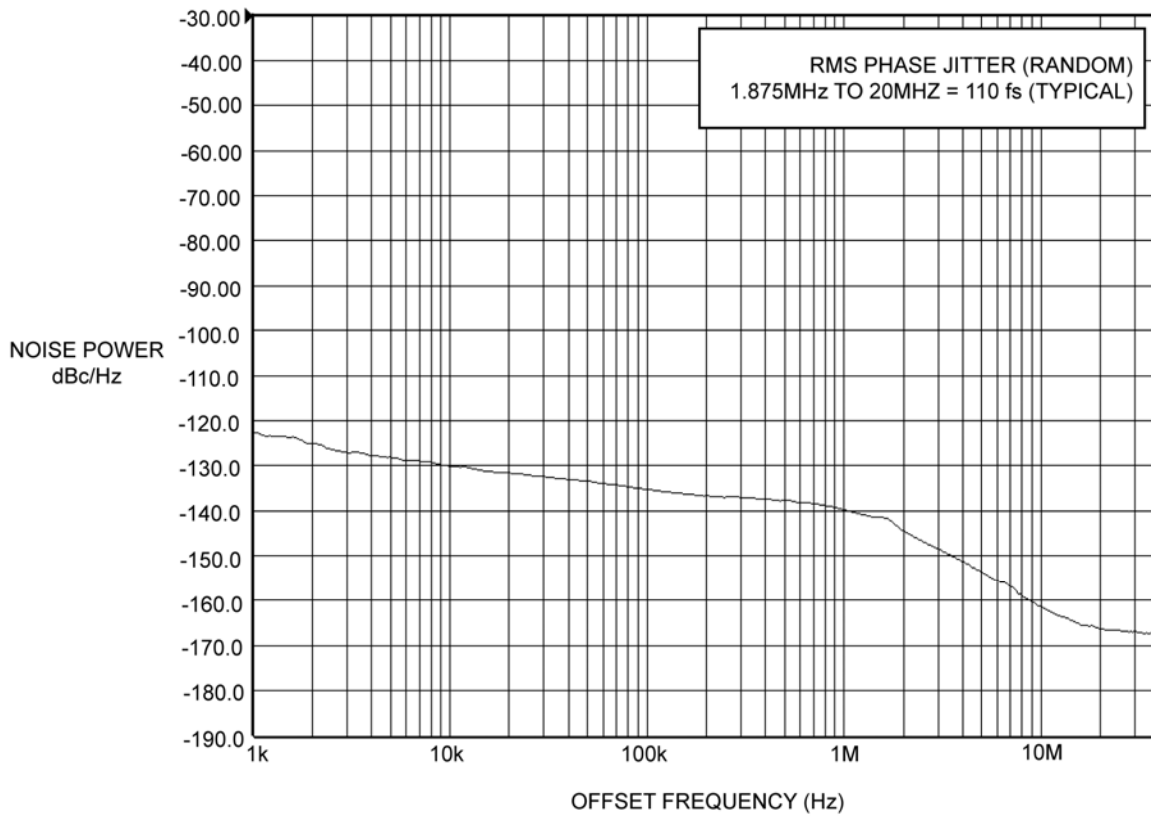
$V_{DD} = V_{DDA} = 2.5V \pm 5\%$  or  $3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$F_{OUT}$	Output Frequency	25MHz Crystal		156.25		MHz
$t_{JITTER}$	RMS Phase Jitter (Output = 156.25 MHz)	Integration Range: 1.875MHz to 20MHz		110		fs
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	80	175	350	ps
$O_{DC}$	Output Duty Cycle		48	50	52	%

- Note:**
- The circuit is designed to meet the AC specifications shown in the above table(s) after thermal equilibrium has been established with a transverse airflow greater than 500 lfpm.

## Crystal Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units
Mode of Oscillation	12pF Load	Fundamental, Parallel Resonant			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitor, C0			3	7	pF
Correlation Drive Level			100	300	$\mu W$



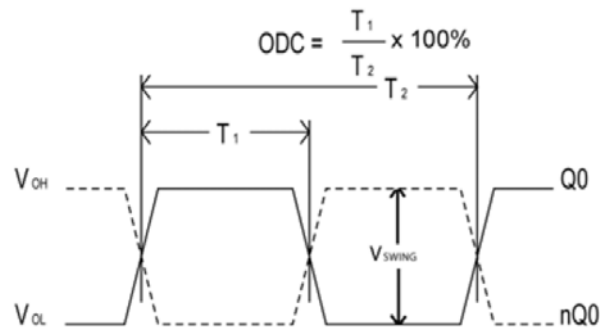


Figure 1. Duty Cycle Timing

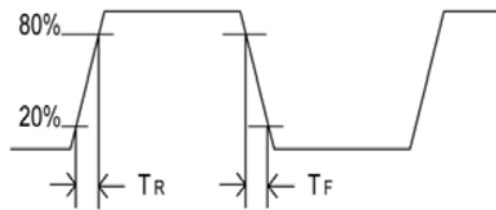
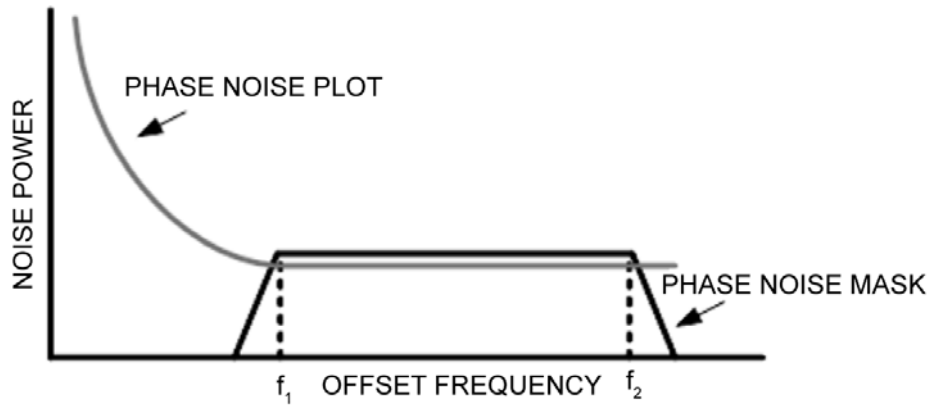


Figure 2. All Outputs Rise/Fall Time



$$RMS\ JITTER = \sqrt{\text{AREA UNDER THE MASKED PHASE NOISE PLOT}}$$

Figure 3. RMS Phase Noise/Jitter

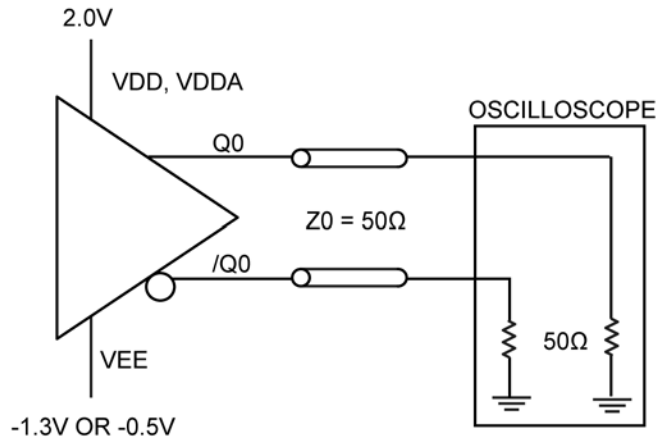


Figure 4. LVPECL Output Load and Test Circuit

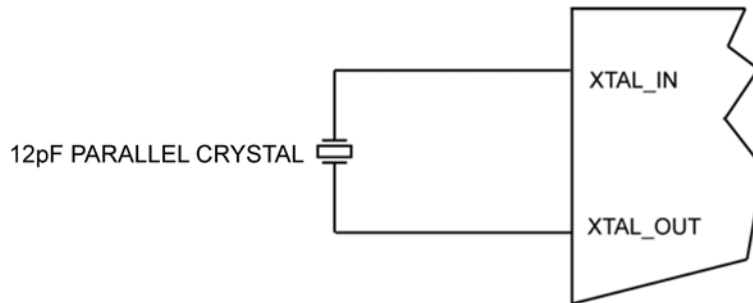
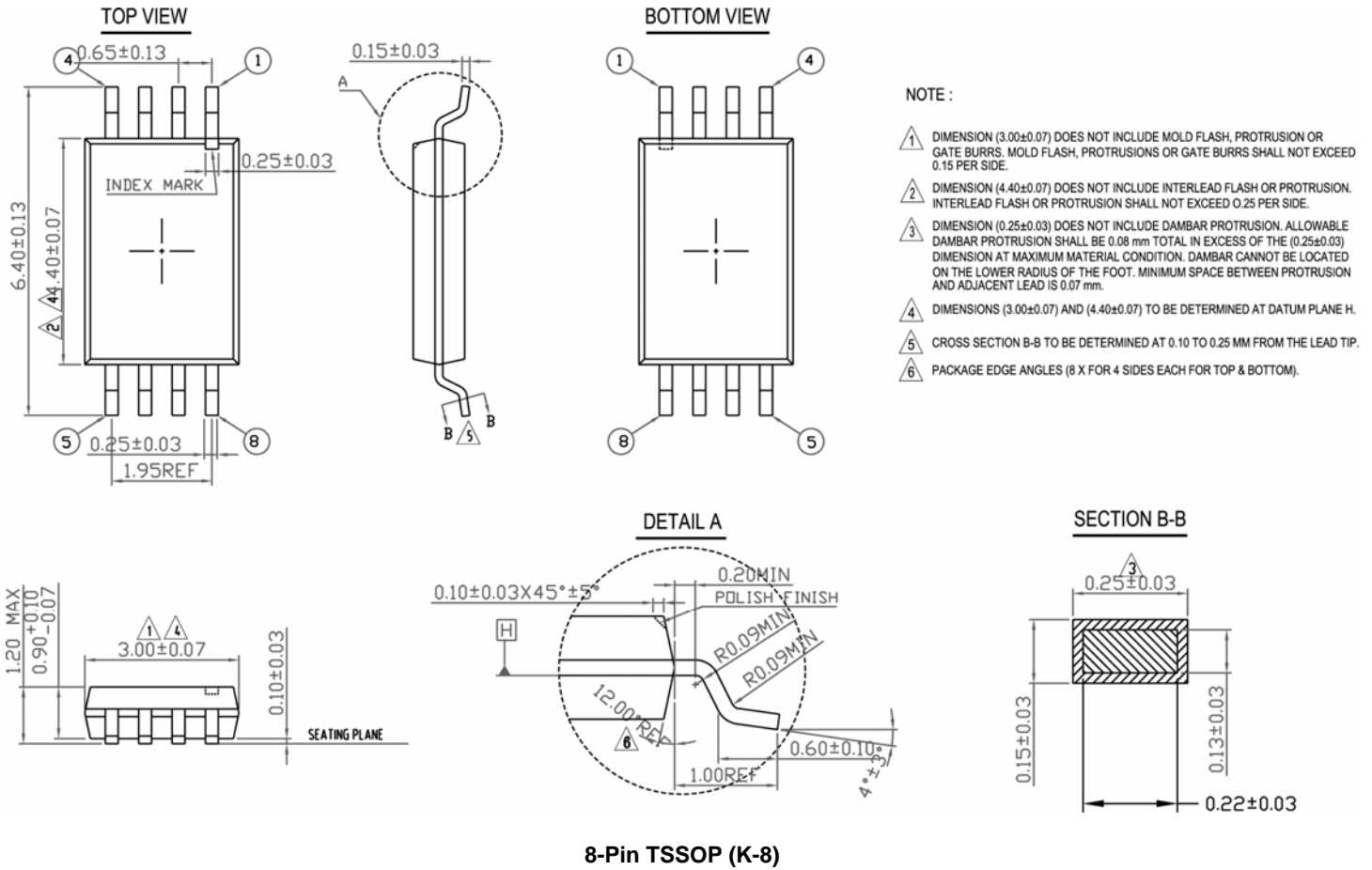


Figure 5. Crystal Input Interface

### Package Information



**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**  
 TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB <http://www.micrel.com>

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