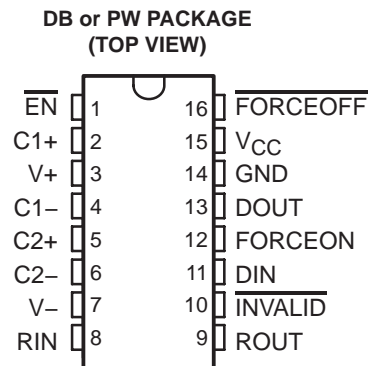


- **Qualified for Automotive Applications**
- **Operates With 3-V to 5.5-V  $V_{CC}$  Supply**
- **Operates Up To 1 Mbit/s**
- **Low Standby Current . . . 1  $\mu$ A Typical**
- **External Capacitors . . .  $4 \times 0.1 \mu$ F**
- **Accepts 5-V Logic Input With 3.3-V Supply**
- **RS-232 Bus-Pin ESD Protection Exceeds  $\pm 15$  kV Using Human-Body Model (HBM)**
- **Auto-Powerdown Feature Automatically Disables Drivers for Power Savings**
- **Applications**
  - Battery-Powered, Hand-Held, and Portable Equipment
  - PDAs and Palmtop PCs
  - Notebooks, Sub-Notebooks, and Laptops
  - Digital Cameras
  - Mobile Phones and Wireless Devices



### description/ordering information

The SN65C3221 consists of one line driver, one line receiver, and a dual charge-pump circuit with  $\pm 15$ -kV ESD protection pin to pin (serial-port connection pins, including GND). This device provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. This device operates at data signaling rates up to 1 Mbit/s and a driver output slew rate of 24 V/ $\mu$ s to 150 V/ $\mu$ s.

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the device does not sense a valid RS-232 signal on the receiver input, the driver output is disabled. If FORCEOFF is set low and EN is high, both the driver and receiver are shut off, and the supply current is reduced to 1  $\mu$ A. Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur. Auto-powerdown can be disabled when FORCEON and FORCEOFF are high. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to the receiver input. The INVALID output notifies the user if an RS-232 signal is present at the receiver input. INVALID is high (valid data) if the receiver input voltage is greater than 2.7 V or less than -2.7 V, or has been between -0.3 V and 0.3 V for less than 30  $\mu$ s. INVALID is low (invalid data) if the receiver input voltage is between -0.3 V and 0.3 V for more than 30  $\mu$ s. See Figure 5 for receiver input levels.

### ORDERING INFORMATION†

T <sub>A</sub>	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TSSOP (PW)	Reel of 2000	SN65C3221PWRQ1	3221Q1
	SSOP (DB)	Reel of 2000	SN65C3221DBRQ	3221Q1

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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# SN65C3221-Q1

## 3-V TO 5.5-V SINGLE-CHANNEL RS-232 COMPATIBLE LINE DRIVER/RECEIVER

SLLS616B – APRIL 2004 – REVISED APRIL 2008

### Function Tables

#### EACH DRIVER

INPUTS			VALID RIN RS-232 LEVEL	OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF			
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

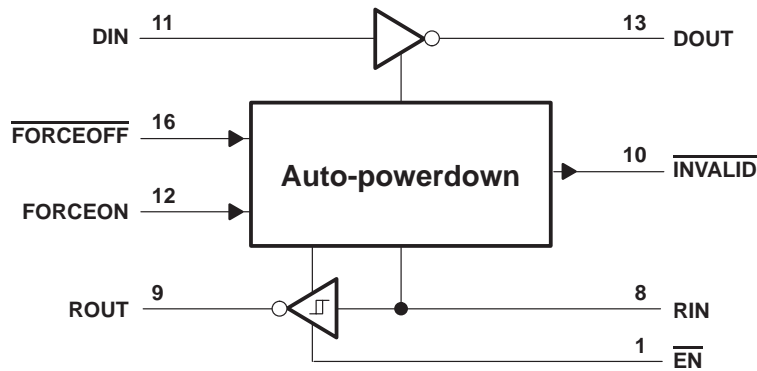
H = high level, L = low level, X = irrelevant, Z = high impedance

#### EACH RECEIVER

INPUTS			VALID RIN RS-232 LEVEL	OUTPUT ROUT
RIN	EN	EN		
L	L	L	X	H
H	L	L	X	L
X	H	H	X	Z
Open	L	L	No	H

H = high level, L = low level, X = irrelevant,  
Z = high impedance (off), Open = disconnected  
input or connected driver off

### logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ (see Note 1)	–0.3 V to 6 V
Positive output supply voltage range, $V+$ (see Note 1)	–0.3 V to 7 V
Negative output supply voltage range, $V-$ (see Note 1)	0.3 V to –7 V
Supply voltage difference, $V+ - V-$ (see Note 1)	13 V
Input voltage range, $V_I$ : Driver ( $\overline{\text{FORCEOFF}}$ , FORCEON, $\overline{\text{EN}}$ )	–0.3 V to 6 V
Receiver	–25 V to 25 V
Output voltage range, $V_O$ : Driver	–10 V to 13.2 V
Receiver (INVALID)	–0.3 V to $V_{CC} + 0.3$ V
Package thermal impedance, $\theta_{JA}$ (see Note 2 and Note 3)	108°C/W
Operating virtual junction temperature, $T_J$	150°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.

- Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
- The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 4 and Figure 6)**

		MIN	NOM	MAX	UNIT	
Supply voltage	$V_{CC} = 3.3$ V	3	3.3	3.6	V	
	$V_{CC} = 5$ V	4.5	5	5.5		
$V_{IH}$ Driver and control high-level input voltage	$V_{CC} = 3.3$ V	2		V		
	$V_{CC} = 5$ V	2.4				
$V_{IL}$ Driver and control low-level input voltage	DIN, $\overline{\text{FORCEOFF}}$ , FORCEON, $\overline{\text{EN}}$			0.8	V	
$V_I$ Driver and control input voltage	DIN, $\overline{\text{FORCEOFF}}$ , FORCEON			0	5.5	V
$V_I$ Receiver input voltage				–25	25	V
$T_A$ Operating free-air temperature				–40	85	°C

NOTE 4: Test conditions are C1–C4 = 0.1  $\mu$ F at  $V_{CC} = 3.3$  V  $\pm$  0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at  $V_{CC} = 5$  V  $\pm$  0.5 V.

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)**

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT	
$I_I$	Input leakage current	$\overline{\text{FORCEOFF}}$ , FORCEON, $\overline{\text{EN}}$		$\pm 0.01$	$\pm 1$	$\mu$ A	
$I_{CC}$	Supply current ( $T_A = 25^\circ\text{C}$ )	Auto-powerdown disabled	No load, $\overline{\text{FORCEOFF}}$ and FORCEON at $V_{CC}$		0.3	1	mA
		Powered off	No load, $\overline{\text{FORCEOFF}}$ at GND		1	10	$\mu$ A
		Auto-powerdown enabled	No load, $\overline{\text{FORCEOFF}}$ at $V_{CC}$ , FORCEON at GND, All RIN are open or grounded		1	10	

‡ All typical values are at  $V_{CC} = 3.3$  V or  $V_{CC} = 5$  V, and  $T_A = 25^\circ\text{C}$ .

NOTE 4: Test conditions are C1–C4 = 0.1  $\mu$ F at  $V_{CC} = 3.3$  V  $\pm$  0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at  $V_{CC} = 5$  V  $\pm$  0.5 V.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V <sub>OH</sub> High-level output voltage	DOUT at R <sub>L</sub> = 3 kΩ to GND, DIN = GND	5	5.4		V
V <sub>OL</sub> Low-level output voltage	DOUT at R <sub>L</sub> = 3 kΩ to GND, DIN = V <sub>CC</sub>	-5	-5.4		V
I <sub>IH</sub> High-level input current	V <sub>I</sub> = V <sub>CC</sub>		±0.01	±1	μA
I <sub>IL</sub> Low-level input current	V <sub>I</sub> at GND		±0.01	±1	μA
I <sub>OS</sub> Short-circuit output current‡	V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0 V		±35	±60	mA
	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0 V		±35	±75	
r <sub>o</sub> Output resistance	V <sub>CC</sub> , V+, and V- = 0 V, V <sub>O</sub> = ±2 V	300	10M		Ω
I <sub>off</sub> Output leakage current	FORCEOFF = GND	V <sub>O</sub> = -10 V to +12 V, V <sub>CC</sub> = 3 V to 3.6 V		±25	μA
		V <sub>O</sub> = ±10 V, V <sub>CC</sub> = 4.5 V to 5.5 V		±25	

† All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

‡ Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
Maximum data rate (see Figure 1)	R <sub>L</sub> = 3 kΩ	C <sub>L</sub> = 1000 pF	250		kbit/s	
		C <sub>L</sub> = 250 pF, V <sub>CC</sub> = 3 V to 4.5 V	1000			
		C <sub>L</sub> = 1000 pF, V <sub>CC</sub> = 4.5 V to 5.5 V	1000			
t <sub>sk(p)</sub> Pulse skew§	C <sub>L</sub> = 150 pF to 2500 pF	R <sub>L</sub> = 3 kΩ to 7 kΩ, See Figure 2		100	ns	
SR(tr) Slew rate, transition region (see Figure 1)	V <sub>CC</sub> = 3.3 V, R <sub>L</sub> = 3 kΩ to 7 kΩ	C <sub>L</sub> = 150 pF to 1000 pF		24	150	V/μs

† All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

§ Pulse skew is defined as |t<sub>pLH</sub> - t<sub>pHL</sub>| of each channel of the same device.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

ESD protection

TERMINAL		TEST CONDITIONS	TYP	UNIT
NAME	NO.			
DOUT	13	HBM	±15	kV



## RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -1 mA	V <sub>CC</sub> -0.6 V	V <sub>CC</sub> -0.1 V		V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 1.6 mA			0.4	V
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>CC</sub> = 3.3 V		1.6	2.4	V
		V <sub>CC</sub> = 5 V		1.9	2.4	
V <sub>IT-</sub>	Negative-going input threshold voltage	V <sub>CC</sub> = 3.3 V	0.6	1.1		V
		V <sub>CC</sub> = 5 V	0.8	1.4		
V <sub>hys</sub>	Input hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )			0.5		V
I <sub>off</sub>	Output leakage current	FORCEOFF = 0 V		±0.05	±10	μA
r <sub>i</sub>	Input resistance	V <sub>I</sub> = ±3 V to ±25 V	3	5	7	kΩ

† All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

NOTE 4: Test conditions are C1-C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2-C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	C <sub>L</sub> = 150 pF, See Figure 3		150		ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level output	C <sub>L</sub> = 150 pF, See Figure 3		150		ns
t <sub>en</sub>	Output enable time	C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See Figure 4		200		ns
t <sub>dis</sub>	Output disable time	C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See Figure 4		200		ns
t <sub>sk(p)</sub>	Pulse skew‡	See Figure 3		50		ns

† All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

‡ Pulse skew is defined as |t<sub>PLH</sub> - t<sub>PHL</sub>| of each channel of the same device.

NOTE 4: Test conditions are C1-C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2-C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

## ESD protection

TERMINAL		TEST CONDITIONS	TYP	UNIT
NAME	NO.			
RIN	8	HBM	±15	kV

**AUTO-POWERDOWN SECTION**

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)**

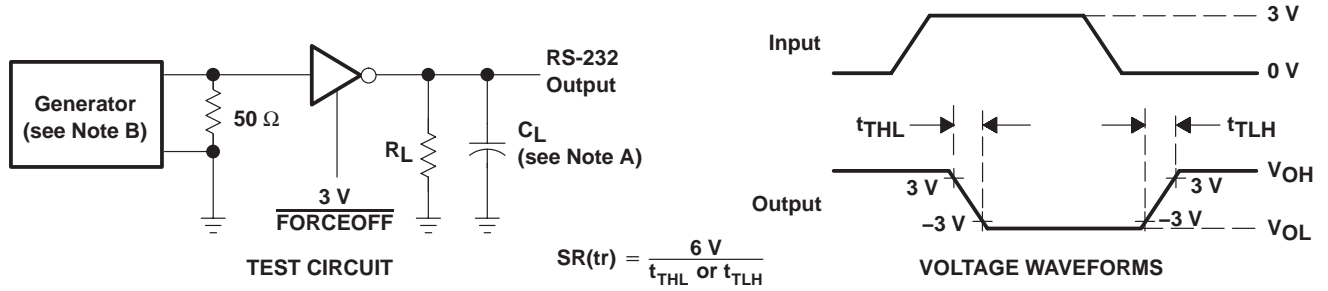
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V <sub>T+</sub> (valid)	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$		2.7	V
V <sub>T-</sub> (valid)	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$	-2.7		V
V <sub>T</sub> (invalid)	Receiver input threshold for $\overline{\text{INVALID}}$ low-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$	-0.3	0.3	V
V <sub>OH</sub>	$\overline{\text{INVALID}}$ high-level output voltage	I <sub>OH</sub> = -1 mA, FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$	V <sub>CC</sub> -0.6		V
V <sub>OL</sub>	$\overline{\text{INVALID}}$ low-level output voltage	I <sub>OL</sub> = 1.6 mA, FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$		0.4	V

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)**

PARAMETER		MIN	TYP†	MAX	UNIT
t <sub>valid</sub>	Propagation delay time, low- to high-level output		1		μs
t <sub>invalid</sub>	Propagation delay time, high- to low-level output		30		μs
t <sub>en</sub>	Supply enable time		100		μs

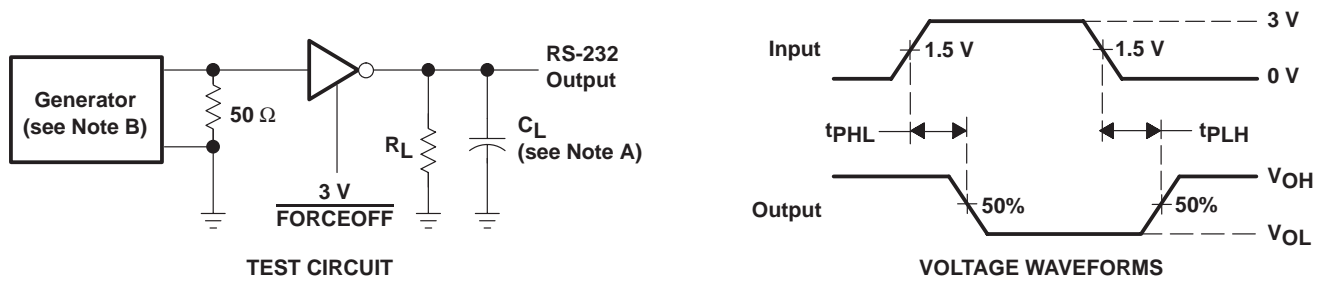
† All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

PARAMETER MEASUREMENT INFORMATION



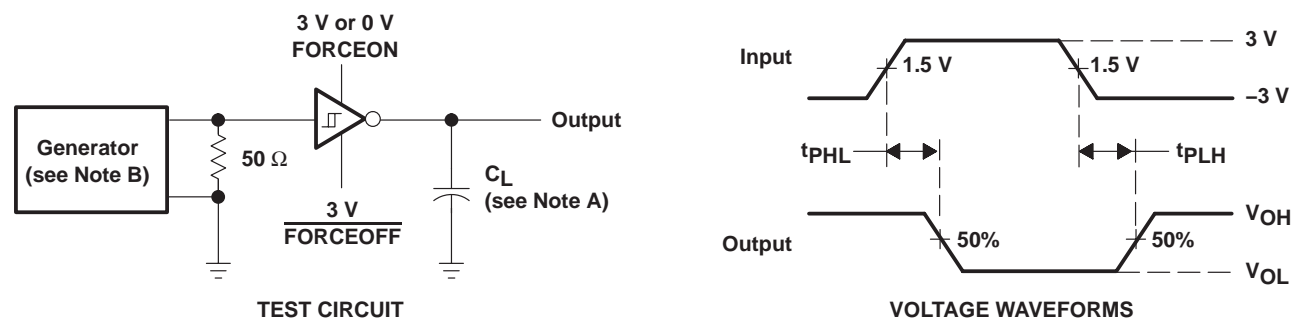
NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

Figure 1. Driver Slew Rate



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

Figure 2. Driver Pulse Skew



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics:  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

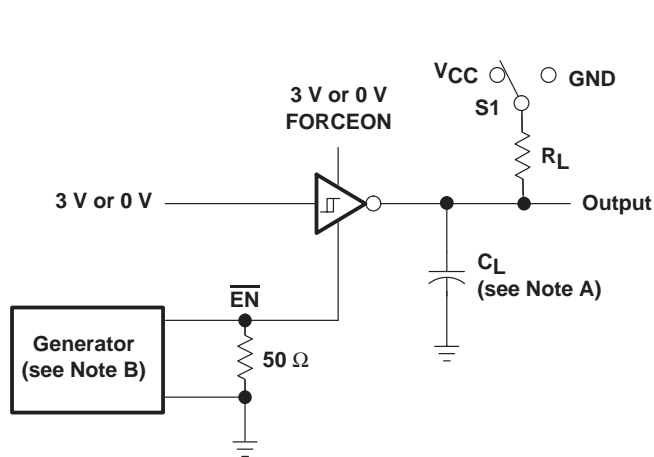
Figure 3. Receiver Propagation Delay Times

# SN65C3221-Q1

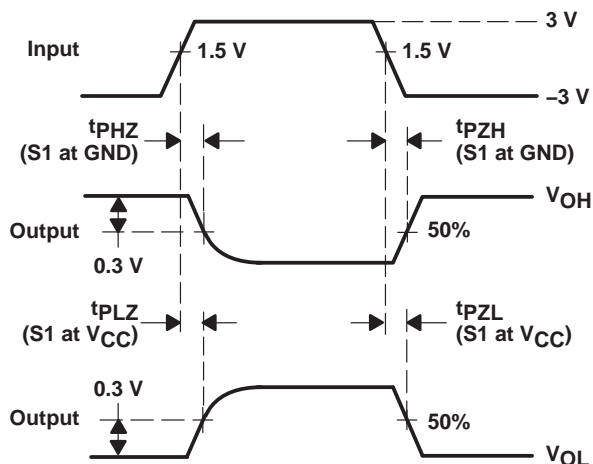
## 3-V TO 5.5-V SINGLE-CHANNEL RS-232 COMPATIBLE LINE DRIVER/RECEIVER

SLLS616B – APRIL 2004 – REVISED APRIL 2008

### PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



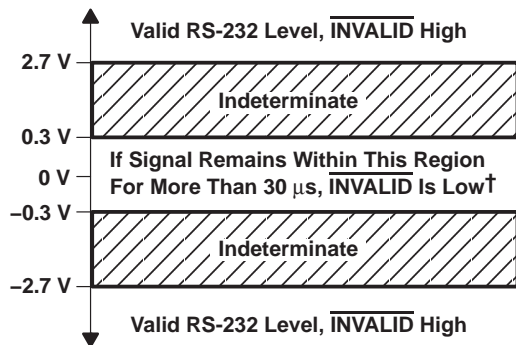
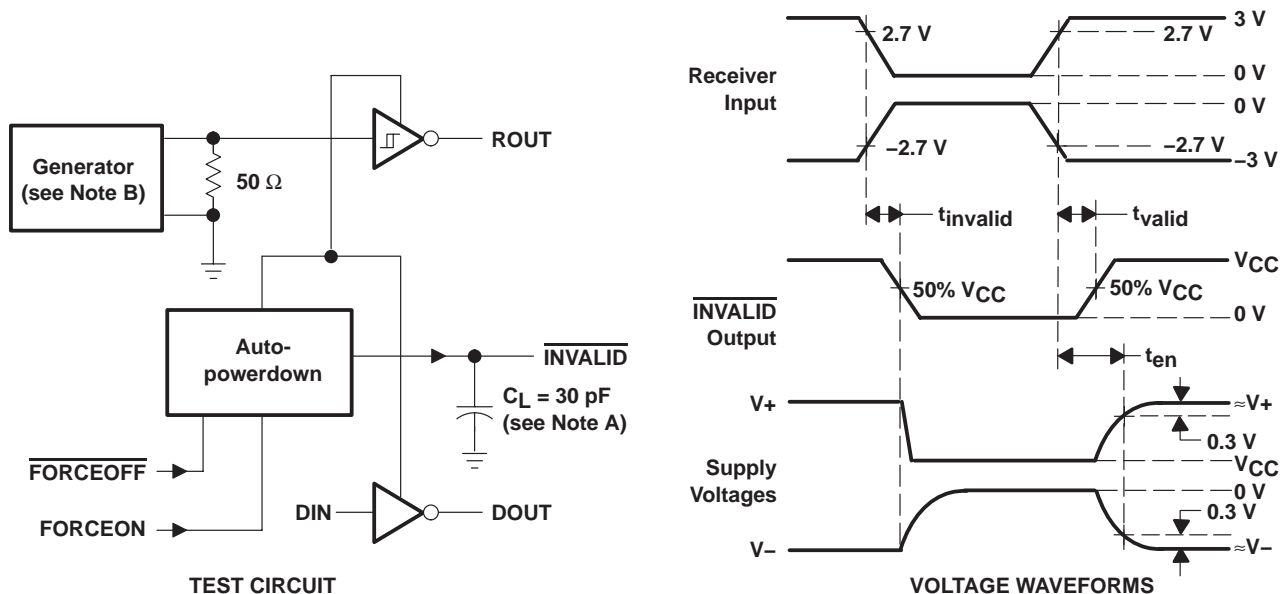
VOLTAGE WAVEFORMS

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .
  - C.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - D.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

Figure 4. Receiver Enable and Disable Times



**PARAMETER MEASUREMENT INFORMATION**



† Auto-powerdown disables drivers and reduces supply current to 1  $\mu$ A.

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics: PRR = 5 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.

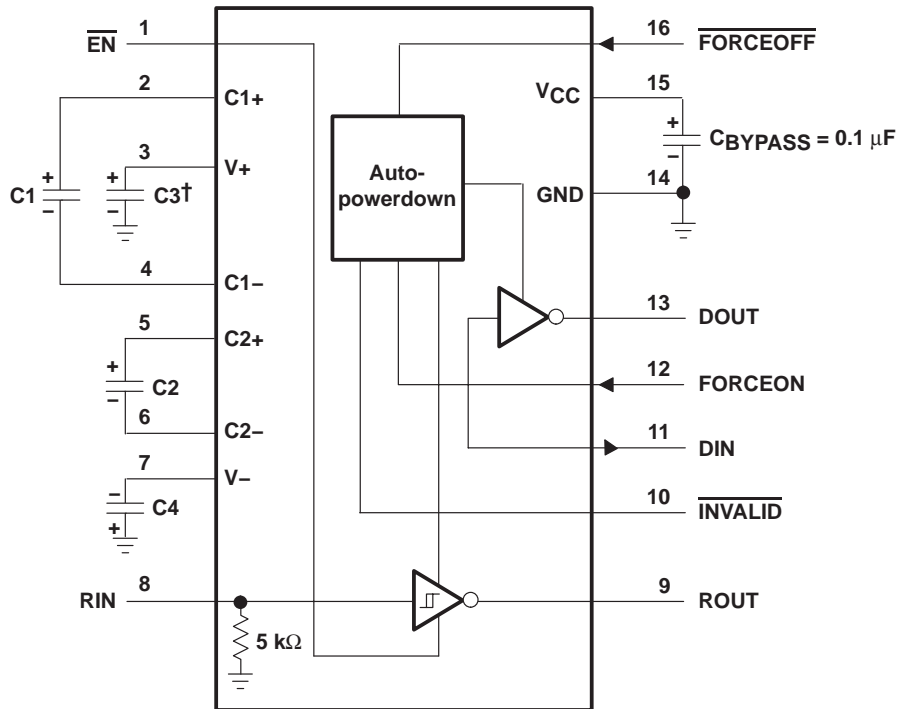
**Figure 5.  $\overline{\text{INVALID}}$  Propagation Delay Times and Driver Enabling Time**

# SN65C3221-Q1

## 3-V TO 5.5-V SINGLE-CHANNEL RS-232 COMPATIBLE LINE DRIVER/RECEIVER

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### APPLICATION INFORMATION



† C3 can be connected to V<sub>CC</sub> or GND.  
 NOTE A: Resistor values shown are nominal.

V<sub>CC</sub> vs CAPACITOR VALUES

V <sub>CC</sub>	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 µF	0.1 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

Figure 6. Typical Operating Circuit and Capacitor Values

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65C3221IPWRG4Q1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB32211	<a href="#">Samples</a>
SN65C3221IPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB32211	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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**OTHER QUALIFIED VERSIONS OF SN65C3221-Q1 :**

- Catalog: [SN65C3221](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C3221IPWRG4Q1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65C3221IPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C3221IPWRG4Q1	TSSOP	PW	16	2000	367.0	367.0	35.0
SN65C3221IPWRQ1	TSSOP	PW	16	2000	367.0	367.0	35.0

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

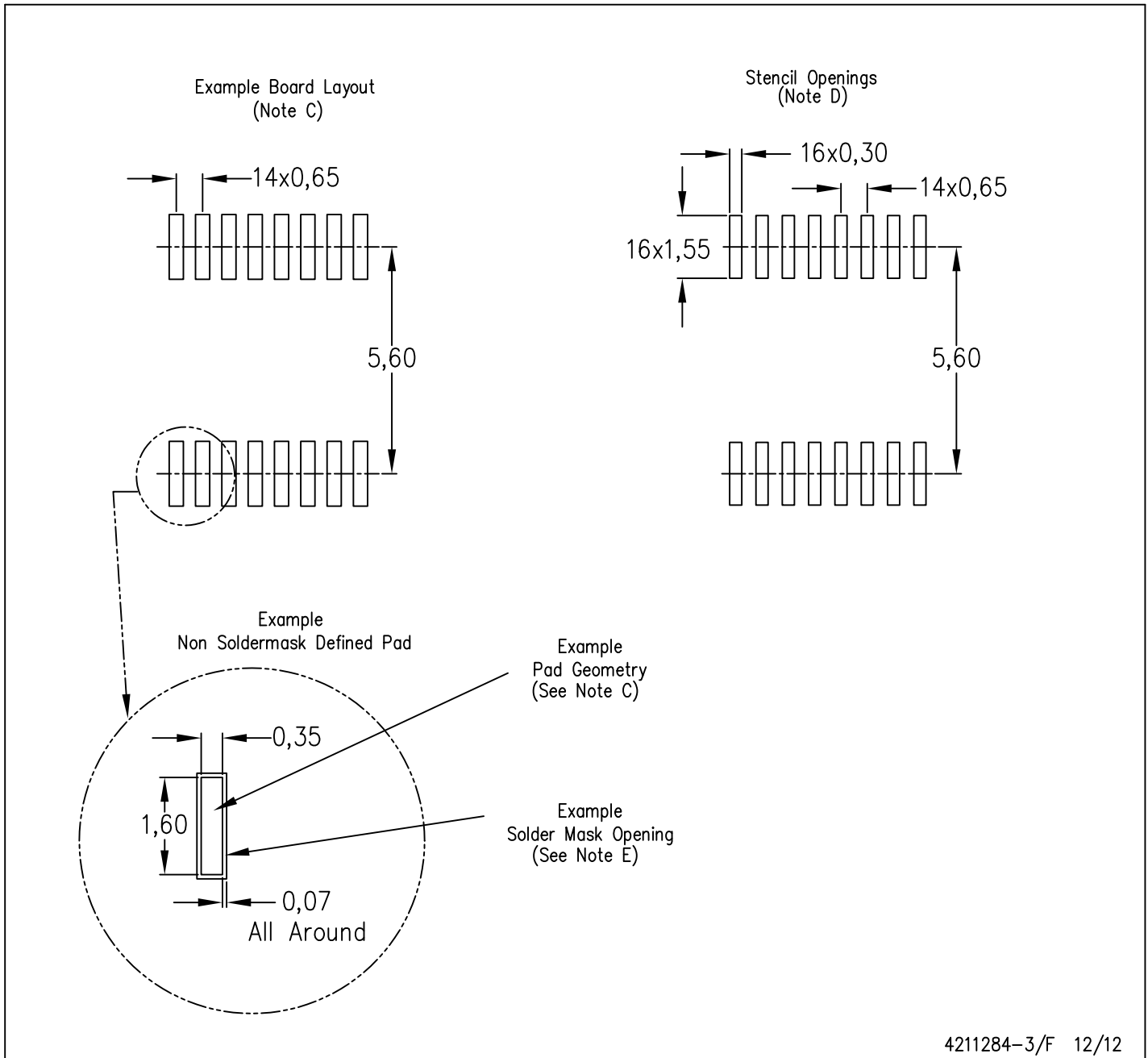


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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