'Turbo' CAN Transceivers for Higher Data Rates and Large Networks Including Features for Functional Safety

Check for Samples: SN65HVD255, SN65HVD256, SN65HVD257

FEATURES

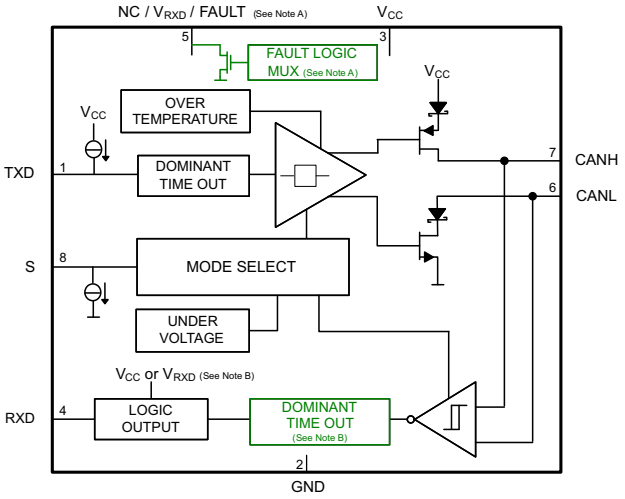
- **Meets the Requirements of ISO11898-2**
- **'Turbo' CAN:**
  - **Short and Symmetrical Propagation Delay Times and Fast Loop Times for Enhanced Timing Margin**
  - **Higher Data Rates in CAN Networks**
- **I/O Voltage Range Supports 3.3V and 5V MCUs**
- **Ideal Passive Behavior When Unpowered**
  - **Bus and Logic Pins are High Impedance (no load)**
  - **Power Up/Down With Glitch Free Operation On Bus**
- **Protection Features**
  - **HBM ESD Protection Exceeds ±12kV**
  - **Bus Fault Protection –27V to 40V**
  - **Undervoltage Protection on Supply Pins**
  - **Driver Dominant Time Out (TXD DTO)**
  - **SN65HVD257: Receiver Dominant Time Out (RXD DTO)**
  - **SN65HVD257: FAULT Output Pin**
  - **Thermal Shutdown Protection**
- **Characterized for –40°C to 125°C Operation**

APPLICATIONS

- **1Mbps Operation in Highly Loaded CAN Networks Down to 10kbps Networks Using TXD DTO**
- **Industrial Automation, Control, Sensors and Drive Systems**
- **Building, Security and Climate Control Automation**
- **Telecom Base Station Status and Control**
- **SN65HVD257: Functional Safety With Redundant and Multi-topology CAN networks**
- **CAN Bus Standards Such as CANopen, DeviceNet, NMEA2000, ARNIC825, ISO11783, CANaerospace**

DESCRIPTION

This CAN transceiver meets the ISO1189-2 High Speed CAN (Controller Area Network) Physical Layer standard. It is designed for data rates in excess of 1 Mbps for CAN in short networks, and enhanced timing margin and higher data rates in long and highly-loaded networks. The device provides many protection features to enhance device and CAN-network robustness. The SN65HVD257 adds additional features, allowing easy design of redundant and multi-topology networks with fault indication for higher levels of functional safety in the CAN system.



A. Pin 5 function is device dependent; NC on SN65HVD255, V_{RXD} for RXD output level-shifting device on SN65HVD256, and FAULT Output on SN65HVD257

B. RXD logic output is driven to 5V V_{CC} on 5V-only supply devices (SN65HVD255, SN65HVD257) and driven to V_{RXD} on output level-shifting device (SN65HVD256).

C. RXD (Receiver) Dominant State Time Out is a device dependent option available only on SN65HVD257.

Figure 1. Functional Block Diagram

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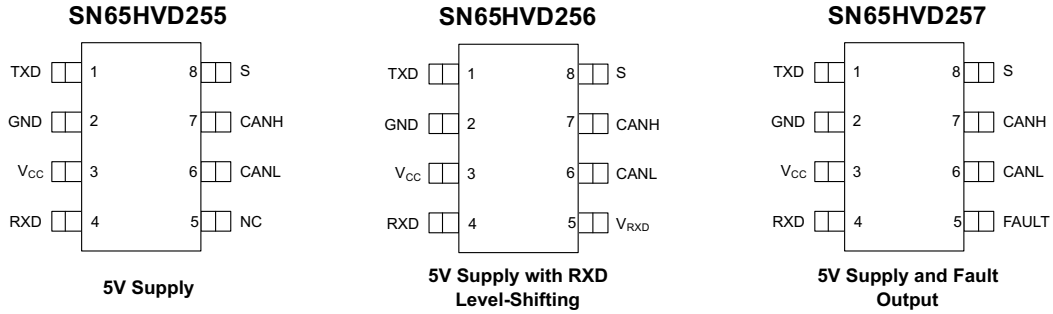
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Figure 2. D PACKAGE (TOP VIEW)



DEVICE OPTIONS

PART NUMBER	I/O SUPPLY for RXD	TXD DTO	RXD DTO	FAULT Output	COMMENT
SN65HVD255	No	Yes	No	No	'251 and '1050 functional upgrade with 'Turbo CAN' fast loop times and TXD DTO protection allowing data rates down to 10kbps
SN65HVD256	Yes	Yes	No	No	'251 and '1050 functional upgrade with 'Turbo CAN' fast loop times and TXD DTO protection allowing data rates down to 10kbps. RXD output level shifting via RXD supply input.
SN65HVD257	No	Yes	Yes	Yes	'251 and '1050 functional upgrade with 'Turbo CAN' fast loop times, TXD & RXD DTO protection allowing data rates down to 10kbps and fault output pin

PIN FUNCTIONS

PIN		TYPE	DESCRIPTION
NAME	NO.		
TXD	1	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
GND	2	GND	Ground connection
V_{CC}	3	Supply	Transceiver 5V supply voltage
RXD	4	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
NC	5	NC	SN65HVD255: No Connect
V_{RXD}		Supply	SN65HVD256: RXD output supply voltage
FAULT		O	SN65HVD257: open drain FAULT output pin
CANL	6	I/O	Low level CAN bus line
CANH	7	I/O	High level CAN bus line
S	8	I	Mode select: S (silent mode) select pin (active high)

ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP SIDE MARKING
–40°C to 125°C	SOIC – D	SN65HVD255D and SN65HVD255DR	HVD255
		SN65HVD256D and SN65HVD256DR	HVD256
		SN65HVD257D and SN65HVD257DR	HVD257

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

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FUNCTIONAL DESCRIPTION

OPERATING MODES

The device has two main operating modes: normal mode and silent mode. Operating mode selection is made via the S input pin.

Table 1. Operating Modes

S Pin	MODE	DRIVER	RECEIVER	RXD Pin
LOW	Normal Mode	Enabled (ON)	Enabled (ON)	Mirrors Bus State(1)
HIGH	Silent Mode	Disabled (OFF)	Enabled (ON)	Mirrors Bus State

(1) Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

CAN BUS STATES

The CAN bus has two states during powered operation of the device; *dominant* and *recessive*. A dominant bus state is when the bus is driven differentially, corresponding to a logic low on the TXD and RXD pin. A recessive bus state is when the bus is biased to V_{CC} / 2 via the high-resistance internal input resistors R_{IN} of the receiver, corresponding to a logic high on the TXD and RXD pins. See Figure 3 and Figure 4.

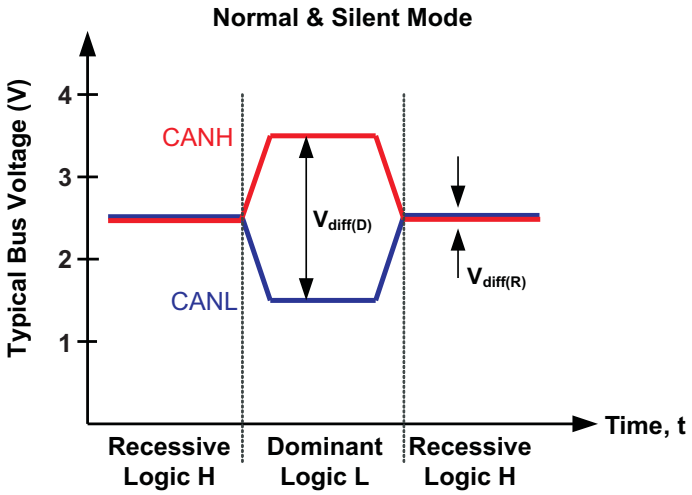

Figure 3. Bus States (Physical Bit Representation)

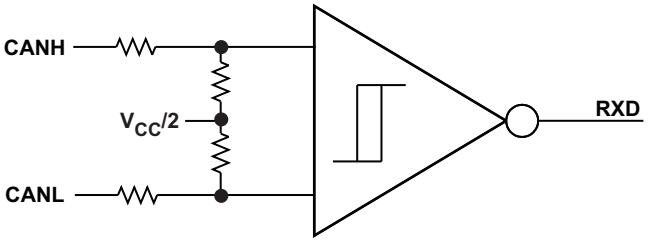

Figure 4. Simplified Recessive Common Mode Bias and Receiver

NORMAL MODE

Select the *normal mode* of device operation by setting S low. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD.

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SILENT MODE

Activate *silent mode* (receive only) by setting S high. The CAN driver is turned off while the receiver remains active and RXD outputs the received bus state.

APPLICATION NOTE: Silent mode may be used to implement *babbling idiot* protection, to ensure that the driver does not disrupt the network during a local fault. Silent mode may also be used in redundant systems to select or de-select the redundant transceiver (driver) when needed.

DRIVER AND RECEIVER FUNCTION TABLES

Table 2. Driver Function Table

DEVICE	INPUTS		OUTPUTS		DRIVEN BUS STATE
	S(1)(2)	TXD(1)(3)	CANH(1)	CANL(1)	
All Devices	L or Open	L	H	L	Dominant
		H or Open	Z	Z	Recessive
	H	X	Z	Z	Recessive

(1) H = high level, L = low level, X= irrelevant, Z = common mode (recessive) bias to V_{CC} / 2. See Figure 3 and Figure 4 for bus state and common mode bias information.
(2) Devices have an internal pull down to GND on S pin. If S pin is open the pin will be pulled low and the device will be in normal mode.
(3) Devices have an internal pull up to V_{CC} on TXD pin. If the TXD pin is open the pin will be pulled high and the transmitter will remain in recessive (non-driven) state.

Table 3. Receiver Function Table

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} - V_{CANL}$	BUS STATE	RXD PIN(1)
Normal or Silent	$V_{ID} \geq 0.9$ V	Dominant	L(2)
	0.5 V < V_{ID} < 0.9 V	?	?
	$V_{ID} \leq 0.5$ V	Recessive	H
	Open ($V_{ID} \approx 0$ V)	Open	H

(1) H = high level, L = low level, ? = indeterminate.
(2) RXD output remains dominant (low) as long as the bus is dominant. On SN65HVD257 device with RXD dominant timeout, once the bus has been dominant longer than the dominant timeout, t_{RXD_DTO}, the RXD pin will return recessive (high). See RXD Dominant Timeout (SN65HVD257) for a description of behavior during receiving a bus stuck dominant condition.

DIGITAL INPUTS AND OUTPUTS

5 V V_{CC} Only Devices (SN65HVD255 and SN65HVD257):

The 5V V_{CC} device is supplied by a single 5 V rail. The digital inputs are 5 V and 3.3 V compatible. This device has a 5 V (V_{CC}) level RXD output. TXD is internally pulled up to V_{CC} and S is internally pulled down to GND.

APPLICATION NOTE: TXD is internally pulled up to V_{CC} and the S pin is internally pulled down to GND. However, the internal bias may only put the device into a known state if the pins float. The internal bias may be inadequate for system-level biasing. TXD pullup strength and CAN bit timing require special consideration when the SN65HVD25x devices are used with an open-drain TXD output on the CAN controller. An adequate external pullup resistor must be used to ensure that the CAN controller output of the µP maintains adequate bit timing input to the SN65HVD25x.

5 V V_{CC} with V_{RXD} RXD output Supply Devices (SN65HVD256):

This device is a 5V V_{CC} CAN transceiver with a separate supply for the RXD output, V_{RXD}. The digital inputs are 5 V and 3.3 V compatible. These devices have a V_{RXD}-level RXD output. TXD remains weakly pulled up to V_{CC}.

APPLICATION NOTE: On device versions with a V_{RXD} supply that shifts the RXD output level, the input pins of the device remain the same. TXD remains weakly pulled up to V_{CC} internally. Thus, a small I_{IH} current flows if the TXD input is used below V_{CC} levels.

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5 V V_{CC} with FAULT Open-Drain Output Device (SN65HVD257):

This device has a FAULT output pin (open-drain). FAULT must be pulled up to V_{CC} or I/O supply level via an external resistor.

APPLICATION NOTE: Because the FAULT output pin is open-drain, it actively pulls down when there is no fault, and becomes high-impedance when a fault condition is detected. An external pullup resistor to the V_{CC} or I/O supply of the system must be used to pull the pin high to indicate a fault to the host microprocessor. The open-drain architecture makes the fault pin compatible with 3.3 V and 5 V I/O-level systems. The pullup current, selected by the pullup resistance value, should be as low as possible while achieving the desired voltage level output in the system with margin against noise.

PROTECTION FEATURES

TXD Dominant Timeout (DTO)

During normal mode (the only mode where the CAN driver is active), the TXD DTO circuit prevents the transceiver from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The DTO circuit timer starts on a falling edge on TXD. The DTO circuit disables the CAN bus driver if no rising edge is seen before the timeout period expires. This frees the bus for communication between other nodes on the network. The CAN driver is re-activated when a recessive signal is seen on TXD pin, thus clearing the TXD DTO condition. The receiver and RXD pin still reflect the CAN bus, and the bus pins are biased to recessive level during a TXD dominant timeout.

APPLICATION NOTE: The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{TXD_DTO} minimum, limits the minimum data rate. Calculate the minimum transmitted data rate by: Minimum Data Rate = 11 / t_{TXD_DTO}.

RXD Dominant Timeout (SN65HVD257)

The SN65HVD257 device has a RXD dominant timeout (RXD DTO) circuit that prevents a bus stuck dominant fault from permanently driving the RXD output dominant (low) when the bus is held dominant longer than the timeout period t_{RXD_DTO}. The RXD DTO timer starts on a falling edge on RXD (bus going dominant). If no rising edge (bus returning recessive) is seen before the timeout constant of the circuit expires (t_{RXD_DTO}), the RXD pin returns high (recessive). The RXD output is re-activated to mirror the bus receiver output when a recessive signal is seen on the bus, clearing the RXD dominant timeout. The CAN bus pins are biased to the recessive level during a RXD DTO.

APPLICATION NOTE: The minimum dominant RXD time allowed by the RXD DTO limits the minimum possible received data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits for the worst case transmission, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{RXD_DTO} minimum, limits the minimum data rate. The minimum received data rate may be calculated by: Minimum Data Rate = 11 / t_{RXD_DTO}.

Thermal Shutdown

If the junction temperature of the device exceeds the thermal shut down threshold the device turns off the CAN driver circuits thus blocking the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature drops below the thermal shutdown temperature of the device.

APPLICATION NOTE: During thermal shutdown the CAN bus drivers turn off; thus no transmission is possible from TXD to the bus. The CAN bus pins are biased to recessive level during a thermal shutdown, and the receiver to RXD path remains operational.

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Undervoltage Lockout

The supply pins have undervoltage detection that places the device in protected mode. This protects the bus during an undervoltage event on either the V_{CC} or V_{RXD} supply pins.

Table 4. Undervoltage Lockout 5V Only Devices (SN65HVD255 and SN65HVD257)

V_{CC}	DEVICE STATE	BUS OUTPUT	RXD
GOOD	Normal	Per Device State and TXD	Mirrors Bus
BAD	Protected	High Impedance	High Impedance (3-state)

Table 5. Undervoltage Lockout 5V and V_{RXD} Device (SN65HVD256)

V_{CC}	V_{RXD}	DEVICE STATE	BUS OUTPUT	RXD
GOOD	GOOD	Normal	Per Device State and TXD	Mirrors Bus
BAD	GOOD	Protected	High Impedance	High (Recessive)
GOOD	BAD	Protected	Recessive	High Impedance (3-state)
BAD	BAD	Protected	High Impedance	High Impedance (3-state)

APPLICATION NOTE: After an undervoltage condition is cleared and the supplies have returned to valid levels, the device typically resumes normal operation in 300 µs.

FAULT Pin (SN65HVD257)

If one or more of the faults (TXD-Dominant Timeout, RXD dominant Timeout, Thermal Shutdown or Undervoltage Lockout) occurs, the FAULT pin (open-drain) turns off, resulting in a high level when externally pulled up to V_{CC} or IO supply.

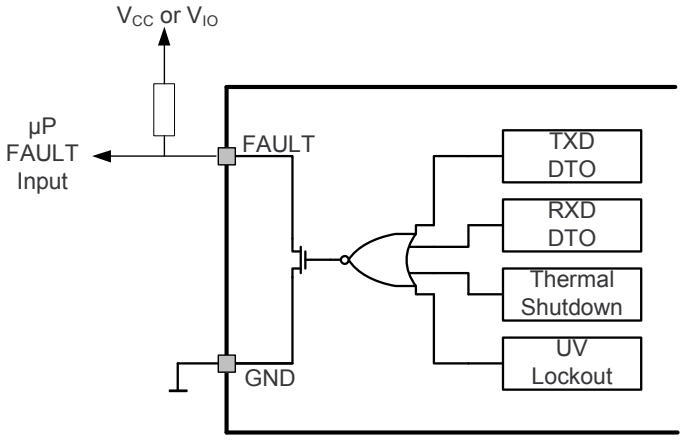

Figure 5. FAULT Pin Function Diagram and Application

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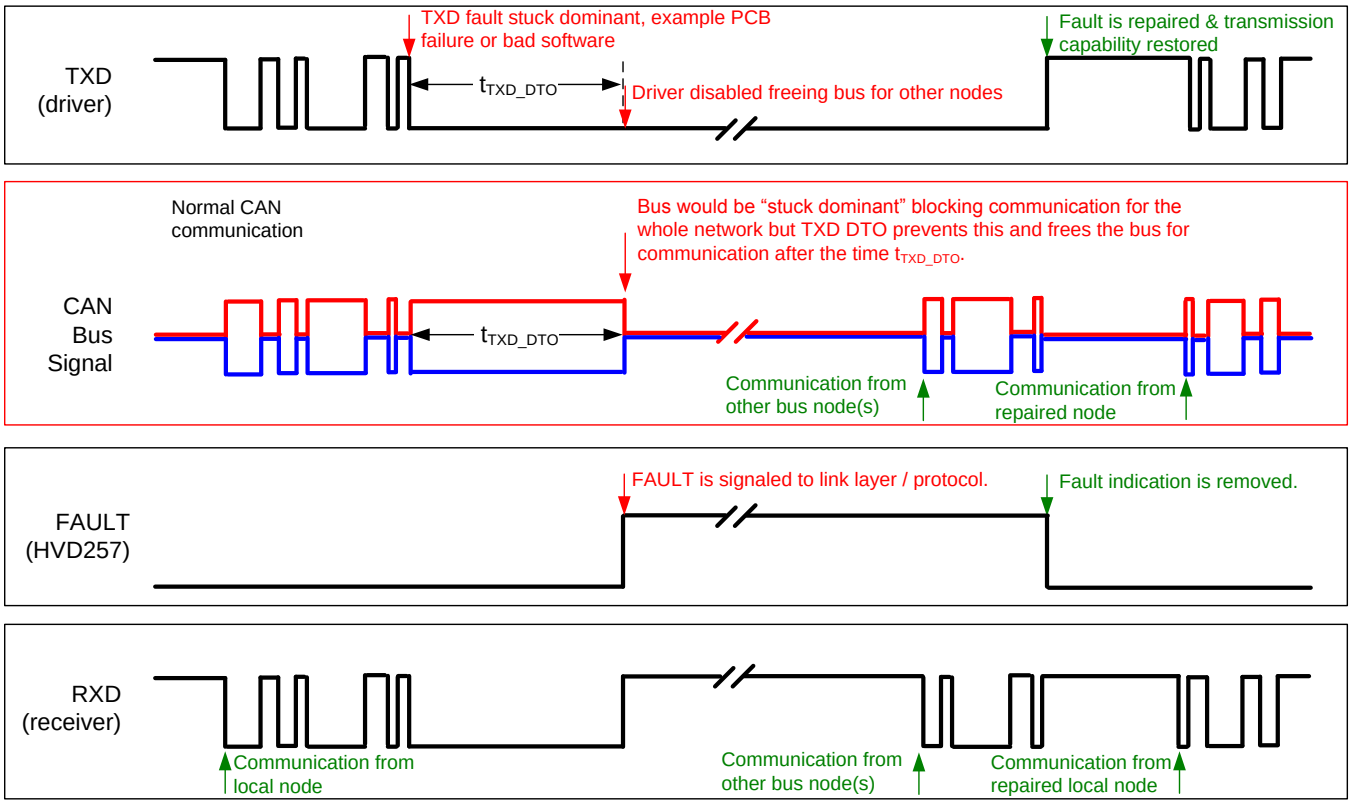

Figure 6. Example Timing Diagram for TXD DTO and FAULT Pin

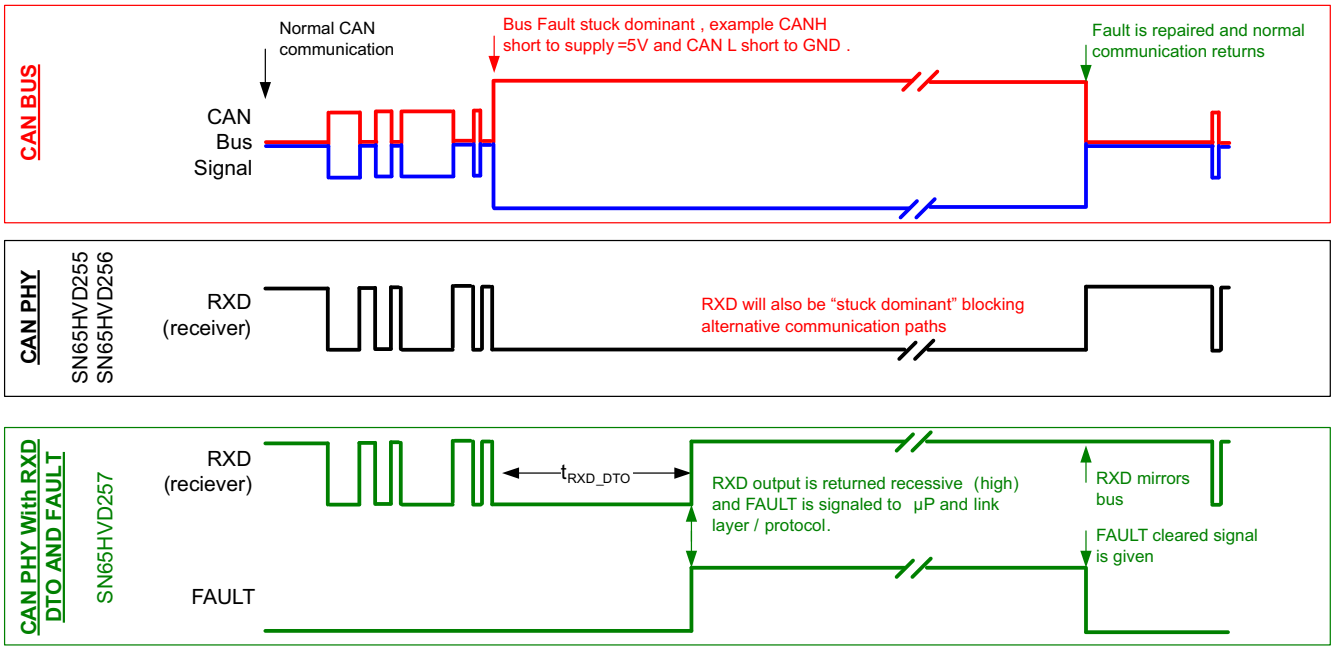

Figure 7. Example Timing Diagram for Devices With and Without RXD DTO and FAULT Pin

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Unpowered Device

The device is designed to be an 'ideal passive' or 'no load' to the CAN bus if it is unpowered. The bus pins (CANH, CANL) have extremely low leakage currents when the device is unpowered so they will not load down the bus. This is critical if some nodes of the network will be unpowered while the rest of the of network remains in operation. The logic pins also have extremely low leakage currents when the device is unpowered to avoid loading down other circuits that may remain powered.

Floating Pins

The device has internal pull ups and pull downs on critical pins to place the device into known states if the pins float. The TXD pin is pulled up to V_{CC} to force a recessive input level if the pin floats. The S pin is pulled down to GND to force the device into normal mode if the pin floats.

CAN Bus Short Circuit Current Limiting

The device has several protection features that limit the short circuit current when a CAN bus line is shorted. These include driver current limiting (dominant and recessive). The device has TXD dominant state time out to prevent permanent higher short circuit current of the dominant state during a system fault. During CAN communication the bus switches between dominant and recessive states with the data and control fields bits, thus the short circuit current may be viewed either as the instantaneous current during each bus state, or as a DC average current. For system current (power supply) and power considerations in the termination resistors and common-mode choke ratings, use the average short circuit current. Determine the ratio of dominant and recessive bits by the data in the CAN frame plus the following factors of the protocol and PHY that force either recessive or dominant at certain times:

- Control fields with set bits
- Bit stuffing
- Interframe space
- TXD dominant time out (fault case limiting)

These ensure a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

APPLICATION NOTE: The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated with the following formula:

$$I_{OS(AVG)} = \%Transmit \times [(\%REC\_Bits \times I_{OS(SS)\_REC}) + (\%DOM\_Bits \times I_{OS(SS)\_DOM})] + [\%Receive \times I_{OS(SS)\_REC}]$$

Where

- $I_{OS(AVG)}$ is the average short circuit current
- %Transmit is the percentage the node is transmitting CAN messages
- %Receive is the percentage the node is receiving CAN messages
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$ is the recessive steady state short circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short circuit current

APPLICATION NOTE: Consider the short circuit current and possible fault cases of the network when sizing the power ratings of the termination resistance and other network components.

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ABSOLUTE MAXIMUM RATINGS(1)(2)

1.0				RATING	UNIT
1.1	V_{CC}	Supply voltage range		–0.3 to 6	V
1.2	V_{RXD}	RXD Output supply voltage range	SN65HVD256	–0.3 to 6 and $V_{RXD} \le V_{CC} + 0.3$	V
1.3	V_{BUS}	CAN Bus I/O voltage range (CANH, CANL)		–27 to 40	V
1.4	V_{Logic_Input}	Logic input pin voltage range (TXD, S)		–0.3 to 6	V
1.5	V_{Logic_Output}	Logic output pin voltage range (RXD)	SN65HVD255, SN65HVD257	–0.3 to 6	V
1.6	V_{Logic_Output}	Logic output pin voltage range (RXD)	SN65HVD256	–0.3 to 6 and $V_I \le V_{RXD} + 0.3$	V
1.7	$I_{O(RXD)}$	RXD (Receiver) output current		12	mA
1.8	$I_{O(FAULT)}$	FAULT output current	SN65HVD257	20	mA
1.9	T_J	Operating virtual junction temperature range (see THERMAL CHARACTERISTICS)		–40 to 150	°C
1.10	T_A	Ambient temperature range (see THERMAL CHARACTERISTICS)		–40 to 125	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

TRANSIENT AND ELECTROSTATIC DISCHARGE PROTECTION

2.0		TEST CONDITIONS		RATING	UNIT
2.1	Human-Body Model	All pins(1)		±2.5	kV
		CAN bus pins (CANH, CANL)(2)		±12	
2.2	Charged-Device Model	All pins(3)		±750	V
2.3	Machine Model	All pins(4)		±250	V
2.4	IEC 61400-4-2 according to GIFT-ICT CAN EMC test spec(5)	CAN bus pins (CANH, CANL) to GND		±8	kV
2.5	ISO7637 Transients according to GIFT - ICT CAN EMC test spec(6)	CAN bus pins (CANH, CANL)	Pulse 1	–100	V
2.6			Pulse 2	+75	V
2.7			Pulse 3a	–150	V
2.8			Pulse 3b	+100	V

(1) Tested in accordance to JEDEC Standard 22, Test Method A114.
(2) Test method based upon JEDEC Standard 22 Test Method A114, CAN bus pins stressed with respect to GND.
(3) Tested in accordance to JEDEC Standard 22, Test Method C101.
(4) Tested in accordance to JEDEC Standard 22, Test Method A115.
(5) IEC 61000-4-2 is a system level ESD test. Results given here are specific to the GIFT-ICT CAN EMC Test specification conditions. Different system level configurations may lead to different results.
(6) ISO7637 is a system level transient test. Results given here are specific to the GIFT-ICT CAN EMC Test specification conditions. Different system level configurations may lead to different results.

RECOMMENDED OPERATING CONDITIONS

3.0				MIN	MAX	UNIT
3.1	V_{CC}	Supply voltage		4.5	5.5	V
3.2	V_{RXD}	RXD supply (SN65HVD256 only)		2.8	5.5	
3.3	V_I or V_{IC}	CAN bus terminal voltage (separately or common mode)		–2	7	
3.4	V_{ID}	CAN bus differential voltage		-6	6	
3.5	V_{IH}	Logic HIGH level input (TXD, S)		2	5.5	
3.6	V_{IL}	Logic LOW level input (TXD, S)		0	0.8	
3.7	$I_{OH(DRVR)}$	CAN BUS Driver High level output current		–70		mA
3.8	$I_{OL(DRVR)}$	CAN BUS Driver Low level output current			70	
3.9	$I_{OH(RXD)}$	RXD pin HIGH level output current		–2		
3.10	$I_{OL(RXD)}$	RXD pin LOW level output current			2	
3.11	$I_{O(FAULT)}$	FAULT pin LOW level output current	SN65HVD257		2	
3.12	T_A	Operational free-air temperature (see THERMAL CHARACTERISTICS)		–40	125	°C

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ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, T_A = –40°C to 125°C (unless otherwise noted). SN65HVD256 device $V_{RXD} = V_{CC}$.

	PARAMETER			TEST CONDITIONS / COMMENT	MIN	TYP(1)	MAX	UNIT
4.0	**SUPPLY CHARACTERISTICS**							
4.1	I_{CC}	5-V Supply current	Normal Mode (Driving Dominant)	See Figure 10, TXD = 0 V, R_L = 50 Ω, C_L = open, R_{CM} = open, S = 0V		60	85	mA
4.2			Normal Mode (Driving Dominant – bus fault)	See Figure 10, TXD = 0 V, S = 0V, CANH = -12V, R_L = open, C_L = open, R_{CM} = open		130	180	
4.3			Normal Mode (Driving Dominant)	See Figure 10, TXD = 0 V, R_L = open (no load), C_L = open, R_{CM} = open, S = 0V		10	20	
4.4			Normal Mode (Recessive)	See Figure 10, TXD = V_{CC}, R_L = 50 Ω, C_L = open, R_{CM} = open, S = 0V		10	20	
4.5			Silent Mode	See Figure 10, TXD = V_{CC}, R_L = 50 Ω,C_L = open, R_{CM} = open, S = V_{CC}		2.5	5	
4.6	I_{RXD}	RXD Supply current (SN65HVD256 only)	All modes	RXD Floating, TXD = 0V			500	µA
4.7	UV_{VCC}	Undervoltage detection on V_{CC} for protected mode			3.5		4.45	V
4.8	$V_{HYS(UVVCC)}$	Hysteresis voltage on UV_{VCC}				200		mV
4.9	UV_{RXD}	Undervoltage detection on V_{RXD} for protected mode (SN65HVD256 only)			1.3		2.75	V
4.10	$V_{HYS(UVRXD)}$	Hysteresis voltage on UV_{RXD} (SN65HVD256 only)				80		mV
5.0	**S PIN (MODE SELECT INPUT)**							
5.1	V_{IH}	HIGH-level input voltage			2			V
5.2	V_{IL}	LOW-level input voltage					0.8	V
5.3	I_{IH}	HIGH-level input leakage current		S = V_{CC} = 5.5 V	7		100	µA
5.4	I_{IL}	Low-level input leakage current		S = 0 V, V_{CC} = 5.5 V	–1	0	1	µA
5.5	$I_{LKG(OFF)}$	Unpowered leakage current		S = 5.5 V, V_{CC} = 0 V, V_{RXD} = 0 V	7	35	100	µA
6.0	**TXD PIN (CAN TRANSMIT DATA INPUT)**							
6.1	V_{IH}	HIGH level input voltage			2			V
6.2	V_{IL}	LOW level input voltage					0.8	V
6.3	I_{IH}	HIGH level input leakage current		TXD = V_{CC} = 5.5 V	–2.5	0	1	µA
6.4	I_{IL}	Low level input leakage current		TXD = 0 V, V_{CC} = 5.5 V	–100	-25	–7	µA
6.5	$I_{LKG(OFF)}$	Unpowered leakage current		TXD = 5.5 V, V_{CC} = 0 V, V_{RXD} = 0 V	–1	0	1	µA
6.6	C_I	Input Capacitance				3.5		pF
7.0	**RXD Pin (CAN RECEIVE DATA OUTPUT)**							
7.1	V_{OH}	HIGH level output voltage		See Figure 11, I_O = –2 mA. For devices with V_{RXD} supply V_{OH} = 0.8 × V_{RXD}	0.8×V_{CC}			V
7.2	V_{OL}	LOW level output voltage		See Figure 11, I_O = 2 mA			0.4	V
7.3	$I_{LKG(OFF)}$	Unpowered leakage current		RXD = 5.5 V, V_{CC} = 0 V, V_{RXD} = 0 V	–1	0	1	µA
7.4	t_R	Output signal rise time		See Receiver Rise Time				
7.5	t_F	Output signal fall time		See Receiver Fall Time				

(1) All typical values are at 25°C and supply voltages of V_{CC} = 5 V and V_{RXD} = 5 V, R_L = 60 Ω.

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ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating conditions, T_A = –40°C to 125°C (unless otherwise noted). SN65HVD256 device V_{RXD} = V_{CC}.

	PARAMETER			TEST CONDITIONS / COMMENT	MIN	TYP(1)	MAX	UNIT
8.0	**DEVICE SWITCHING CHARACTERISTICS**							
8.1	$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant		See Figure 13, S = 0 V, R_L = 60 Ω, C_L = 100 pF, C_{L_RXD} = 15 pF			150	ns
8.2	$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive					150	
8.3	I_{MODE}	Mode change time, from Normal to Silent or from Silent to Normal		See Figure 12			20	µS
9.0	**DRIVER ELECTRICAL CHARACTERISTICS**							
9.1	$V_{O(D)}$	Bus output voltage (dominant	CANH	See Figure 3 and Figure 10, TXD = 0 V, S = 0 V, R_L = 60 Ω, C_L = open, R_{CM} = open	2.75		4.5	V
9.2			CANL		0.5		2.25	
9.3	$V_{O(R)}$	Bus output voltage (recessive)		See Figure 3 and Figure 10, TXD = V_{CC}, V_{RXD} = V_{CC}, S = V_{CC} or 0 V (2), R_L = open (no load), R_{CM} = open	2	0.5×V_{CC}	3	V
9.4	$V_{OD(D)}$	Differential output voltage (dominant)		See Figure 3 and Figure 10, TXD = 0 V, S = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = 330 Ω, –2 V ≤ V_{CM} ≤ 7 V, 4.75 V≤ V_{CC} ≤ 5.25 V	1.5		3	V
9.5				See Figure 3 and Figure 10, TXD = 0 V, S = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = 330 Ω, –2 V ≤ V_{CM} ≤ 7 V, 4.5V ≤ V_{CC} ≤ 5.5 V	1.25		3.2	
9.6	$V_{OD(R)}$	Differential output voltage (recessive)		See Figure 3 and Figure 10, TXD = V_{CC}, S = 0 V, R_L = 60 Ω, C_L = open, R_{CM} = open	–0.12		0.012	V
9.7				See Figure 3 and Figure 10, TXD = V_{CC}, S = 0 V, R_L = open (no load), C_L = open, R_{CM} = open, –40°C ≤ T_A ≤ 85°C	–0.100		0.050	
9.8	V_{SYM}	Output symmetry (dominant or recessive) (V_{CC} – $V_{O(CANH)}$ – $V_{O(CANL)}$)		See Figure 3 and Figure 10, S at 0 V, R_L = 60 Ω, C_L = open, R_{CM} = open	–0.4		0.4	V
9.9	$I_{OS(SS)\_DOM}$	short circuit steady-state output current, Dominant		See Figure 3 and Figure 15, V_{CANH} = 0 V, CANL = open, TXD = 0 V	–160			mA
9.10				See Figure 3 and Figure 15, V_{CANL} = 32 V, CANH = open, TXD = 0 V			160	
9.11	$I_{OS(SS)\_REC}$	short circuit steady-state output current, Recessive		See Figure 3 and Figure 15, –20 V ≤ V_{BUS} ≤ 32 V, Where V_{BUS} = CANH = CANL, TXD = V_{CC}, Normal and Silent Modes	–8		8	mA
9.12	C_O	Output capacitance		See receiver input capacitance				

(2) For the bus output voltage (recessive) will be the same if the device is in normal mode with S pin LOW or if the device is in silent mode with the S pin is HIGH.

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ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating conditions, T_A = –40°C to 125°C (unless otherwise noted). SN65HVD256 device $V_{RXD} = V_{CC}$.

	PARAMETER		TEST CONDITIONS / COMMENT	MIN	TYP(1)	MAX	UNIT
10.0	**DRIVER SWITCHING CHARACTERISTICS**						
10.1	t_{pHR}	Propagation delay time, HIGH TXD to Driver Recessive	See Figure 10, S = 0 V, R_L = 60 Ω, C_L = 100 pF, R_{CM} = open		50	70	ns
10.2	t_{pLD}	Propagation delay time, LOW TXD to Driver Dominant			40	70	
10.3	$t_{sk(p)}$	Pulse skew ($\lvert t_{pHR} - t_{pLD} \rvert$)			10		
10.4	t_R	Differential output signal rise time			10	30	
10.5	t_F	Differential output signal fall time			17	30	
10.6	$t_{R(10k)}$	Differential output signal rise time, R_L = 10 kΩ	See Figure 10, S = 0 V, R_L = 10 kΩ, C_L = 10 pF, R_{CM} = open			35	ns
10.7	$t_{F(10k)}$	Differential output signal fall time, R_L = 10 kΩ				100	
10.8	t_{TXD_DTO}	Dominant timeout(3)	See Figure 14, R_L = 60 Ω, C_L = open	1175		3700	µs
11.0	**RECEIVER ELECTRICAL CHARACTERISTICS**						
11.1	V_{IT+}	Positive-going input threshold voltage, normal mode	See Figure 11, Table 3 and Table 6			900	mV
11.2	V_{IT-}	Negative-going input threshold voltage, normal mode		500			mV
11.3	V_{HYS}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)			125		mV
11.4	$I_{IOFF(LKG)}$	Power-off (unpowered) bus input leakage current	$C_{ANH} = C_{ANL}$ = 5 V, V_{CC} = 0 V, V_{RXD} = 0 V			5.5	µA
11.5	C_I	Input capacitance to ground (CANH or CANL)	TXD = V_{CC}, $V_{RXD} = V_{CC}$, V_I = 0.4 sin (4E6 π t) + 2.5 V		25		pF
11.6	C_{ID}	Differential input capacitance	TXD = V_{CC}, $V_{RXD} = V_{CC}$, V_I = 0.4 sin (4E6 π t)		10		pF
11.7	R_{ID}	Differential input resistance	TXD = $V_{CC} = V_{RXD}$ = 5 V, S = 0 V	30		80	kΩ
11.8	R_{IN}	Input resistance (CANH or CANL)		15		40	kΩ
11.9	$R_{IN(M)}$	Input resistance matching: $[1 - R_{IN(CANH)} / R_{IN(CANL)}] \times 100\%$	$V_{(CANH)} = V_{(CANL)}$, –40°C ≤ T_A ≤ 85°C	–3%		3%	
12.0	**RECEIVER SWITCHING CHARACTERISTICS**						
12.1	t_{pRH}	Propagation delay time, recessive input to high output	See Figure 11, C_{L_RXD} = 15 pF		70	90	ns
12.2	t_{pDL}	Propagation delay time, dominant input to low output			70	90	ns
12.3	t_R	Output signal rise time			4	20	ns
12.4	t_F	Output signal fall time			4	20	ns
12.5	t_{RXD_DTO}(4)	Receiver dominant time out (SN65HVD257 only) See Figure 8, C_{L_RXD} = 15 pF		1380		4200	µs

(3) The TXD dominant timeout (t_{TXD_DTO}) disables the driver of the transceiver once the TXD has been dominant longer than t_{TXD_DTO}, which releases the bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after TXD has been returned HIGH (recessive). While this protects the bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{TXD_DTO} minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11 / t_{TXD_DTO} = 11 bits / 1175 µs = 9.4 kbps.

(4) The RXD timeout (t_{RXD_DTO}) disables the driver of the transceiver once the RXD has been dominant longer than t_{RXD_DTO}, which releases the bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after RXD has been returned HIGH (recessive). While this protects the bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on RXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{RXD_DTO} minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11 / t_{RXD_DTO} = 11 bits / 1380 µs = 8 kbps.

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ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating conditions, T_A = –40°C to 125°C (unless otherwise noted). SN65HVD256 device V_{RXD} = V_{CC}.

	PARAMETER		TEST CONDITIONS / COMMENT	MIN	TYP(1)	MAX	UNIT
13.0	**FAULT Pin (Fault Output), SN65HVD257 only**						
13.1	I_{CH}	Output current high level	FAULT = V_{CC}, See Figure 9	–10		10	µA
13.2	I_{CL}	Output current low level	FAULT = 0.4 V, See Figure 9	5	12		mA

THERMAL CHARACTERISTICS

13.0	THERMAL METRIC(1)		TEST CONDITIONS	TYP	UNIT
13.1	θ_{JA}	Junction-to-air thermal resistance	High-K thermal resistance(2)	107.5	°C/W
13.2	θ_{JB}	Junction-to-board thermal resistance(3)		48.9	
13.3	$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance(4)		56.7	
13.4	Ψ_{JT}	Junction-to-top characterization parameter(5)		12.1	
13.5	Ψ_{JB}	Junction-to-board characterization parameter(6)		48.2	
13.6	P_D	Average power dissipation	V_{CC} = 5 V, V_{RXD} = 5 V, T_J = 27°C, R_L = 60 Ω, S at 0 V, Input to TXD at 250 kHz, 25% duty cycle square wave, C_{L_RXD} = 15 pF. Typical CAN operating conditions at 500kbps with 25% transmission (dominant) rate.	115	mW
13.7			V_{CC} = 5.5 V, V_{RXD} = 5.5 V, T_J = 150°C, R_L = 50 Ω, S at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_{L_RXD} = 15 pF. Typical high load CAN operating conditions at 1mbps with 50% transmission (dominant) rate and loaded network.	268	
13.8		Thermal shutdown temperature		170	°C
13.9		Thermal shutdown hysteresis		5	°C

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) he junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(5) The junction-to-top characterization parameter, Ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, Ψ_{JB} estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).

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PARAMETER MEASUREMENT INFORMATION

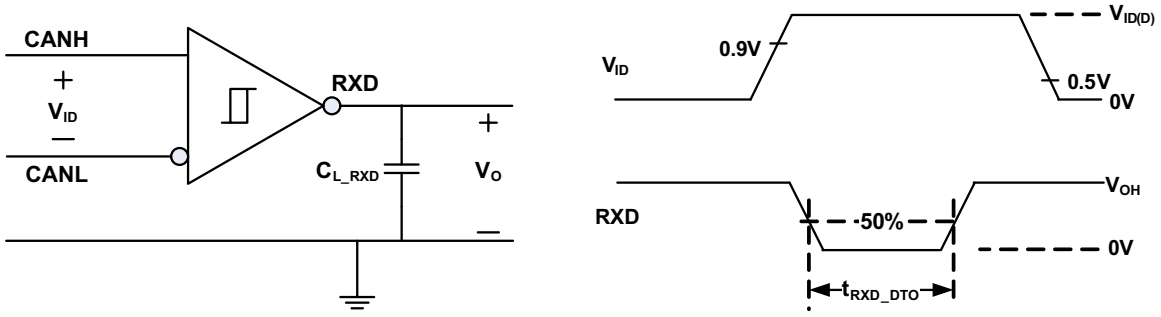

Figure 8. RXD Dominant Timeout Test Circuit and Measurement

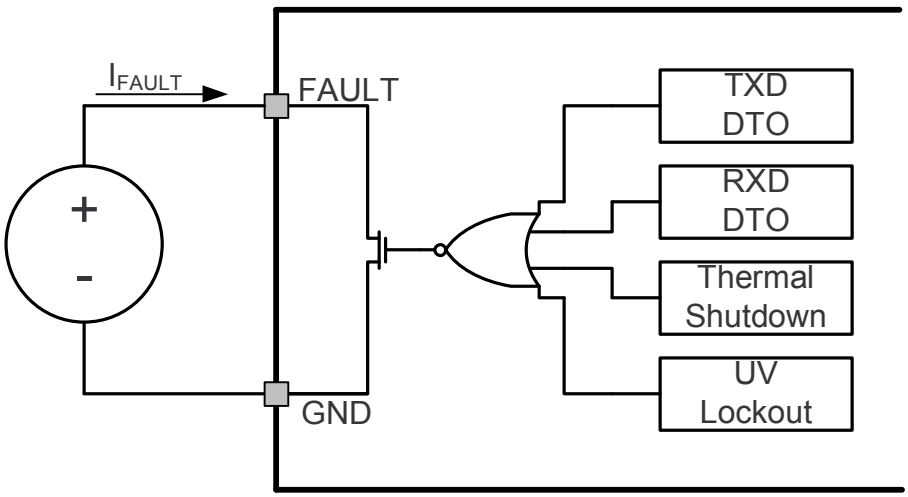

Figure 9. FAULT Test and Measurement

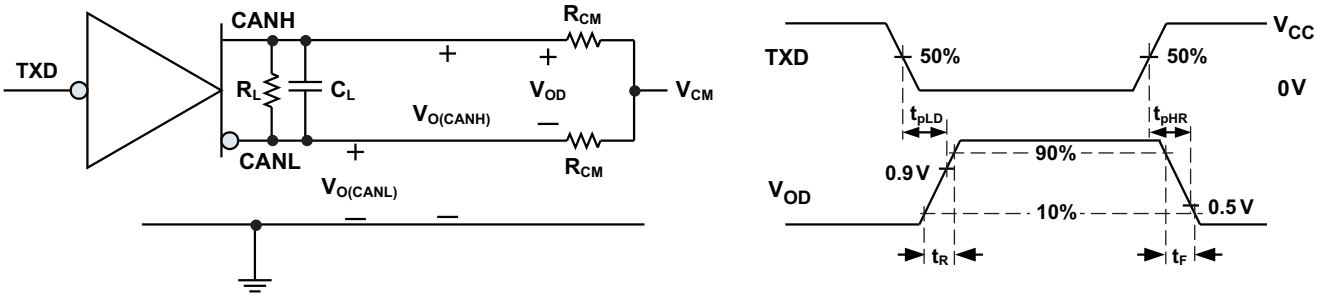

Figure 10. Driver Test Circuit and Measurement

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PARAMETER MEASUREMENT INFORMATION (continued)

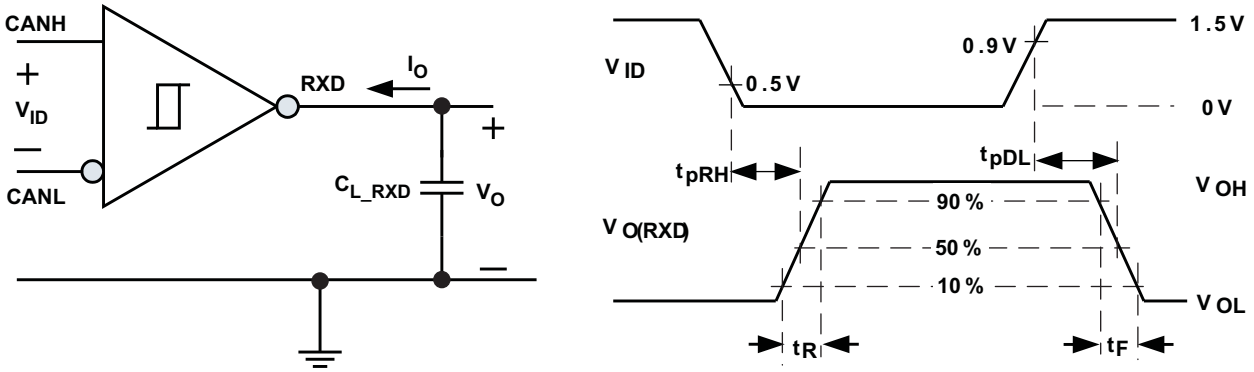

Figure 11. Receiver Test Circuit and Measurement

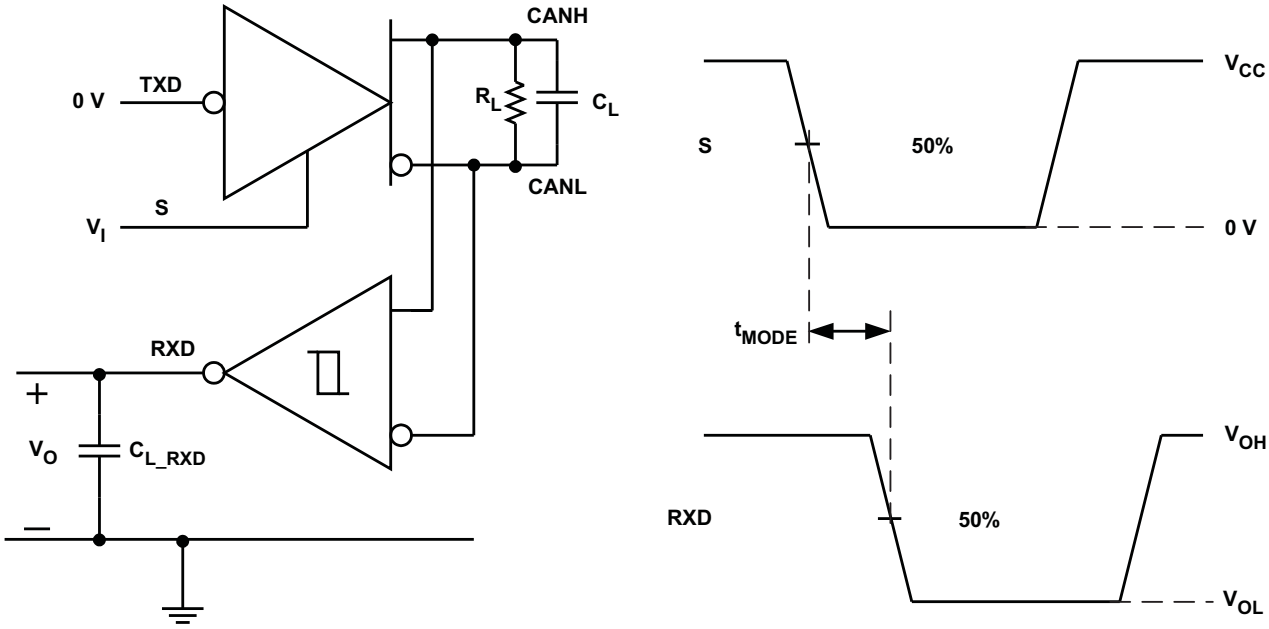

Figure 12. t_{MODE} Test Circuit and Measurement

Table 6. Receiver Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	R_{XD}	
-1.1V	-2.0 V	900 mV	L	V_{OL}
7.0 V	6.1 V	900 mV	L	
-1.5 V	-2.0 V	500 mV	H	V_{OH}
7.0 V	6.5 V	500 mV	H	
Open	Open	X	H	

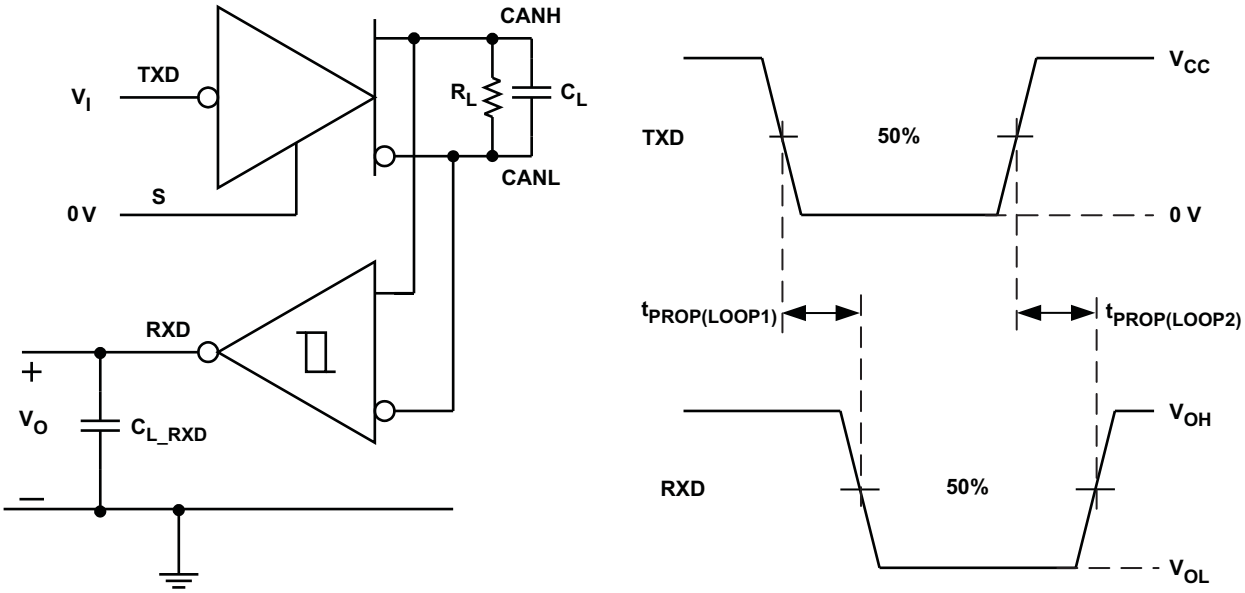

Figure 13. $T_{PROP(LOOP)}$ Test Circuit and Measurement

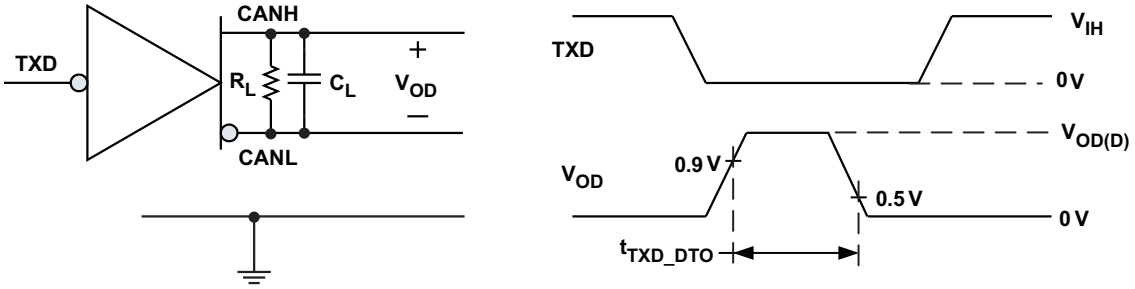

Figure 14. TXD Dominant Timeout Test Circuit and Measurement

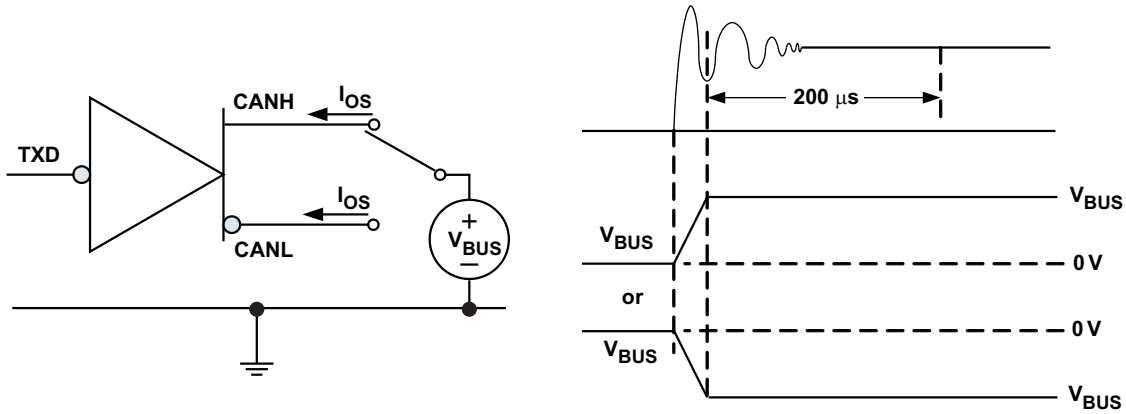

Figure 15. Driver Short Circuit Current Test and Measurement

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APPLICATION INFORMATION

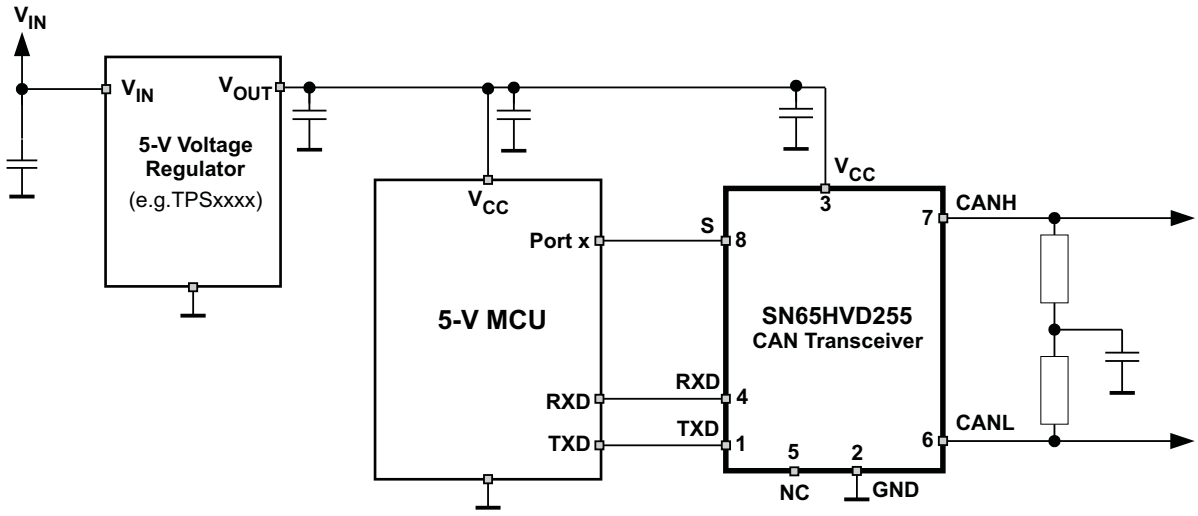

Figure 16. Typical 5V Application

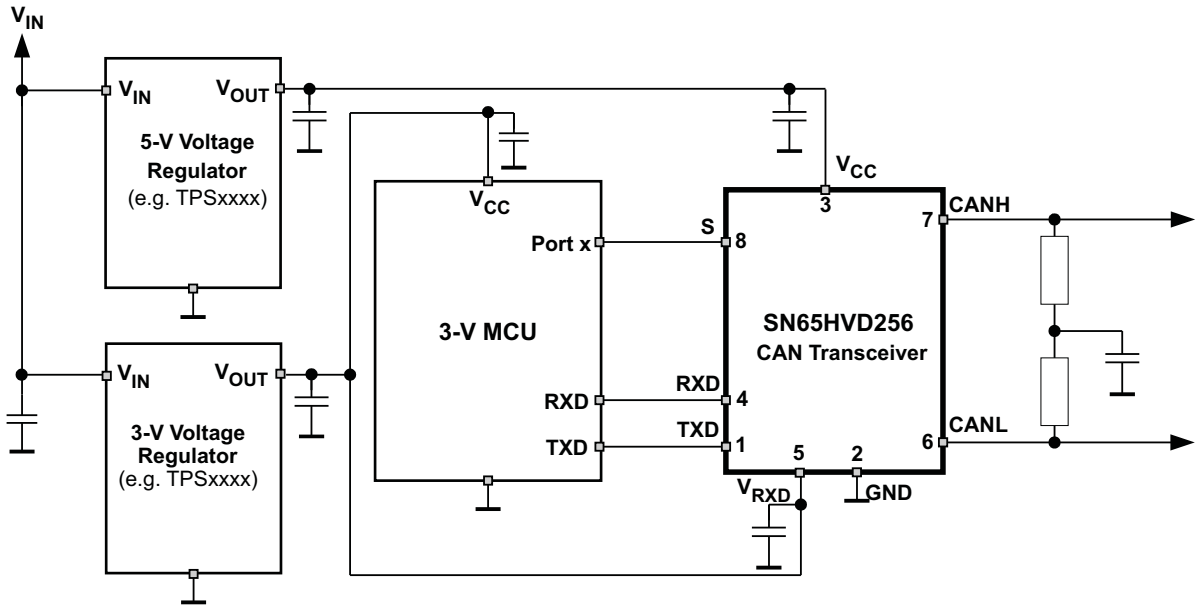

Figure 17. Typical 3.3V Application

BUS LOADING, LENGTH AND NUMBER OF NODES

The ISO11898 Standard specifies a maximum bus length of 40m and maximum stub length of 0.3m with a maximum of 30 nodes. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires a transceiver with high input impedance such as the SN65HVD25x family.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO11898. They have made system level trade offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, DeviceNet and NMEA200.

A CAN network design is a series of tradeoffs, but these devices operate over wide common-mode range. In ISO11898-2 the driver differential output is specified with a 60Ω load (the two 120Ω termination resistors in parallel) and the differential output must be greater than 1.5V. The SN65HVD25x family is specified to meet the 1.5V requirement with a 45Ω load incorporating the worst case including parallel transceivers. The differential input resistance of the SN65HVD25x is a minimum of 30KΩ. If 167 SN65HVD25x family transceivers are in parallel on a bus, this is equivalent to a 180Ω differential load worst case. That transceiver load of 180Ω in parallel with the 60Ω gives a total 45Ω. Therefore, the SN65HVD25x family theoretically supports over 167 transceivers on a single bus segment with margin to the 1.2V minimum differential input at each node. However for CAN network design margin must be given for signal loss across the system & cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is typically much lower. Bus length may also be extended beyond the original ISO11898 standard of 40m by careful system design and datarate tradeoffs. For example CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO11898 CAN standard. In using this flexibility comes the responsibility of good network design and balancing these tradeoffs.

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CAN TERMINATION

The ISO11898 standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with 120 Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus the termination must be carefully placed so that it is not removed from the bus.

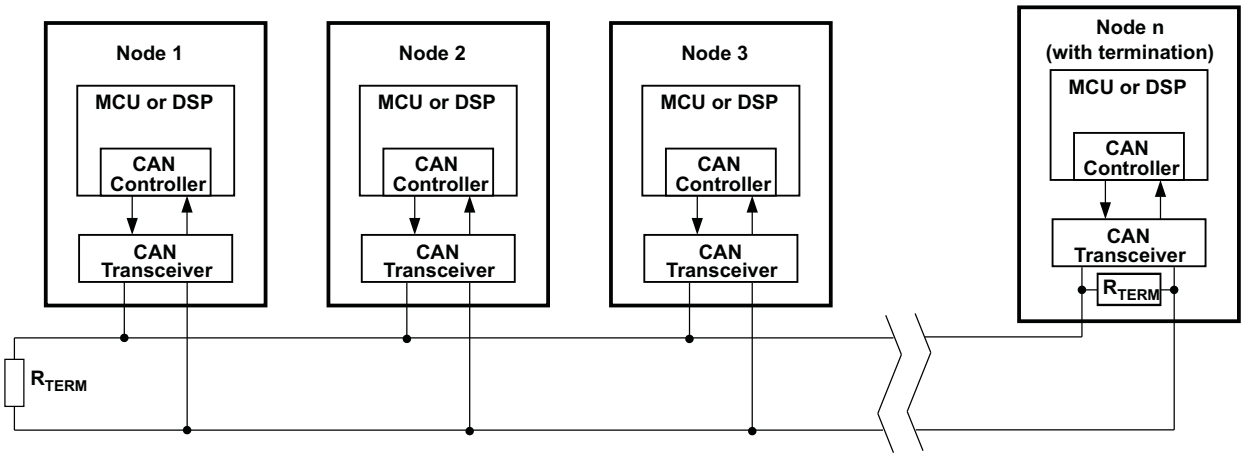


Figure 18. Typical CAN Bus

Termination may be a single 120 Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used. (See Figure 19). Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

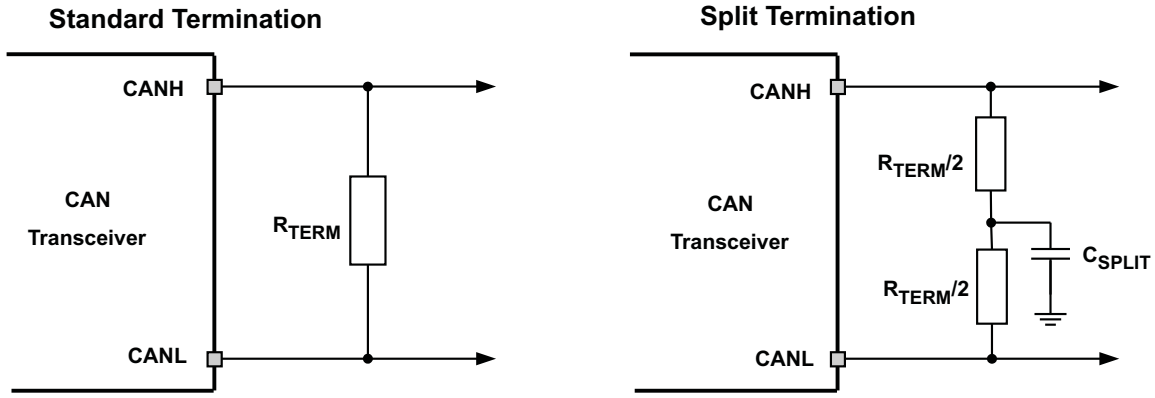


Figure 19. CAN Bus Termination Concepts

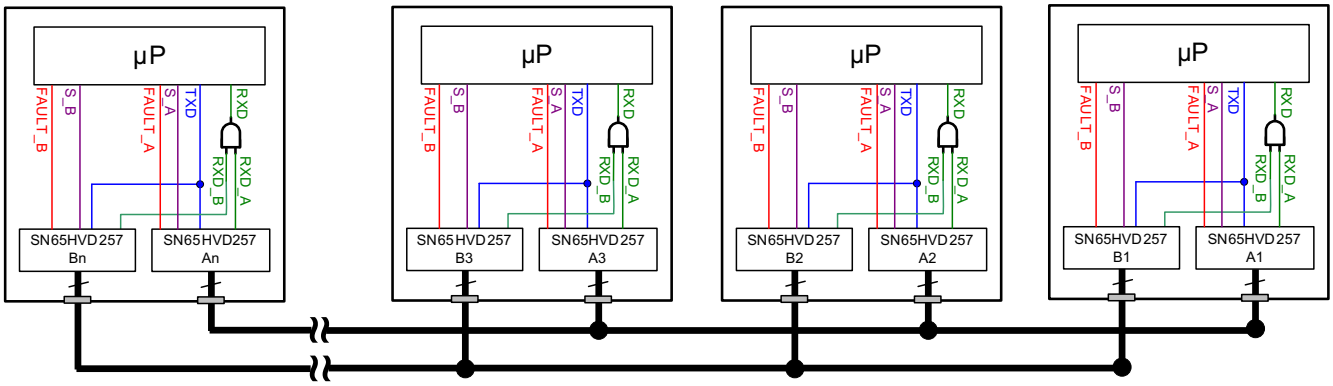
Example: Functional Safety Using the SN65HVD257 in a Redundant Physical Layer CAN Network Topology

CAN is a standard linear bus topology using 120 Ω twisted pair cabling. The SN65HVD257 CAN device includes several features to use the CAN physical layer in nonstandard topologies with only one CAN link layer controller (µP) interface. This allows much greater flexibility in the physical topology of the bus while reducing the digital controller and software costs. The combination of RXD DTO and the FAULT output allows great flexibility, control and monitoring of these applications.

A simple example of this flexibility is to use two SN65HVD257 devices in parallel with an AND gate to achieve redundancy (parallel) of the physical layer (cabling & PHYs) in a CAN network.

For the CAN bit-wise arbitration to work, the RXD outputs of the transceivers must connect via AND gate logic so that a dominant bit (low) from any of the branches is received by the link layer logic (µP), and appears to the link layer and above as a single physical network. The RXD DTO feature prevents a bus stuck dominant fault in a single branch from taking down the entire network by forcing the RXD pin for the transceivers on the branch with the fault back to the recessive after the t_{RXD_DTO} time. The remaining branch of the network continues to function. The FAULT pin of the transceivers on the branch with the fault indicates this via the FAULT output to their host processors, which diagnose the failure condition. The S pin (silent mode pin) may be used to put a branch in silent mode to check each branch for other faults. Thus it is possible to implement a robust and redundant CAN network topology in a very simple and low cost manner.

These concepts can be expanded into more complicated & flexible CAN network topologies to solve various system level challenges with a networked infrastructure.



A. CAN nodes with termination are PHY A, PHY B, PHY An and PHY Bn.

B. RXD DTO prevents a single branch-stuck-dominant condition from blocking the redundant branch via the AND logic on RXD. The transceivers signal a received bus stuck dominant fault via the FAULT pin. The system detects which branch is stuck dominant, and issues a system warning. Other network faults on a single branch that appear as recessive (not blocking the redundant network) may be detected through diagnostic routines, and using the Silent Mode of the PHYs to use only one branch at a time for transmission during diagnostic mode. This combination allows robust fault detection and recovery within single branches so that they may be repaired and again provide redundancy of the physical layer.

Figure 20. Typical Redundant Physical Layer Topology Using the SN65HVD257

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REVISION HISTORY

Changes from Original (December 2011) to Revision A **Page**

- Updates the Features list 1
- Updated the Applications list 1
- Added text to the Description "The SN65HVD257 adds additional.." 1
- Changed Figure 1 - Functional Block Diagram to include HVD257 and Note changes. 1
- Added SN65HVD257 to the D PACKAGE OPTIONS images 2
- Changed the DEVICE OPTIONS table 2
- Added SN65HVD257 FAULT pin to the PIN FUNCTIONS table 2
- Added SN65HVD257 to the Ordering Information table 2
- Added footnote for SN65HVD257 function to Table 3 4
- Added 5 V V_{CC} with FAULT Open-Drain Output Device (SN65HVD257) section 5
- Added RXD Dominant Timeout (SN65HVD257) section 5
- Added FAULT pin information 6
- Added SN65HVD257 FAULT pin information to the Abs Max table 9
- Added FAULT pin information to the ROC table 9
- changed R_{ID} - Differential input resistance value from 3 kΩ to 30 kΩ 12
- Added t_{RXD_DTO} - SN65HVD257 information 12
- Added Figure 8 "RXD Dominant Timeout Test Circuit and Measurement" 14
- Added Figure 9 "FAULT Test and Measurement" 14
- Added Example: Functional Safety Using the SN65HVD257 in a Redundant Physical Layer CAN Network Topology section 20

Changes from Revision A (June 2012) to Revision B **Page**

- Added SN65HVD257 status to production in Ordering Information table 2

Changes from Revision B (June 2012) to Revision C **Page**

- Added Figure 6 - Example Timing Diagram for TXD DTO and FAULT Pin 7
- Added Table 6 - Receiver Differential Input Voltage Threshold Test 15
- Added - Bus loading, length and number of nodes section to Application Information 18

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD255D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD255	Samples
SN65HVD255DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD255	Samples
SN65HVD256D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD256	Samples
SN65HVD256DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD256	Samples
SN65HVD257D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD257	Samples
SN65HVD257DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD257	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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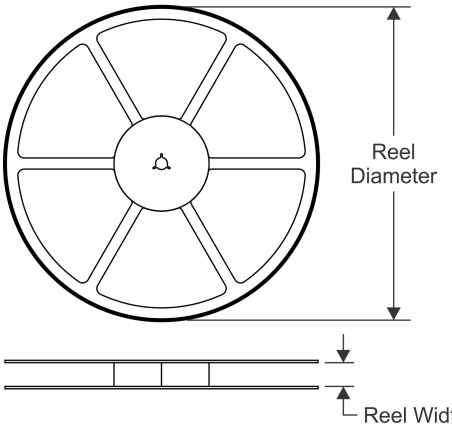
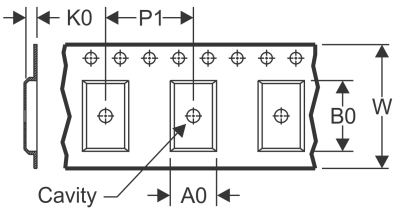
TAPE AND REEL INFORMATION

REEL DIMENSIONS

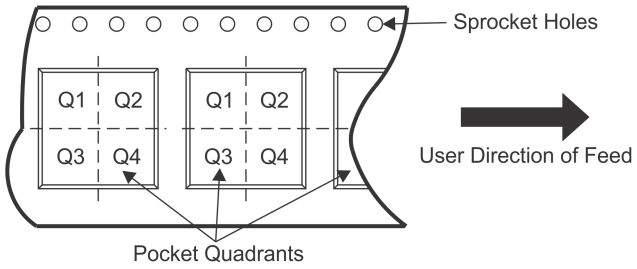


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

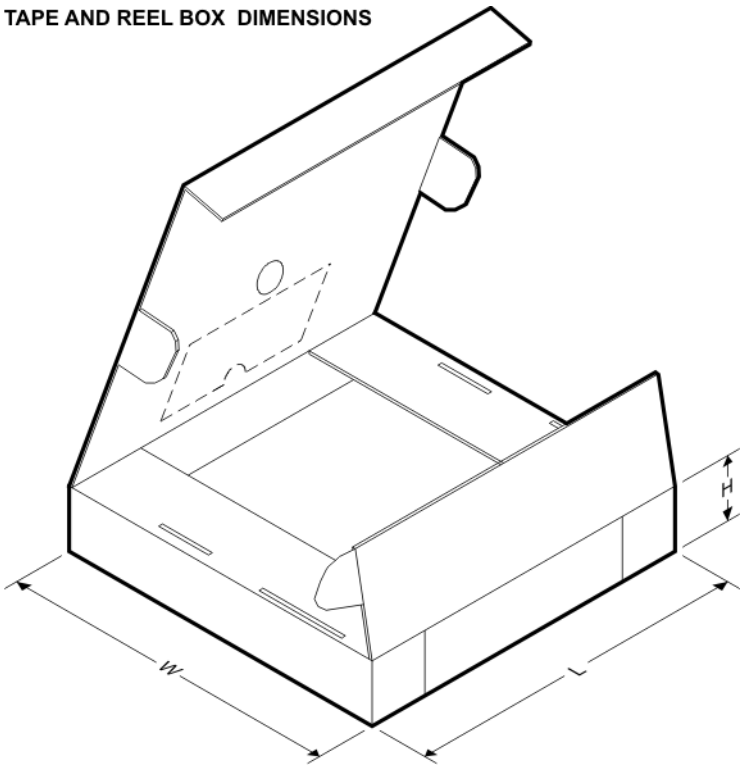
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD255DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD256DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD257DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

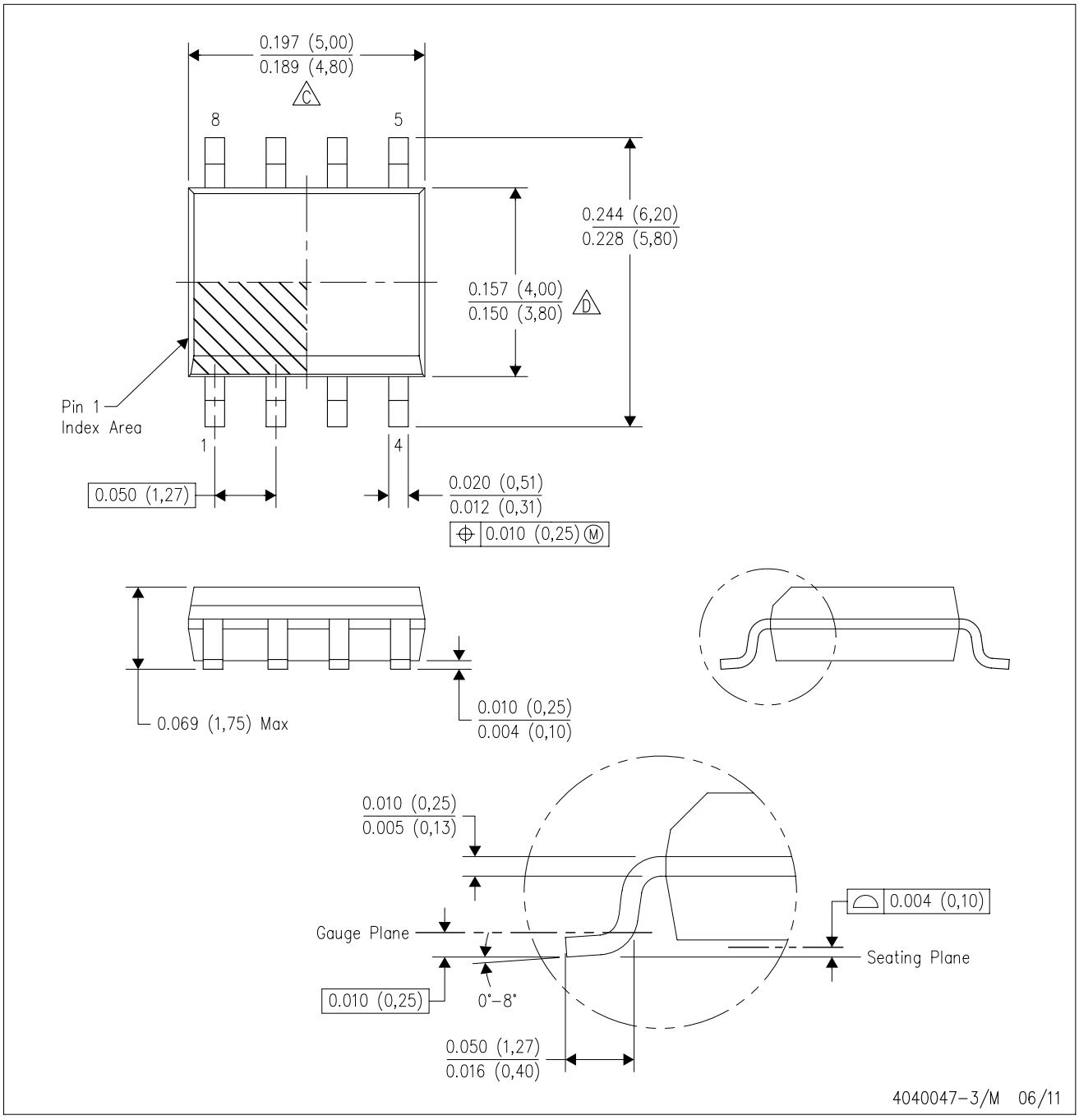
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

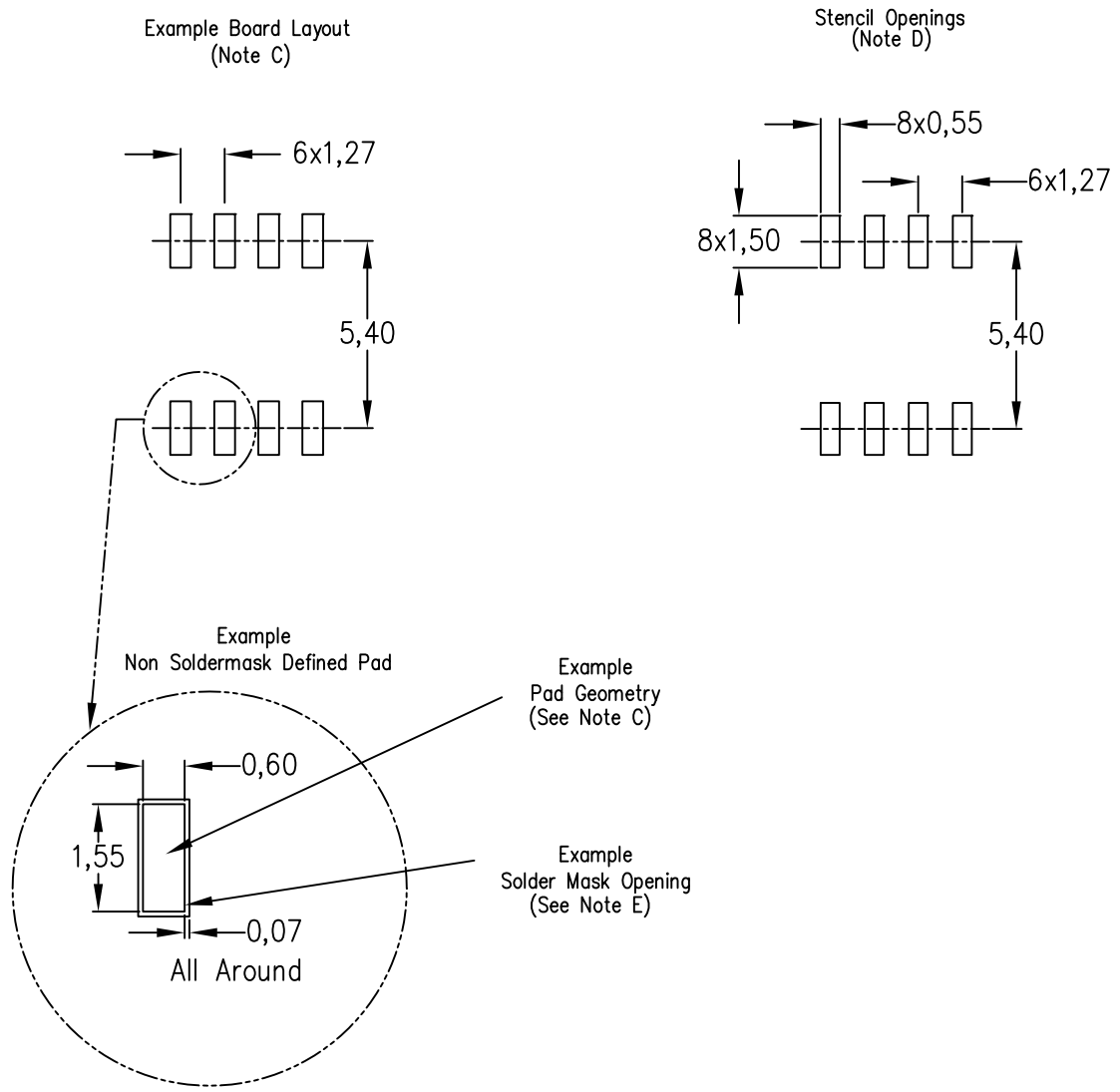
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD255DR	SOIC	D	8	2500	340.5	338.1	20.6
SN65HVD256DR	SOIC	D	8	2500	340.5	338.1	20.6
SN65HVD257DR	SOIC	D	8	2500	340.5	338.1	20.6

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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