3.3 V ECL 1:2 Fanout Buffer

FEATURES

- 1:2 ECL Fanout Buffer
- Operating Range
  - PECL V_{CC} = 3.0 V to 3.8 V With V_{EE} = 0 V
  - NECL: V_{CC} = 0 V with V_{EE} = –3.0 to –3.8V
- 5 ps Skew Between Outputs
- Support for Clock Frequencies > 2.0 GHz
- 265 ps Typical Propagation Delay
- Deterministic Output Value for Open Input Conditions or When Inputs = V_{EE}
- Built-in Temperature Compensation
- Drop in Compatible to MC10LVEL11, MC100LVEL11
- Built-In Input Pull Down Resistors

APPLICATIONS

- Data and Clock Transmission Over Backplane
- Signaling Level Conversion

DESCRIPTION

The SN65LVEL11 is a fully differential 1:2 ECL fanout buffer. The device includes circuitry to maintain a known logic level when inputs are in open condition. The SN65LVEL11 is functionally equivalent to SN65EL11 with improved performance. The SN65LVEL11 is housed in an industry standard SOIC-8 package and is also available in the TSSOP-8 package option.

PINOUT ASSIGNMENT

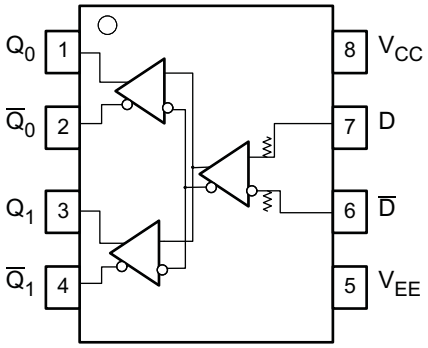


Table 1. Pin Description

PIN	FUNCTION
D, $\overline{D}$	PECL/ECL data inputs
Q_0, $\overline{Q}_0$, Q_1, $\overline{Q}_1$	PECL/ECL outputs
V_{CC}	Positive supply
V_{EE}	Negative supply

ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE	LEAD FINISH
SN65LVEL11D	SN65LVEL11	SOIC	NiPdAu
SN65LVEL11DGK	SN65LVEL11	SOIC-TSSOP	NiPdAu

(1) Leaded device options not initially available. Contact TI sales representative for further details.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

PARAMETER	CONDITION	VALUE	UNIT
Absolute PECL mode supply voltage, V_{CC}	V_{EE} = 0 V	6	V
Absolute NECL mode power supply, V_{EE}	V_{CC} = 0 V	–6	V
PECL mode input voltage	V_{EE} = 0 V; $V_I \le$ VCC	6	V
NECL mode input voltage	V_{CC} = 0 V; $V_I \ge V_{EE}$	–6	V
Output current	Continuous	50	mA
	Surge	100	
Operating temperature range		–40 to 85	°C
Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

POWER DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	POWER RATING T_A < 25°C (mW)	THERMAL RESISTANCE, JUNCTION TO AMBIENT NO AIRFLOW	DERATING FACTOR T_A > 25°C (mW/°C)	POWER RATING T_A = 85°C (mW)
SOIC	Low-K	719	139	7	288
	High-K	840	119	8	336
SOIC-TSSOP	Low-K	469	213	5	188
	High-K	527	189	5	211

THERMAL CHARACTERISTICS

PARAMETER		PACKAGE	VALUE	UNIT
θ_{JB}	Junction-to Board Thermal Resistance	SOIC	79	°C/W
		SOIC-TSSOP	120	
θ_{JC}	Junction-to Case Thermal Resistance	SOIC	98	°C/W
		SOIC-TSSOP	74	

KEY ATTRIBUTES

CHARACTERISTICS	VALUE
Internal input pull down resistor	75 kΩ
Moisture sensitivity level	Level 1
Flammability rating (Oxygen Index: 28 to 34)	UL 94 V-0 at 0.125 in
ESD-HBM	4 kV
ESD-machine model	200 V
ESD-charge device model	2 kV
Meets or exceeds JEDEC Spec EIA/JESD78 latchup test	

LVPECL DC CHARACTERISTICS[1] (V_{CC} = 3.3 V, V_{EE} = 0.0 V[2])

CHARACTERISTICS		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Power Supply Current		20	25		20	25		21	25	mA
V_{OH}	Output HIGH Voltage [3]	2215		2420	2215	2286	2420	2215		2420	mV
V_{OL}	Output LOW Voltage[3]	1470		1680	1470	1584	1680	1470		1680	mV
V_{IH}	Input High Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1490		1825	1490		1825	1490		1825	mV
V_{IHCMR}	Input HIGH voltage common mode range (Differential) [4]										V
	V_{pp} < 500 mV	1.2		3.1	1.1		3.1	1.1		3.1	
	V_{pp} > 500 mV	1.4		3.1	1.3		3.1	1.3		3.1	
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW current										
	D	0.5			0.5			0.5			µA
	$\overline{D}$	–600			–600			–600			

(1) Device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V
(3) Outputs are terminated through a 50 Ω resistor to V_{CC} – 2.0 V.
(4) V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} min and 1 V.

LVPNECL DC CHARACTERISTICS[1] (V_{EE} = –3.3 V; V_{CC} = 0.0 V;) [2]

CHARACTERISTICS		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{EE}	Power supply current		20	25		20	25		21	25	mA
V_{OH}	Output HIGH voltage [3]	–1085		–880	–1085	–1013	–880	–1085		–880	mV
V_{OL}	Output LOW voltage[3]	–1830		–1620	–1830	–1722	–1620	–1830		–1620	mV
V_{IH}	Input high voltage (Single-Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW voltage (Single-Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{IHCMR}	Input HIGH voltage common mode range (Differential) [4]										V
	V_{pp} < 500 mV	–2.1		–0.2	–2.2		–0.2	–2.2		–0.2	
	V_{pp} > 500 mV	–1.9		–0.2	–2.0		–0.2	–2.0		–0.2	
I_{IH}	Input HIGH current			150			150			150	µA
I_{IL}	Input LOW current										
	D	0.5			0.5			0.5			µA
	$\overline{D}$	–600			–600			–600			

(1) Device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
(3) Outputs are terminated through a 50 Ω resistor to V_{CC} – 2.0 V.
(4) VIHCMR min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between VPP min and 1 V.

AC CHARACTERISTICS [1](V_{CC} = 3.3 V; V_{EE} = 0.0 V or V_{CC} = 0.0 V; V_{EE} = –3.3 V)[2]

CHARACTERISTIC		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	Max switching frequency[3] See Figure 6		2.9			2.7			2.4		GHz
t_{PLH}/t_{PHL}	Propagation delay to output	235		350	235		350	235		350	ps
t_{SKEW}	Within device skew[4]		10	18		10	18		10	18	ps
	Device to device skew[5]		10	25		10	25		10	25	ps
	Duty cycle skew[6]		5	15		5	15		5	15	ps
t_{JITTER}	Random clock jitter (RMS)		0.2			0.2			0.2		ps
V_{PP}	Input swing[7]	200		1000	200		1000	200		1000	mV
t_r/t_f	Output rise/fall times Q (20%–80%)	150		300	150		300	150		300	ps

(1) Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) V_{EE} can vary ±0.3 V
(3) Maximum switching frequency measured at output amplitude of 300 mVpp.
(4) Within-device skew is defined as identical transitions on similar paths through a device.
(5) Device-Device Skew is defined as identical transitions at identical Vcc levels.
(6) Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
(7) $V_{PP(min)}$ is the minimum input swing for which AC parameters are assured.

Typical Termination for Output Driver

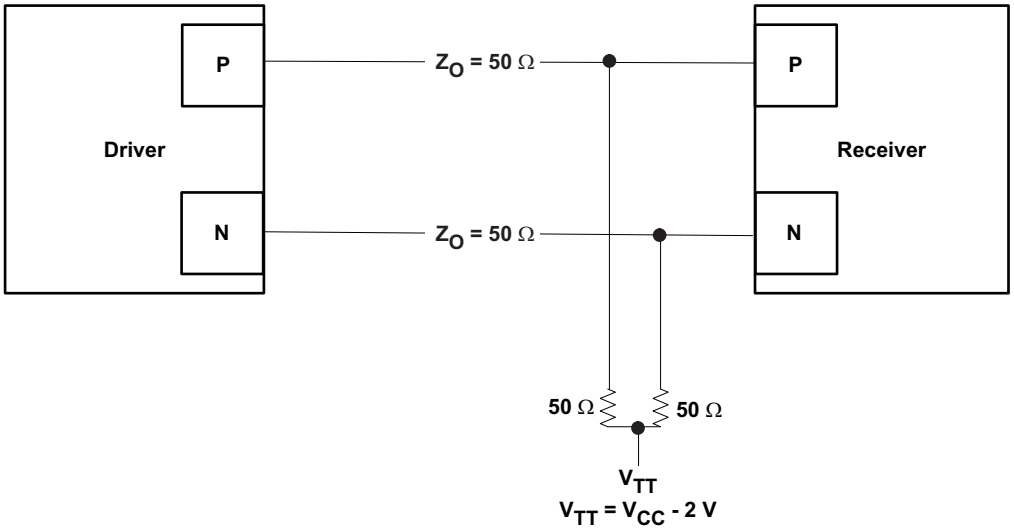


Figure 1. Termination for Output Driver

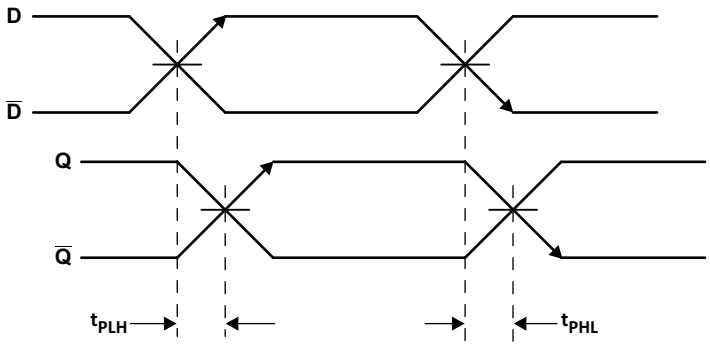


Figure 2. Propagation Delay

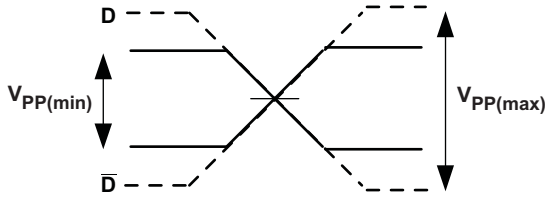


Figure 3. Input Voltage Swing

Figure 4. Output Rise and Fall Times

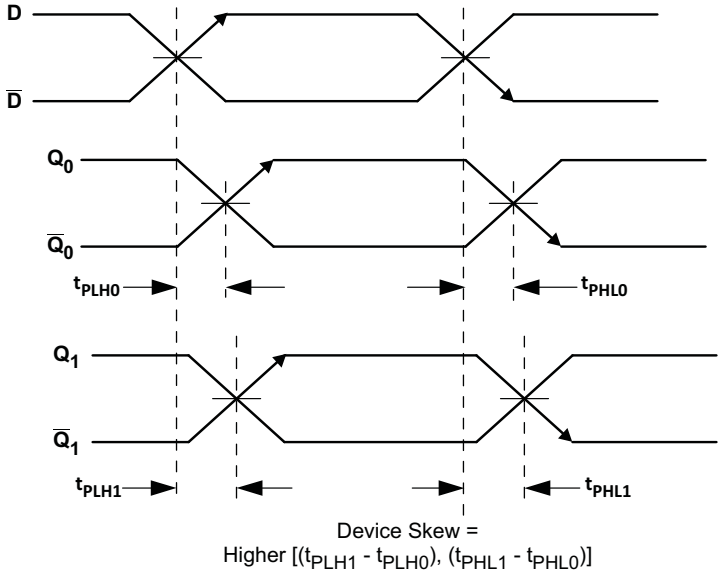


Figure 5. Device Skew

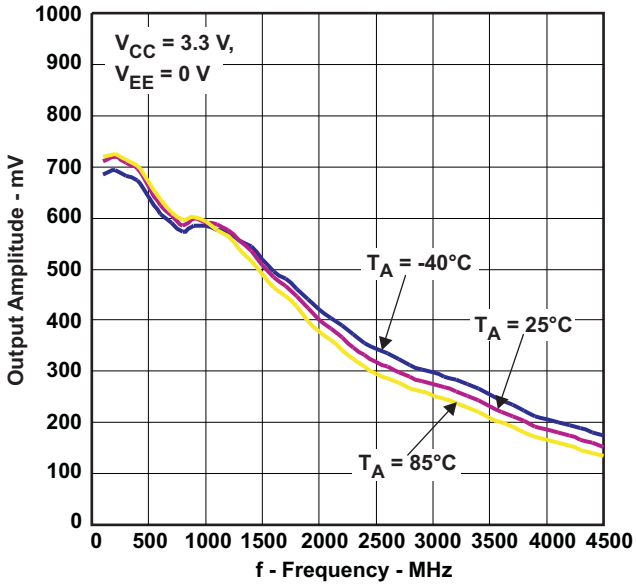


Figure 6. Output Amplitude vs Frequency

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVEL11D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVEL11	Samples
SN65LVEL11DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SINI	Samples
SN65LVEL11DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-1-260C-UNLIM	-40 to 85	SINI	Samples
SN65LVEL11DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVEL11	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

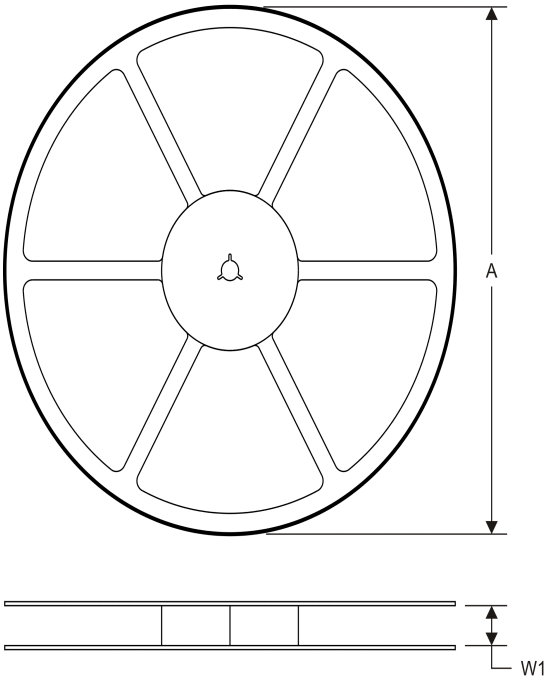
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

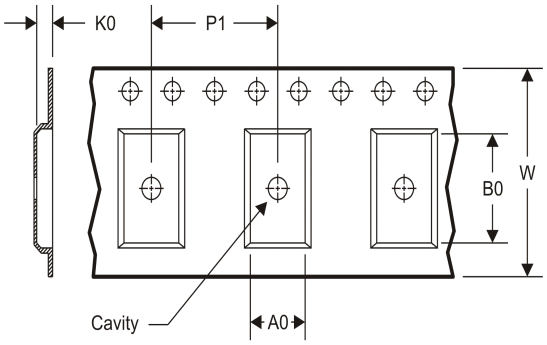
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



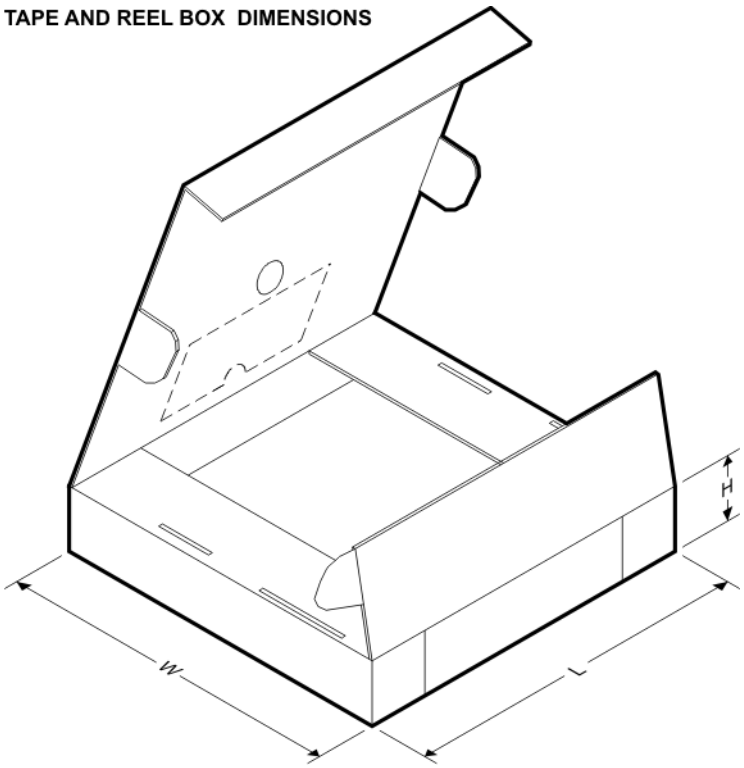
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVEL11DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65LVEL11DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

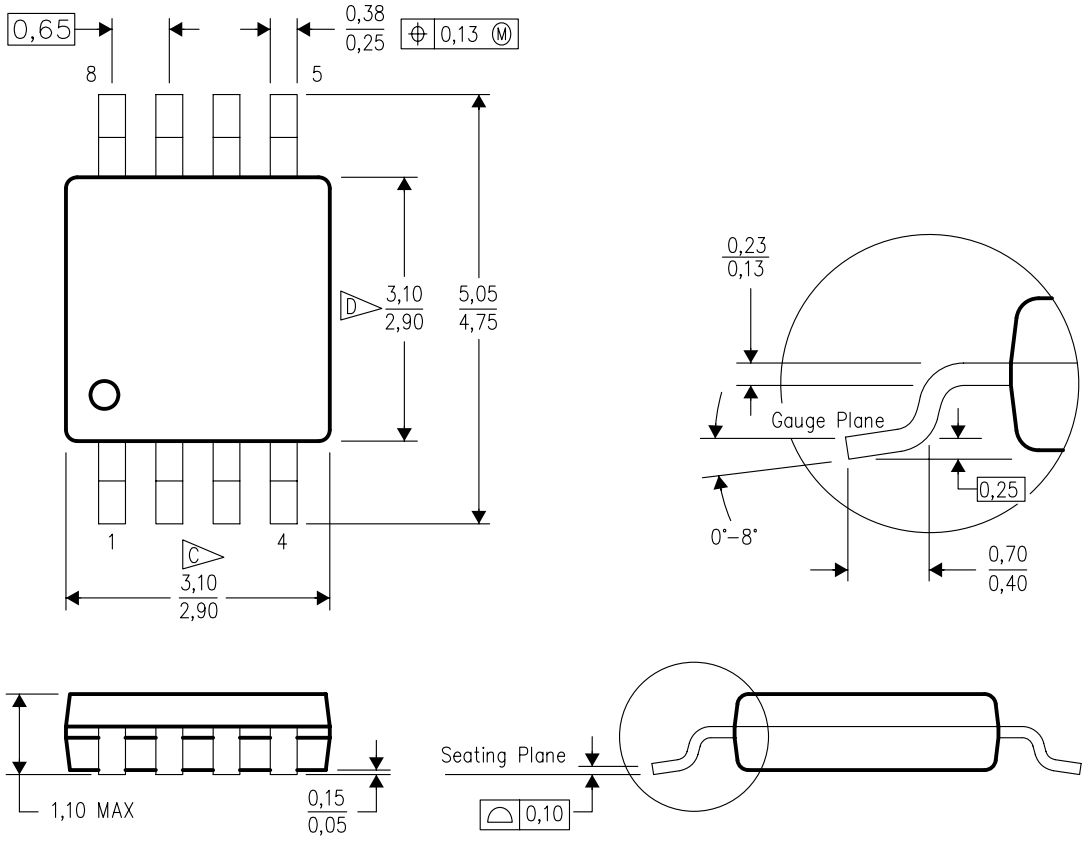
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVEL11DGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
SN65LVEL11DR	SOIC	D	8	2500	367.0	367.0	35.0

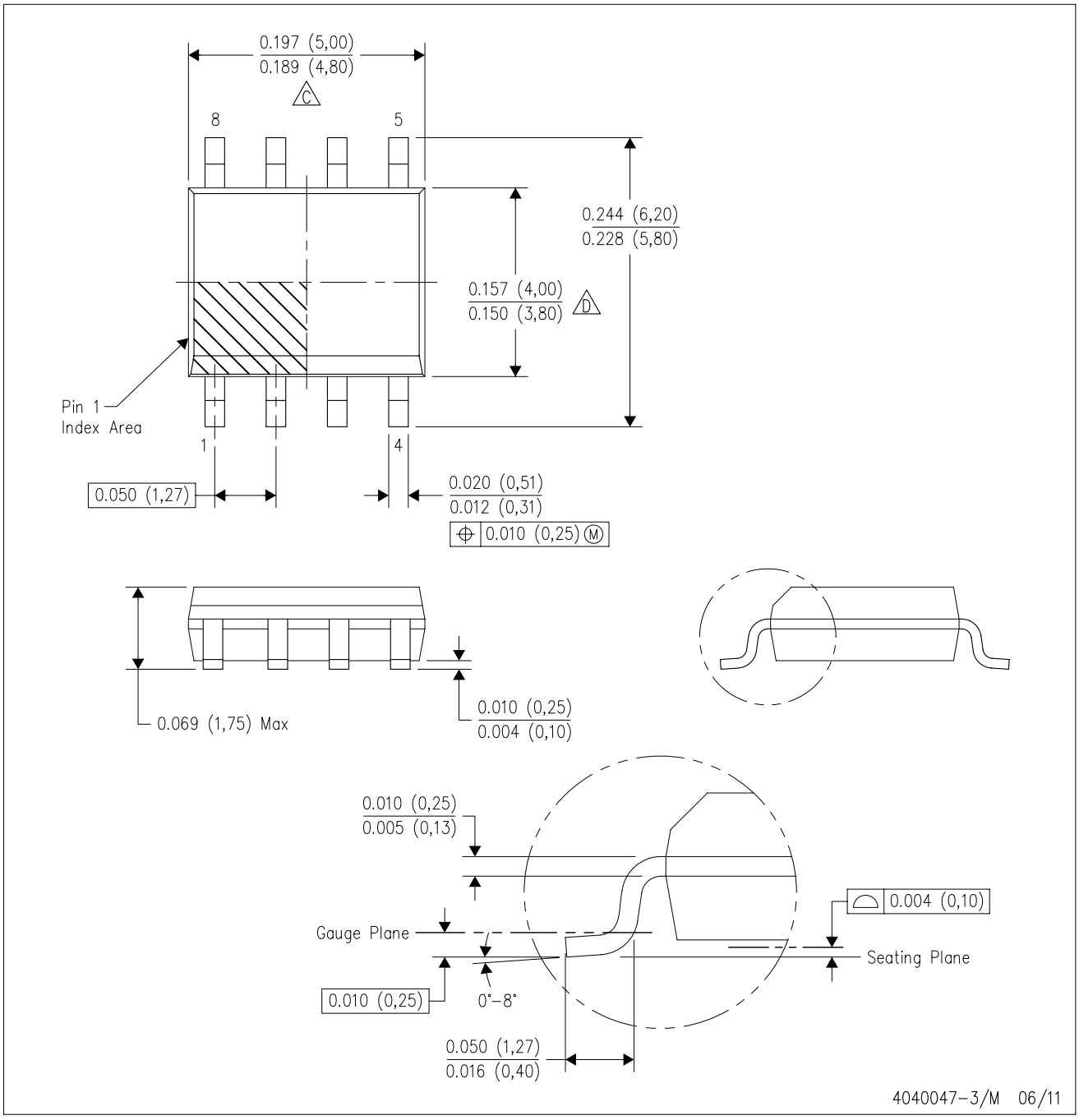
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

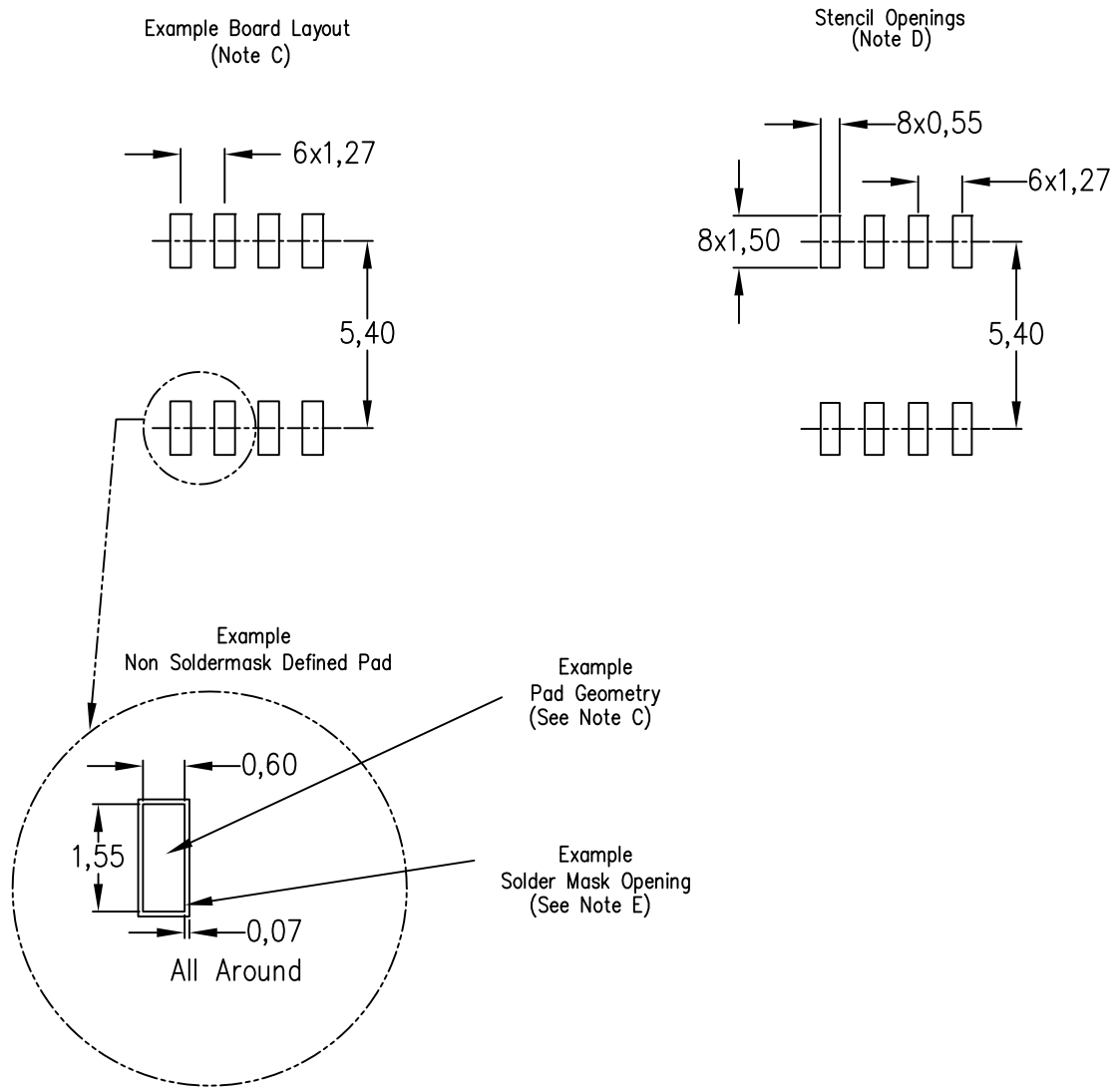
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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