Dual Channel USB3.0 Redriver/Equalizer

Check for Samples: SN65LVPE502A, SN65LVPE502B

FEATURES

- **Single Lane USB 3.0 Equalizer/Redriver**
- **Selectable Equalization, De-Emphasis and Output Swing Control**
- **Integrated Termination**
- **Hot-Plug Capable**
- **Low Active Power (U0 state)**
  - **315 mW (TYP), V_{CC} = 3.3V**
- **USB 3.0 Low Power Support**
  - **7 mW (TYP) When no Connection Detected**
  - **70 mW (TYP) When Link in U2/U3 Mode**
- **Excellent Jitter and Loss Compensation Capability:**
  - **>40" of Total 4 mil Stripline on FR4**
- **Small Foot Print – 3 x 3mm and 4 x 4mm 24-pin QFN Packages**
- **High Protection Against ESD Transient**
  - **HBM: 5,000 V**
  - **CDM: 1,500 V**
  - **MM: 200 V**

APPLICATIONS

- **Notebooks, Desktops, Docking Stations, Active Cable, Backplane and Active Cable**

DESCRIPTION

The SN65LVPE502x is a dual channel, single lane USB 3.0 redriver and signal conditioner supporting data rates of 5.0Gbps. The device complies with USB 3.0 spec revision 1.0, supporting electrical idle condition and low frequency periodic signals (LFPS) for USB 3.0 power management modes.

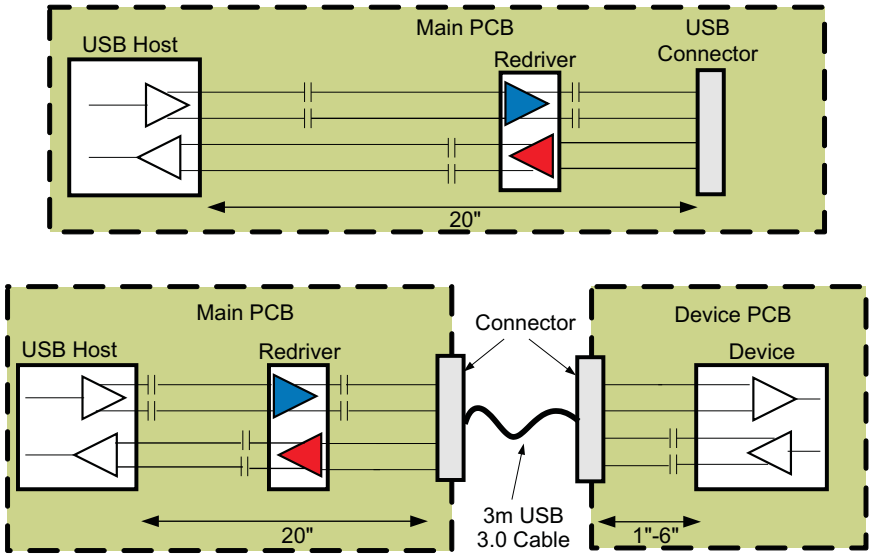


Figure 1. Typical Application

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

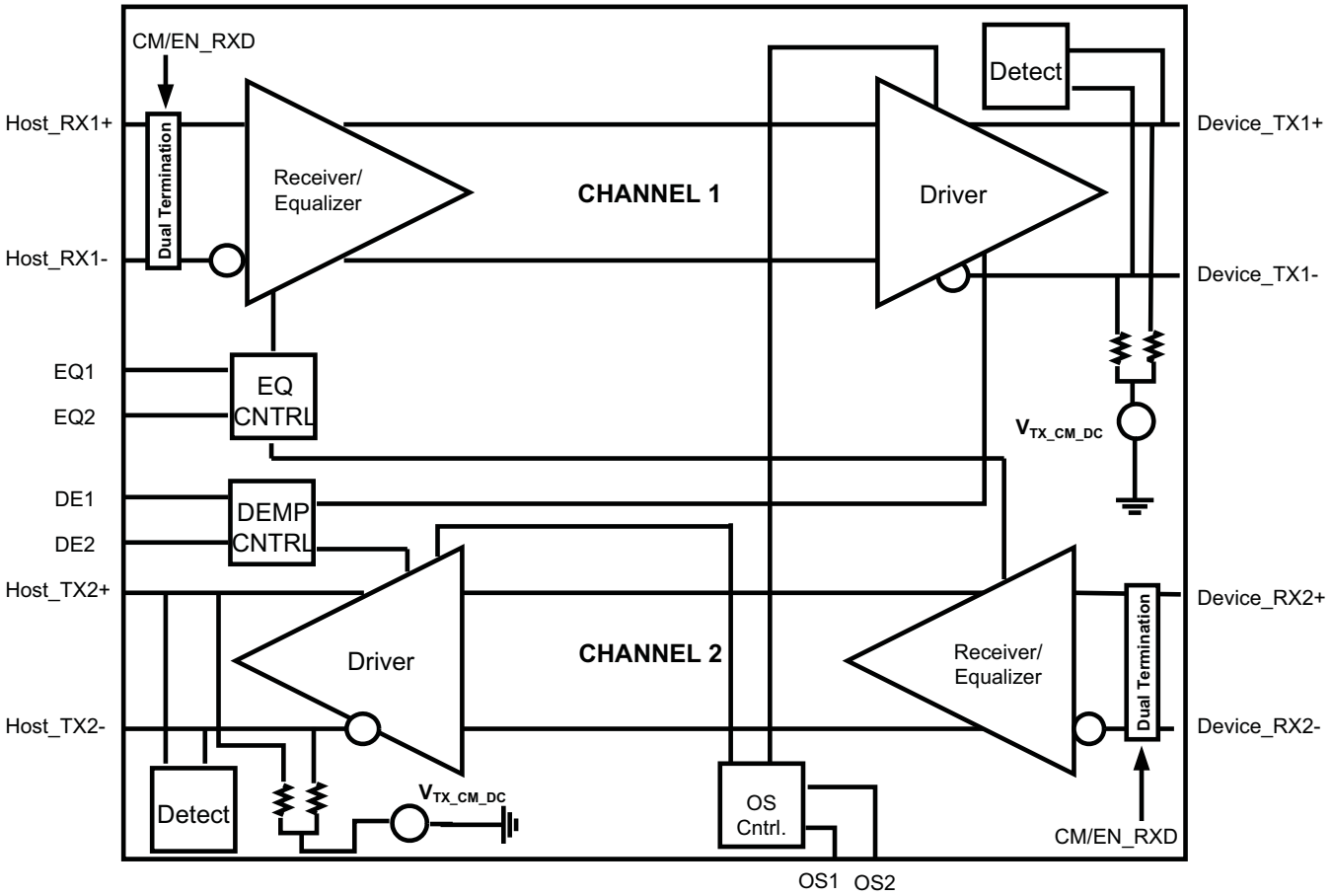


Figure 2. Data Flow Block Diagram

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Supply voltage range(2)	V_{CC}	–0.5	4	V
Voltage range	Differential I/O	–0.5	4	V
	Control I/O	–0.5	VCC + 0.5	V
Electrostatic discharge	Human body model(3)	±5000		V
	Charged-device model(4)	±1500		V
	Machine model(5)	±200		V
Continuous power dissipation		See the Thermal Table		

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A

THERMAL INFORMATION

THERMAL METRIC(1)		RGE PACKAGE	RLL PACKAGE	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	46	41.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	42	43.2	
θ_{JB}	Junction-to-board thermal resistance	13	11.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	4	6.3	
Ψ_{JT}	Junction-to-top characterization parameter		1.1	
Ψ_{JB}	Junction-to-board characterization parameter		11.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

THERMAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX(1)	UNIT
P_D	Device power dissipation	RSVD, EN_RXD, EQ cntrl pins = NC, K28.5 pattern at 5 Gbps, V_{ID} = 1000 mV_{p-p}		330	450	mW
P_{Slp}	Device power dissipation in sleep mode	EN_RXD = GND		0.03	0.4	mW

(1) The maximum rating is simulated under 3.6V VCC.

Device Power

The SN65LVPE502x is designed to operate from a single 3.3V supply.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply voltage		3	3.3	3.6	V
$C_{COUPLING}$	AC Coupling capacitor		75		200	nF
	Operating free-air temperature		-40		85	°C
DEVICE PARAMETERS						
I_{CC}	Supply current	EN_RXD, RSVD, EQ cntrl = NC, K28.5 pattern at 5 Gbps, VID = 1000mVp-p		100	120	mA
$ICC_{Rx.Detect}$		In Rx.Detect mode		2	5	
ICC_{sleep}		EN_RXD = GND		0.01	0.1	
ICC_{U2-U3}		Link in USB low power state		21		
	Maximum data rate				5	Gbps
t_{ENB}	Device enable time	Sleep mode exit time EN_RXD L → H With Rx termination present			100	µs
t_{DIS}	Device disable time	Sleep mode entry time EN_RXD H → L			2	µs
$T_{RX.DETECT}$	Rx.Detect start event	Power-up time			100	µs
CONTROL LOGIC						
V_{IH}	High level input voltage		2.8		V_{CC}	V
V_{IL}	Low level input voltage		–0.3		0.5	V
V_{HYS}	Input hysteresis			150		mV
I_{IH}	High level input current	OSx, EQx, DEx = V_{CC}			30	µA
		EN_RXD = V_{CC}			1	
		RSVD = V_{CC}			30	
I_{IL}	Low level input current	OSx, EQx, DEx = GND	–30			µA
		EN_RXD = GND	–30			
		RSVD = GND	–1			

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER AC/DC						
$Vin_{diff\_p\text{-}p}$	RX1, RX2 input voltage swing	AC coupled differential RX peak to peak signal	100		1200	mVpp
VCM_RX	RX1, RX2 common mode voltage			3.3		V
Vin_{COM_P}	RX1, RX2 AC peak common mode voltage	Measured at Rx pins with termination enabled			150	mVP
Z_{CM_RX}	DC common mode impedance		18	26	30	Ω
Z_{diff_RX}	DC differential input impedance		72	80	120	Ω
$Z_{RX\_High\_IMP+}$	DC Input high impedance	Device in sleep mode Rx termination not powered measured with respect to GND over 500mV max	50	85		kΩ
$V_{RX\text{-}LFPS\text{-}DETpp}$	Low frequency periodic signaling (LFPS) detect threshold	Measured at receiver pin, below minimum output is squelched, above max input signal is passed to output	100		300	mVpp
$RL_{RX\text{-}DIFF}$	Differential return loss	50 MHz – 1.25 GHz	10	11		dB
		1.25 GH – 2.5 GHz	6	7		
$RL_{RX\text{-}CM}$	Common mode return loss	50 MHz– 2.5 GHz	11	13		dB
TRANSMITTER AC/DC						
$V_{TXDIFF\_TB\_P\text{-}P}$	Differential peak-to-peak output voltage (VID = 800, 1200 mVpp, 5 Gbps)	R_L = 100 Ω ±1%, DEx, OSx = NC, **Transition Bit**	800	1042	1200	mV
		R_L = 100 Ω ±1%, DEx = NC, OSx = GND **Transition Bit**		908		
		R_L = 100 Ω ±1%, DEx = NC, OSx = VCC **Transition Bit**		1127		
$V_{TXDIFF\_NTB\_P\text{-}P}$		R_L = 100 Ω ±1%, DEx=NC, OSx = 0,1,NC **Non-Transition Bit**		1042		mV
		R_L = 100 Ω ±1%, DEx=0 OSx = 0,1,NC **Non-Transition Bit**		661		
		R_L = 100 Ω ±1%, DEx=1 OSx = 0,1,NC **Non-Transition Bit**		507		
DE	De-emphasis level OS1,2 = NC (for OS1, 2 = 1 and 0 see Table 2)	DE1/DE2 = NC		0		dB
		DE1/DE2 = 0 (SN65LVPE502ARLL)		–3.5		
		DE1/DE2 = 0 (SN65LVPE502ARGE, SNLVPE502BRGE)	–3.0	–3.5	–4.0	
		DE1/DE2 = 1		–6.0		
T_{DE}	De-emphasis width			0.85		UI
Z_{diff_TX}	DC differential impedance		72	90	120	Ω
Z_{CM_TX}	DC common mode impedance	Measured w.r.t to AC ground over 0-500mV	18	23	30	Ω
RL_{diff_TX}	Differential return loss	f = 50 MHz – 1.25 GHz	9	10		dB
		f = 1.25 GHz – 2.5 GHz	6	7		
RL_{CM_TX}	Common mode return loss	f = 50 MHz – 2.5 GHz	11	12		dB
I_{TX_SC}	TX short circuit current	TX± shorted to GND			60	mA
$V_{TX\_CM\_DC}$	Transmitter DC common-mode voltage	OSx = NC	2.0	2.6	3.0	V
$V_{TX\_CM\_AC\_Active}$	TX AC common mode voltage active			30	100	mVpp
$VT_{X\_idle\_diff\text{-}AC\text{-}pp}$	Electrical idle differential peak to peak output voltage	HPF to remove DC	0		10	mVpp
$V_{TX\_CM\_DeltaU1\text{-}U0}$	Absolute delta of DC CM voltage during active and idle states			35	200	mV
$V_{TX\_idle\_diff\text{-}DC}$	DC Electrical idle differential output voltage	Voltage must be low pass filtered to remove any AC component	0		10	mV
V_{detect}	Voltage change to allow receiver detect	Positive voltage to sense receiver termination			600	mV
t_R, t_F	Output rise/fall time	20%–80% of differential voltage measured 1" from the output pin	30	65		ps
t_{RF_MM}	Output rise/fall time mismatch	20%–80% of differential voltage measured 1" from the output pin		1.5	20	ps
T_{diff_LH}, T_{diff_HL}	Differential propagation delay	De-Emphasis = –3.5 dB (CH 0 and CH 1). Propagation delay between 50% level at input and output		305	370	ps
$t_{idleEntry}$, $t_{idleExit}$	Idle entry and exit times	See Figure 4		4	6	ns

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
C_{TX}	Tx input capacitance to GND	At 2.5 GHz		1.25		pF
JITTER						
T_{TX-EYE} (1) (2)	**Total jitter (Tj) at point A**	Device setting: OS1 = L, DE1 = –6 dB, EQ1 = 7 dB		0.23	0.5	UI(3)pp
DJ_{TX} (2)	Deterministic jitter (Dj)			0.14	0.3	
RJ_{TX} (2) (4)	Random jitter (Rj)			0.08	0.2	
T_{TX-EYE} (1) (2)	**Total jitter (Tj) at point B**	Device setting: OS2 = H, DE2 = –6 dB, EQ2 = 7dB		0.15	0.5	UI(3)Pp
DJ_{TX} (2)	Deterministic jitter (Dj)			0.07	0.3	
RJ_{TX} (2) (4)	Random jitter (Rj)			0.08	0.2	

(1) Includes RJ at 10^{-12} BER
(2) Determininstic jitter measured with K28.5 pattern, Random jitter measured with K28.5 pattern at the ends of reference channel in Figure 6, VID=1000mVpp, 5Gbps, –3.5dB DE from source
(3) UI = 200ps
(4) Rj calculated as 14.069 times the RMS random jitter for 10^{-12} BER

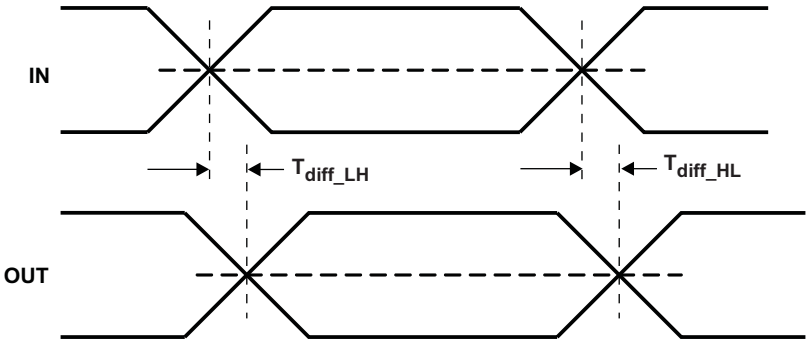


Figure 3. Propagation Delay

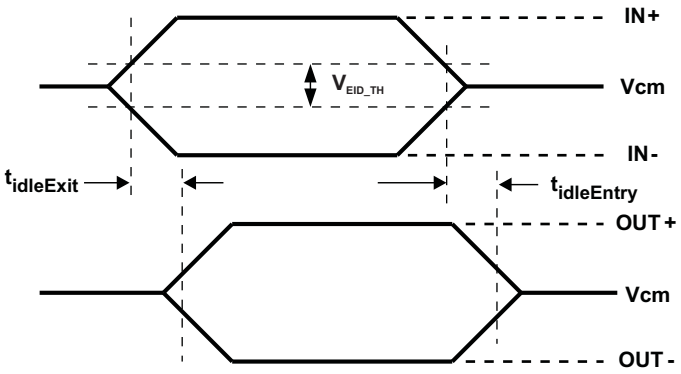


Figure 4. Electrical Idle Mode Exit and Entry Delay

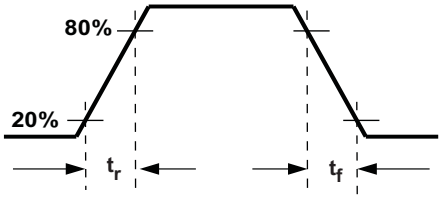


Figure 5. Ouput Rise and Fall Times

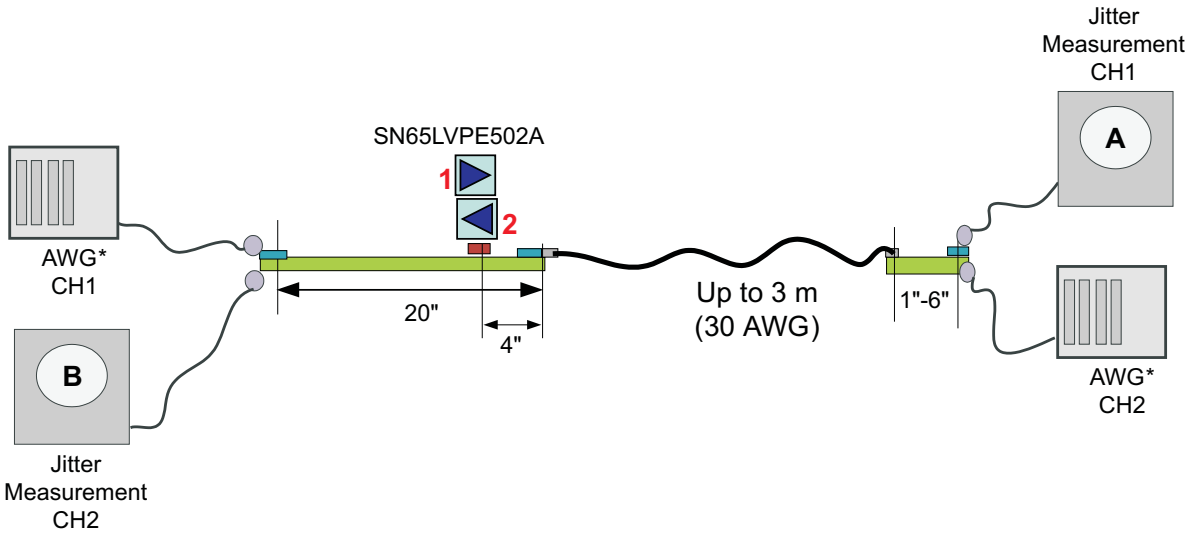


Figure 6. Jitter Measurement Setup

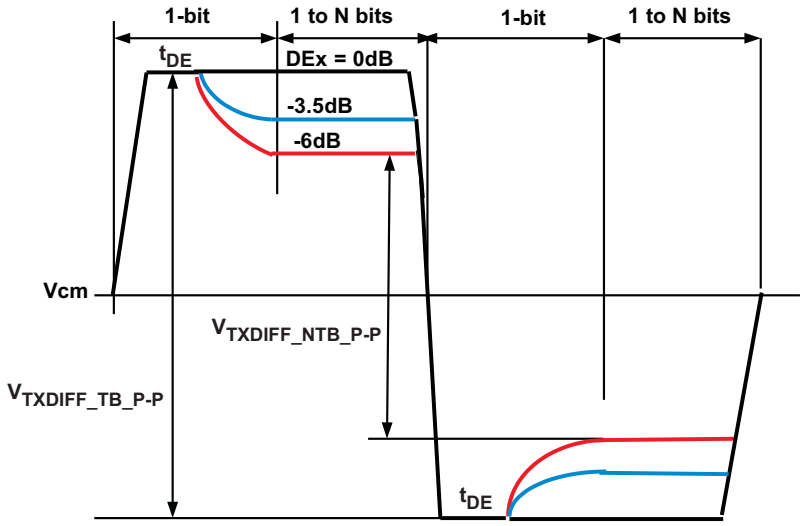
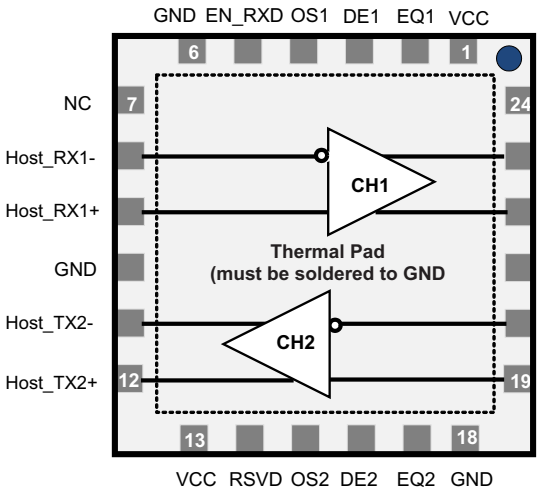


Figure 7. Output De-Emphasis Levels OSx = NC

DEVICE INFORMATION

SN65LVPE502A RGE PACKAGE (Top View)



SN65LVPE502B RGE PACKAGE (Top View)

SN65LVPE502A RLL PACKAGE (Top View)

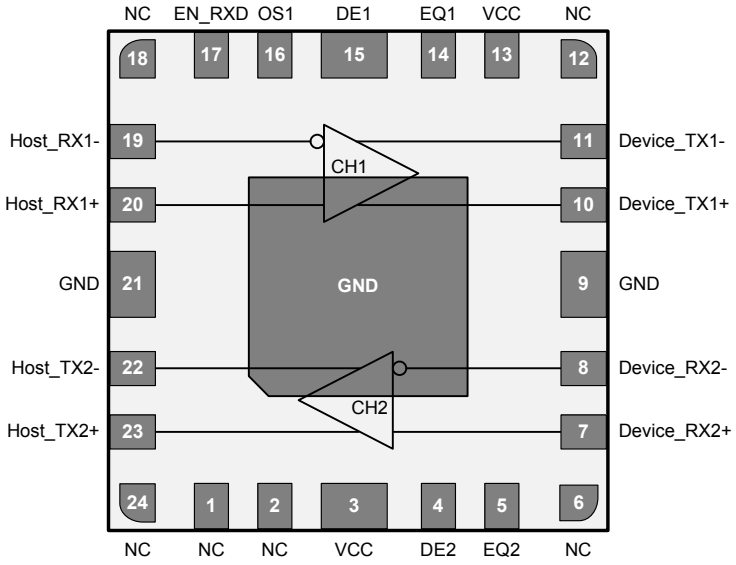


Table 1. Pin Functions

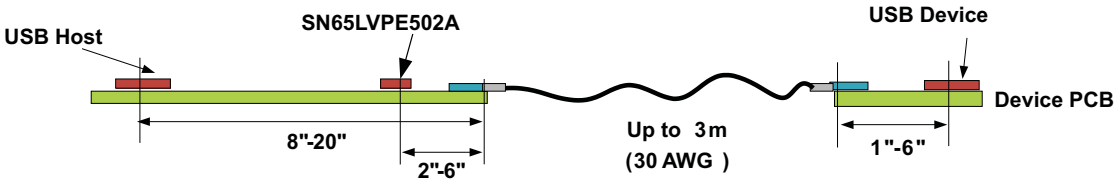
PIN				I/O Type	Description
'LVPE502A RGE	'LVPE502B RGE	'LVPE502A RLL	Name		
HIGH SPEED DIFFERENTIAL I/O PINS					
8	20	19	Host_RX1–	I, CML	Non-inverting and inverting CML differential input for CH1 and CH2. These pins are tied to an internal voltage bias by dual termination resistor circuit. Pins labeled "Host" must connect to the USB 3.0 host side. Pins labeled "Device" must connect to the USB 3.0 device side.
9	19	20	Host_RX1+	I, CML	
20	8	8	Device_RX2–	I, CML	
19	9	7	Device_RX2+	I, CML	
23	11	11	Device_TX1–	O, CML	Non-inverting and inverting CML differential output for CH1 and CH2. These pins are tied to an internal voltage bias by termination resistors. Pins labeled "Host" must connect to the USB 3.0 host side. Pins labeled "Device" must connect to the USB 3.0 device side.
22	12	10	Device_TX1+	O, CML	
11	23	22	Host_TX2–	O, CML	
12	22	23	Host_TX2+	O, CML	
DEVICE CONTROL PIN					
5	17	17	EN_RXD	I, LVCMOS	Sets device operation modes per Table 2. Internally pulled to V_{CC}.
14	—	—	RSVD	I, LVCMOS	RSVD. Can be left as No-Connect.
7, 24	2, 3, 4, 6, 14, 18, 24	1, 2, 6, 12, 18, 24	NC	No-Connect	Pads are not internally connected.
EQ CONTROL PINS (1)					
3, 16	16, 5	15, 4	DE1, DE2	I, LVCMOS	Selects de-emphasis settings for CH1 and CH2 per Table 2. Internally tied to $V_{CC}/2$
2, 17	15, 7	14, 5	EQ1, EQ2	I, LVCMOS	Selects equalization settings for CH1 and CH2 per Table 2. Internally tied to $V_{CC}/2$
4, 15	—	16, NC (2)	OS1, OS2	I, LVCMOS	Selects output amplitude for CH1 and CH2 per Table 2. Internally tied to $V_{CC}/2$
POWER PINS (3)					
1,13	1, 13	3	VCC	Power	Positive supply; should be 3.3V ±10%
6, 10, 18, 21, Thermal Pad	10, 21, Thermal Pad	9, Thermal Pad	GND	Power	Supply Ground

(1) Internally biased to $V_{CC}/2$ with >200kΩ pull-up/pull-down. When pins are left as NC board leakage at this pin pad must be < 1 µA otherwise drive to Vcc/2 to assert mid-level state
(2) The 'LVPE502A RLL has OS2 internally No-Connect, to select the 1042 mVpp level on TX2.
(3) For 'LVPE502B, pins 10 and 21 must be connected to GND, while 6 and 18 may be NC. For the 'LVPE502A RGE, it is recommended that at least two of the four pins (6, 10, 18, 21) be connected to ground.

Table 2. Signal Control Pin Setting

OUTPUT SWING AND EQ CONTROL (at 2.5 GHz)			
OSx(1)	**TRANSISTION BIT AMPLITUDE (TYP mVpp)**	**EQx(1)**	**EQUALIZATION (dB)**
NC (default)	1042	NC (default)	0
0	908	0	7
1	1127	1	15
OUTPUT DE CONTROL (at 2.5 GHz)			
DEx(1)	**OSx(1) = NC**	**OSx(1) = 0**	**OSx(1) = 1**
NC (default)	0 dB	0 dB	0 dB
0	–3.5 dB	–2.2 dB	–4.4 dB
1	–6.0 dB	–5.2 dB	–6.0 dB
CONTROL PINS SETTINGS			
EN_RXD	**DEVICE FUNCTION**		
1 (default)	Normal Operation		
0	Sleep Mode		

(1) Where x = Channel 1 or Channel 2



NOTE: For more detailed placement example of redriver see typical eye diagrams and jitter plots at end of data sheet.

Figure 8. Redriver Placement Example

DETAILED DESCRIPTION

Host- and Device-side Pins

The SN65LVPE502x features a link state machine that makes the device transparent on the USB 3.0 bus while minimizing power. The state machine relies on the system host to be connected to the pins named “Host”. USB 3.0 devices must be connected to the pins named “Device”. Multiple SN65LVPE502x devices may be used in series.

Programmable EQ, De-Emphasis and Amplitude Swing

The SN65LVPE502x is designed to minimize signal degradation effects such as crosstalk and inter-symbol interference (ISI) that limits the interconnect distance between two devices. The input stage of each channel offers selectable equalization settings that can be programmed to match loss in the channel. The differential outputs provide selectable de-emphasis to compensate for the anticipated distortion USB 3.0 signal will experience. Level of de-emphasis will depend on the length of interconnect and its characteristics. The SN65LVPE502x provides a unique way to tailor output de-emphasis on a per channel basis with use of DE and OS pins. All Rx and Tx equalization settings supported by the device are programmed by six 3-state pins as shown in Table 2.

Low Power Modes

Device supports three low power modes as described below

1. Sleep Mode

   Initiated anytime EN_RXD undergoes a high to low transition and stays low or when device powers up with EN_RXD set low. In sleep mode both input and output terminations are held at HiZ and device ceases operation to conserve power. Sleep mode max power consumption is 1mW, entry time is 2µs, device exits sleep mode to Rx.Detect mode after EN_RXD is driven to Vcc, exit time is 100µs max.

2. RX Detect Mode--When no remote device is connected

   Anytime 'LVPE502x detects a break in link (i.e. when upstream device is disconnected) or after power-up fails to find a remote device, 'LVPE502x goes to Rx Detect mode and conserves power by shutting down majority of its internal circuitry. In this mode input termination for both channels are driven to Hi-Z. In Rx Detect mode device power is <10mW (TYP) or less than 5% of its normal operating power . This feature is very useful in saving system power in mobile applications like notebook PC where battery life is critical.

   Anytime an upstream device gets reconnected the redriver automatically senses the connection and goes to normal operating mode. This operation requires no setting to the device.

3. U2/U3 Mode

   With the help of internal timers the device tracks when link enters USB 3.0 low power modes U2 and U3; in these modes link is in electrical idle state. 'LVPE502x will selectively turn-off internal circuitry to save on power. Typical power saving is about 75% lower than normal operating mode. The device will automatically revert to active mode when signal activity (LFPS) is detected.

Receiver Detection

At Power Up or Reset

After power-up or anytime EN_RXD is toggled, RX.Detect cycle is performed by first setting Rx termination for each channel to Hi-Z, device then starts sensing for receiver termination that may be attached at the other end of each TX.

If receiver is detected on both channel

- The TX and RX terminations are switched to Z_{DIFF_TX}, Z_{DIFF_RX} respectively.

If no receiver is detected on one or both channels

- The transmitter is pulled to Hi-Z
- The channel is put in low power mode
- Device attempts to detect Rx termination in 12 ms (TYP) interval until termination is found or device is put in sleep mode

During U2/U3 Link State

Rx detection is also performed periodically when link is in U2/U3 states. However in these states during Rx detection, input termination is not automatically disabled before performing Rx.Detect. If termination is found device goes back to its low power state if termination is not found then device disables its input termination and then jumps to power-up RX.Detect state.

Electrical Idle Support

Electrical idle support is needed for low frequency periodic signaling (LFPS) used in USB 3.0 side band communication. A link is in an electrical idle state when the TX± voltage is held at a steady constant value like the common mode voltage. 'LVPE502x detects an electrical idle state when RX± voltage at the device pin falls below VRX_LFPS_DIFFp-p min. After detection of an idle state in a given channel the device asserts electrical idle state in its corresponding TX. When RX± voltage exceeds VRX_LFPS_DIFFp-p max normal operation is restored and output start passing input signal. Electrical idle exit and entry time is speccified at < 6ns.

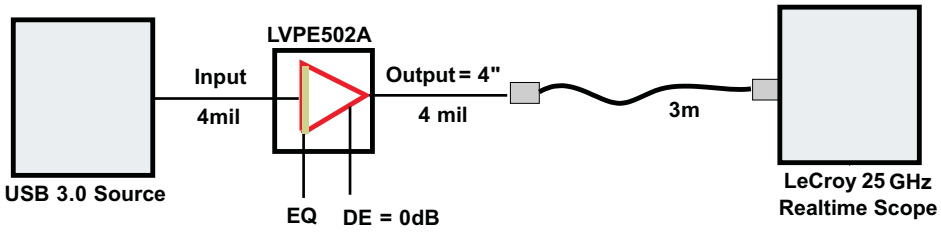
TYPICAL EYE DIAGRAM AND PERFORMANCE CURVES

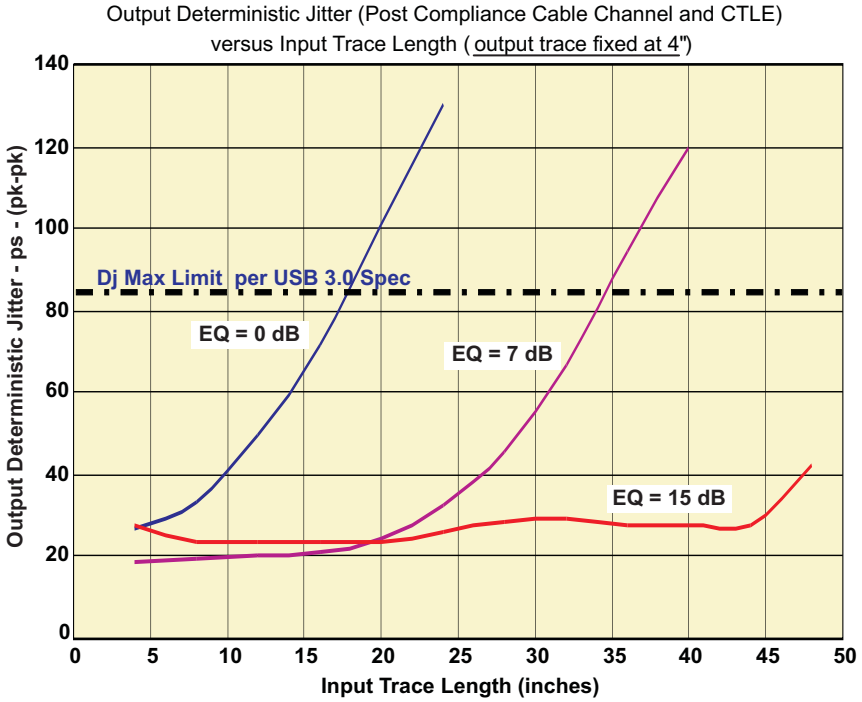
Measurement equipment details:

- Generator (source) LeCroy PERT3,
- Signal: 5Gbps, 1000mVp-p, 3.5 dB De-Emphasis
- Tj and Dj measurements based on CP0 (USB 3 compliance pattern) which is D0.0 or logical idle with SKP sequences removed
- Rj measurements based on CP1 or D10.2 symbol containing alternating 0s and 1s at Nyquist frequency
- Oscilloscope (Sink) LeCroy 25GHz Real Time Oscilloscope
- LeCroy QualiPHY software used to measure jitter and collect compliance eye diagrams

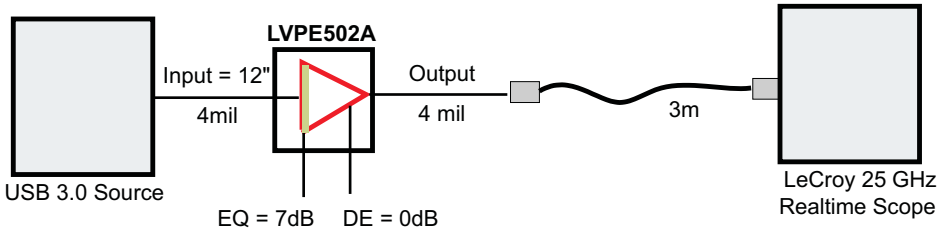
Device Operating Conditions: VCC = 3.3 V, Temp = 25°C, EQx/DEx/OSx set to their default value when not mentioned

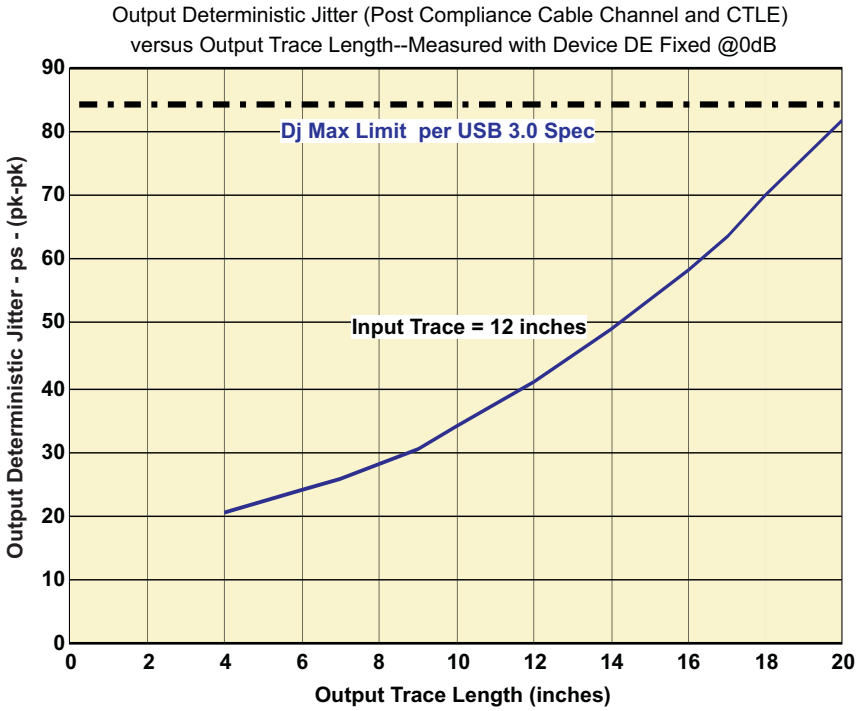
PLOT #1 FIXED OUTPUT TRACE +3m USB 3 CABLE WITH VARIABLE INPUT TRACE



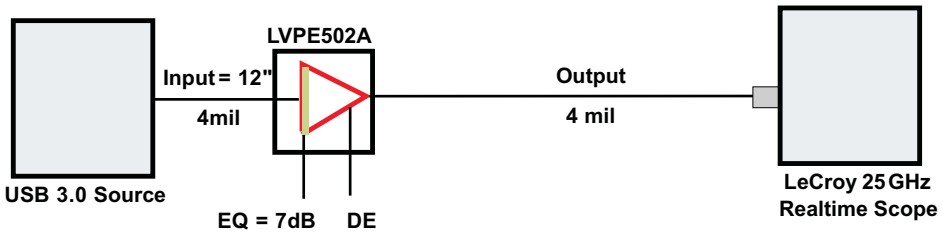


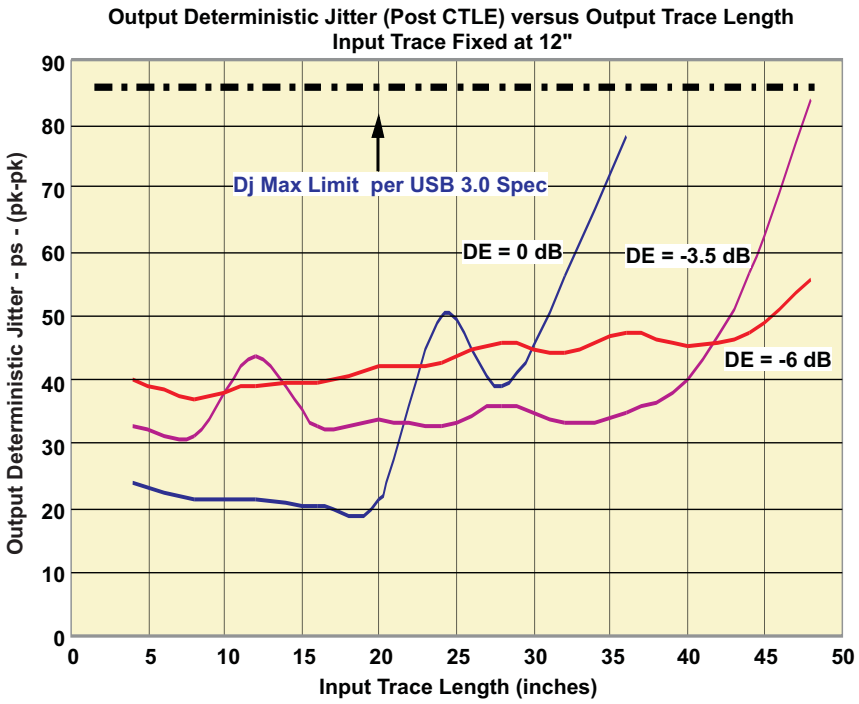
PLOT #2 FIXED INPUT TRACE WITH VARIABLE OUTPUT TRACE and +3m USB 3.0 CABLE





PLOT #3 FIXED INPUT TRACE WITH VARIABLE OUTPUT TRACE and (No Cable)

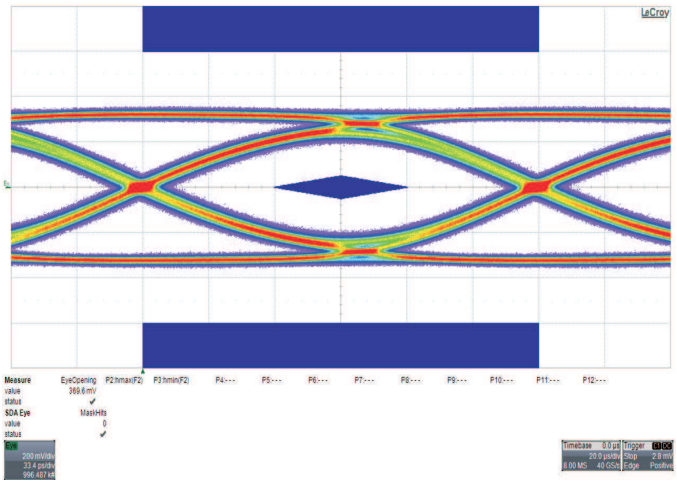




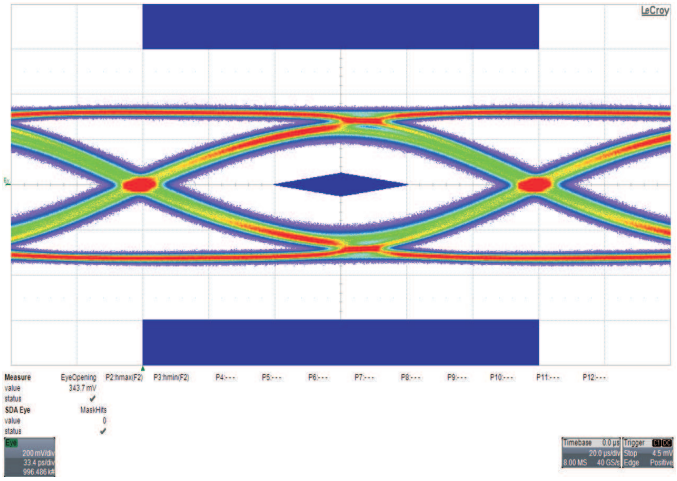
USB 3.0 MASK EYE DIAGRAM TEST

CASE I FIXED OUTPUT AND VARIABLE INPUT TRACE

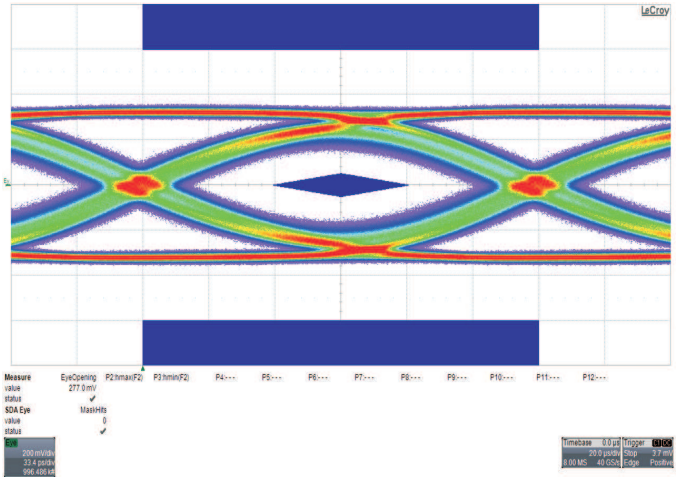
DE= 0dB, EQ = 0dB, Input = 4", Output = 4" + 3m Cable



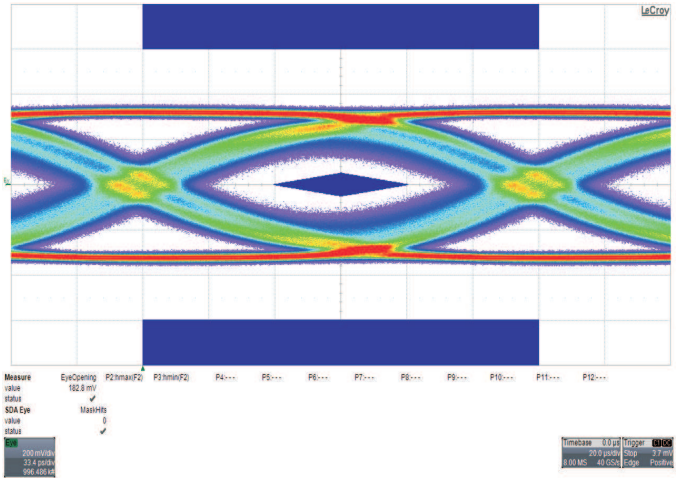
DE= 0dB, EQ = 0dB, Input = 8”, Output = 4” + 3m Cable



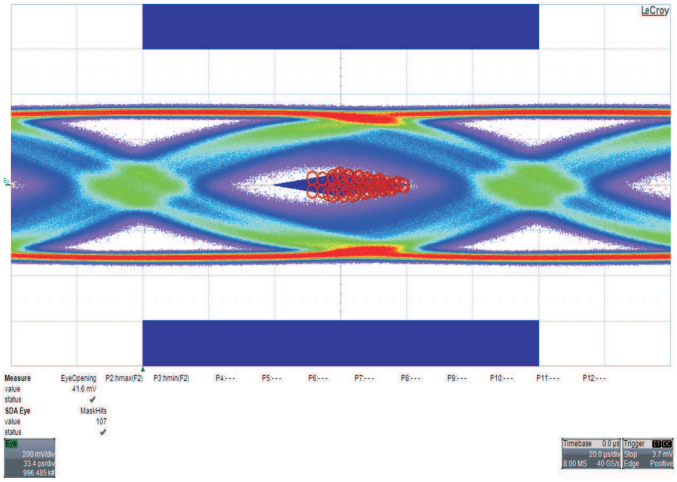
DE= 0dB, EQ = 0dB, Input = 12”, Output = 4” + 3m Cable



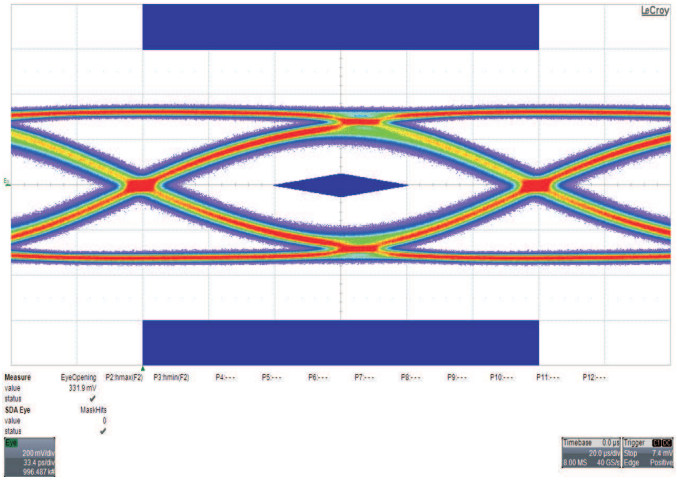
DE= 0dB, EQ = 0dB, Input = 16”, Output = 4” + 3m Cable



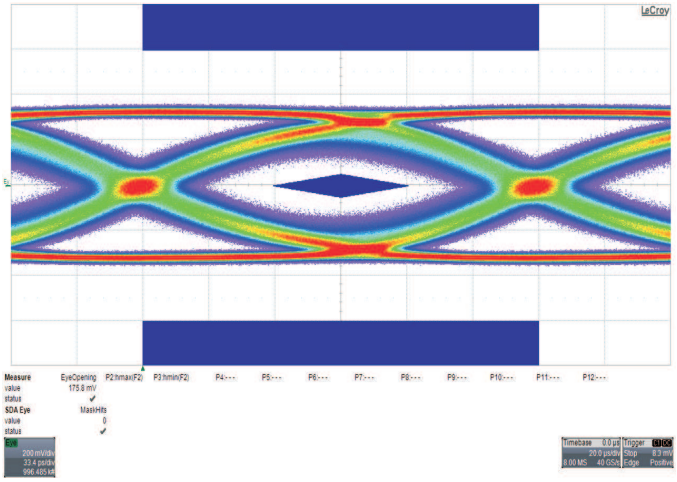
DE= 0dB, EQ = 0dB, Input = 20”, Output = 4” + 3m Cable



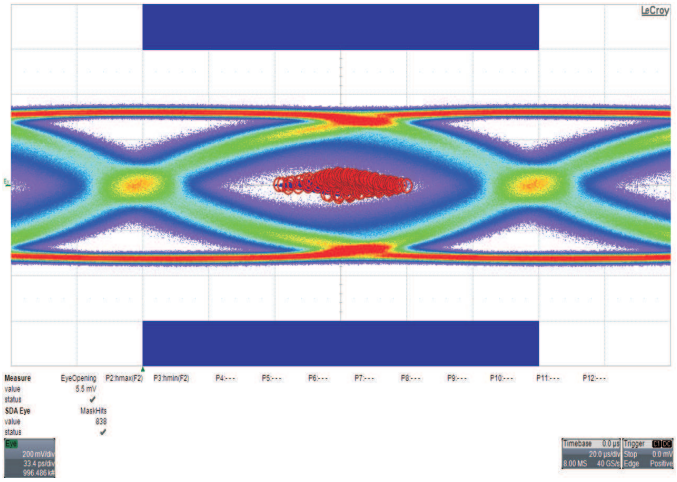
DE= 0dB, EQ = 7dB, Input = 24”, Output = 4” + 3m Cable



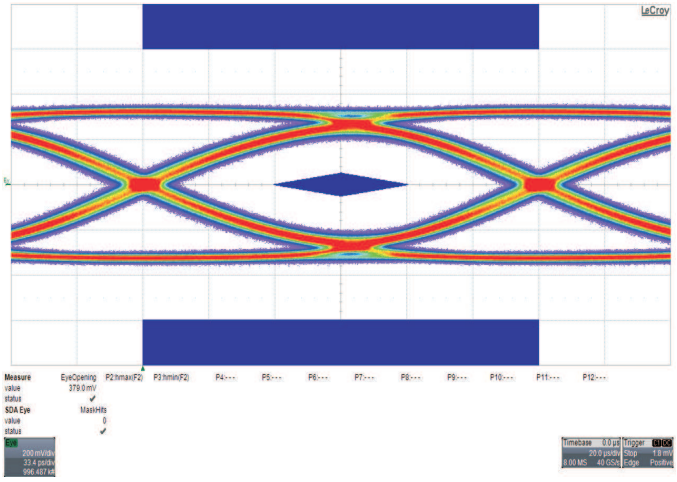
DE= 0dB, EQ = 7dB, Input = 32”, Output = 4” + 3m Cable



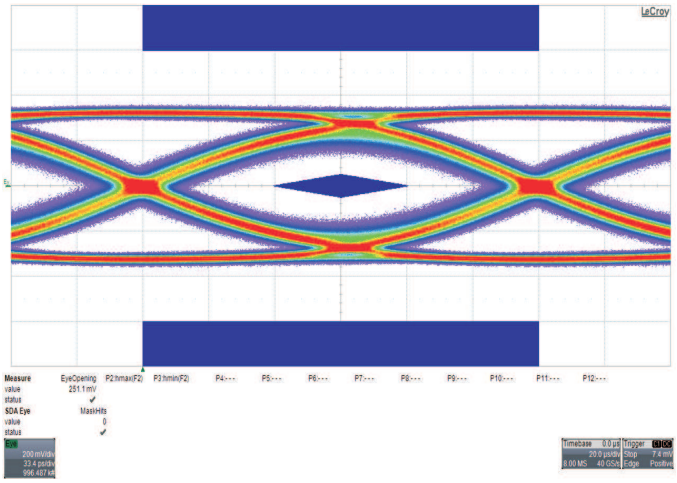
DE= 0dB, EQ = 7dB, Input = 36”, Output = 4” + 3m Cable



DE= 0dB, EQ = 15dB, Input = 36”, Output = 4” + 3m Cable

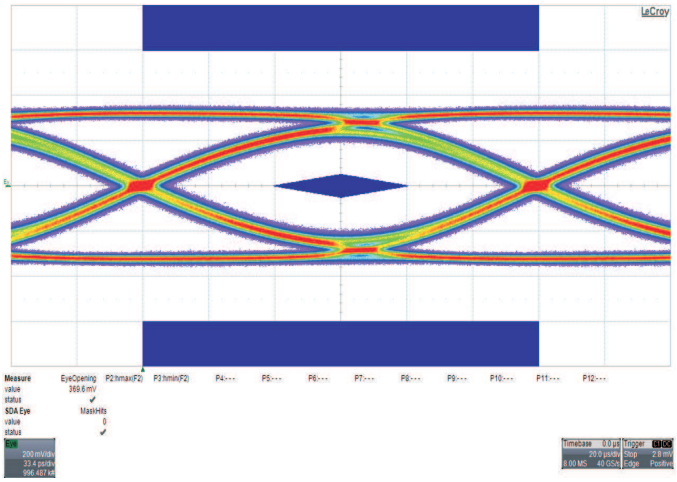


DE= 0dB, EQ = 15dB, Input = 48”, Output = 4” + 3m Cable

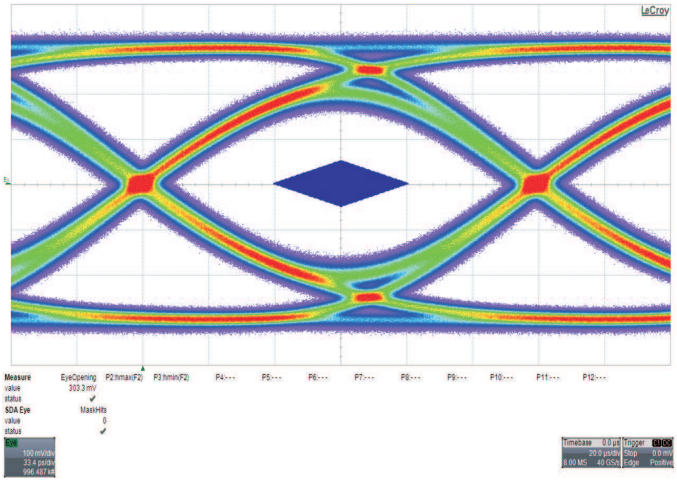


CASE II FIXED INPUT AND VARIABLE OUTPUT TRACE+ 3m CABLE

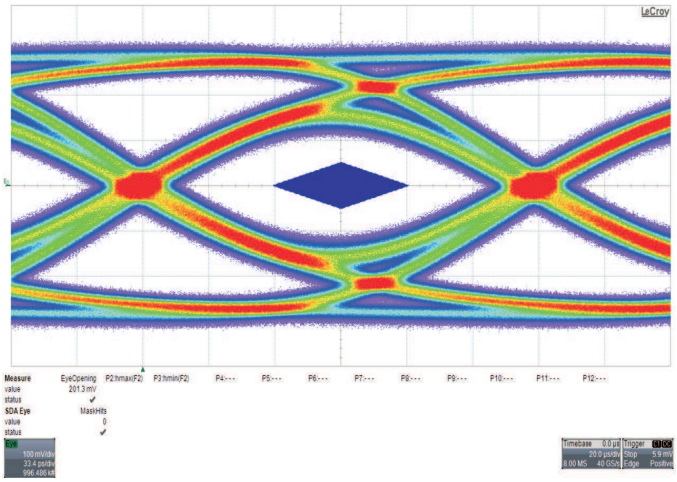
DE= 0dB, EQ = 7dB, Input = 12”, Output = 4” + 3m Cable



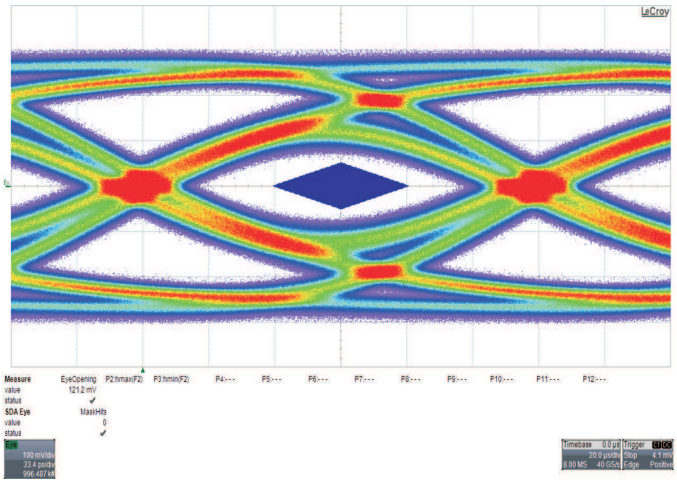
DE= 0dB, EQ = 7dB, Input = 12”, Output = 8” + 3m Cable



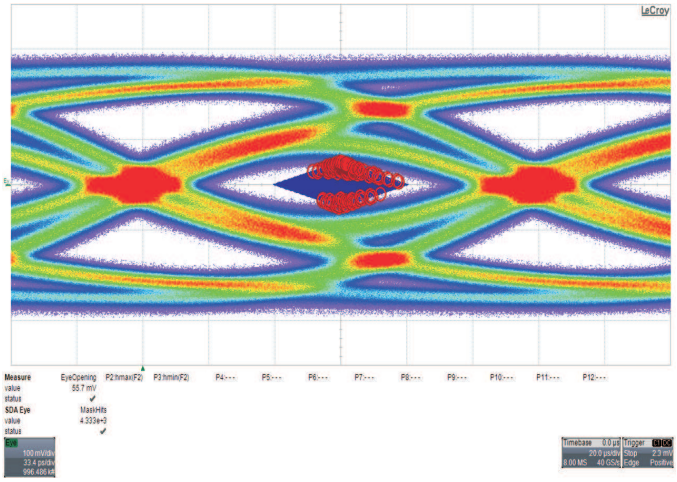
DE= 0dB, EQ = 7dB, Input = 12”, Output = 12” + 3m Cable



DE= 0dB, EQ = 7dB, Input = 12”, Output = 16” + 3m Cable

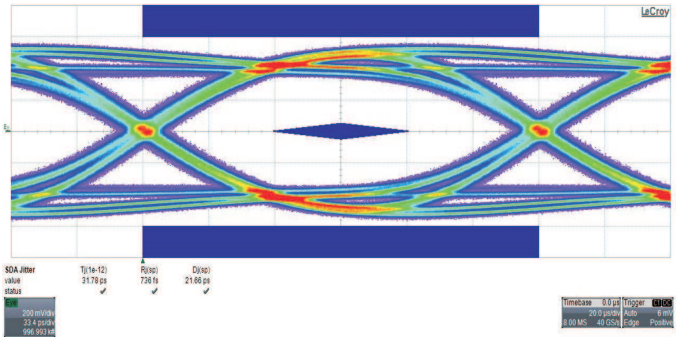


DE= 0dB, EQ = 7dB, Input = 12”, Output = 20” + 3m Cable

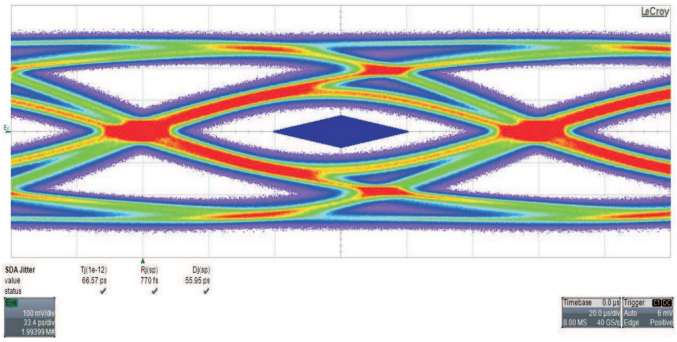


CASE III FIXED INPUT AND VARIABLE OUTPUT TRACE (No Cable)

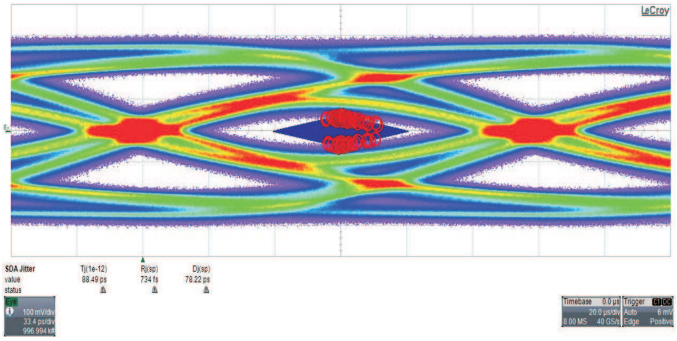
DE= 0dB, EQ = 7dB, Input = 12”, Output = 8”



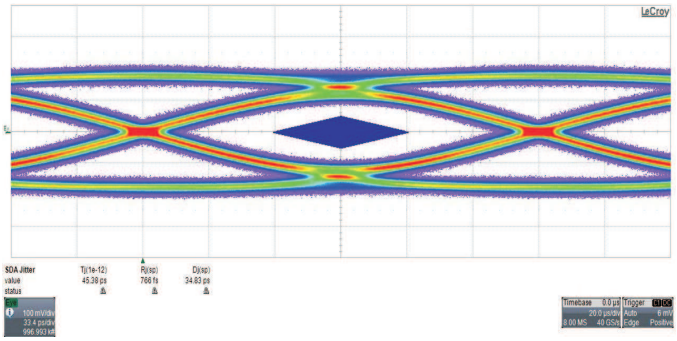
DE= 0dB, EQ = 7dB, Input = 12”, Output = 32”



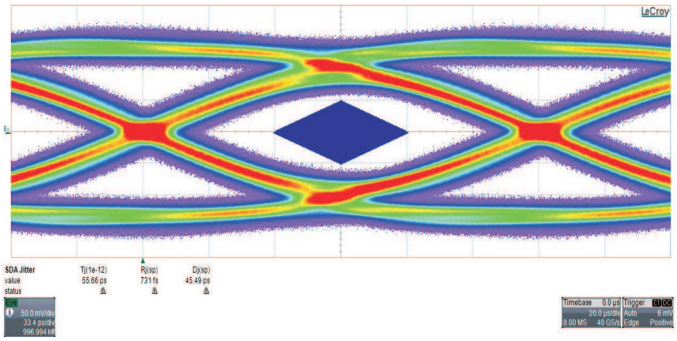
DE= 0dB, EQ = 7dB, Input = 12”, Output = 36”



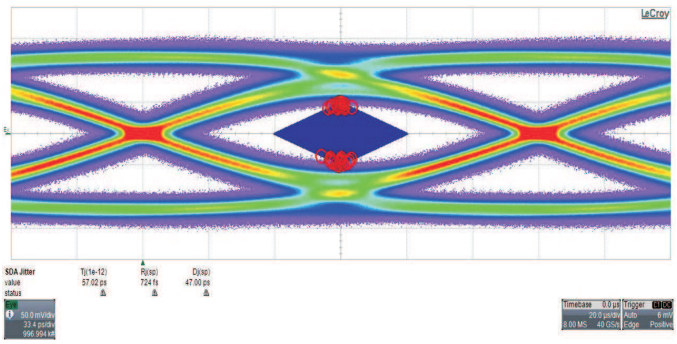
DE= -3.5dB, EQ = 7dB, Input = 12”, Output = 36”



DE= -6.0dB, EQ = 7dB, Input = 12”, Output = 40”



DE= -6.0dB, EQ = 7dB, Input = 12”, Output = 44”



REVISION HISTORY

Changes from Original (March 2012) to Revision A **Page**

- Deleted the Ordering Information Table 2

Changes from Revision A (March 2012) to Revision B **Page**

- Added device SN65LVPE502B 1
- Changed Feature From: Small Foot Print – 24 Pin (4mm x 4mm) QFN Package To: Small Foot Print – 3x3mm and 4x4mm 24-pin QFN Packages 1
- Deleted pinout bottom View 8
- Added pinout package RLL 8
- Added RLL to the Pin Function table 9
- Added Section - Host- and Device-side Pins 11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVPE502ARGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 85	502A	Samples
SN65LVPE502ARLLR	ACTIVE	VQFN	RLL	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 85	SN502A	Samples
SN65LVPE502ARLLT	PREVIEW	VQFN	RLL	24	250	TBD	Call TI	Call TI	0 to 85		
SN65LVPE502BRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		502B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

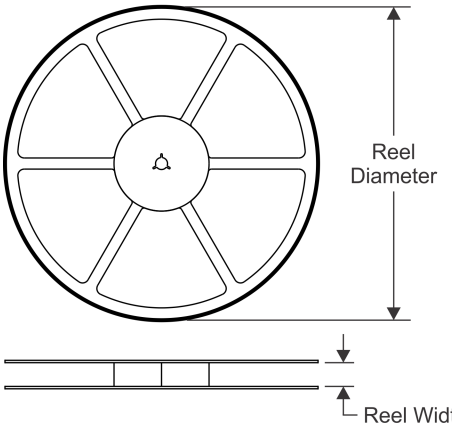
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

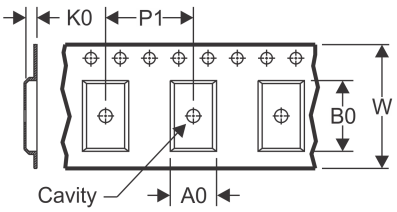
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

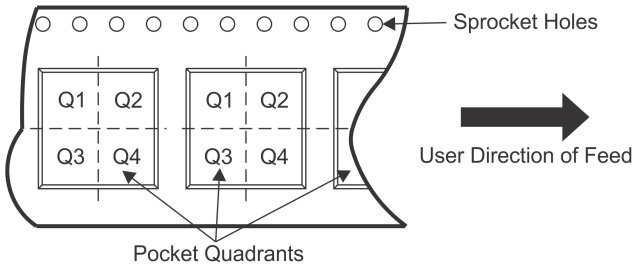


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

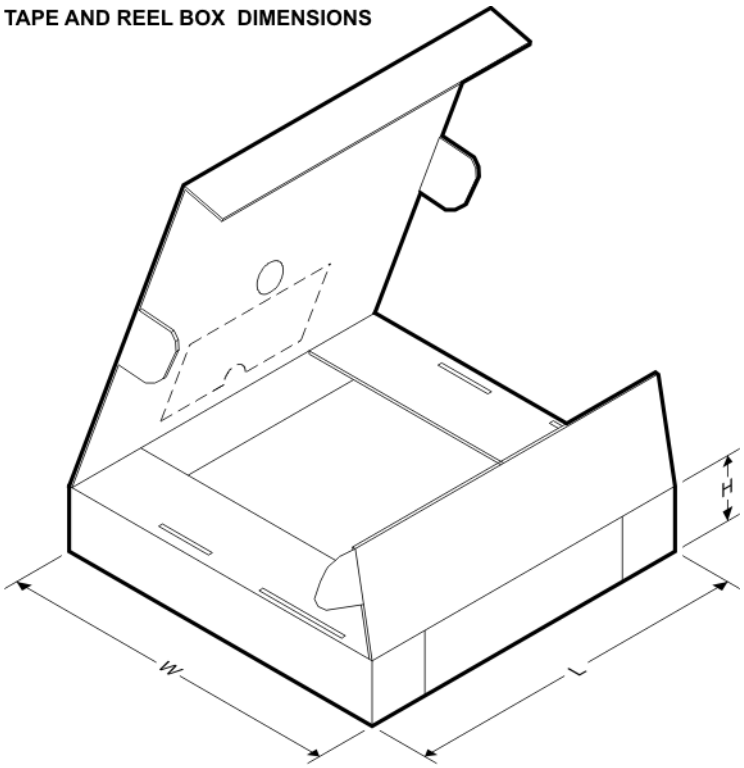
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVPE502ARGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN65LVPE502BRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

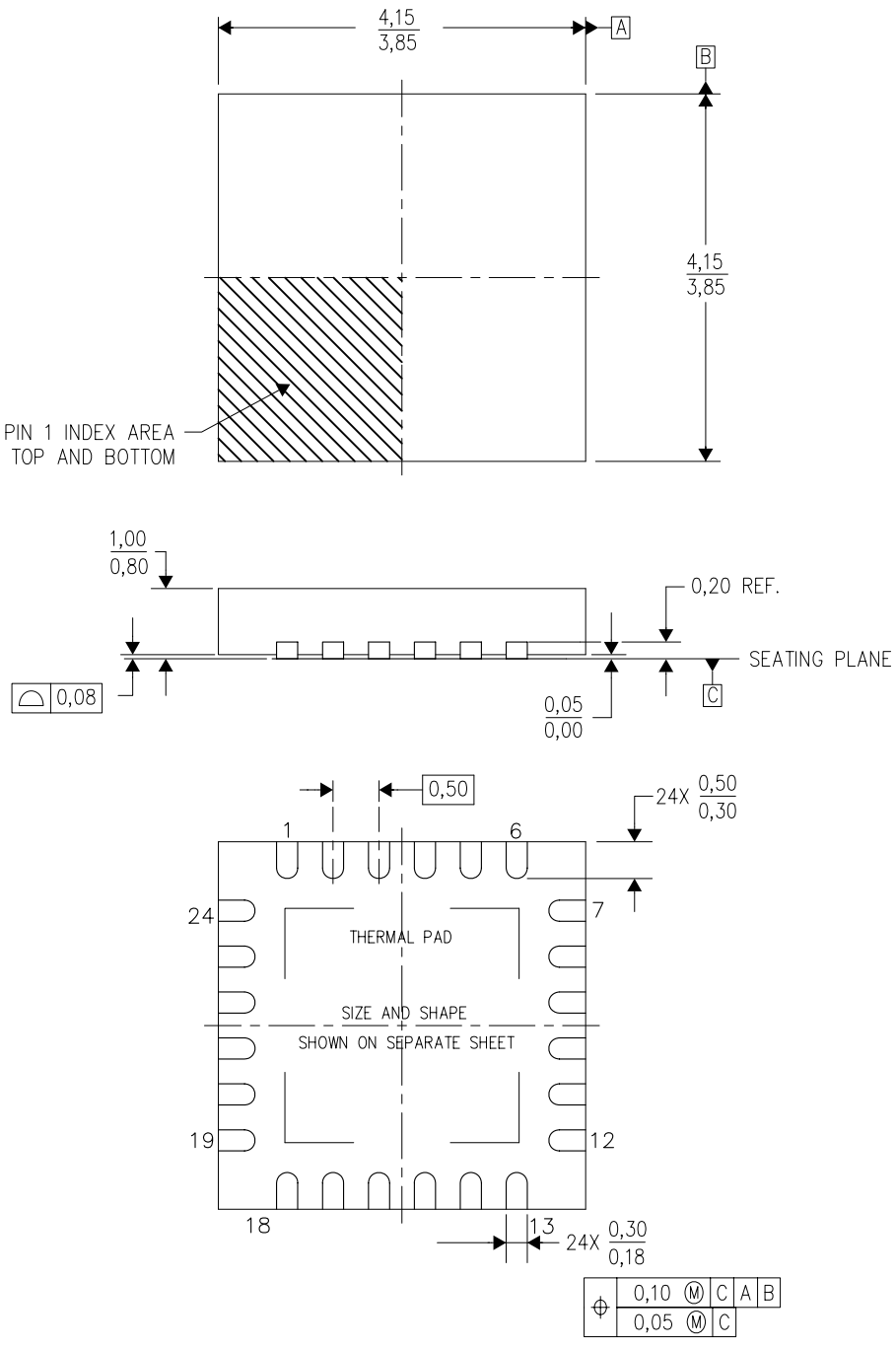
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVPE502ARGER	VQFN	RGE	24	3000	367.0	367.0	35.0
SN65LVPE502BRGER	VQFN	RGE	24	3000	367.0	367.0	35.0

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

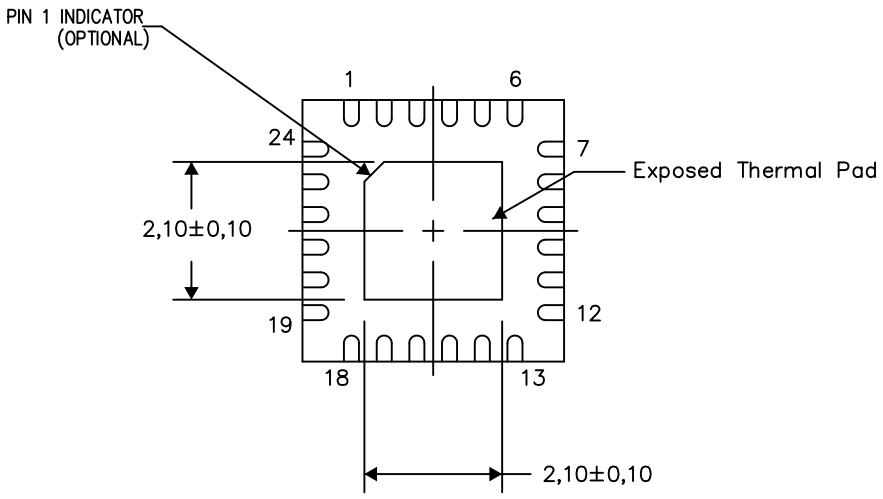
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



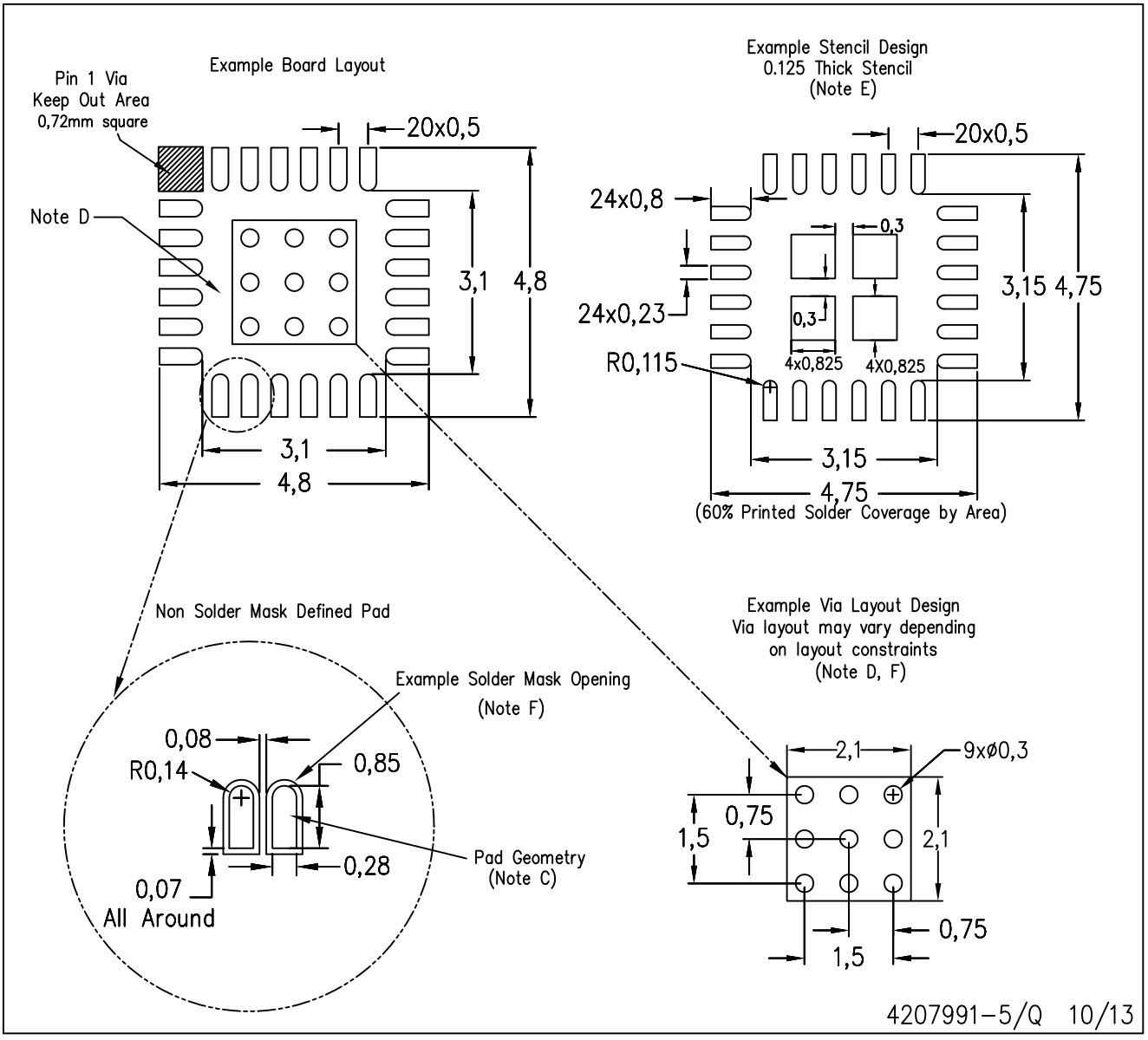
Bottom View

Exposed Thermal Pad Dimensions

4206344–6/AE 10/13

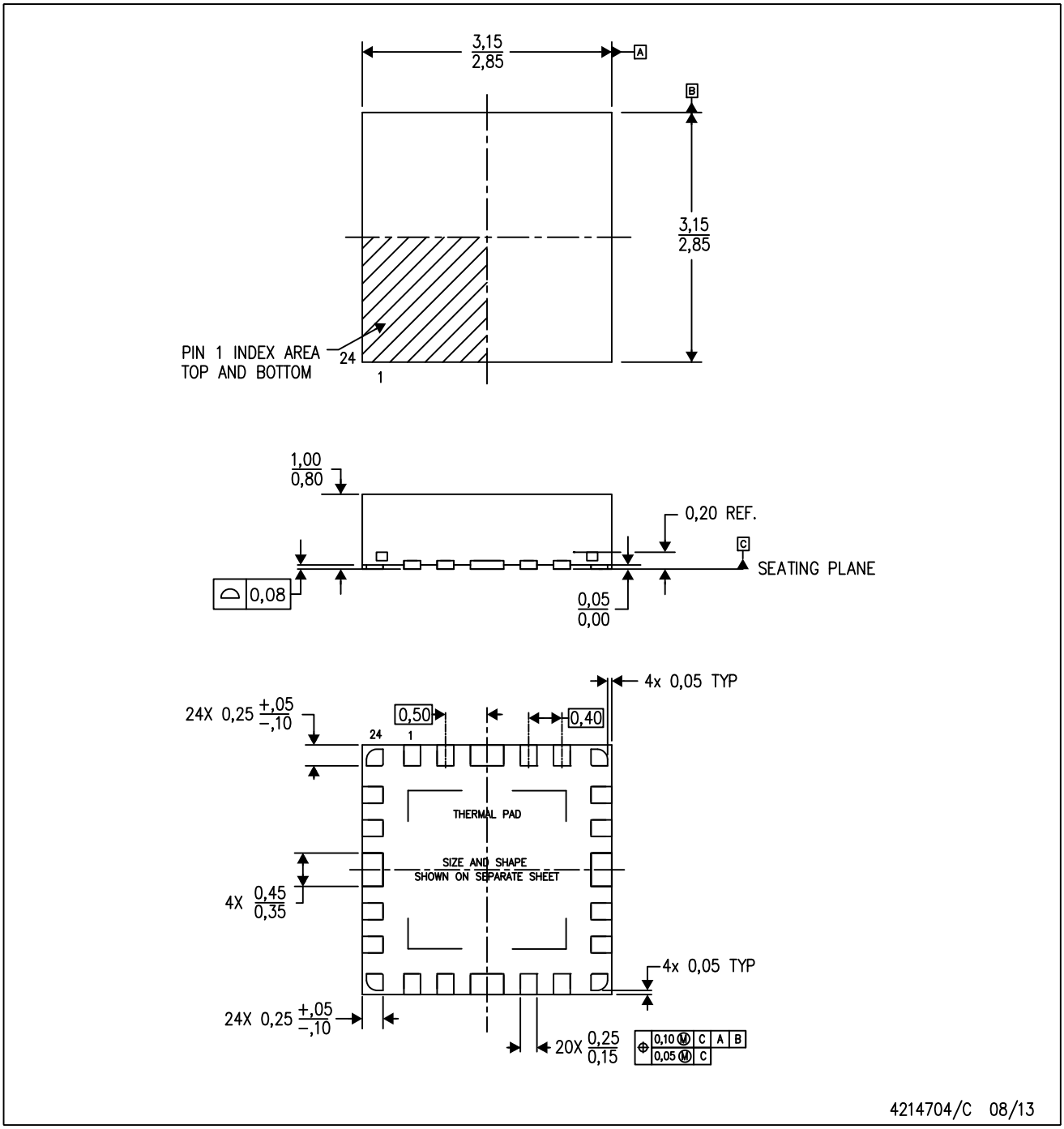
NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

RLL (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

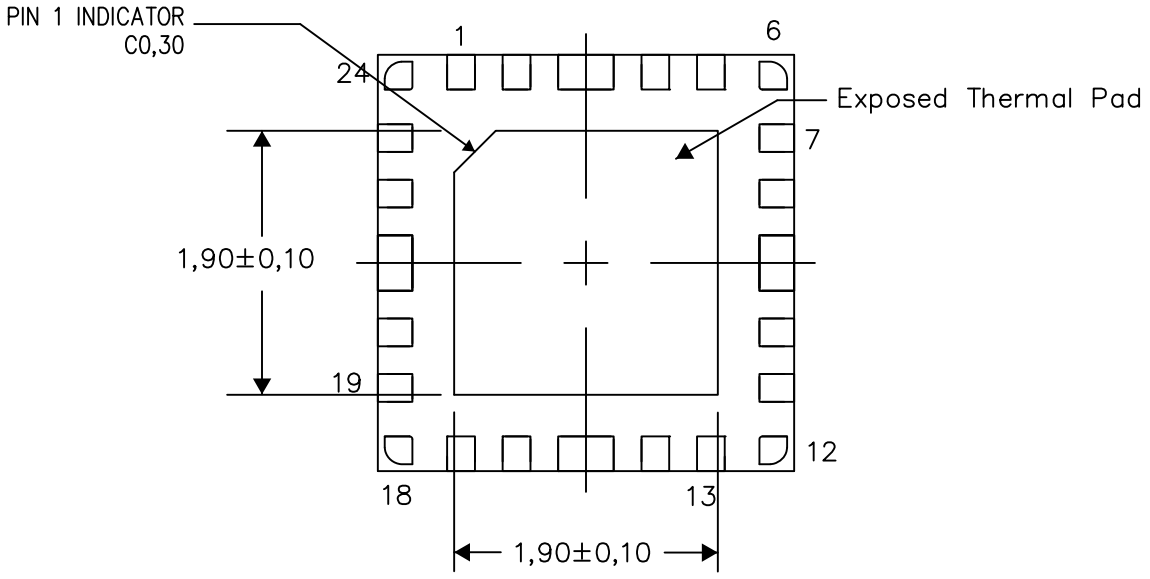
RLL (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4214706/D 08/13

NOTE: All linear dimensions are in millimeters

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