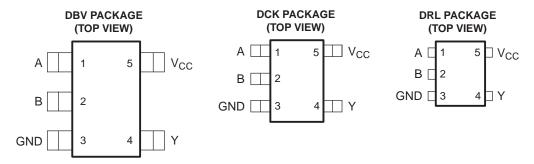
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FEATURES

- Controlled Baseline
 - One Assembly Site
 - One Test Site
 - One Fabrication Site
- Extended Temperature Performance of -55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree (1)
- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- . Operating Range of 2 V to 5.5 V
- Max t_{pd} of 8.5 ns at 5 V
- Low Power Consumption, 10 μA Max I_{CC}
- ±8 mA Output Drive at 5 V
- Schmitt Trigger Action at All Inputs Makes the Circuit Tolerant for Slower Input Rise and Fall Time
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This device contains a single 2-input NOR gate that performs the Boolean function $Y = \overline{A} \bullet \overline{B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

ORDERING INFORMATION(1)

T _A	PACKAG	E ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOT (SC-70) - DCK	Reel of 3000	SN74AHC1G02MDCKREP	CGC

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



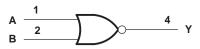
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FUNCTION TABLE

IN	PUTS	OUTPUT
Α	В	Υ
Н	Х	L
Х	Н	L
L	L	Н

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
V_{I}	Input voltage range ⁽²⁾		-0.5	7	V
V_{O}	Output voltage range (2)		-0.5	V _{CC} + 0.5	V
I_{IK}	Input clamp current	V ₁ < 0		-20	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O = 0$ to V_{CC}		±20	mA
IO	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V _{CC} or GND	V _{CC} or GND		±50	mA
θ_{JA}	Package thermal impedance (3)	DCK package		252	°C/W
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed. The package thermal impedance is calculated in accordance with JESD 51-7.

SN74AHC1G02-EP SINGLE 2-INPUT POSITIVE-NOR GATE

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Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2	5.5	V
		V _{CC} = 2 V	1.5		
V_{IH}	High-level input voltage	V _{CC} = 3 V	2.1		V
		V _{CC} = 5.5 V	3.85		
		V _{CC} = 2 V		0.5	
V_{IL}	Low-level input voltage	V _{CC} = 3 V		0.9	V
		V _{CC} = 5.5 V		1.65	
VI	Input voltage		0	5.5	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 2 V		-50	μΑ
I _{OH}	High-Level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3$		-4	A
		$V_{CC} = 5 \text{ V} \pm 0.5$		-8	mA
		V _{CC} = 2 V		50	μΑ
I _{OL}	Low-Level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3$		4	A
		$V_{CC} = 5 V \pm 0.5$		8	mA
A+/A.,	land transition via a set fall vata	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		100	20/1
Δt/Δv	Input transition rise or fall rate	$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		20	ns/V
T _A	Operating free-air temperature		-55	125	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V	TA	= 25°C		$T_A = -55^{\circ}C TC$	O 125°C	UNIT
PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP	MAX	MIN	MAX	UNII
		2 V	1.9	2		1.9		
	$I_{OH} = -50 \mu A$	3 V	2.9	3		2.9		
V _{OH}		4.5 V	4.4	4.5		4.4		V
	$I_{OH} = -4 \text{ mA}$	3 V	2.58			2.48		
	$I_{OH} = -8 \text{ mA}$	4.5 V	3.94			3.8		
		2 V			0.1		0.1	
	$I_{OL} = 50 \mu A$	3 V			0.1		0.1	
V _{OL}		4.5 V			0.1		0.1	V
	$I_{OL} = 4 \text{ mA}$	3 V			0.36		0.44	
	$I_{OL} = 8 \text{ mA}$	4.5 V			0.36		0.44	
l _l	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	μΑ
I _{cc}	$V_I = V_{CC}$ or GND, $O = 0$	5.5 V			1		10	μΑ
C _i	$V_I = V_{CC}$ or GND	5 V		4	10		10	pF

Switching Characteristics

over operating free-air temperature range, $V_{CC} = 3.3 \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T,	չ = 25°C		T _A = -55°C T	O 125°C	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	UNII
t _{PLH}	A or P	V	C _ 50 pE		8.1	11.4	1	13	20
t _{PHL}	A or B	r	$C_L = 50 \text{ pF}$		8.1	11.4	1	13	ns

Switching Characteristics

over operating free-air temperature range, $V_{CC} = 5 \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T,	λ = 25°C		T _A = -55°C	ΓΟ 125°C	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	UNII
t _{PLH}	A or D	V	C		5.1	7.5	1	8.5	20
t _{PHL}	A or B	r	$C_L = 50 \text{ pF}$		5.1	7.5	1	8.5	ns

Operating Characteristics

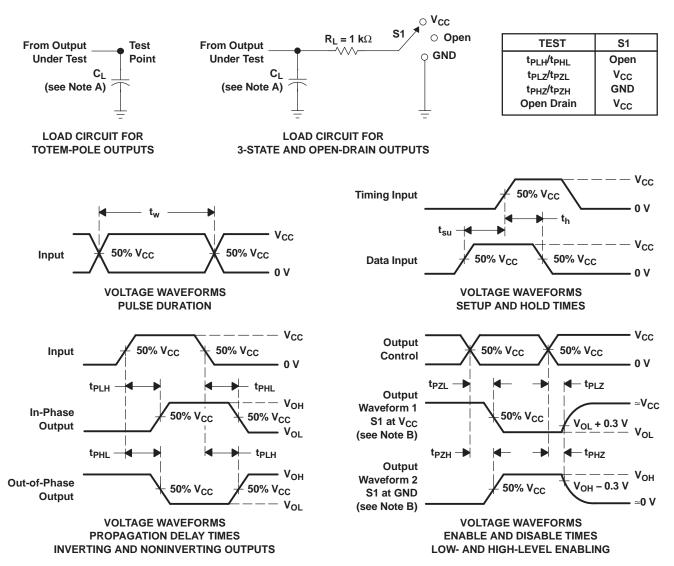
 V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	15	pF





PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 3 ns. $t_f \leq$ 3 ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

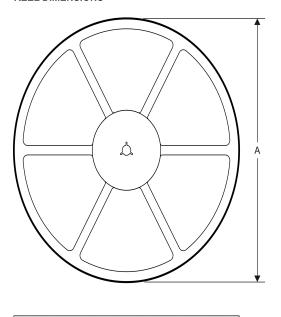
Figure 1. Load Circuit and Voltage Waveforms

PACKAGE MATERIALS INFORMATION

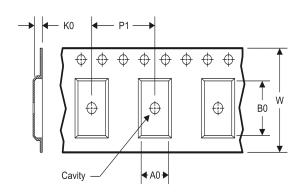
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC1G02MDCKRE P	SC70	DCK	5	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC1G02MDCKREP	SC70	DCK	5	3000	202.0	201.0	28.0

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



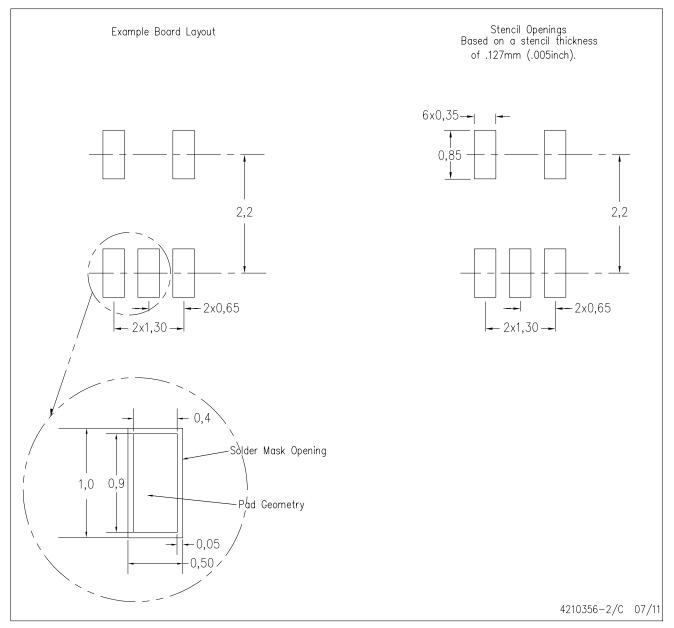
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.



DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



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