

16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

Check for Samples: [SN74AUCH16374](#)

FEATURES

- Member of the Texas Instruments Widebus™ Family
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max t_{pd} of 2.8 ns at 1.8 V
- Low Power Consumption, 20 μ A Max I_{CC}
- ± 8 -mA Output Drive at 1.8 V
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION/ORDERING INFORMATION

This 16-bit edge-triggered D-type flip-flop is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

DGG OR DGV PACKAGE
(TOP VIEW)

1OE	1	48	1CLK
1Q1	2	47	1D1
1Q2	3	46	1D2
GND	4	45	GND
1Q3	5	44	1D3
1Q4	6	43	1D4
V_{CC}	7	42	V_{CC}
1Q5	8	41	1D5
1Q6	9	40	1D6
GND	10	39	GND
1Q7	11	38	1D7
1Q8	12	37	1D8
2Q1	13	36	2D1
2Q2	14	35	2D2
GND	15	34	GND
2Q3	16	33	2D3
2Q4	17	32	2D4
V_{CC}	18	31	V_{CC}
2Q5	19	30	2D5
2Q6	20	29	2D6
GND	21	28	GND
2Q7	22	27	2D7
2Q8	23	26	2D8
2OE	24	25	2CLK

The SN74AUCH16374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.



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ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74AUCH16374DGGR	AUCH16374
	TVSOP – DGV	Tape and reel	SN74AUCH16374DGVR	MJ374
	VFBGA – GQL	Tape and reel	SN74AUCH16374GQLR	MJ374
	VFBGA – ZQL	Tape and reel	SN74AUCH16374ZQLR	MJ374

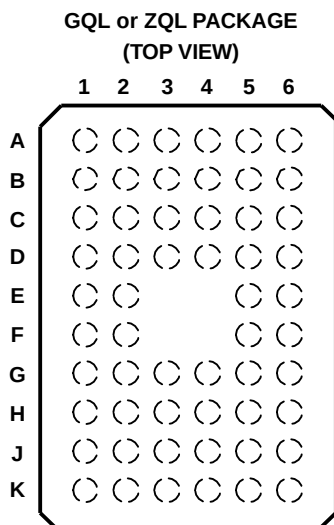
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

DESCRIPTION/ORDERING INFORMATION(CONTINUED)

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.


TERMINAL ASSIGNMENTS⁽¹⁾

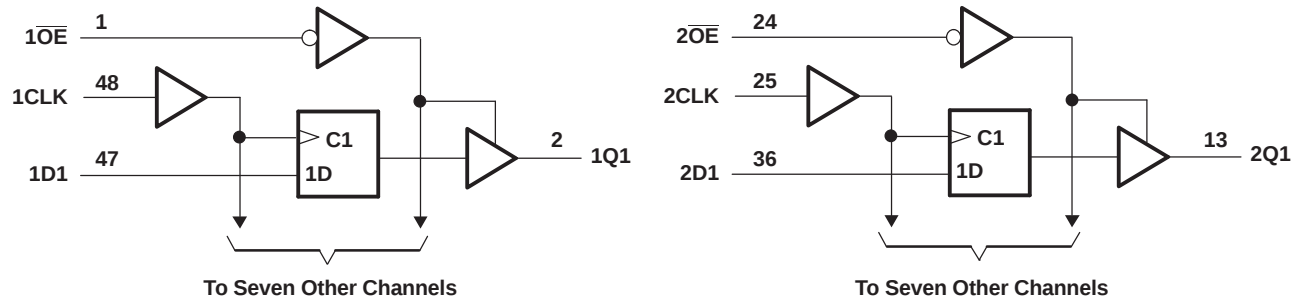
	1	2	3	4	5	6
A	1 $\overline{OE}$	NC	NC	NC	NC	1CLK
B	1Q2	1Q1	GND	GND	1D1	1D2
C	1Q4	1Q3	V _{CC}	V _{CC}	1D3	1D4
D	1Q6	1Q5	GND	GND	1D5	1D6
E	1Q8	1Q7			1D7	1D8
F	2Q1	2Q2			2D2	2D1
G	2Q3	2Q4	GND	GND	2D4	2D3
H	2Q5	2Q6	V _{CC}	V _{CC}	2D6	2D5
J	2Q7	2Q8	GND	GND	2D8	2D7
K	2 $\overline{OE}$	NC	NC	NC	NC	2CLK

(1) NC - No internal connection

**FUNCTION TABLE
(EACH FLIP-FLOP)**

INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	↑	H	H
L	↑	L	L
L	H or L	X	Q ₀
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG and DGV packages.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	−0.5	3.6	V
V _I	Input voltage range ⁽²⁾	−0.5	3.6	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	−0.5	3.6	V
V _O	Output voltage range ⁽²⁾	−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	−50	mA
I _{OK}	Output clamp current	V _O < 0	−50	mA
I _O	Continuous output current		±20	mA
Continuous current through each V _{CC} or GND			±100	mA
θ _{JA}	Package thermal impedance ⁽³⁾	DGG package	70	°C/W
		DGV package	58	
		ZQL/GQL package	42	
T _{stg}	Storage temperature range	−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

Recommended operating conditions			MIN	MAX	UNIT
V _{CC}	Supply voltage		0.8	2.7	V
V _{IH}	High-level input voltage	V _{CC} = 0.8 V	V _{CC}		V
		V _{CC} = 1.1 V to 1.95 V	0.65 × V _{CC}		
		V _{CC} = 2.3 V to 2.7 V	1.7		
V _{IL}	Low-level input voltage	V _{CC} = 0.8 V	0		V
		V _{CC} = 1.1 V to 1.95 V	0.35 × V _{CC}		
		V _{CC} = 2.3 V to 2.7 V	0.7		
V _I	Input voltage		0	3.6	V
V _O	Output voltage	Active state	0	V _{CC}	V
		3-state	0	3.6	V
I _{OH}	High-level output current	V _{CC} = 0.8 V	−0.7		mA
		V _{CC} = 1.1 V	−3		
		V _{CC} = 1.4 V	−5		
		V _{CC} = 1.65 V	−8		
		V _{CC} = 2.3 V	−9		
I _{OL}	Low-level output current	V _{CC} = 0.8 V	0.7		mA
		V _{CC} = 1.1 V	3		
		V _{CC} = 1.4 V	5		
		V _{CC} = 1.65 V	8		
		V _{CC} = 2.3 V	9		
Δt/Δv	Input transition rise or fall rate			20	ns/V
T _A	Operating free-air temperature		−40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{OH}		$I_{OH} = -100\ \mu A$	0.8 V to 2.7 V	$V_{CC} - 0.1$			V
		$I_{OH} = -0.7\ mA$	0.8 V	0.55			
		$I_{OH} = -3\ mA$	1.1 V	0.8			
		$I_{OH} = -5\ mA$	1.4 V	1			
		$I_{OH} = -8\ mA$	1.65 V	1.2			
		$I_{OH} = -9\ mA$	2.3 V	1.8			
V_{OL}		$I_{OL} = 100\ \mu A$	0.8 V to 2.7 V	0.2			V
		$I_{OL} = 0.7\ mA$	0.8 V	0.25			
		$I_{OL} = 3\ mA$	1.1 V	0.3			
		$I_{OL} = 5\ mA$	1.4 V	0.4			
		$I_{OL} = 8\ mA$	1.65 V	0.45			
		$I_{OL} = 9\ mA$	2.3 V	0.6			
I_I	All inputs	$V_I = V_{CC}$ or GND	0 to 2.7 V			± 5	μA
I_{BHL} ⁽²⁾		$V_I = 0.35\ V$	1.1 V	10			μA
		$V_I = 0.47\ V$	1.4 V	15			
		$V_I = 0.57\ V$	1.65 V	20			
		$V_I = 0.7\ V$	2.3 V	40			
I_{BHH} ⁽³⁾		$V_I = 0.8\ V$	1.1 V	-5			μA
		$V_I = 0.9\ V$	1.4 V	-15			
		$V_I = 1.07\ V$	1.65 V	-20			
		$V_I = 1.7\ V$	2.3 V	-40			
I_{BHLO} ⁽⁴⁾	$V_I = 0$ to V_{CC}		1.3 V	75			μA
			1.6 V	125			
			1.95 V	175			
			2.7 V	275			
I_{BHHO} ⁽⁵⁾	$V_I = 0$ to V_{CC}		1.3 V	-75			μA
			1.6 V	-125			
			1.95 V	-175			
			2.7 V	-275			
I_{off}		V_I or $V_O = 2.7\ V$	0			± 10	μA
I_{OZ}		$V_O = V_{CC}$ or GND	2.7 V			± 10	μA
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	0.8 V to 2.7 V			20	μA
C_i		$V_I = V_{CC}$ or GND	2.5 V		3		pF
C_o		$V_O = V_{CC}$ or GND	2.5 V		5		pF

(1) All typical values are at $T_A = 25^\circ C$.

(2) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

(3) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

(4) An external driver must source at least I_{BHLO} to switch this node from low to high.

(5) An external driver must sink at least I_{BHHO} to switch this node from high to low.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

		V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V		V _{CC} = 1.5 V ± 0.1 V		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		UNIT
		TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	85	250		250		250		250		MHz
t _w	Pulse duration, CLK high or low	5.9	1.9		1.9		1.9		1.9		ns
t _{su}	Setup time, data before CLK↑	1.4	1.2		0.7		0.6		0.6		ns
t _h	Hold time, data after CLK↑	0.1	0.4		0.4		0.4		0.4		ns

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V		V _{CC} = 1.5 V ± 0.1 V		V _{CC} = 1.8 V ± 0.15 V			V _{CC} = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
f _{max}			85	250		250		250			250		MHz
t _{pd}	CLK	Q	7.3	1	4.5	0.8	2.9	0.7	1.5	2.8	0.7	2.2	ns
t _{en}	$\overline{OE}$	Q	7	1.2	5.3	0.8	3.6	0.8	1.5	2.9	0.7	2.2	ns
t _{dis}	$\overline{OE}$	Q	8.2	2	7.1	1	4.8	1.4	2.7	4.5	0.5	2.2	ns

Operating Characteristics⁽¹⁾

T_A = 25°C

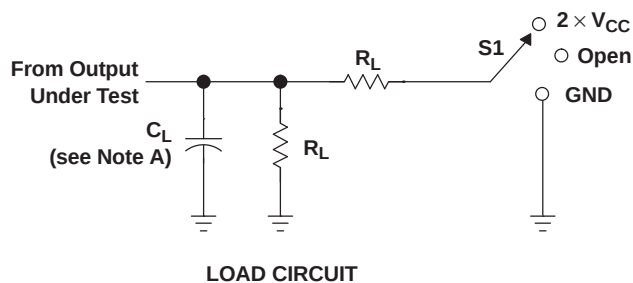
PARAMETER			TEST CONDITIONS	V _{CC} = 0.8 V	V _{CC} = 1.2 V	V _{CC} = 1.5 V	V _{CC} = 1.8 V	V _{CC} = 2.5 V	UNIT
				TYP	TYP	TYP	TYP	TYP	
C _{pd} ⁽²⁾ (each output)	Power dissipation capacitance	Outputs enabled, 1 output switching	1 f _{data} = 5 MHz, 1 f _{clk} = 10 MHz, 1 f _{out} = 5 MHz, $\overline{OE}$ = GND, C _L = 0 pF	24	24	24.1	26.2	31.2	pF
C _{pd} ⁽²⁾ (Z)	Power dissipation capacitance	Outputs disabled, 1 clock and 1 data switching	1 f _{data} = 5 MHz, 1 f _{clk} = 10 MHz, f _{out} = not switching, $\overline{OE}$ = V _{CC} , C _L = 0 pF	7.5	7.5	8	9.4	13.2	pF
C _{pd} ⁽³⁾ (each clock)	Power dissipation capacitance	Outputs disabled, clock only switching	1 f _{data} = 0 MHz, 1 f _{clk} = 10 MHz, f _{out} = not switching, $\overline{OE}$ = V _{CC} , C _L = 0 pF	13.8	13.8	14	14.7	17.5	pF

(1) Total device C_{pd} for multiple (n) outputs switching and (y) clocks inputs switching = {n * C_{pd} (each output)} + {y * C_{pd} (each clock)}.

(2) C_{pd} (each output) is the C_{pd} for each data bit (input and output circuitry) as it operates at 5 MHz (Note: the clock is operating at 10 MHz in this test, but its I_{CC} component has been subtracted out).

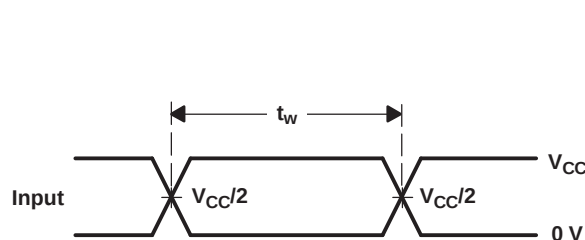
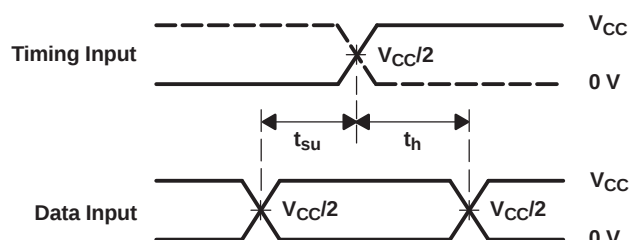
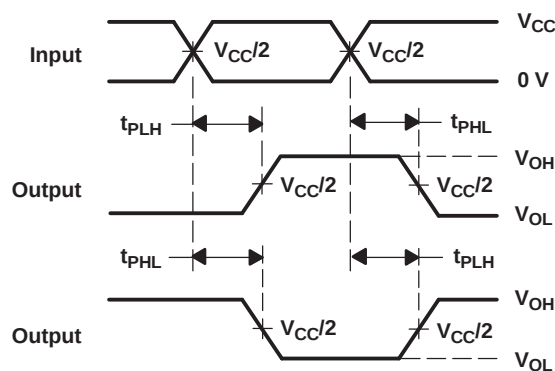
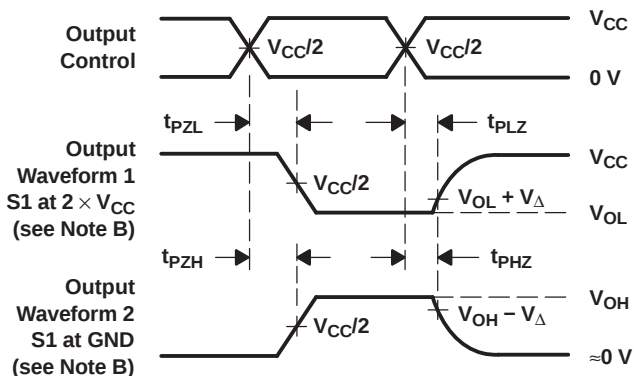
(3) C_{pd} (each clock) is the C_{pd} for the clock circuitry only as it operates at 10 MHz.

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_{Δ}
0.8 V	15 pF	2 k Ω	0.1 V
1.2 V $\pm$ 0.1 V	15 pF	2 k Ω	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	2 k Ω	0.1 V
1.8 V $\pm$ 0.15 V	30 pF	1 k Ω	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 Ω	0.15 V

VOLTAGE WAVEFORMS
PULSE DURATIONVOLTAGE WAVEFORMS
SETUP AND HOLD TIMESVOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTSVOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, $Z_O = 50 \Omega$, slew rate $\geq$ 1 V/ns.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

Changes from Revision D (May 2005) to Revision E**Page**

-
- Added new ZQL package to the datasheet. [2](#)
-

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
74AUCH16374DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74AUCH16374DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74AUCH16374DGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74AUCH16374DGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUCH16374DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUCH16374DGV	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUCH16374GQLR	OBSOLETE	BGA MICROSTAR JUNIOR	GQL	56		TBD	Call TI	Call TI	
SN74AUCH16374ZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUCH16374DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74AUCH16374DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74AUCH16374ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

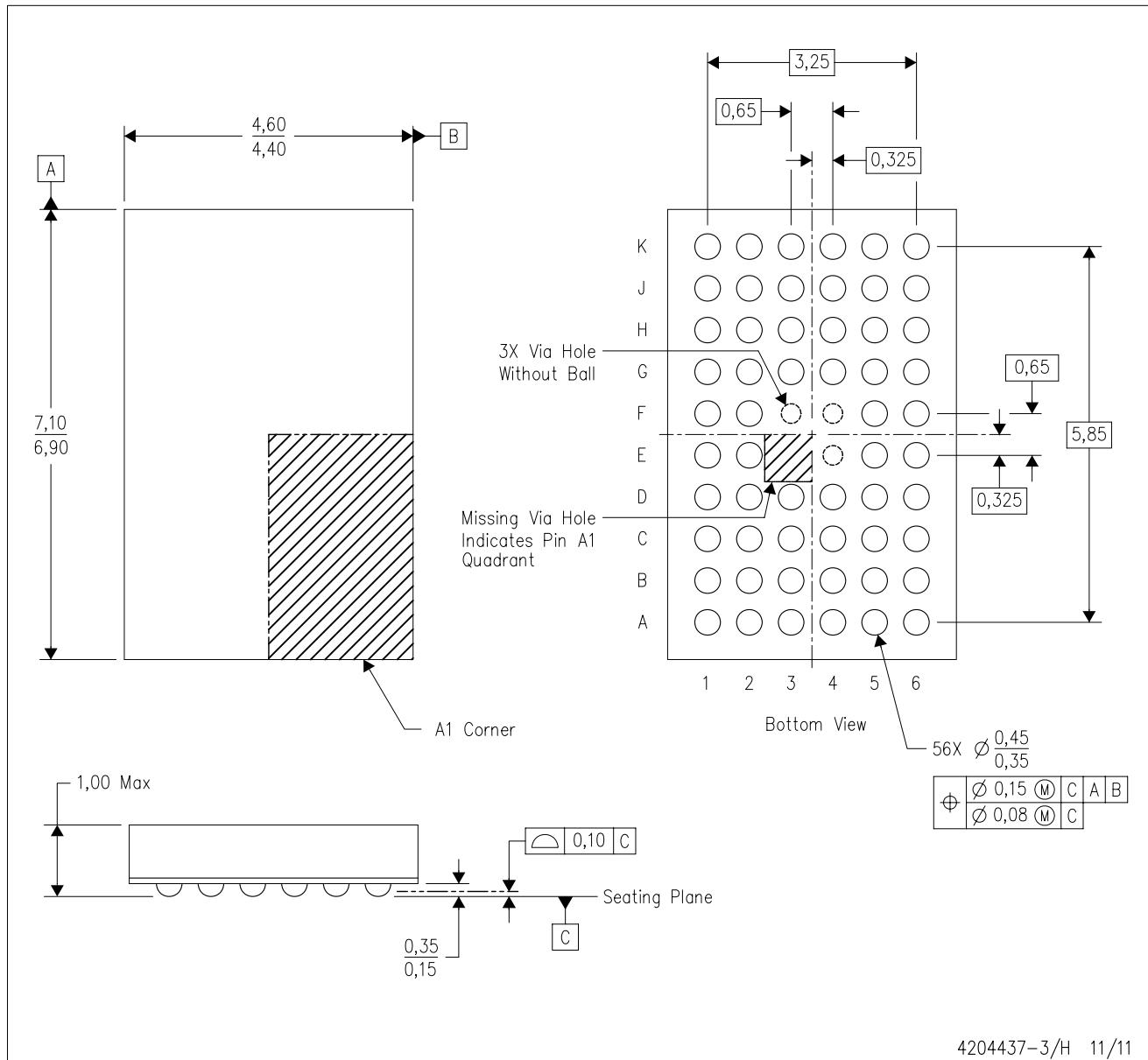


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUCH16374DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74AUCH16374DGVR	TVSOP	DGV	48	2000	367.0	367.0	38.0
SN74AUCH16374ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	333.2	345.9	28.6

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-285 variation BA-2.
 - D. This package is Pb-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

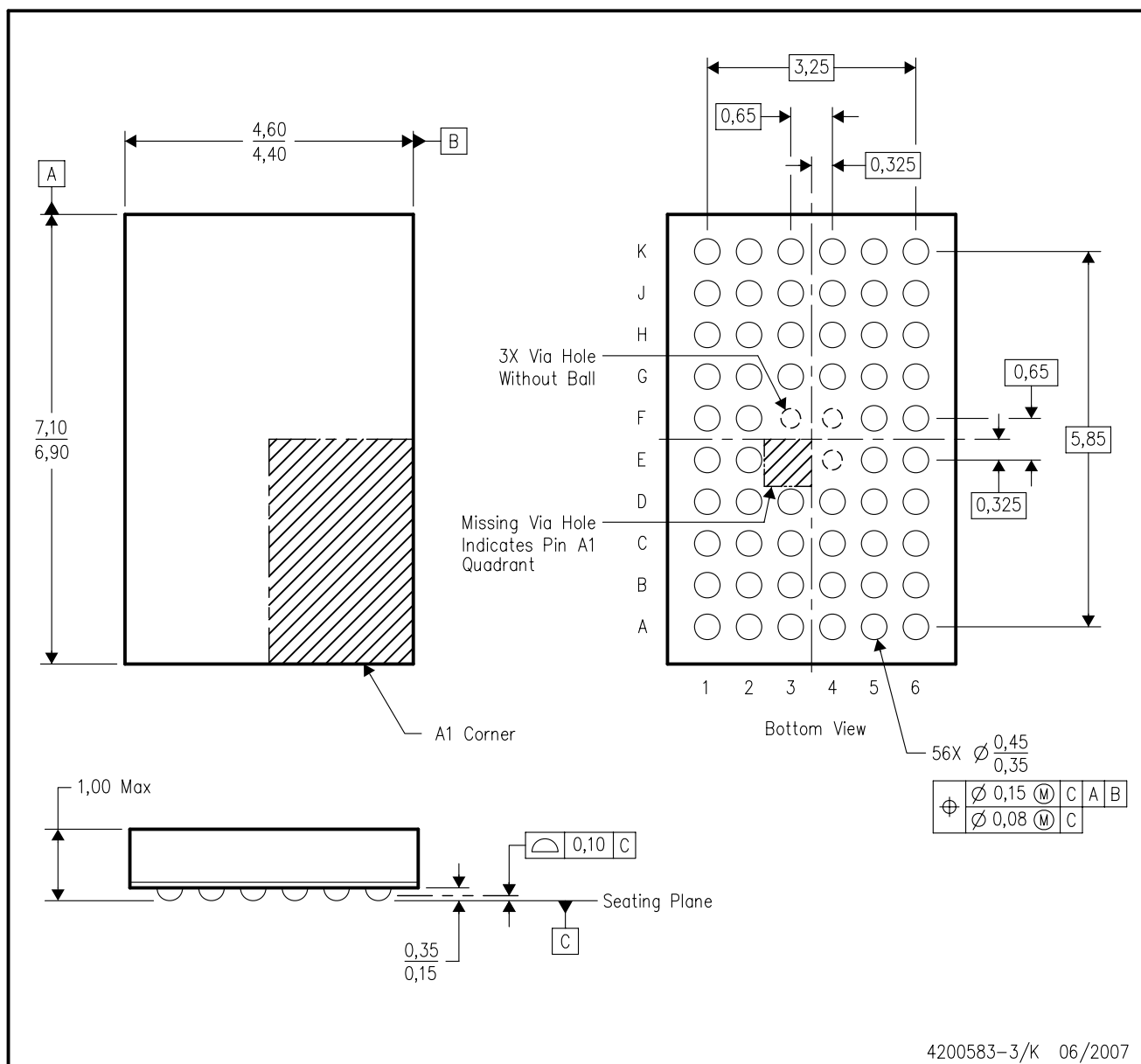
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Falls within JEDEC MO-285 variation BA-2.
 - This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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