

DUAL FET BUS SWITCH

2.5-V/3.3-V LOW-VOLTAGE HIGH-BANDWIDTH BUS SWITCH

Check for Samples: [SN74CB3Q3305](#)

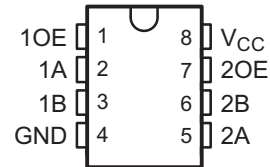
FEATURES

- **High-Bandwidth Data Path (up to 500 MHz)**

For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C*, *CB3T*, and *CB3Q Signal-Switch Families*, literature number SCDA008.

- **5-V Tolerant I/Os With Device Powered Up or Powered Down**
- **Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range ($r_{on} = 3 \Omega$ Typ)**
- **Rail-to-Rail Switching on Data I/O Ports**
 - 0- to 5-V Switching With 3.3-V V_{CC}
 - 0- to 3.3-V Switching With 2.5-V V_{CC}
- **Bidirectional Data Flow With Near-Zero Propagation Delay**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)} = 3.5 \text{ pF}$ Typ)**
- **Fast Switching Frequency ($f_{OE} = 20 \text{ MHz}$ Max)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption ($I_{CC} = 0.25 \text{ mA}$ Typ)**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- **Supports Both Digital and Analog Applications: USB Interface, Differential Signal Interface, Bus Isolation, Low-Distortion Signal Gating**

**PW PACKAGE
(TOP VIEW)**



**DCU PACKAGE
(TOP VIEW)**



DESCRIPTION/ORDERING INFORMATION

The SN74CB3Q3305 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3305 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3305 is organized as two 1-bit switches with separate output-enable (1OE, 2OE) inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When OE is high, the associated 1-bit bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When OE is low, the associated 1-bit bus switch is OFF and a high-impedance state exists between the A and B ports.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION

T _A	PACKAGE (1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING (2)
-40°C to 85°C	TSSOP – PW	Tube	SN74CB3Q3305PW	BU305
		Tape and reel	SN74CB3Q3305PWR	
	VSSOP – DCU	Tape and reel	SN74CB3Q3305DCUR	GAR_

- (1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (2) The last character designates assembly/test site.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

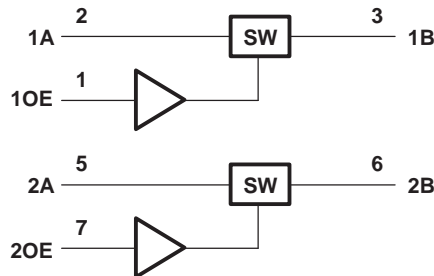
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

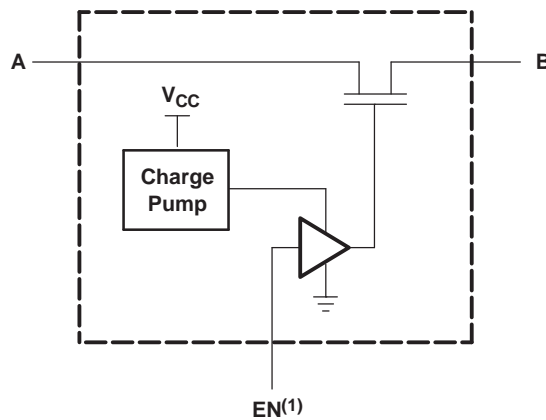
Table 1. FUNCTION TABLE (EACH BUS SWITCH)

INPUT OE	INPUT/OUTPUT A	FUNCTION
H	B	A port = B port
L	Z	Disconnect

LOGIC DIAGRAM (POSITIVE LOGIC)



SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



(1) EN is the internal enable signal applied to the switch.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	4.6	V
V_{IN}	Control input voltage range ^{(2) (3)}	-0.5	7	V
$V_{I/O}$	Switch I/O voltage range ^{(2) (3) (4)}	-0.5	7	V
I_{IK}	Control input clamp current	$V_{IN} < 0$		-50 mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$		-50 mA
$I_{I/O}$	ON-state switch current ⁽⁵⁾			±64 mA
	Continuous current through V_{CC} or GND			±100 mA
θ_{JA}	Package thermal impedance ⁽⁶⁾			88 °C/W
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
- (5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT	
V_{CC}	Supply voltage	2.3	3.6	V	
V_{IH}	High-level control input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	5.5	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2	5.5	
V_{IL}	Low-level control input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0	0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0	0.8	
$V_{I/O}$	Data input/output voltage	0	5.5	V	
T_A	Operating free-air temperature	-40	85	°C	

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽²⁾	MAX	UNIT
V_{IK}		$V_{CC} = 3.6\text{ V}$,	$I_I = -18\text{ mA}$			-1.8	V
I_{IN}	Control inputs	$V_{CC} = 3.6\text{ V}$,	$V_{IN} = 0\text{ to }5.5\text{ V}$			± 1	μA
I_{OZ} ⁽³⁾		$V_{CC} = 3.6\text{ V}$,	$V_O = 0\text{ to }5.5\text{ V}$, $V_I = 0$,	Switch OFF, $V_{IN} = V_{CC}\text{ or GND}$		± 1	μA
I_{off}		$V_{CC} = 0$,	$V_O = 0\text{ to }5.5\text{ V}$, $V_I = 0$			1	μA
I_{CC}		$V_{CC} = 3.6\text{ V}$,	$I_{I/O} = 0$, Switch ON or OFF,	$V_{IN} = V_{CC}\text{ or GND}$		0.25 0.7	mA
ΔI_{CC} ⁽⁴⁾	Control inputs	$V_{CC} = 3.6\text{ V}$, One input at 3 V, Other inputs at V_{CC} or GND				25	μA
I_{CCD} ⁽⁵⁾	Per control input	$V_{CC} = 3.6\text{ V}$,	A and B ports open, Control input switching at 50% duty cycle		0.040	0.045	mA/ MHz
C_{in}	Control inputs	$V_{CC} = 3.3\text{ V}$,	$V_{IN} = 5.5\text{ V}$, 3.3 V, or 0		2.5	3.5	pF
$C_{io(OFF)}$		$V_{CC} = 3.3\text{ V}$,	Switch OFF, $V_{IN} = V_{CC}\text{ or GND}$,	$V_{I/O} = 5.5\text{ V}$, 3.3 V, or 0		3.5 5	pF
$C_{io(ON)}$		$V_{CC} = 3.3\text{ V}$,	Switch ON, $V_{IN} = V_{CC}\text{ or GND}$,	$V_{I/O} = 5.5\text{ V}$, 3.3 V, or 0		8 10.5	pF
r_{on} ⁽⁶⁾		$V_{CC} = 2.3\text{ V}$, TYP at $V_{CC} = 2.5\text{ V}$	$V_I = 0$, $I_O = 30\text{ mA}$		3	8	Ω
			$V_I = 1.7\text{ V}$, $I_O = -15\text{ mA}$		3.5	9	
		$V_{CC} = 3\text{ V}$	$V_I = 0$, $I_O = 30\text{ mA}$		3	6	
			$V_I = 2.4\text{ V}$, $I_O = -15\text{ mA}$		3.5	8	

(1) V_{IN} and I_{IN} refer to control inputs. V_I , V_O , I_I , and I_O refer to data pins.

(2) All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
f_{OE} ⁽¹⁾	OE	A or B		10		20	MHz
t_{pd} ⁽²⁾	A or B	B or A		0.09		0.15	ns
t_{en}	OE	A or B	1	5	1	4.5	ns
t_{dis}	OE	A or B	1	4.5	1	5	ns

(1) Maximum switching frequency for control input ($V_O > V_{CC}$, $V_I = 5\text{ V}$, $R_L \geq 1\text{ M}\Omega$, $C_L = 0$)

(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

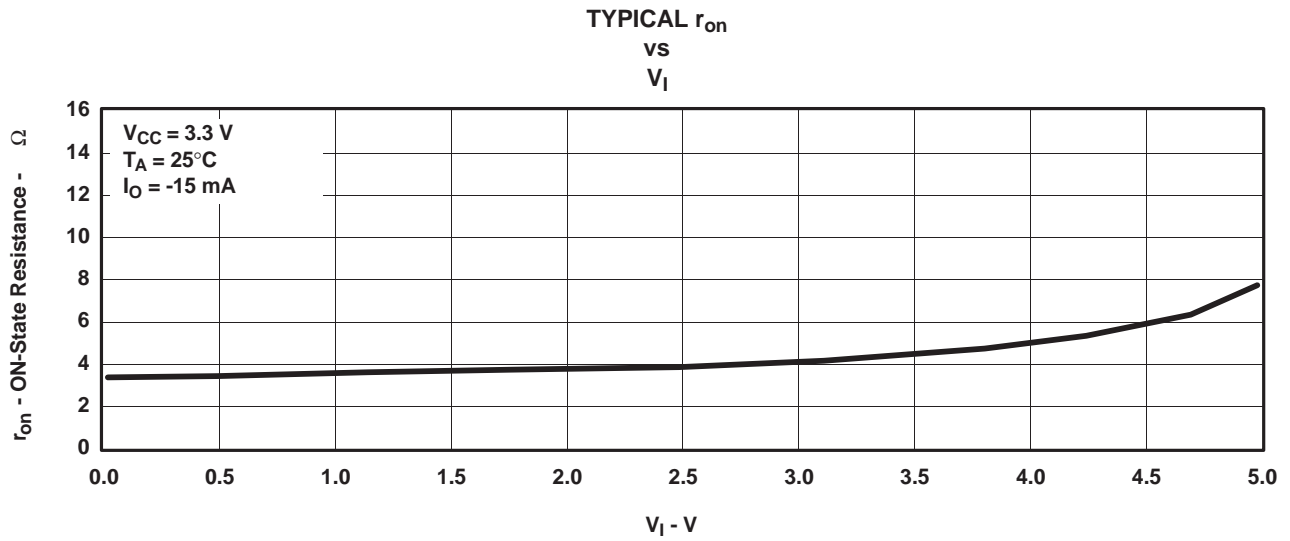


Figure 1. Typical r_{on} vs V_I

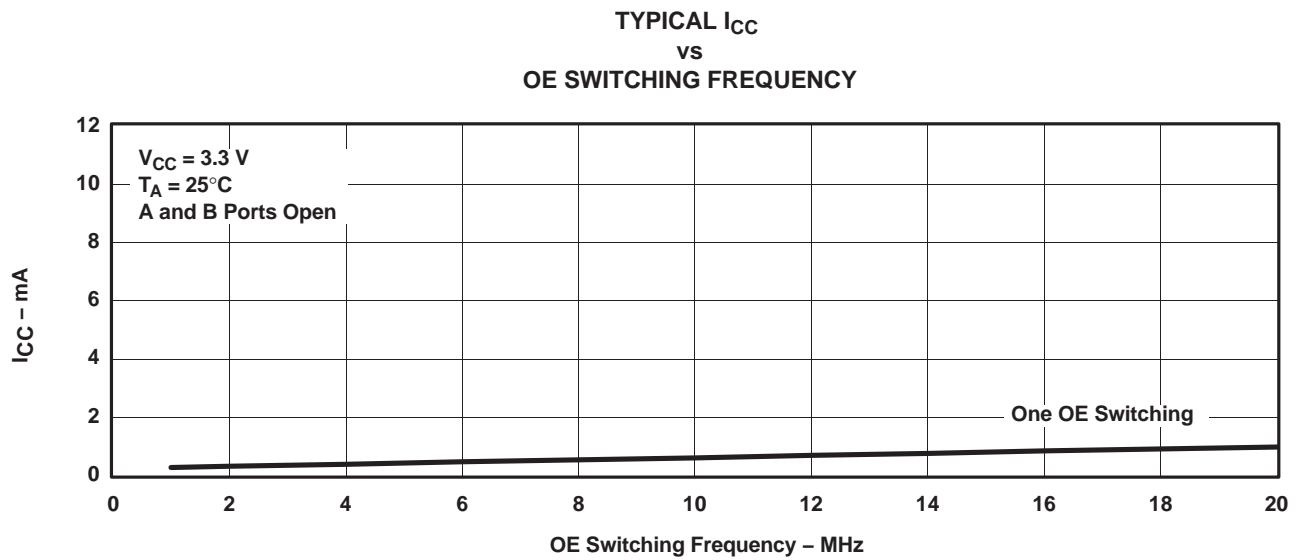
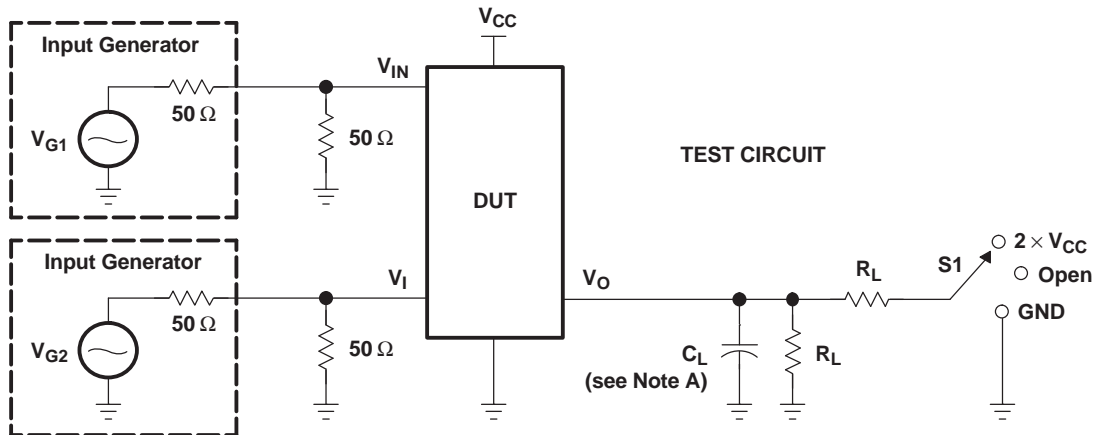
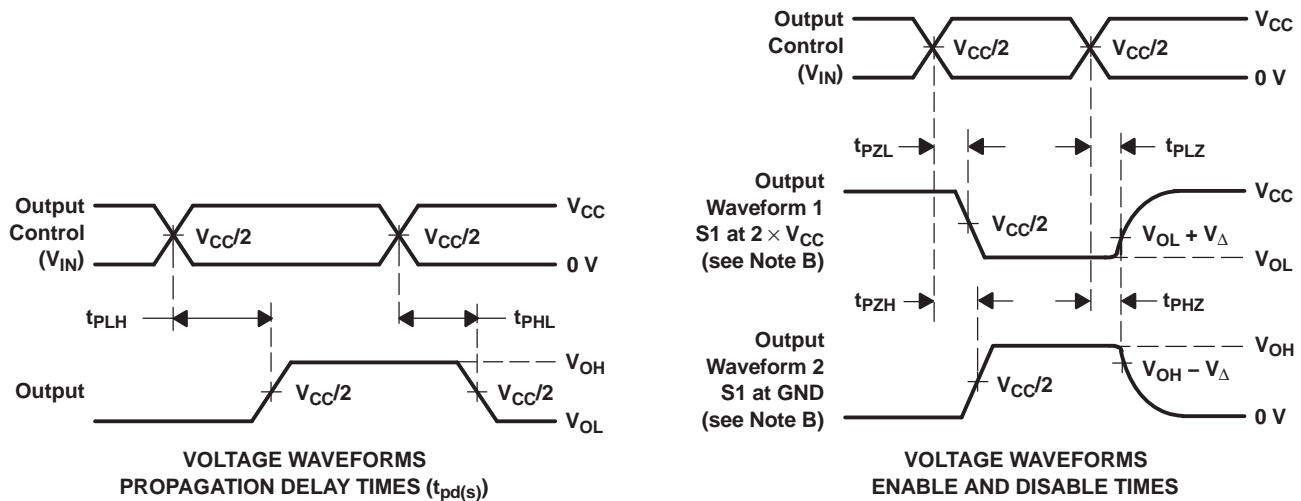


Figure 2. Typical I_{CC} vs OE Switching Frequency

PARAMETER MEASUREMENT INFORMATION



TEST	V _{CC}	S1	R _L	V _I	C _L	V _Δ
t _{pd(s)}	2.5 V ± 0.2 V	Open	500 Ω	V _{CC} or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	V _{CC} or GND	50 pF	
t _{PLZ} /t _{PZL}	2.5 V ± 0.2 V	2 × V _{CC}	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × V _{CC}	500 Ω	GND	50 pF	0.3 V
t _{PHZ} /t _{PZH}	2.5 V ± 0.2 V	GND	500 Ω	V _{CC}	30 pF	0.15 V
	3.3 V ± 0.3 V	GND	500 Ω	V _{CC}	50 pF	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - t_{PZL} and t_{PZH} are the same as t_{en}.
 - t_{PLH} and t_{PHL} are the same as t_{pd(s)}. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
 - All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74CB3Q3305DCURE4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(GARQ ~ GARR)	Samples
74CB3Q3305DCURG4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(GARQ ~ GARR)	Samples
SN74CB3Q3305DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	(GARQ ~ GARR)	Samples
SN74CB3Q3305PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU305	Samples
SN74CB3Q3305PWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU305	Samples
SN74CB3Q3305PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU305	Samples
SN74CB3Q3305PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	BU305	Samples
SN74CB3Q3305PWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU305	Samples
SN74CB3Q3305PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU305	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3Q3305DCUR	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74CB3Q3305PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

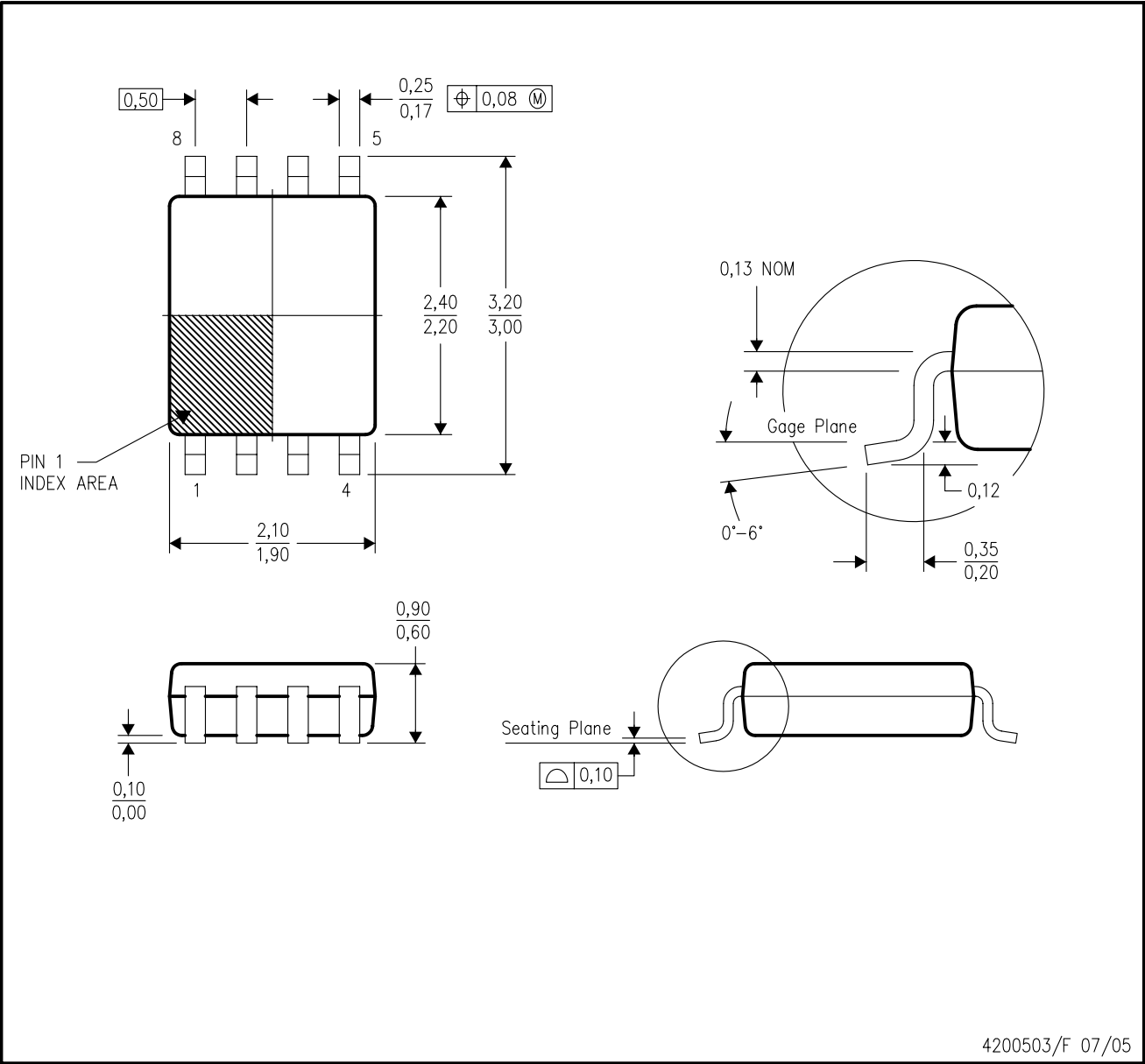
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3Q3305DCUR	US8	DCU	8	3000	202.0	201.0	28.0
SN74CB3Q3305PWR	TSSOP	PW	8	2000	364.0	364.0	27.0

DCU (R-PDSO-G8)

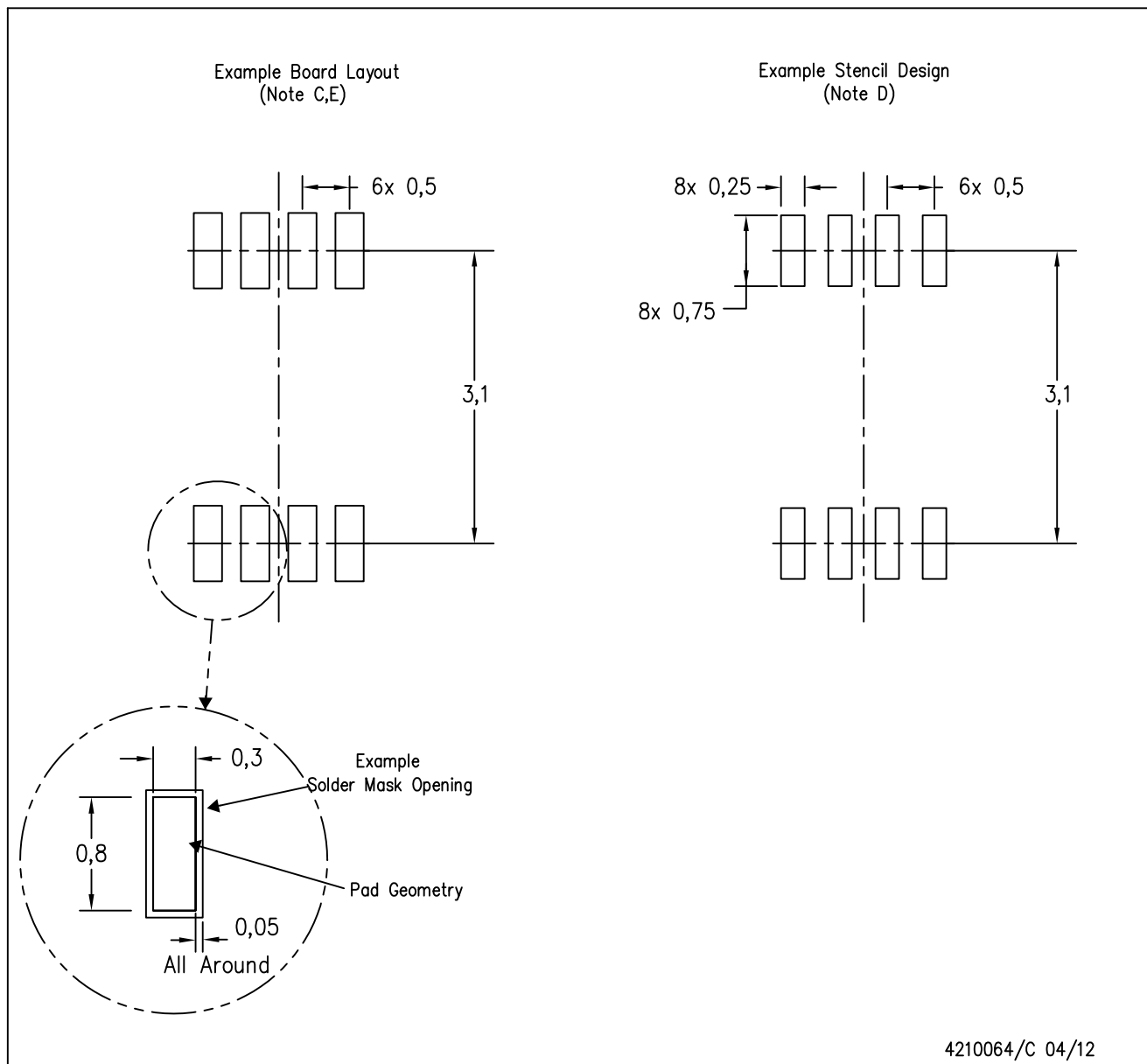
PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)





- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

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