

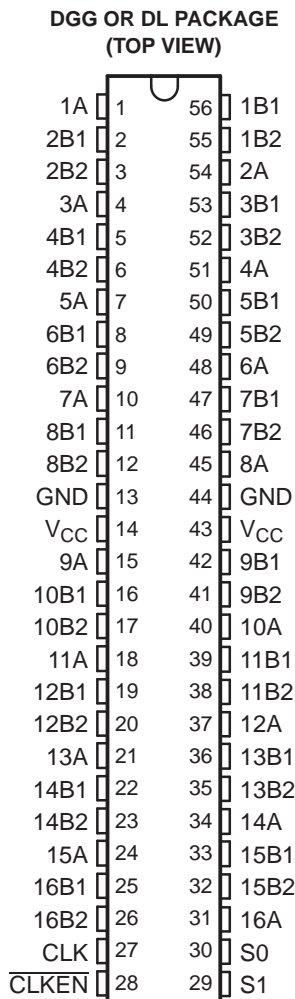
FEATURES

- Member of the Texas Instruments Widebus™ Family
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input and Output Levels

DESCRIPTION/ ORDERING INFORMATION

The SN74CBT16232 is a synchronous 16-bit 1-of-2 FET multiplexer/demultiplexer used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path.

Two select (S0 and S1) inputs control the data flow. A clock (CLK) and a clock enable ($\overline{\text{CLKEN}}$) synchronize the device operation. When $\overline{\text{CLKEN}}$ is high, the bus switch remains in the last clocked function.



ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74CBT16232DL	CBT16232
		Tape and reel	SN74CBT16232DLR	
	TSSOP – DGG	Tape and reel	SN74CBT16232DGGR	CBT16232

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



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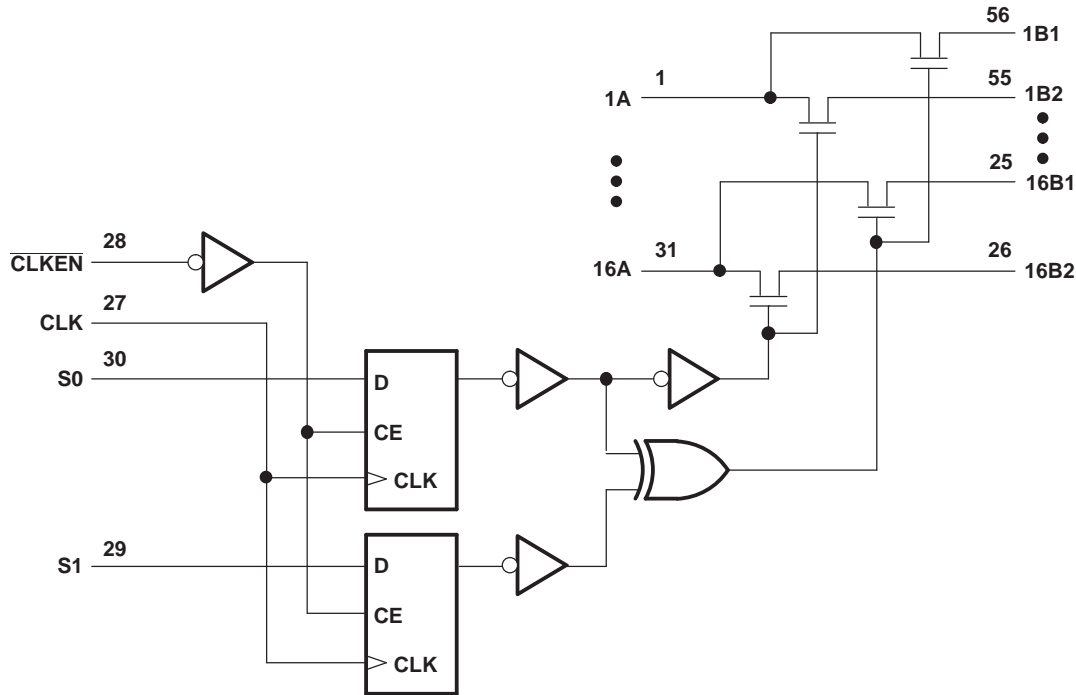
SN74CBT16232 SYNCHRONOUS 16-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

SCDS009N—MAY 1995—REVISED JUNE 2007

FUNCTION TABLE

INPUTS				FUNCTION
S1	S0	CLK	CLKEN	
X	X	X	H	Last state
L	L	↑	L	Disconnect
L	H	↑	L	A = B1 and A = B2
H	L	↑	L	A = B1
H	H	↑	L	A = B2

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
V _I	Input voltage range ⁽²⁾	-0.5	7	V
	Continuous channel current		128	mA
I _{IK}	Input clamp current		-50	mA
		V _I < 0		
		DGG package		64
θ _{JA}	Package thermal impedance ⁽³⁾	DL package		56
T _{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4	5.5	V
V _{IH}	High-level input voltage	2		V
V _{IL}	Low-level input voltage		0.8	V
T _A	Operating free-air temperature	-40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IK}		V _{CC} = 4.5 V,	I _I = -18 mA			-1.2	V
I _I		V _{CC} = 5.5 V,	V _I = 5.5 V or GND			±1	μA
I _{CC}		V _{CC} = 5.5 V,	I _O = 0, V _I = V _{CC} or GND			3	μA
ΔI _{CC} ⁽²⁾	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V, Other inputs at V _{CC} or GND			2.5	mA
C _I	Control inputs	V _I = 3 V or 0			4.5		pF
C _{io(OFF)}	A port	V _O = 3 V or 0, $\overline{\text{CLKEN}}$ = 0, S0 and S1 = GND			6.5		pF
	B port				4		
r _{on} ⁽³⁾		V _{CC} = 4 V, TYP at V _{CC} = 4 V	V _I = 2.4 V, I _I = 15 mA		14	20	Ω
			V _I = 0, I _I = 64 mA		5	7	
		V _{CC} = 4.5 V	V _I = 0, I _I = 30 mA		5	7	
			V _I = 2.4 V, I _I = 15 mA		10	15	

(1) All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

(2) This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

(3) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

			V _{CC} = 4 V		V _{CC} = 5 V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		150		150		MHz
t _w	Pulse duration	CLK high or low	3.3		3.3		ns
t _{su}	Setup time	S0, S1 before CLK↑	2.2		1.9		ns
		$\overline{\text{CLKEN}}$ before CLK↑	2.4		1.9		
t _h	Hold time	S0, S1 after CLK↑	0.5		1		ns
		$\overline{\text{CLKEN}}$ after CLK↑	1.9		1.8		

SN74CBT16232

SYNCHRONOUS 16-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

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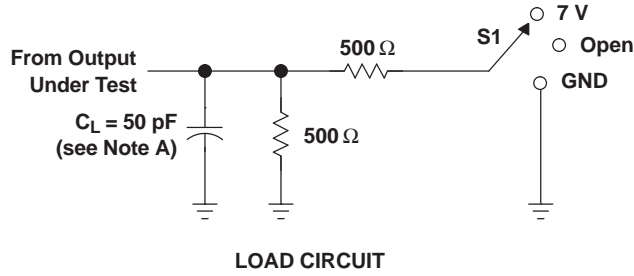
Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

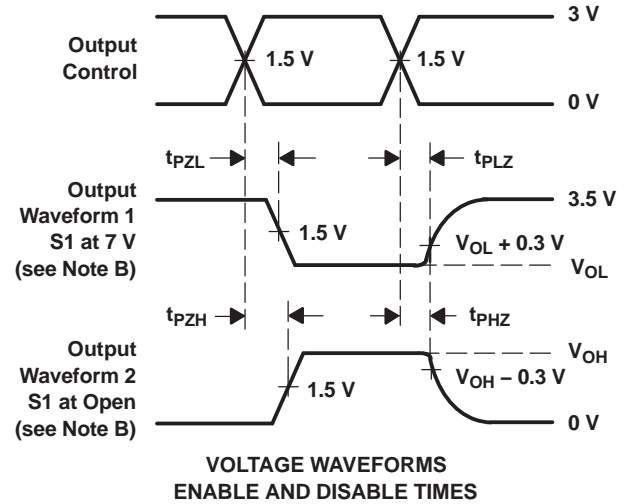
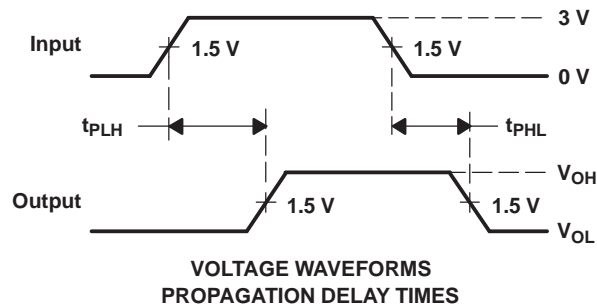
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			150		150		MHz
$t_{pd}^{(1)}$	A or B	B or A		0.35		0.25	ns
t_{pd}	CLK	A or B		6.7	2	5.8	ns
t_{en}	CLK	A, B1, B2		7.2	1.8	6.2	ns
		B1 and B2		8.5	3.1	7.9	
t_{dis}	CLK	A or B		6.3	1.9	6.2	ns

- (1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74CBT16232DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBT16232DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16232DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16232DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16232DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16232DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16232DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

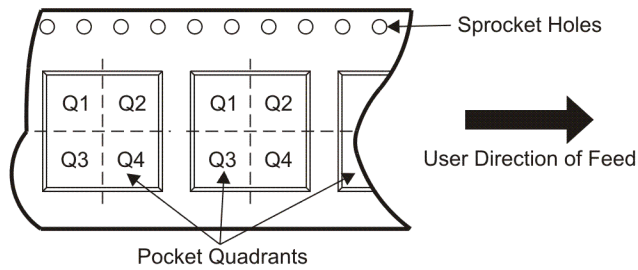
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TAPE AND REEL INFORMATION



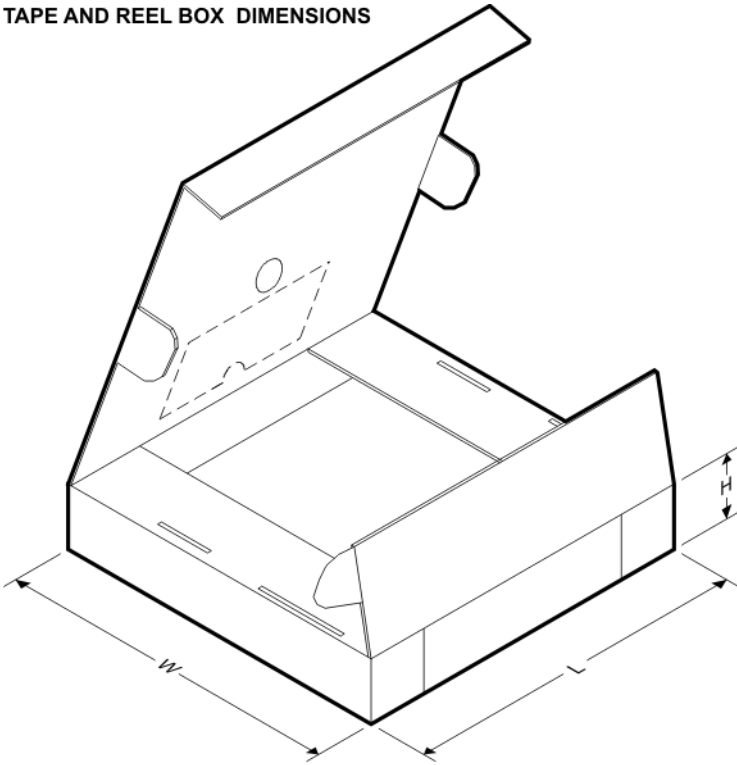
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT16232DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74CBT16232DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



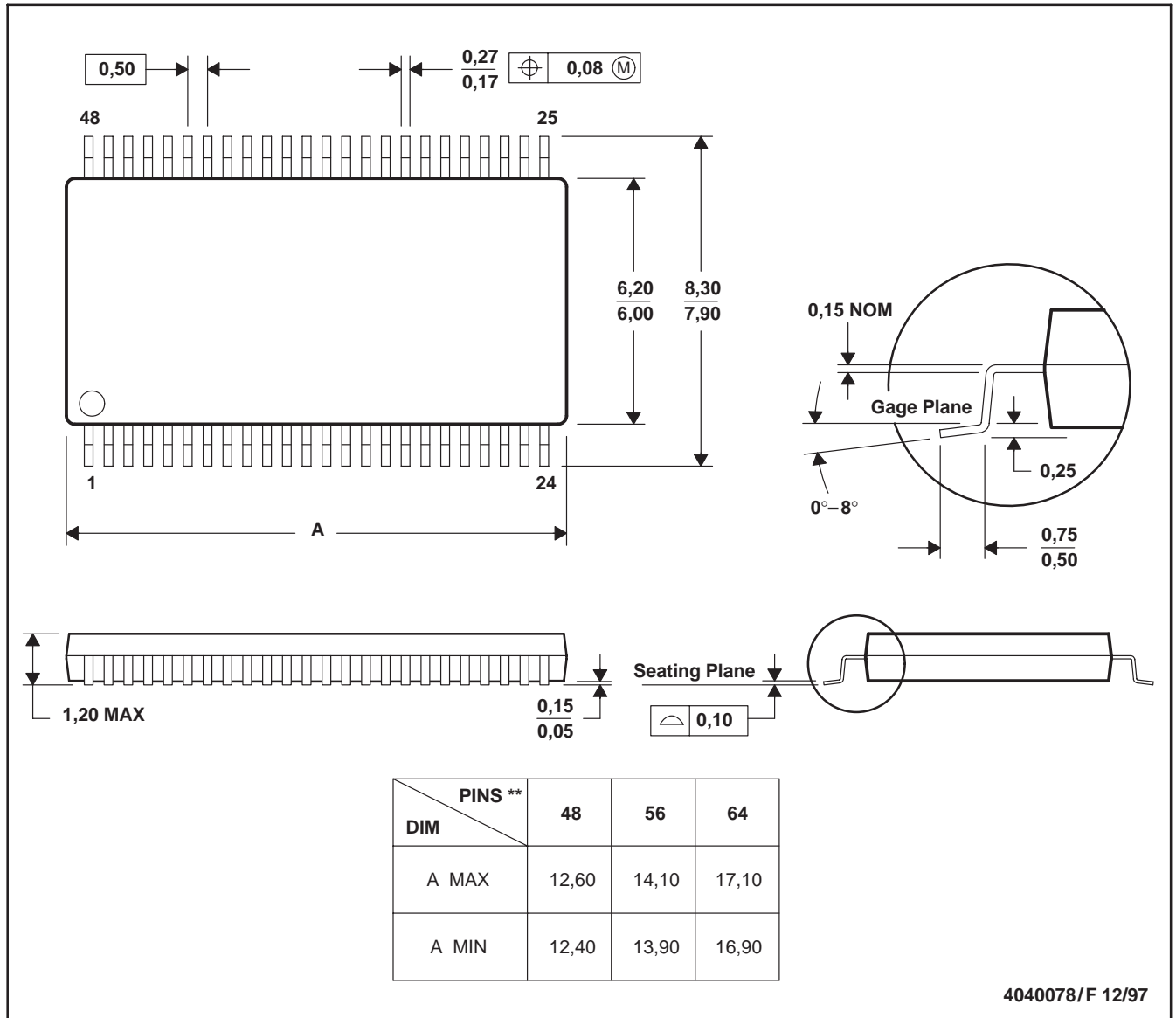
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT16232DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74CBT16232DLR	SSOP	DL	56	1000	346.0	346.0	49.0

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

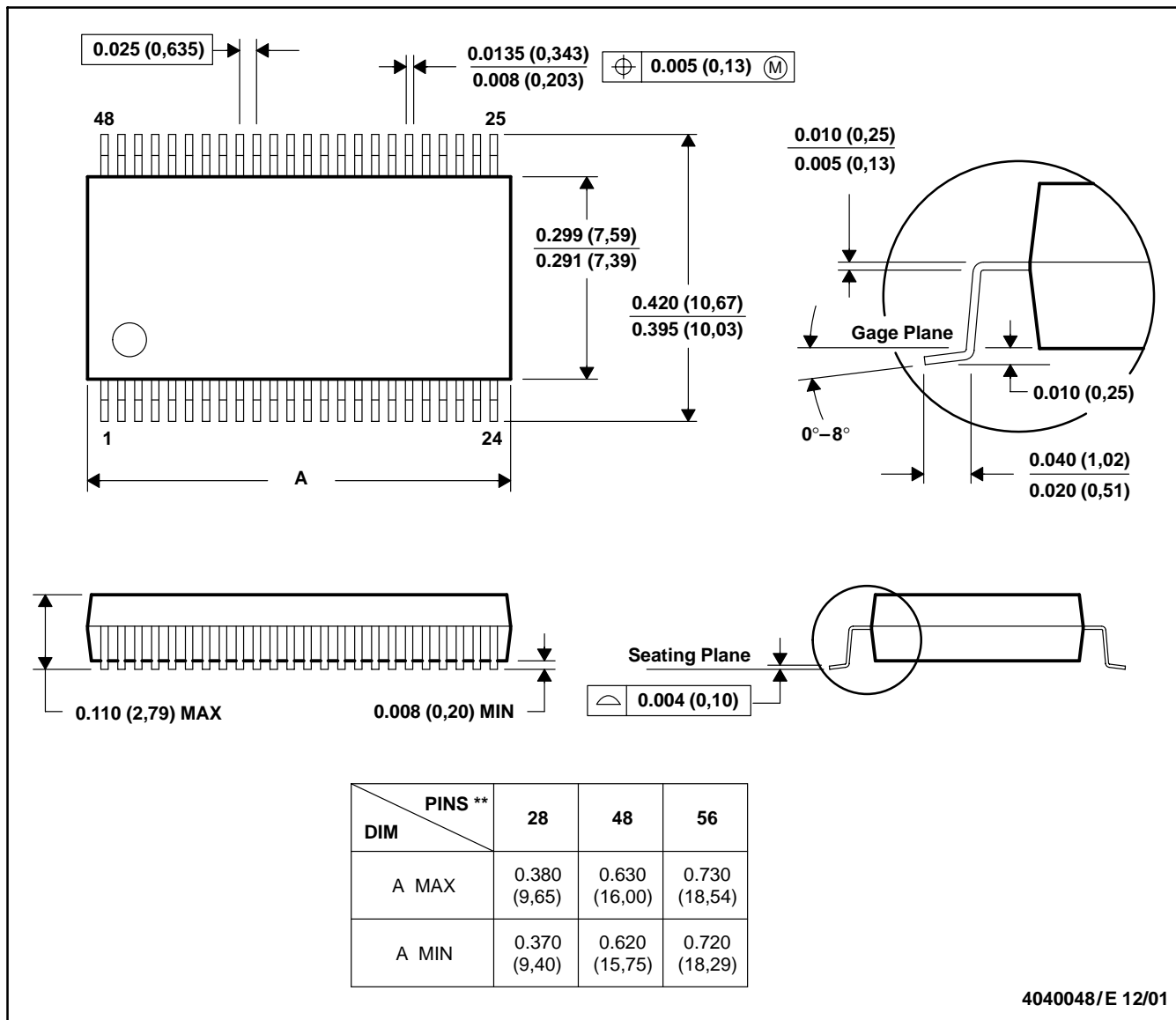


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

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