

SN54LV594A, SN74LV594A 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

SCLS4131 – APRIL 1998 – REVISED APRIL 2005

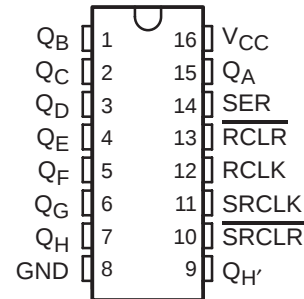
- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 6.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce)
<0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot)
>2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage
- Independent Direct Overriding Clears on Shift and Storage Registers
- Independent Clocks for Shift and Storage Registers
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

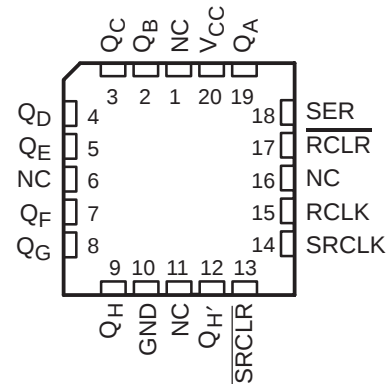
The 'LV594A devices are 8-bit shift registers designed for 2-V to 5.5-V V_{CC} operation.

These devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks (RCLK, SRCLK) and direct overriding clear ($\overline{\text{RCLR}}$, $\overline{\text{SRCLR}}$) inputs are provided on the shift and storage registers. A serial output (Q_H) is provided for cascading purposes.

SN54LV594A . . . J OR W PACKAGE
SN74LV594A . . . D, DB, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV594A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Tube of 40	SN74LV594AD	LV594A
		Reel of 2500	SN74LV594ADR	
	SOP – NS	Reel of 2000	SN74LV594ANSR	74LV594A
	SSOP – DB	Reel of 2000	SN74LV594ADBR	LV594A
	TSSOP – PW	Tube of 90	SN74LV594APW	LV594A
		Reel of 2000	SN74LV594APWR	
		Reel of 250	SN74LV594APWT	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LV594AJ	SNJ54LV594AJ
	CFP – W	Tube of 150	SNJ54LV594AW	SNJ54LV594AW
	LCCC – FK	Tube of 55	SNJ54LV594AFK	SNJ54LV594AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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**TEXAS
INSTRUMENTS**

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SN54LV594A, SN74LV594A

8-BIT SHIFT REGISTERS

WITH OUTPUT REGISTERS

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description/ordering information (continued)

The shift-register (SRCLK) and storage-register (RCLK) clocks are positive-edge triggered. If the clocks are tied together, the shift register always is one clock pulse ahead of the storage register.

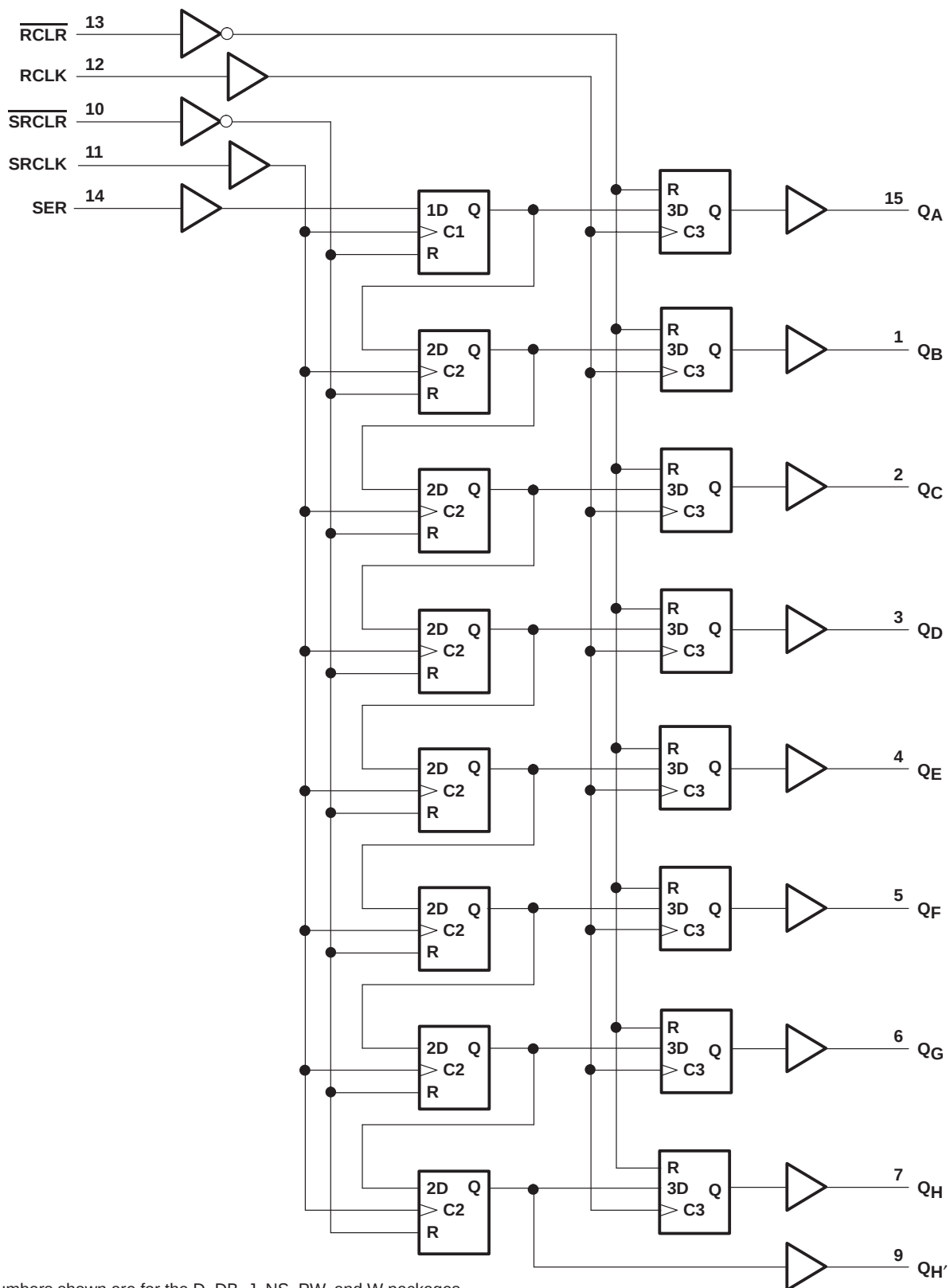
FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCLK	SRCLR	RCLK	RCLR	
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of shift register goes high. Other stages store the data of previous stage, respectively.
L	↓	H	X	X	Shift register state is not changed.
X	X	X	X	L	Storage register is cleared.
X	X	X	↑	H	Shift register data is stored in the storage register.
X	X	X	↓	H	Storage register state is not changed.

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logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, NS, PW, and W packages.

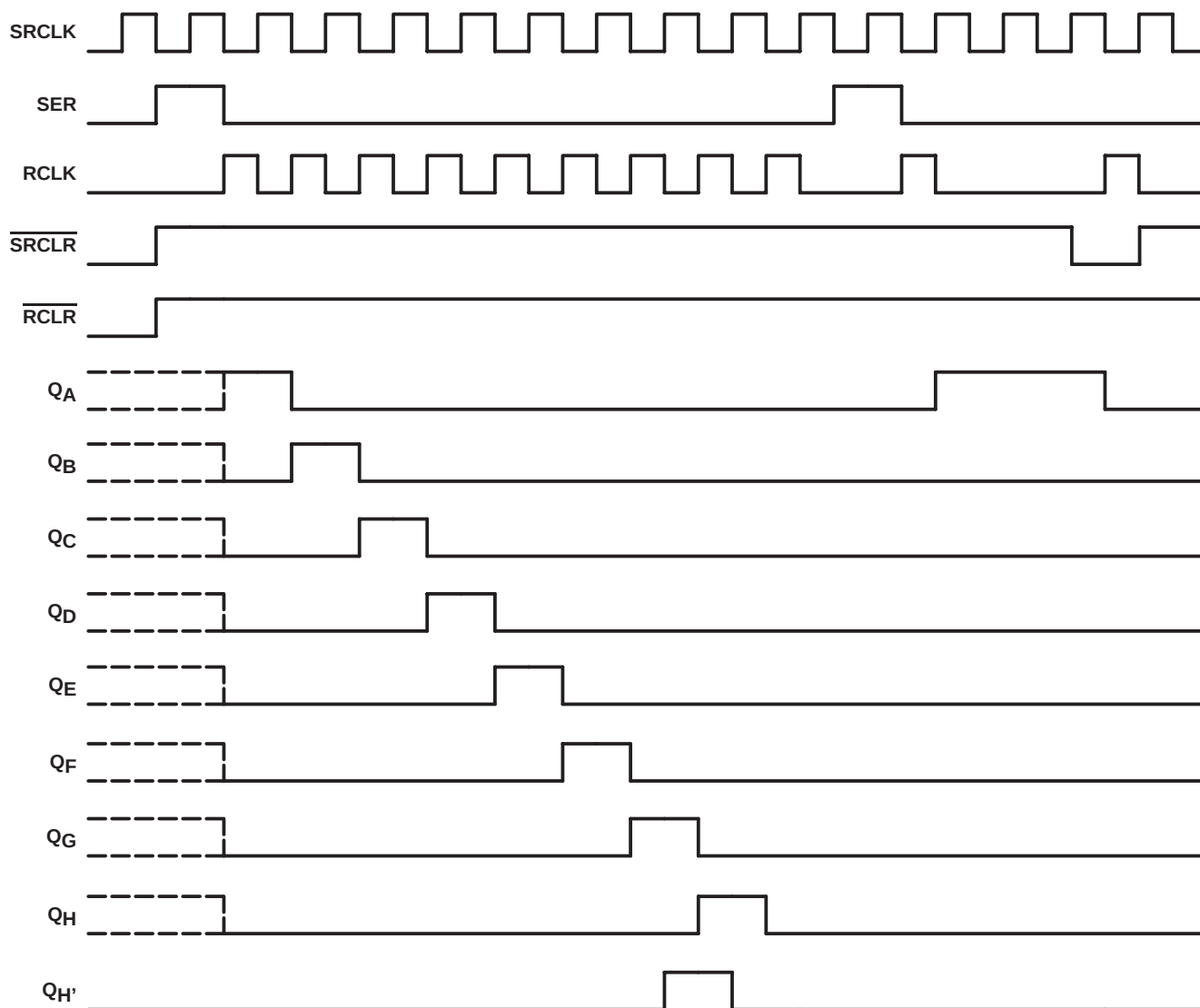


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timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	73°C/W
DB package	82°C/W
NS package	64°C/W
PW package	108°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 4)

			SN54LV594A		SN74LV594A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3		V _{CC} × 0.3		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	−50		−50		μA
		V _{CC} = 2.3 V to 2.7 V	−2		−2		mA
		V _{CC} = 3 V to 3.6 V	−6		−6		
		V _{CC} = 4.5 V to 5.5 V	−12		−12		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 2.3 V to 2.7 V	2		2		mA
		V _{CC} = 3 V to 3.6 V	6		6		
		V _{CC} = 4.5 V to 5.5 V	12		12		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	200		200		ns/V
		V _{CC} = 3 V to 3.6 V	100		100		
		V _{CC} = 4.5 V to 5.5 V	20		20		
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV594A			SN74LV594A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1			V _{CC} -0.1			V
	I _{OH} = -2 mA	2.3 V	2			2			
	I _{OH} = -6 mA	3 V	2.48			2.48			
	I _{OH} = -12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	V _I = 5.5 V or GND	0 to 5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V	3.5			3.5			pF

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		SN54LV594A		SN74LV594A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	RCLK or SRCLK high or low	7		7.5		7.5		ns
		RCLR or SRCLR low	6		6.5		6.5		
t_{su}	Setup time	SER before SRCLK $\uparrow$	5.5		5.5		5.5		ns
		SRCLK $\uparrow$ before RCLK $\uparrow$	8		9		9		
		SRCLR low before RCLK $\uparrow$	8.5		9.5		9.5		
		SRCLR high (inactive) before SRCLK $\uparrow$	6		6.8		6.8		
		RCLR high (inactive) before RCLK $\uparrow$	6.7		7.6		7.6		
t_h	Hold time	SER after SRCLK $\uparrow$	1.5		1.5		1.5		ns

[†] This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		SN54LV594A		SN74LV594A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	RCLK or SRCLK high or low	5.5		5.5		5.5		ns
		RCLR or SRCLR low	5		5		5		
t_{su}	Setup time	SER before SRCLK $\uparrow$	3.5		3.5		3.5		ns
		SRCLK $\uparrow$ before RCLK $\uparrow$	8		8.5		8.5		
		SRCLR low before RCLK $\uparrow$	8		9		9		
		SRCLR high (inactive) before SRCLK $\uparrow$	4.2		4.8		4.8		
		RCLR high (inactive) before RCLK $\uparrow$	4.6		5.3		5.3		
t_h	Hold time	SER after SRCLK $\uparrow$	1.5		1.5		1.5		ns

[†] This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		SN54LV594A		SN74LV594A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	RCLK or SRCLK high or low	5		5		5		ns
		RCLR or SRCLR low	5.2		5.2		5.2		
t_{su}	Setup time	SER before SRCLK $\uparrow$	3		3		3		ns
		SRCLK $\uparrow$ before RCLK $\uparrow$	5		5		5		
		SRCLR low before RCLK $\uparrow$	5		5		5		
		SRCLR high (inactive) before SRCLK $\uparrow$	2.9		3.3		3.3		
		RCLR high (inactive) before RCLK $\uparrow$	3.2		3.7		3.7		
t_h	Hold time	SER after SRCLK $\uparrow$	2		2		2		ns

[†] This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV594A		SN74LV594A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			C _L = 15 pF	65*	80*		45*		45		MHz
			C _L = 50 pF	60	70		40		40		
t _{PLH}	RCLK	Q _A -Q _H	C _L = 15 pF		6.4*	10.6*	1*	11.1*	1	11.1	ns
t _{PHL}					6.3*	10.4*	1*	11.1*	1	11.1	
t _{PLH}	SRCLK	Q _H '			7.4*	12.1*	1*	12.8*	1	12.8	
t _{PHL}					7.2*	11.6*	1*	12.8*	1	12.8	
t _{PHL}	$\overline{\text{RCLR}}$	Q _A -Q _H			7.9*	12.7*	1*	13.6*	1	13.6	
	$\overline{\text{SRCLR}}$	Q _H '			7.4*	11.9*	1*	13.1*	1	13.1	
t _{PLH}	RCLK	Q _A -Q _H	C _L = 50 pF		9.5	14.1	1	14.6	1	14.6	ns
t _{PHL}					10.8	15.5	1	17.2	1	17.2	
t _{PLH}	SRCLK	Q _H '			10.6	15.7	1	16.5	1	16.5	
t _{PHL}					11.3	16.1	1	18.6	1	18.6	
t _{PHL}	$\overline{\text{RCLR}}$	Q _A -Q _H			12.1	17.4	1	19	1	19	
	$\overline{\text{SRCLR}}$	Q _H '			11.6	16.5	1	18.6	1	18.6	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV594A		SN74LV594A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			C _L = 15 pF	80*	120*		70*		70		MHz
			C _L = 50 pF	55	105		50		50		
t _{PLH}	RCLK	Q _A -Q _H	C _L = 15 pF		4.6*	8*	1*	8.5*	1	8.5	ns
t _{PHL}					4.9*	8.2*	1*	8.8*	1	8.8	
t _{PLH}	SRCLK	Q _H '			5.4*	9.1*	1*	9.7*	1	9.7	
t _{PHL}					5.5*	9.2*	1*	9.9*	1	9.9	
t _{PHL}	$\overline{\text{RCLR}}$	Q _A -Q _H			6*	9.8*	1*	10.6*	1	10.6	
	$\overline{\text{SRCLR}}$	Q _H '			5.6*	9.2*	1*	10*	1	10	
t _{PLH}	RCLK	Q _A -Q _H	C _L = 50 pF		6.9	10.5	1	11.1	1	11.1	ns
t _{PHL}					8.1	11.9	1	13.1	1	13.1	
t _{PLH}	SRCLK	Q _H '			7.7	11.7	1	12.4	1	12.4	
t _{PHL}					8.4	12.5	1	13.9	1	13.9	
t _{PHL}	$\overline{\text{RCLR}}$	Q _A -Q _H			9.1	13.1	1	14.4	1	14.4	
	$\overline{\text{SRCLR}}$	Q _H '			8.5	12.4	1	14	1	14	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV594A		SN74LV594A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			C _L = 15 pF	135*	170*		115*		115		MHz
			C _L = 50 pF	120	140		95		95		
t _{PLH}	RCLK	Q _A -Q _H	C _L = 15 pF		3.3*	6.2*	1*	6.5*	1	6.5	ns
t _{PHL}					3.7*	6.5*	1*	6.9*	1	6.9	
t _{PLH}	SRCLK	Q _H '			3.7*	6.8*	1*	7.2*	1	7.2	
t _{PHL}					4.1*	7.2*	1*	7.6*	1	7.6	
t _{PHL}	$\overline{\text{RCLR}}$	Q _A -Q _H			4.5*	7.6*	1*	8.2*	1	8.2	
	$\overline{\text{SRCLR}}$	Q _H '			4.1*	7.1*	1*	7.6*	1	7.6	
t _{PLH}	RCLK	Q _A -Q _H	C _L = 50 pF		4.9	7.8	1	8.3	1	8.3	ns
t _{PHL}					5.8	8.9	1	9.7	1	9.7	
t _{PLH}	SRCLK	Q _H '			5.5	8.6	1	9.1	1	9.1	
t _{PHL}					6	9.2	1	10.1	1	10.1	
t _{PHL}	$\overline{\text{RCLR}}$	Q _A -Q _H			6.6	10	1	10.7	1	10.7	
	$\overline{\text{SRCLR}}$	Q _H '			6	9.2	1	10.1	1	10.1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74LV594A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.1	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.8		V
$V_{IH(D)}$	High-level dynamic input voltage		2.31		V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$f = 10\text{ MHz}$	3.3 V	93	pF
			5 V	112	

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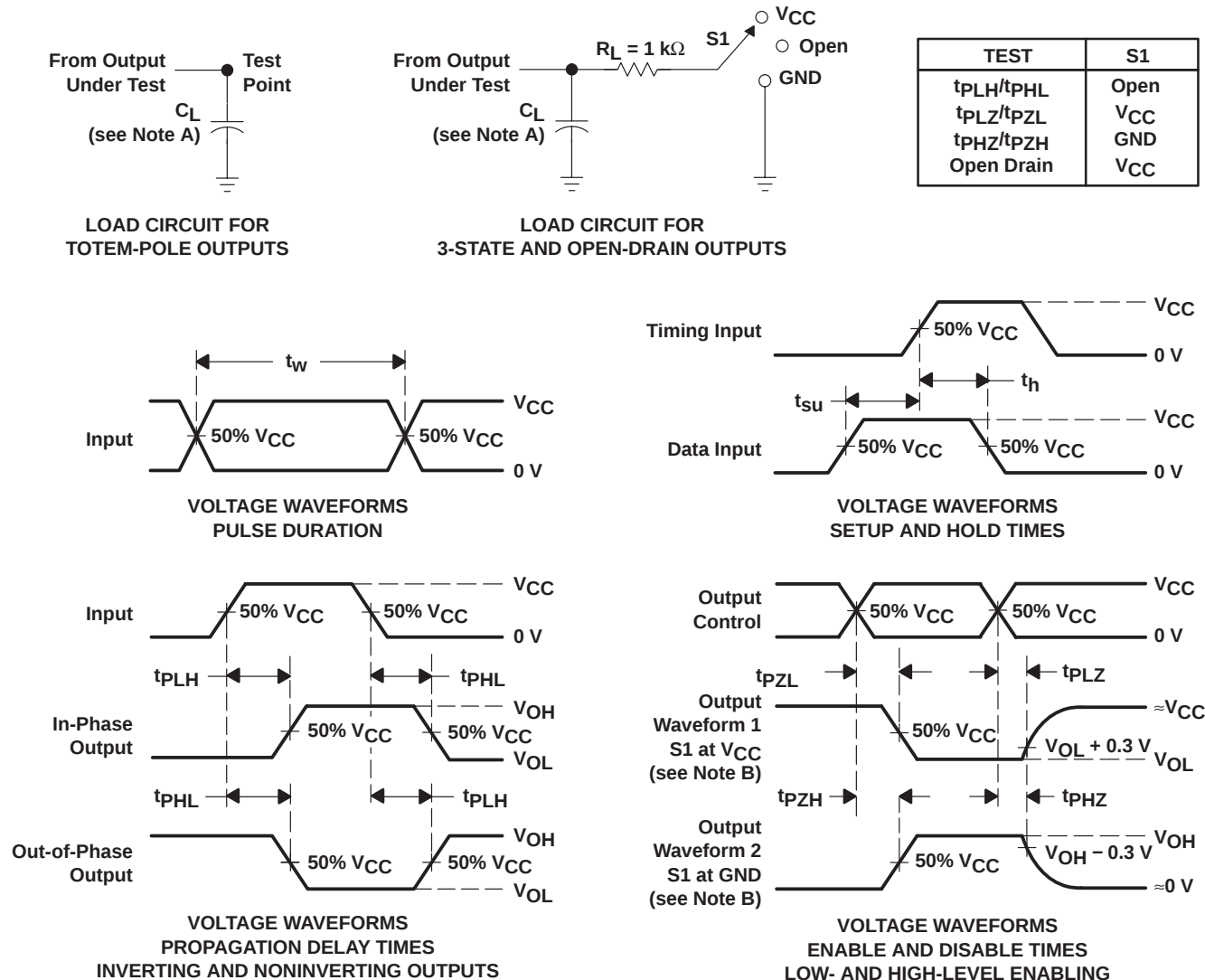
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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - The outputs are measured one at a time, with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV594AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV594A	Samples
SN74LV594ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV594A	Samples
SN74LV594ADBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV594A	Samples
SN74LV594ADBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV594A	Samples
SN74LV594ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV594A	Samples
SN74LV594ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV594A	Samples
SN74LV594ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV594A	Samples
SN74LV594ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV594A	Samples
SN74LV594ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV594A	Samples
SN74LV594APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV594A	Samples
SN74LV594APWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV594A	Samples
SN74LV594APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV594A	Samples
SN74LV594APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	LV594A	Samples
SN74LV594APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV594A	Samples
SN74LV594APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV594A	Samples
SN74LV594APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV594A	Samples
SN74LV594APWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV594A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV594APWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV594A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV594ADBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LV594ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV594APWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
SN74LV594APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV594APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV594APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV594ADBR	SSOP	DB	16	2000	367.0	367.0	38.0
SN74LV594ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV594APWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74LV594APWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV594APWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV594APWT	TSSOP	PW	16	250	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211283-4/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

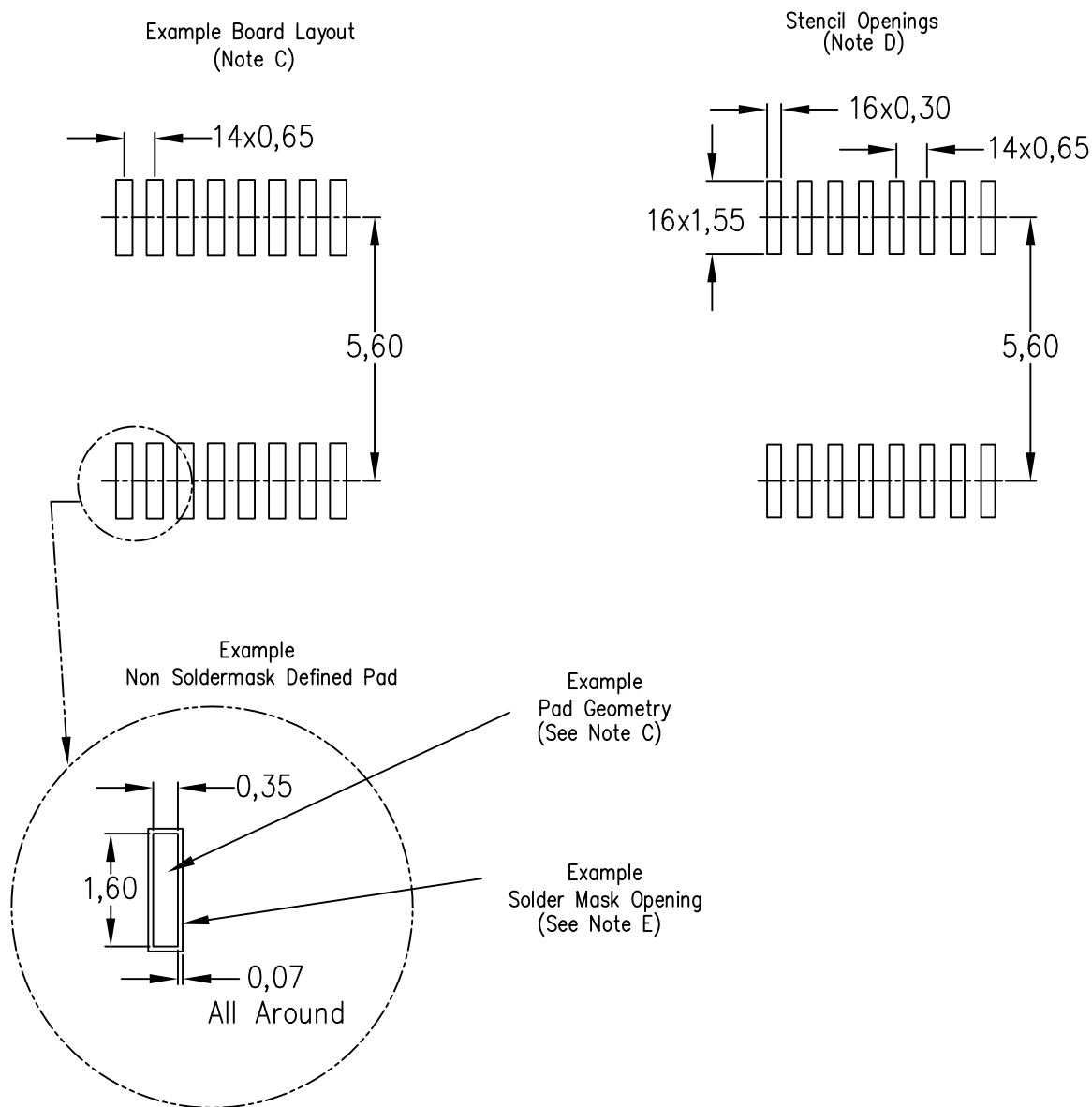


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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