

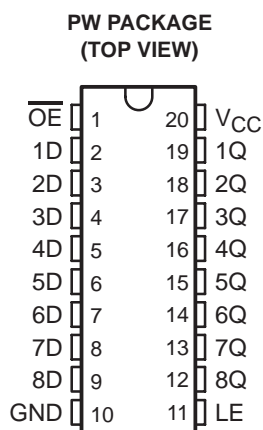
SN74LVTH573-EP

3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCBS773 – NOVEMBER 2003

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down To 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.



description/ordering information

This octal latch is designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight latches of the SN74LVTH573 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|------------|---------------|-----------------------|------------------|
| -40°C to 85°C | TSSOP – PW | Tape and reel | SN74LVTH573IPWREP | LH573EP |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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description/ordering information

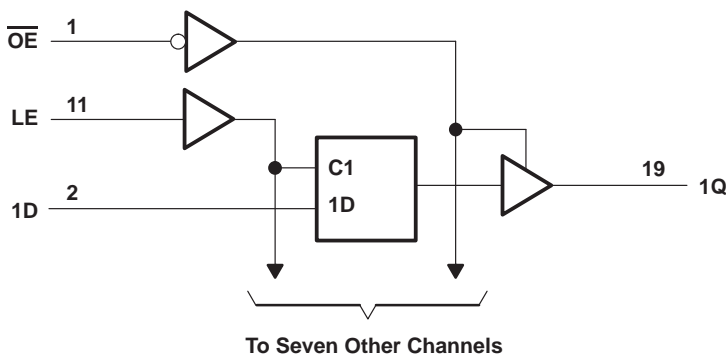
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE
(each latch)

| INPUTS | | | OUTPUT Q |
|-----------------|----|---|-------------|
| \overline{OE} | LE | D | |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q_0 |
| H | X | X | Z |

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 4.6 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high state, V_O (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Current into any output in the low state, I_O | 128 mA |
| Current into any output in the high state, I_O (see Note 2) | 64 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | –50 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | –50 mA |
| Package thermal impedance, θ_{JA} (see Note 3) | 83°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 4)

| | | MIN | MAX | UNIT |
|--------------------------|------------------------------------|-----------------|-----|--------------|
| V_{CC} | Supply voltage | 2.7 | 3.6 | V |
| V_{IH} | High-level input voltage | 2 | | V |
| V_{IL} | Low-level input voltage | | 0.8 | V |
| V_I | Input voltage | | 5.5 | V |
| I_{OH} | High-level output current | | -32 | mA |
| I_{OL} | Low-level output current | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | 200 | | μ s/V |
| T_A | Operating free-air temperature | -40 | 85 | $^{\circ}$ C |

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|----------------------|----------------|---|-----------------------------|--------------|------|-----------|---------|
| V_{IK} | | $V_{CC} = 2.7$ V, | $I_I = -18$ mA | | | -1.2 | V |
| V_{OH} | | $V_{CC} = 2.7$ V to 3.6 V, | $I_{OH} = -100$ μ A | $V_{CC}-0.2$ | | | V |
| | | $V_{CC} = 2.7$ V, | $I_{OH} = -8$ mA | 2.4 | | | |
| | | $V_{CC} = 3$ V, | $I_{OH} = -32$ mA | 2 | | | |
| V_{OL} | | $V_{CC} = 2.7$ V | $I_{OL} = 100$ μ A | | | 0.2 | V |
| | | | $I_{OL} = 24$ mA | | | 0.5 | |
| | | $V_{CC} = 3$ V | $I_{OL} = 16$ mA | | | 0.4 | |
| | | | $I_{OL} = 32$ mA | | | 0.5 | |
| | | | $I_{OL} = 64$ mA | | | 0.55 | |
| I_I | Control inputs | $V_{CC} = 0$ or 3.6 V, | $V_I = 5.5$ V | | | 10 | μ A |
| | | $V_{CC} = 3.6$ V, | $V_I = V_{CC}$ or GND | | | ± 1 | |
| | Data inputs | $V_{CC} = 3.6$ V | $V_I = V_{CC}$ | | | 1 | |
| | | | $V_I = 0$ | | | -5 | |
| I_{off} | | $V_{CC} = 0$, | V_I or $V_O = 0$ to 4.5 V | | | ± 100 | μ A |
| $I_{I(hold)}$ | Data inputs | $V_{CC} = 3$ V | $V_I = 0.8$ V | | | 75 | μ A |
| | | | $V_I = 2$ V | | | -75 | |
| | | $V_{CC} = 3.6$ V‡, | $V_I = 0$ to 3.6 V | | | ± 500 | |
| I_{OZH} | | $V_{CC} = 3.6$ V, | $V_O = 3$ V | | | 5 | μ A |
| I_{OZL} | | $V_{CC} = 3.6$ V, | $V_O = 0.5$ V | | | -5 | μ A |
| I_{OZPU} | | $V_{CC} = 0$ to 1.5 V, $V_O = 0.5$ V to 3 V, $\overline{OE} = \text{don't care}$ | | | | ± 100 | μ A |
| I_{OZPD} | | $V_{CC} = 1.5$ V to 0, $V_O = 0.5$ V to 3 V, $\overline{OE} = \text{don't care}$ | | | | ± 100 | μ A |
| I_{CC} | | $V_{CC} = 3.6$ V, $I_O = 0$, $V_I = V_{CC}$ or GND | Outputs high | | | 0.19 | mA |
| | | | Outputs low | | | 5 | |
| | | | Outputs disabled | | | 0.19 | |
| ΔI_{CC}^{\S} | | $V_{CC} = 3$ V to 3.6 V, One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND | | | | 0.2 | mA |
| C_i | | $V_I = 3$ V or 0 | | | | 3 | pF |
| C_o | | $V_O = 3$ V or 0 | | | | 7 | pF |

† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^{\circ}$ C.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.



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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | UNIT |
|----------|-----------------------------|---|-----|-------------------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| t_w | Pulse duration, LE high | 3 | | 3 | | ns |
| t_{su} | Setup time, data before LE↓ | 0.7 | | 0.6 | | ns |
| t_h | Hold time, data after LE↓ | 1.5 | | 1.7 | | ns |

switching characteristics over recommended free-air temperature, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | | $V_{CC} = 2.7\text{ V}$ | | UNIT |
|-----------|-----------------|----------------|---|------|-----|-------------------------|-----|------|
| | | | MIN | TYP† | MAX | MIN | MAX | |
| t_{PLH} | D | Q | 1.5 | 2.6 | 3.9 | | 4.5 | ns |
| t_{PHL} | | | 1.5 | 2.9 | 3.9 | | 4.5 | |
| t_{PLH} | LE | Q | 1.9 | 2.9 | 4.2 | | 4.9 | ns |
| t_{PHL} | | | 1.9 | 2.9 | 4.2 | | 4.9 | |
| t_{PZH} | \overline{OE} | Q | 1.5 | 3.2 | 5.1 | | 5.9 | ns |
| t_{PZL} | | | 1.5 | 3.9 | 5.1 | | 5.9 | |
| t_{PHZ} | \overline{OE} | Q | 2 | 3.5 | 4.9 | | 5.5 | ns |
| t_{PLZ} | | | 2 | 3.2 | 4.6 | | 4.9 | |

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

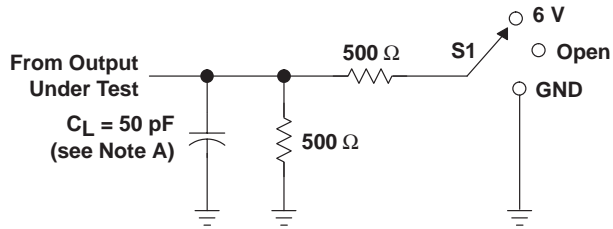
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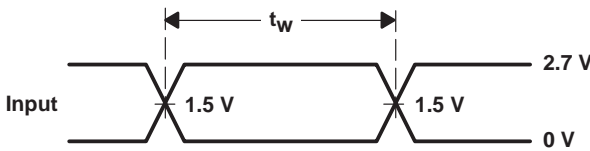
WITH 3-STATE OUTPUTS

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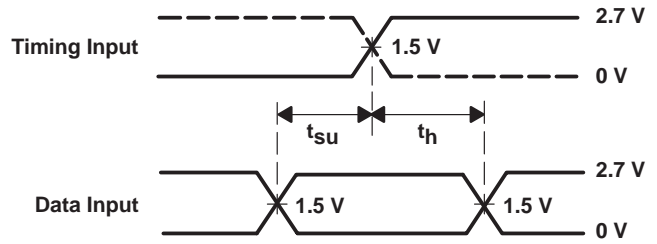
PARAMETER MEASUREMENT INFORMATION



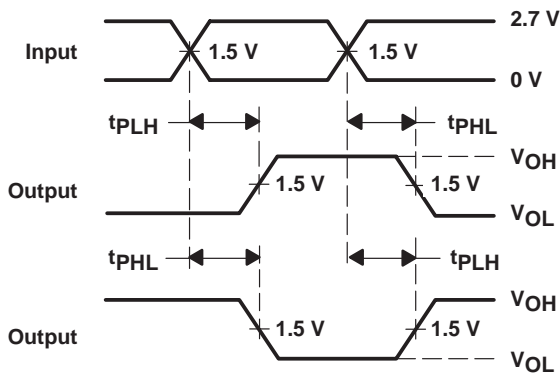
LOAD CIRCUIT



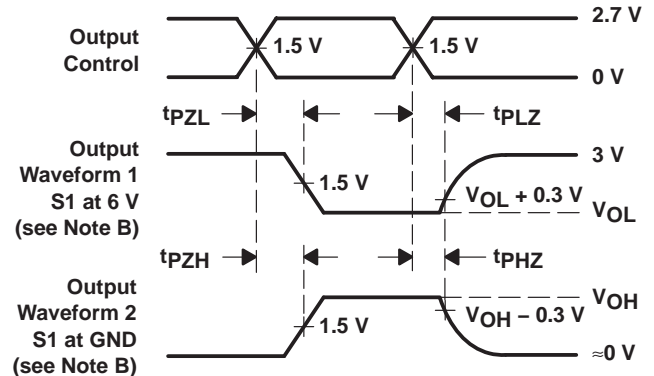
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|-------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| SN74LVTH573IPWREP | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LH573EP | Samples |
| V62/04678-01XE | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LH573EP | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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- Catalog: [SN74LVTH573](#)

- Military: [SN54LVTH573](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVTH573IPWREP | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVTH573IPWREP | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |

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