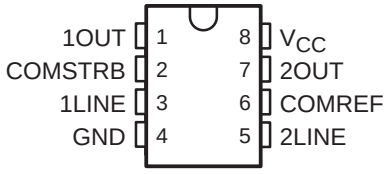
SLLS080C – JANUARY 1977 – REVISED APRIL 1998

- **Single 5-V Supply**
- **±100-mV Sensitivity**
- **For Application as:**
  - **Single-Ended Line Receiver**
  - **Gated Oscillator**
  - **Level Comparator**
- **Adjustable Reference Voltage**
- **TTL Outputs**
- **TTL-Compatible Strobe**
- **Designed for Party-Line (Data-Bus) Applications**
- **Common Reference-Voltage Pin**
- **Common Strobe**

P OR PS† PACKAGE
(TOP VIEW)



† The PS package is only available left-ended taped and reeled (order SN75140 PSR).

description

This device consists of a dual single-ended line receiver with TTL-compatible strobes and outputs. The reference voltage (switching threshold) is applied externally and can be adjusted from 1.5 V to 3.5 V, making it possible to optimize noise immunity for a given system design. Due to the low input current (less than 100 μA), the device is suited ideally for party-line (data-bus) systems.

The SN75140 has a common reference-voltage pin and a common strobe.

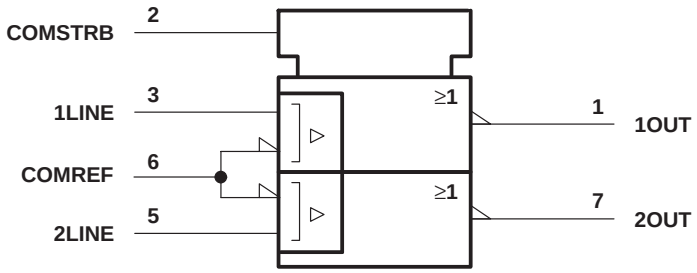
The SN75140 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each receiver)

LINE INPUT	STROBE	OUTPUT
≤ V_{ref} – 100 mV	L	H
≥ V_{ref} + 100 mV	X	L
X	H	L

H = high level, L = low level, X = irrelevant

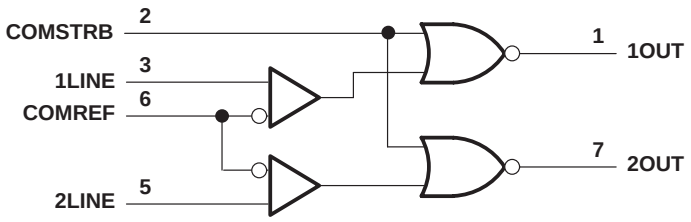
logic symbol‡



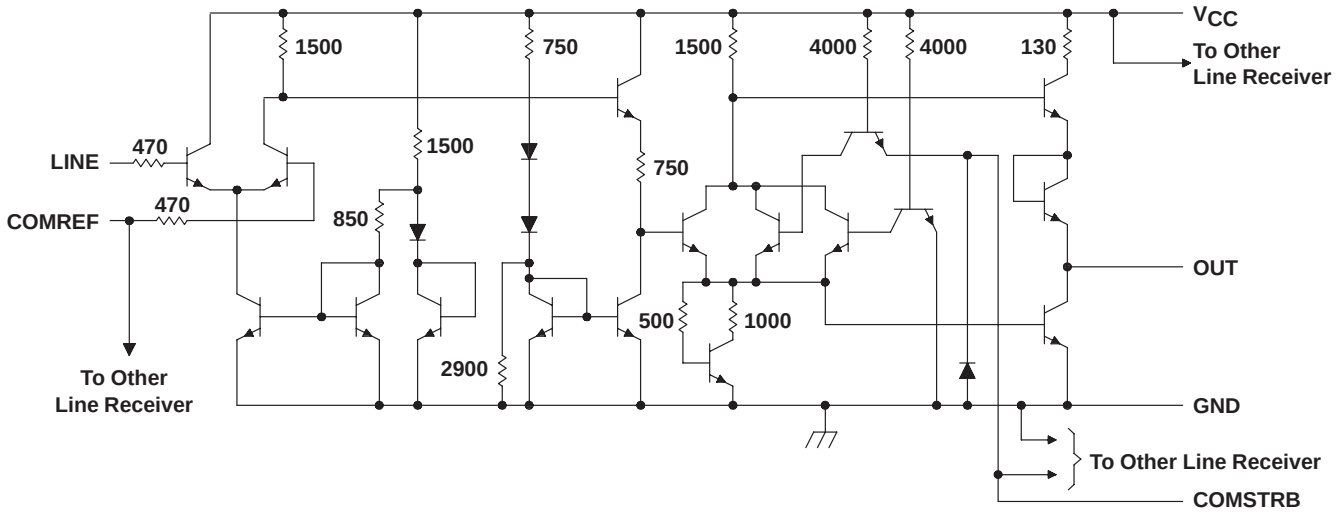
‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

logic diagram (positive logic)



schematic (each receiver)



NOTE: Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Reference input voltage, V_{ref} . . . . . 5.5 V
Line input voltage range with respect to GND . . . . . –2 V to 5.5 V
Line input voltage with respect to V_{ref} . . . . . ±5 V
Strobe input voltage . . . . . 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Unless otherwise specified, voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
P	1000 mW	8.0 mW/°C	640 mW
PS	450 mW	3.6 mW/°C	288 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Reference input voltage, V_{ref}	1.5		3.5	V
High-level line input voltage, $V_{IH(L)}$	V_{ref}+0.1		V_{CC}–1	V
Low-level line input voltage, $V_{IL(L)}$	0		V_{ref}–0.1	V
High-level strobe input voltage, $V_{IH(S)}$	2		5.5	V
Low-level strobe input voltage, $V_{IL(S)}$	0		0.8	V
Operating free-air temperature range, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ±10%, V_{ref} = 1.5 V to 3.5 V (unless otherwise noted)

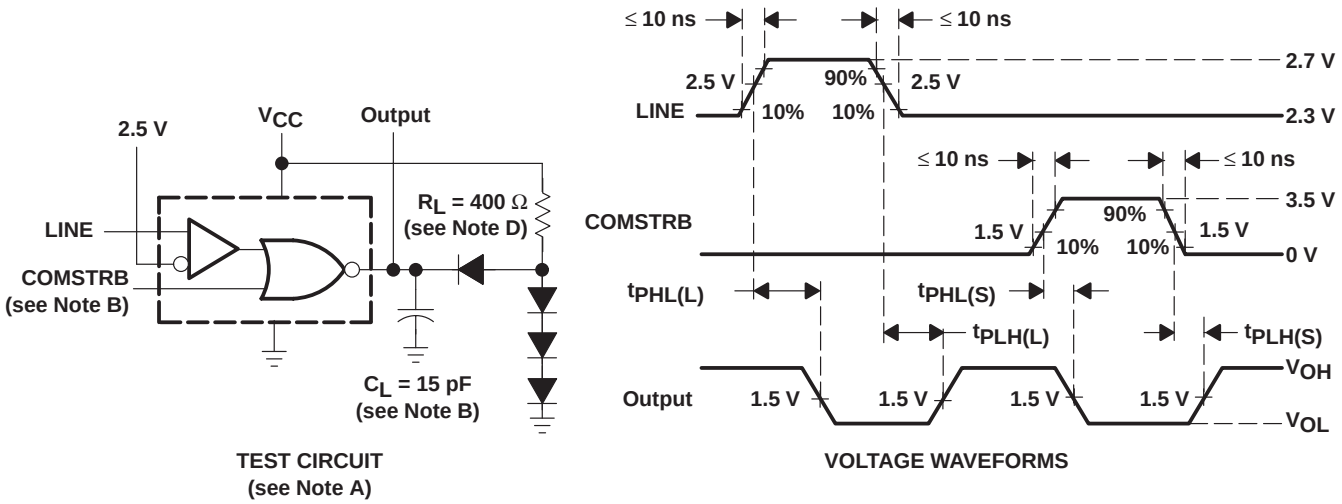
PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Strobe input clamp voltage		$I_{I(S)}$ = –12 mA					–1.5	V
V_{OH}	High-level output voltage		$V_{IL(L)}$ = V_{ref} – 100 mV,	$V_{IL(S)}$ = 0.8 V,	I_{OH} = –400 µA	2.4			V
V_{OL}	Low-level output voltage		$V_{IH(L)}$ = V_{ref} + 100 mV,	$V_{IL(S)}$ = 0.8 V,	I_{OL} = 16 mA			0.4	V
			$V_{IL(L)}$ = V_{ref} – 100 mV,	$V_{IH(S)}$ = 2 V,	I_{OL} = 16 mA			0.4	
$I_{I(S)}$	Strobe input current at maximum input voltage	Strobe	$V_{I(S)}$ = 5.5 V					1	mA
		COMSTRB						2	
I_{IH}	High-level input current	Strobe	$V_{I(S)}$ = 2.4 V					40	µA
		COMSTRB						80	
		LINE	$V_{I(L)}$ = 3.5 V,	V_{ref} = 1.5 V			35	100	
		Reference	$V_{I(L)}$ = 0,	V_{ref} = 3.5 V			35	100	
		COMREF					70	200	
I_{IL}	Low-level input current	Strobe	$V_{I(S)}$ = 0.4 V					–1.6	mA
		COMSTRB						–3.2	
		LINE	$V_{I(L)}$ = 0,	V_{ref} = 1.5 V				–10	µA
		Reference	$V_{I(L)}$ = 1.5 V,	V_{ref} = 0				–10	
		COMREF						–20	
I_{OS}	Short-circuit output current‡		V_{CC} = 5.5 V			–18		–55	mA
I_{CCH}	Supply current, output high		$V_{I(S)}$ = 0,	$V_{I(L)}$ = V_{ref} – 100 mV			18	30	mA
I_{CCL}	Supply current, output low		$V_{I(S)}$ = 0,	$V_{I(L)}$ = V_{ref} + 100 mV			20	35	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Only one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, V_{ref} = 2.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(L)}$	Propagation delay time, low- to high-level output from LINE	C_L = 15 pF, R_L = 400 kΩ, See Figure 1		22	35	ns
$t_{PHL(L)}$	Propagation delay time, high- to low-level output from LINE	C_L = 15 pF, R_L = 400 kΩ, See Figure 1		22	30	ns
$t_{PLH(S)}$	Propagation delay time, low- to high-level output from COMSTRB	C_L = 15 pF, R_L = 400 kΩ, See Figure 1		12	22	ns
$t_{PHL(S)}$	Propagation delay time, high- to low-level output from COMSTRB	C_L = 15 pF, R_L = 400 kΩ, See Figure 1		8	15	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_O = 50 Ω.
B. Unused strobes are to be grounded.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N3064.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

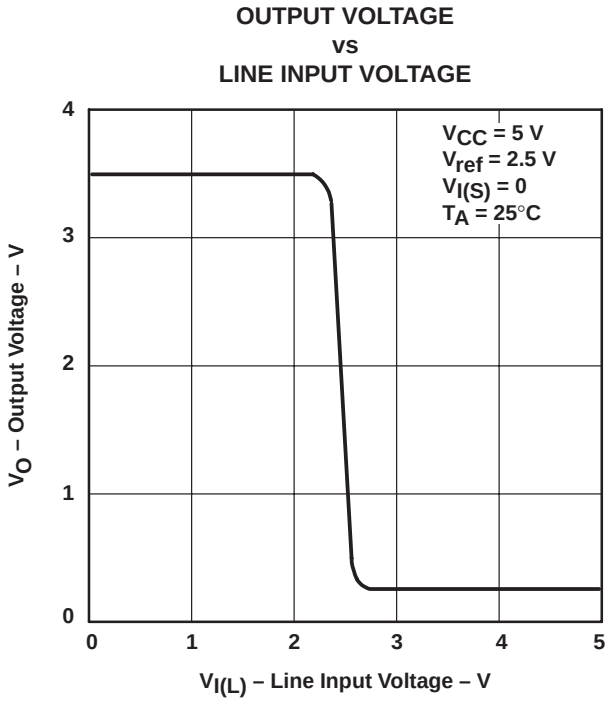


Figure 2

APPLICATION INFORMATION

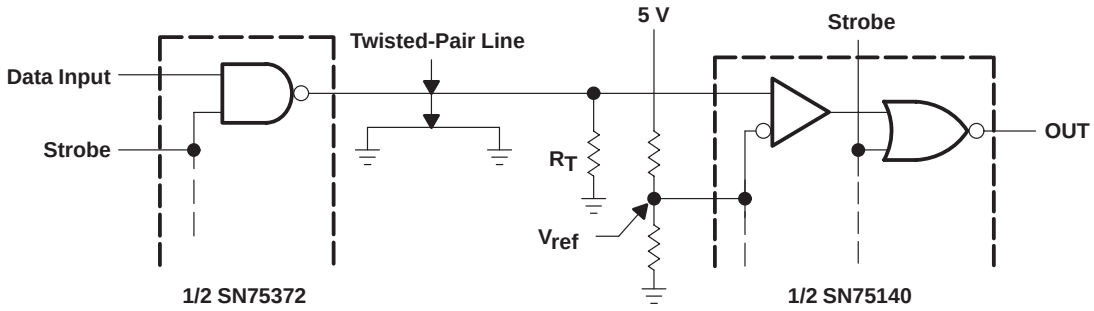
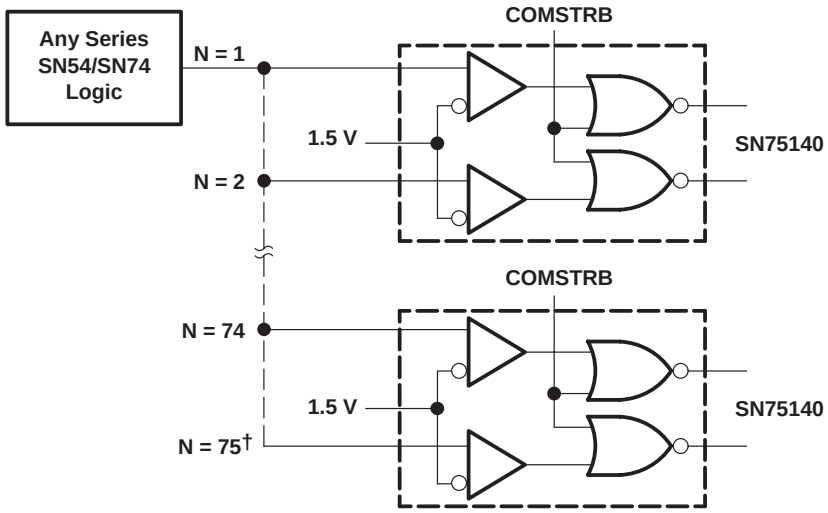


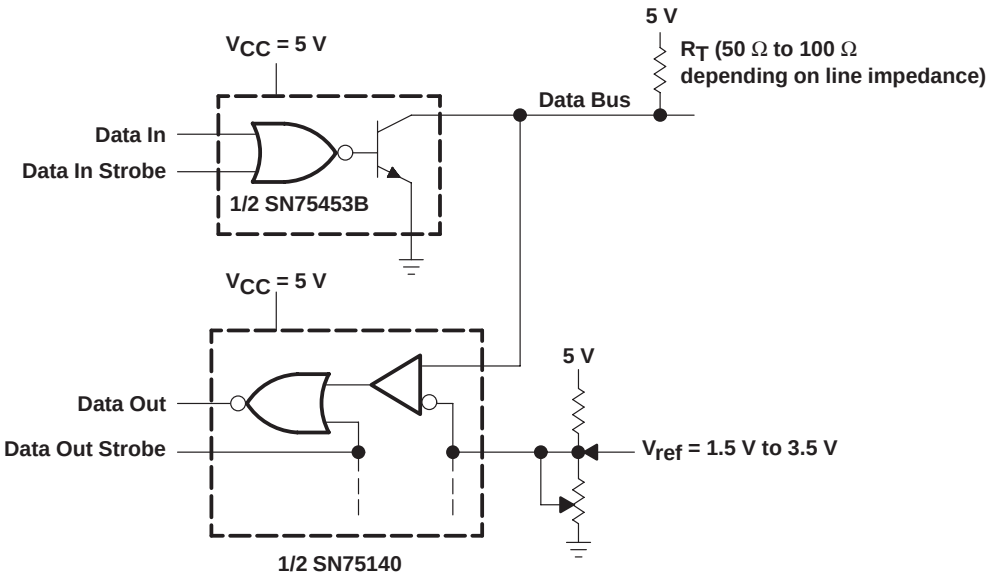
Figure 3. Line Receiver



† Although most series SN54/SN74 circuits have a >2.4-V output at 400 μA, they typically are capable of maintaining a >2.4-V output level under a load of 7.5 mA.

Figure 4. High Fanout From Standard TTL Gate

APPLICATION INFORMATION



NOTE A: Using this arrangement, as many as 100 transceivers can be connected to a single data bus. The adjustable reference-voltage feature allows the noise margin to be optimized for a given system. The complete dual bus transceiver (SN75453B driver and SN75140 receiver) can be assembled in approximately the same space required by a single 16-pin package and only one power supply is required (5 V). Data in and data out are TTL compatible.

Figure 5. Dual Bus Transceiver

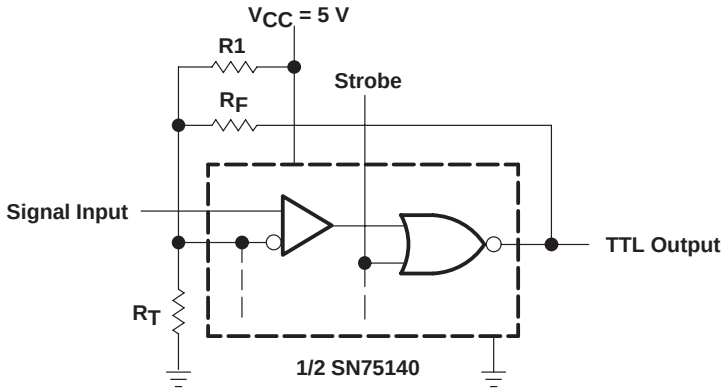
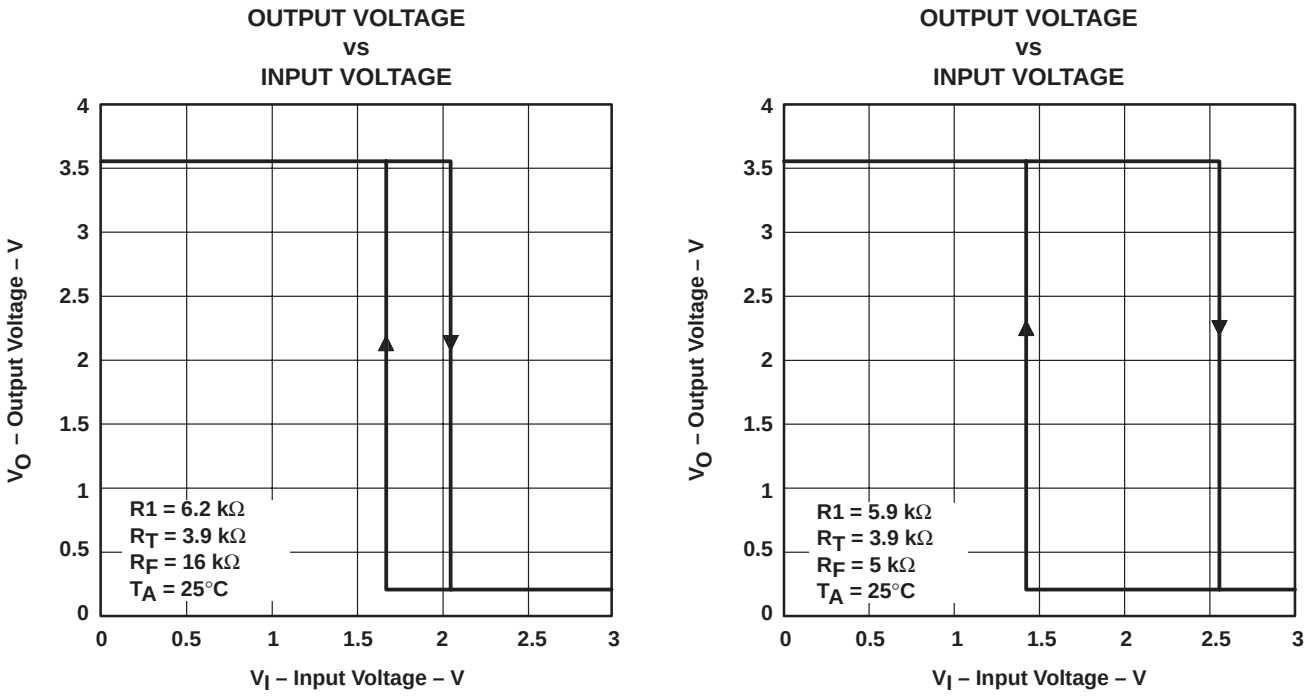


Figure 6. Schmitt Trigger

APPLICATION INFORMATION



NOTE A: Slowly changing input levels from data lines, optical detectors, and other types of transducers can be converted to standard TTL signals with this Schmitt-trigger circuit. R_1, R_F, and R_T can be adjusted for the desired hysteresis and trigger levels.

Figure 7. Examples of Transfer Characteristics

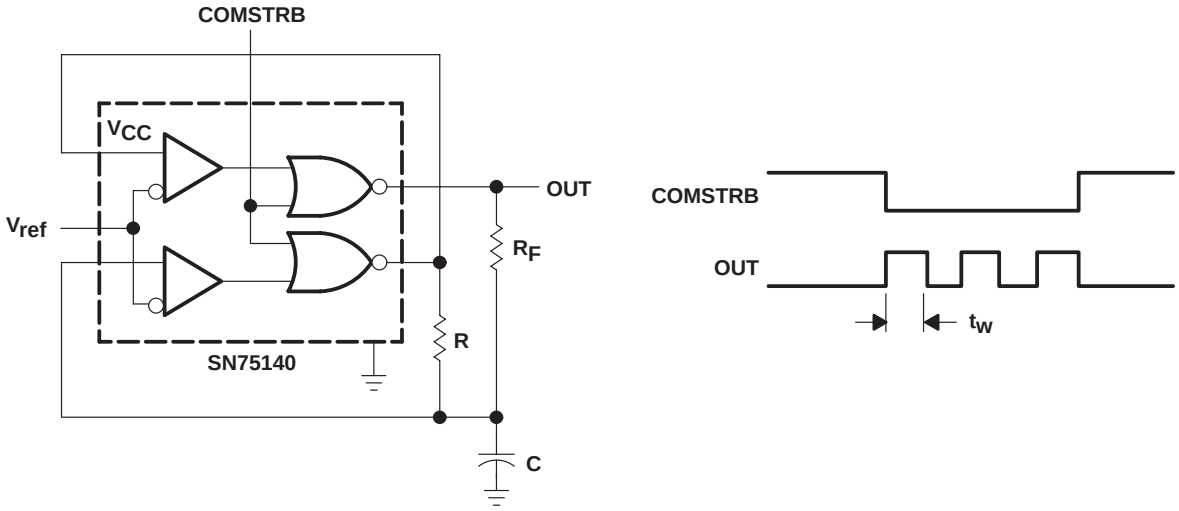


Figure 8. Gated Oscillator

APPLICATION INFORMATION

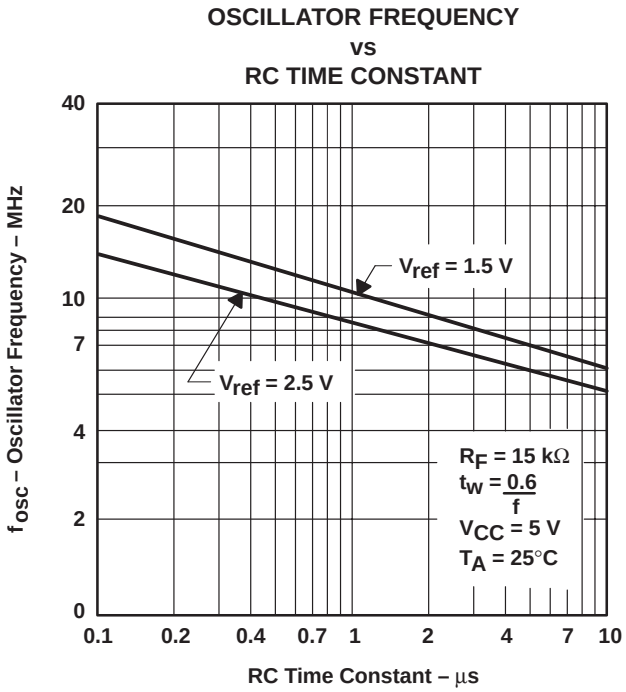


Figure 9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN75140D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	Samples Not Available
SN75140DR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	Samples Not Available
SN75140JG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	Samples Not Available
SN75140P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Contact TI Distributor or Sales Office
SN75140PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Contact TI Distributor or Sales Office
SN75140PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN75140PSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN75140PSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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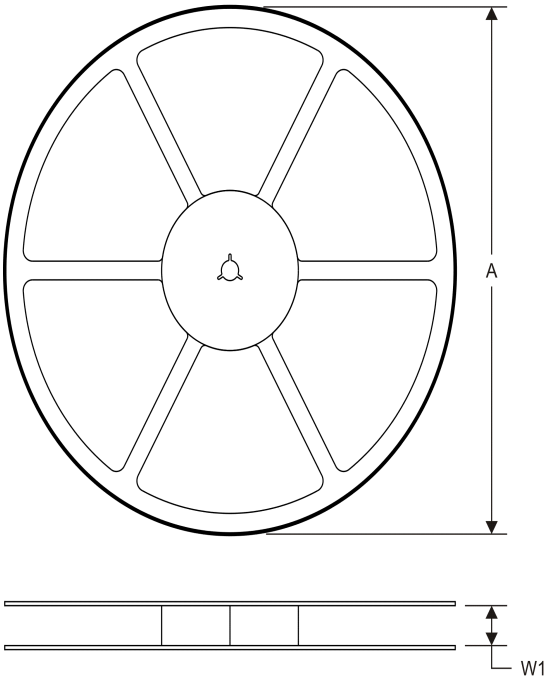
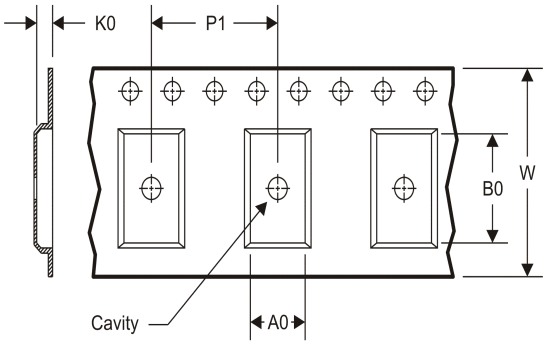
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



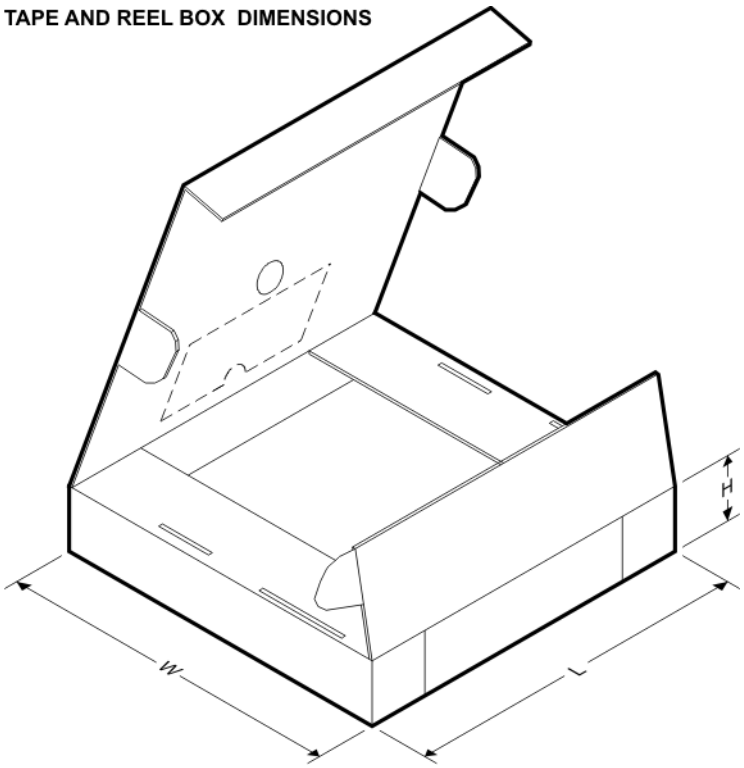
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75140PSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

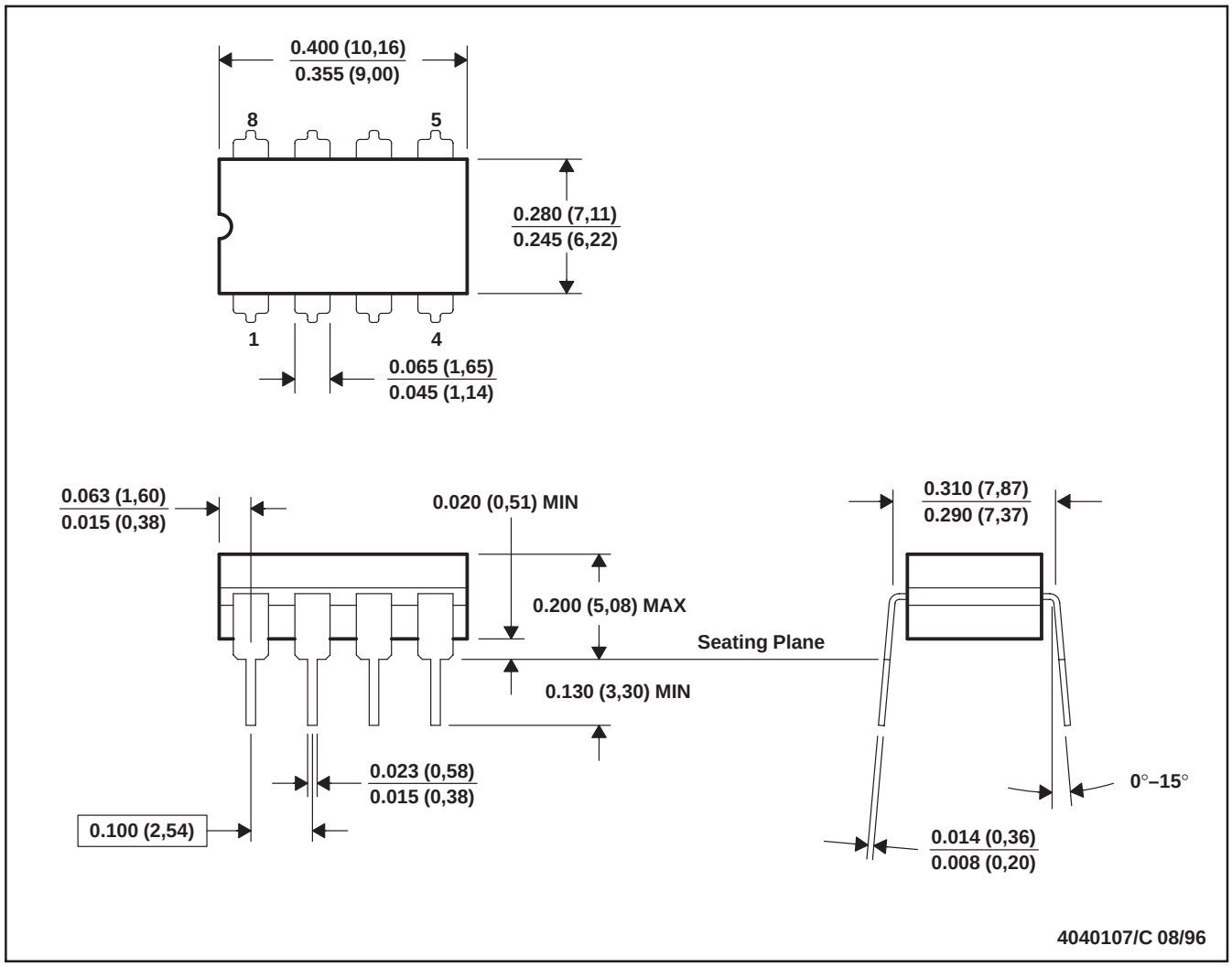


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75140PSR	SO	PS	8	2000	367.0	367.0	38.0

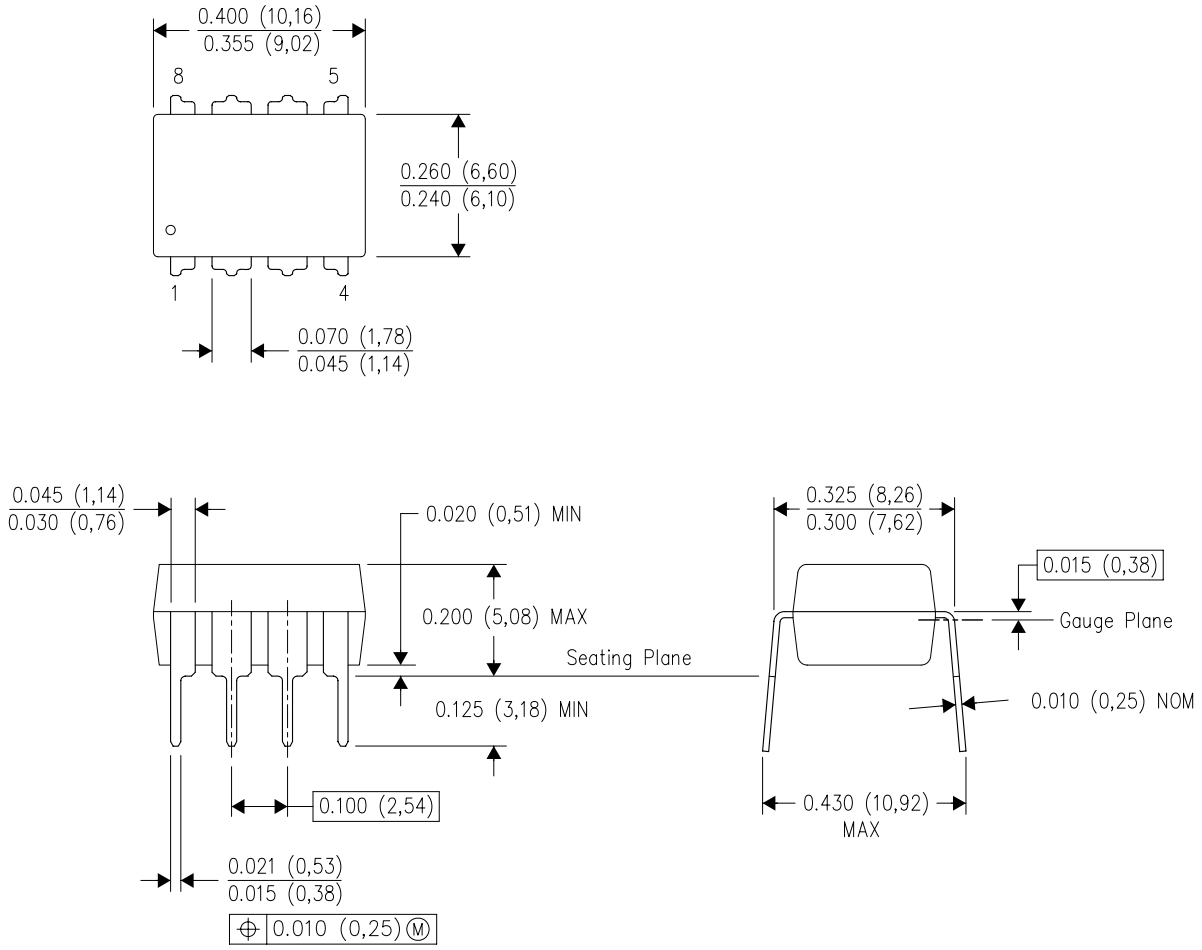
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



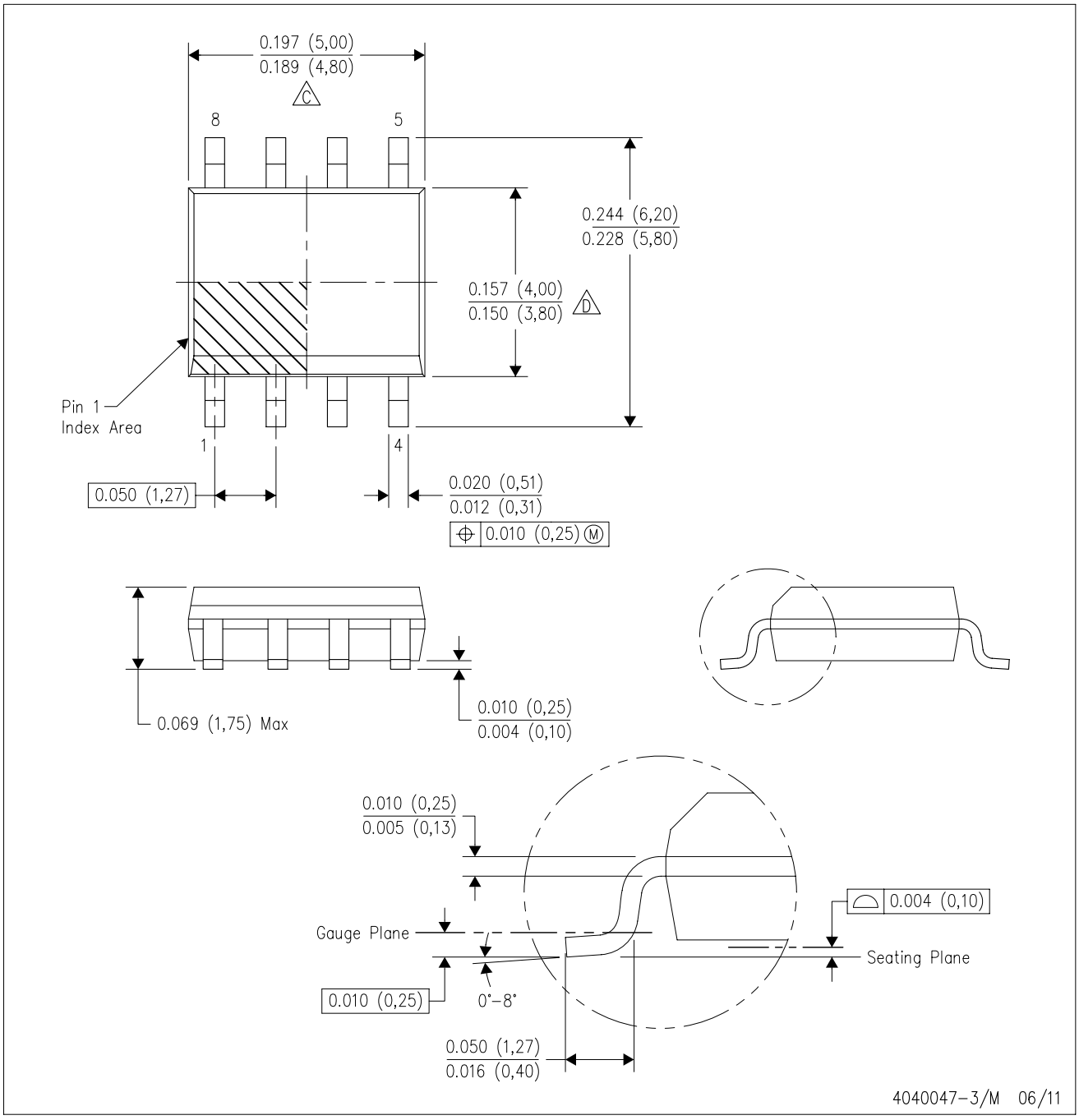
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

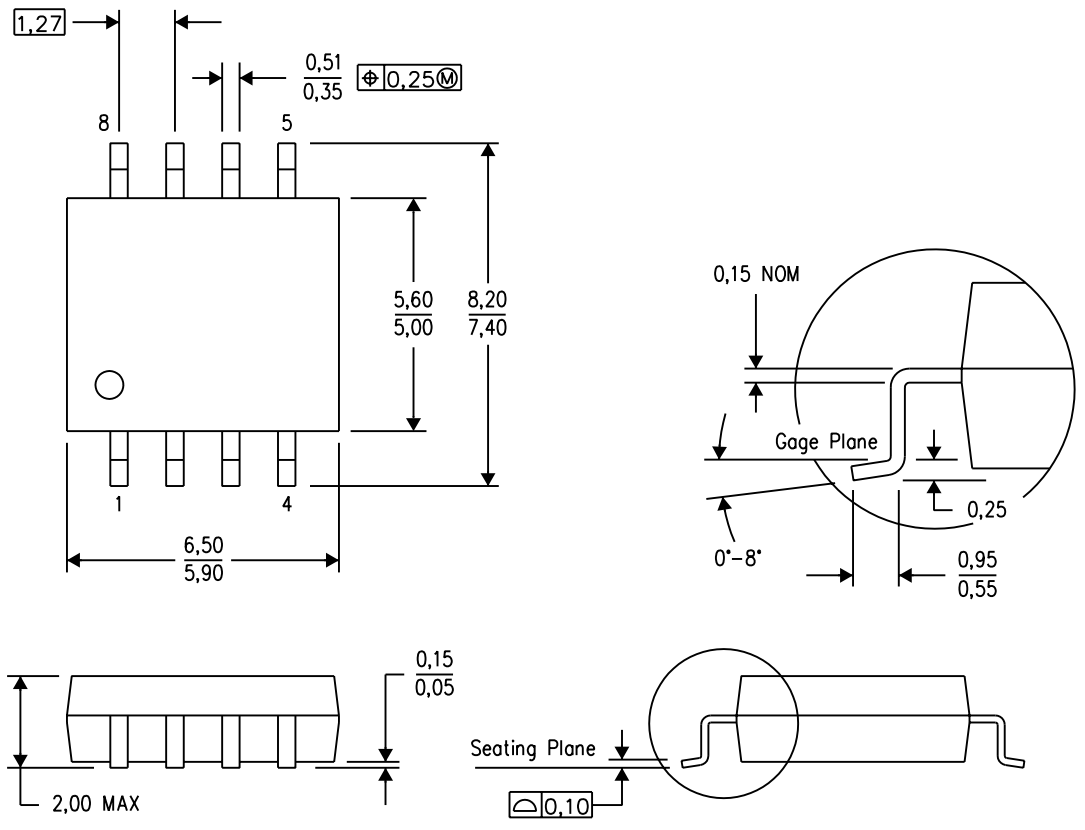
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

MECHANICAL DATA

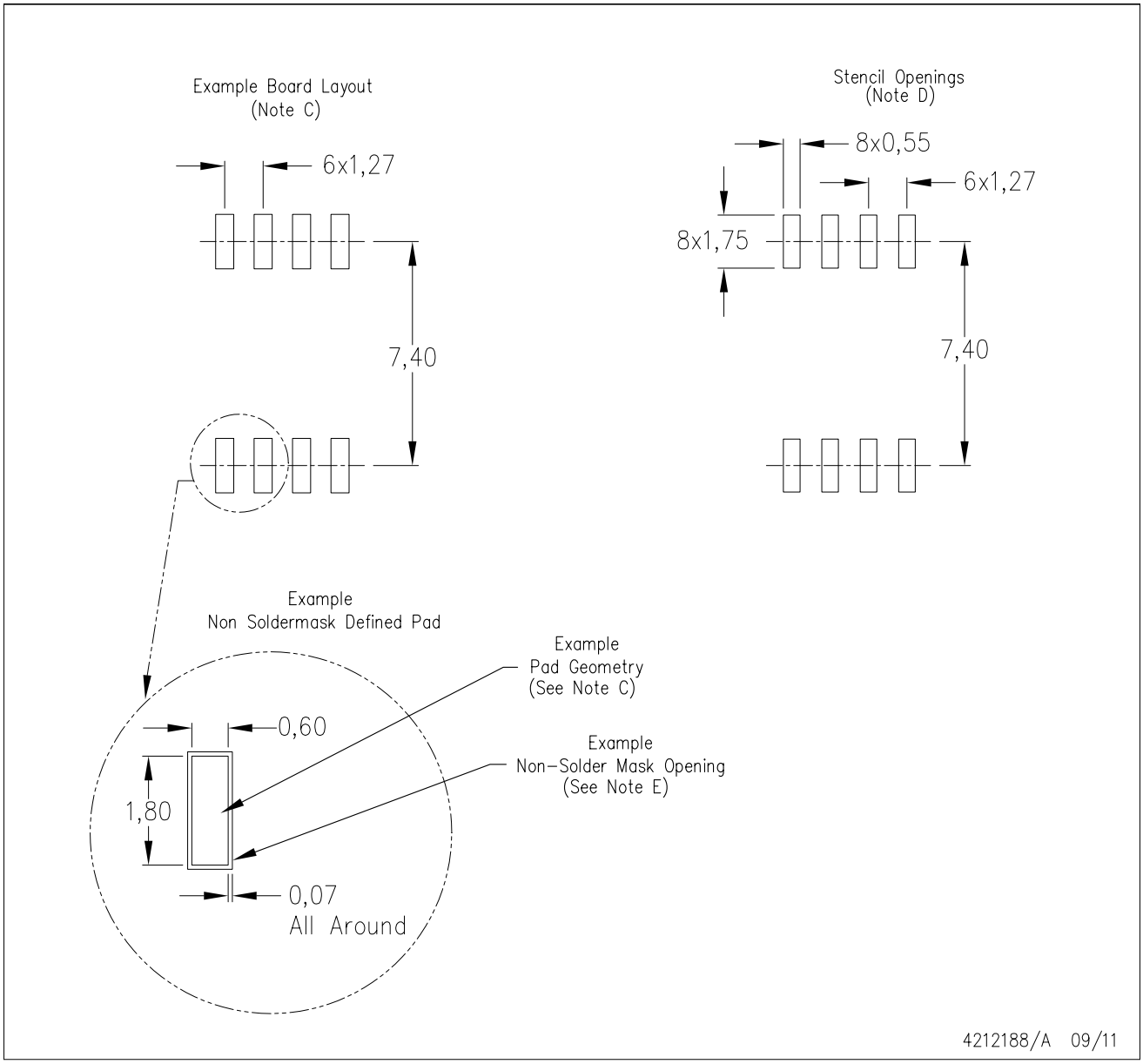
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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