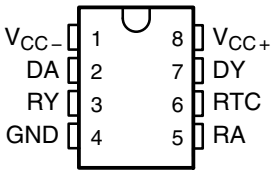
SLLS017C – JULY 1986 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI EIA/TIA-232-E and ITU Recommendation V.28**
- **10-mA Current Limited Output**
- **Wide Range of Supply Voltage**
  V_{CC} = 4.5 V to 15 V
- **Low Power . . . 130 mW**
- **Built-In 5-V Regulator**
- **Response Control Provides:**
  Input Threshold Shifting
  Input Noise Filtering
- **Power-Off Output Resistance . . . 300 Ω Typ**
- **Driver Input TTL Compatible**

D OR P PACKAGE
TOP VIEW

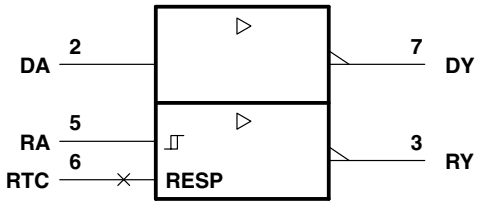


description

The SN75155 monolithic line driver and receiver is designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by ANSI EIA/TIA-232-E. A response control input is provided for the receiver. A resistor or a resistor and a bias voltage can be connected between the response control input and ground to provide noise filtering. The driver used is similar to the SN75188. The receiver used is similar to the SN75189A.

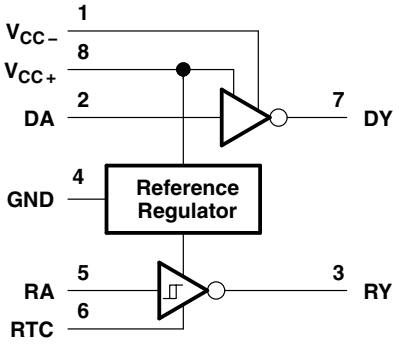
The SN75155 is characterized for operation from 0°C to 70°C.

logic symbol†

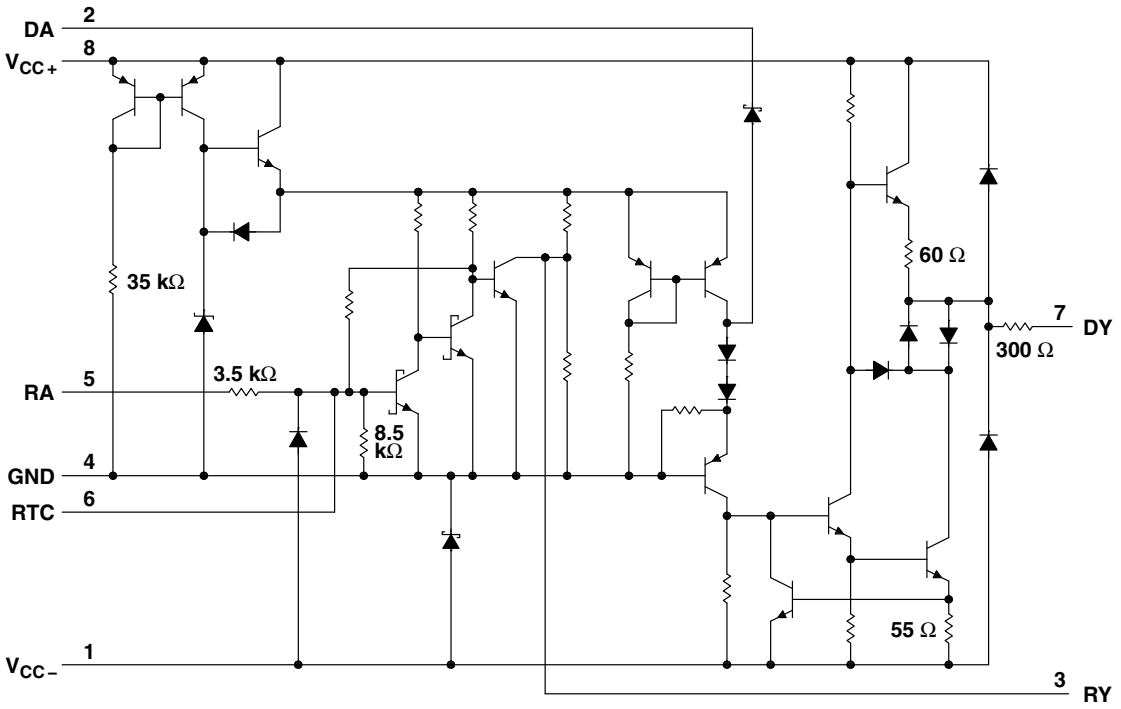


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

logic diagram



schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC-} (see Note 1) . . . . . –15 V
Input voltage range, V_I: Driver . . . . . –15 V to 15 V
Receiver . . . . . –30 V to 30 V
Output voltage range (driver), V_O . . . . . –15 V to 15 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	4.5	12	15	V
Supply voltage, V_{CC-}	−4.5	−12	−15	V
Output voltage, driver, $V_{O(D)}$			±15	V
Input voltage, receiver, $V_{I(R)}$	−25		25	V
High-level input voltage, driver, V_{IH}	2			V
Low-level input voltage, driver, V_{IL}			0.8	V
Response control current			±5.5	mA
Output current, receiver, $I_{O(R)}$			24	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

total device

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
I_{CCH+}	High-level supply current	V_{CC+} = 5 V,	V_{CC-} = −5 V	$V_{I(D)}$ = 2 V, $V_{I(R)}$ = 2.3 V, Output open		6.3	8.1	mA
		V_{CC+} = 9 V,	V_{CC-} = −9 V			9.1	11.9	
		V_{CC+} = 12 V,	V_{CC-} = −12 V			10.4	14	
I_{CCL+}	Low-level supply current	V_{CC+} = 5 V,	V_{CC-} = −5 V	$V_{I(D)}$ = 0.8 V, $V_{I(R)}$ = 0.6 V, Output open		2.5	3.4	mA
		V_{CC+} = 9 V,	V_{CC-} = −9 V			3.7	5.1	
		V_{CC+} = 12V,	V_{CC-} = −12 V			4.1	5.6	
I_{CC+}	Supply current	V_{CC+} = 5 V,	V_{CC-} = 0	$V_{I(R)}$ = 2.3 V, $V_{I(D)}$ = 0		4.8	6.4	mA
		V_{CC+} = 9 V,	V_{CC-} = 0			6.7	9.1	
I_{CCH-}	High-level supply current	V_{CC+} = 5 V,	V_{CC-} = −5 V	$V_{I(D)}$ = 2 V, $V_{I(R)}$ = 2.3 V Output open		−2.4	−3.1	mA
		V_{CC+} = 9 V,	V_{CC-} = −9 V			−3.9	−4.9	
		V_{CC+} = 12 V,	V_{CC-} = −12 V			−4.8	−6.1	
I_{CCL-}	Low-level supply current	V_{CC+} = 5 V,	V_{CC-} = −5 V	$V_{I(D)}$ = 0.8 V, $V_{I(R)}$ = 0.6 V, Output open		−0.2	−0.35	mA
		V_{CC+} = 9 V,	V_{CC-} = −9 V			−0.25	−0.4	
		V_{CC+} = 12 V,	V_{CC-} = −12 V			−0.27	−0.45	

† All typical values are at T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 12 V, V_{CC-} = −12 V (unless otherwise noted)

driver section

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, R_L = 3 kΩ	V_{CC+} = 5 V,	V_{CC-} = −5 V	3.2	3.7		V
			V_{CC+} = 9 V,	V_{CC-} = −9 V	6.5	7.2		
			V_{CC+} = 12 V,	V_{CC-} = −12 V	8.9	9.8		
V_{OL}	Low-level output voltage (see Note 2)	V_{IH} = 2 V, R_L = 3 kΩ	V_{CC+} = 5 V,	V_{CC-} = −5 V		−3.6	−3.2	V
			V_{CC+} = 9 V,	V_{CC-} = −9 V		−7.1	−6.4	
			V_{CC+} = 12 V,	V_{CC-} = −12 V		−9.7	−8.8	
I_{IH}	High-level input current	V_I = 7 V					5	μA
I_{IL}	Low-level input current	V_I = 0				−0.73	−1.2	mA
$I_{OS(H)}$	High-level short-circuit output current	V_I = 0.8 V, V_O = 0			−7	−12	−14.5	mA
$I_{OS(L)}$	Low-level short-circuit output current	V_I = 2 V, V_O = 0			6.5	11.5	15	mA
r_O	Output resistance with power off	V_O = −2 V to 2 V				300		Ω

receiver section (see Figure 1)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshhold voltage				1.2	1.9	2.3	V
V_{IT-}	Negative-going input threshhold voltage				0.6	0.95	1.2	V
V_{hys}	Hystresis voltage ($V_{IT+} - V_{IT-}$)				0.6			V
$V_{O(H)}$	High-level output voltage	V_I = 0.6 V, I_{OH} = 10 μA	V_{CC+} = 5 V,	V_{CC-} = −5 V	3.7	4.1	4.5	V
			V_{CC+} = 12 V,	V_{CC-} = −12 V	4.4	4.7	5.2	
		V_I = 0.6 V, I_{OH} = 0.4 mA	V_{CC+} = 5 V,	V_{CC-} = −5 V	3.1	3.4	3.8	
			V_{CC+} = 12 V,	V_{CC-} = −12 V	3.6	4	4.5	
$V_{O(L)}$	Low-level output voltage	V_I = 2.3 V,	I_{OL} = 24 mA			0.2	0.3	V
I_{IH}	High-level input current	V_I = 2 5 V			3.6	6.7	10	mA
		V_I = 3 V			0.43	0.67	1	mA
I_{IL}	Low-level input current	V_I = −25 V			−3.6	−6.7	−10	mA
		V_I = −3 V			−0.43	−0.67	−1	mA
I_{OS}	Short-circuit output current	V_I = 0.6 V				−2.8	−3.7	mA

† All typical values are at T_A = 25°C.

NOTE 2: The algebraic limit system, in which the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic voltage levels only (e.g., if −8.8 V is the maximum, the typical value is a more negative value).

switching characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = – 5 V, C_L = 50 pF (unless otherwise noted)

driver section (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high level output	R_L = 3 kΩ		250	480	ns
t_{PHL}	Propagation delay time, high- to low level output			80	150	
t_r	Output rise time	R_L = 3 kΩ		67	180	ns
		R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF		2.4	3	µs
t_f	Output fall time	R_L = 3 kΩ		48	160	ns
		R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF		1.9	3	µs

receiver section (see Figure 3)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high level output	R_L = 400 Ω		175	245	ns
t_{PHL}	Propagation delay time, high- to low level output			37	100	
t_r	Output rise time	R_L = 400 Ω		255	360	ns
t_f	Output fall time	R_L = 400 Ω		23	50	ns

† All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

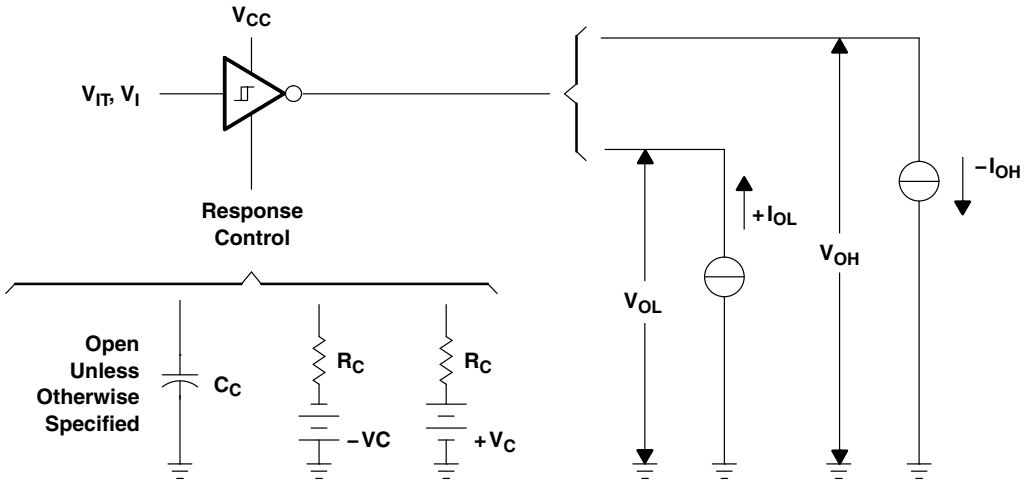
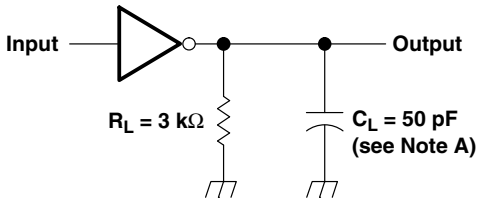
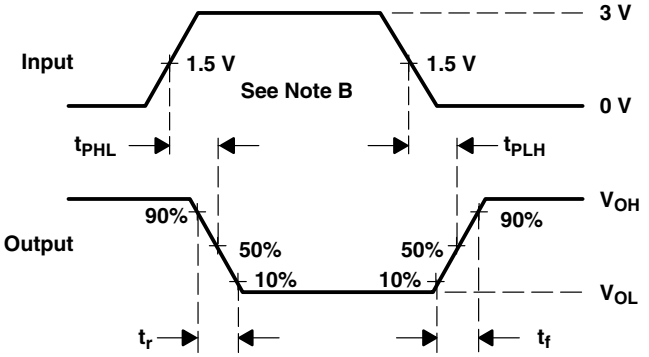


Figure 1. Receiver Section Test Circuit (V_{IT+}, V_{IT-}, V_{OH}, V_{OL})

PARAMETER MEASUREMENT INFORMATION



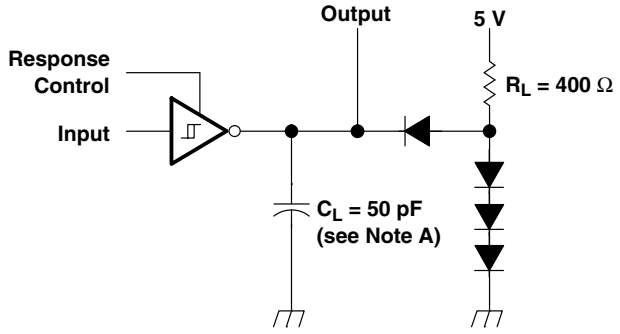
TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input waveform is supplied by a generator with the following characteristics: Z_O = 50 Ω, t_w = 1 μs, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 2. Driver Section Switching Test Circuit and Voltage Waveforms



TEST CIRCUIT

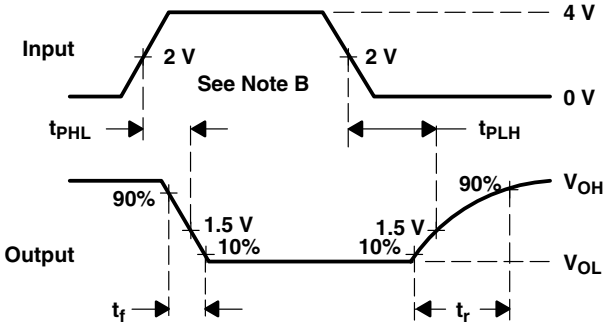


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Figure 3. Receiver Section Switching Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

DRIVER
VOLTAGE TRANSFER CHARACTERISTICS

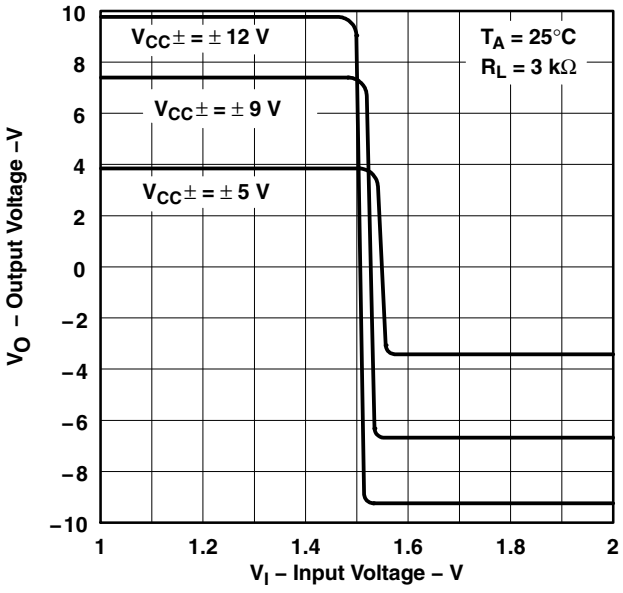


Figure 4

DRIVER
OUTPUT CURRENT
vs
OUTPUT VOLTAGE

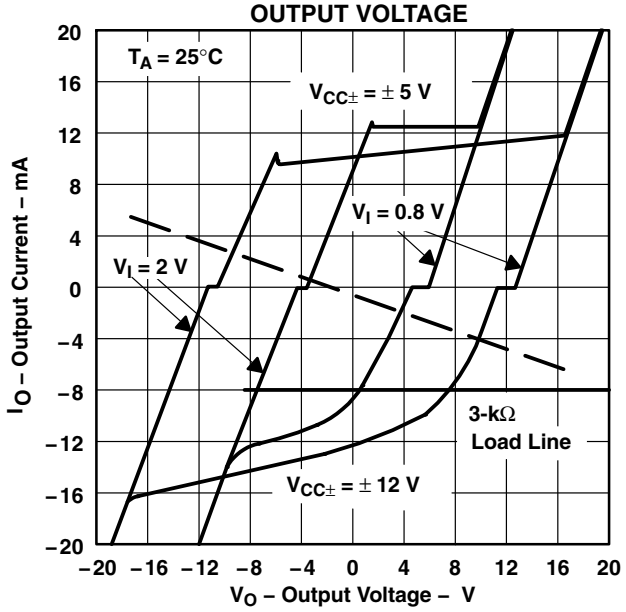


Figure 5

DRIVER
SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

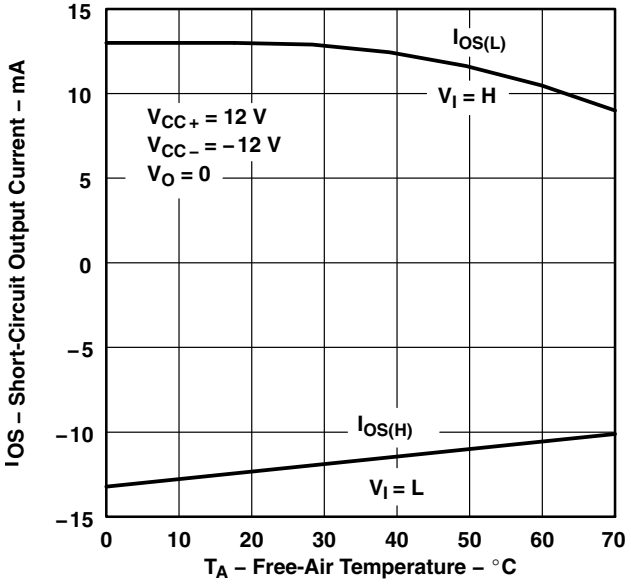


Figure 6

DRIVER
SLEW RATE
vs
LOAD CAPACITANCE

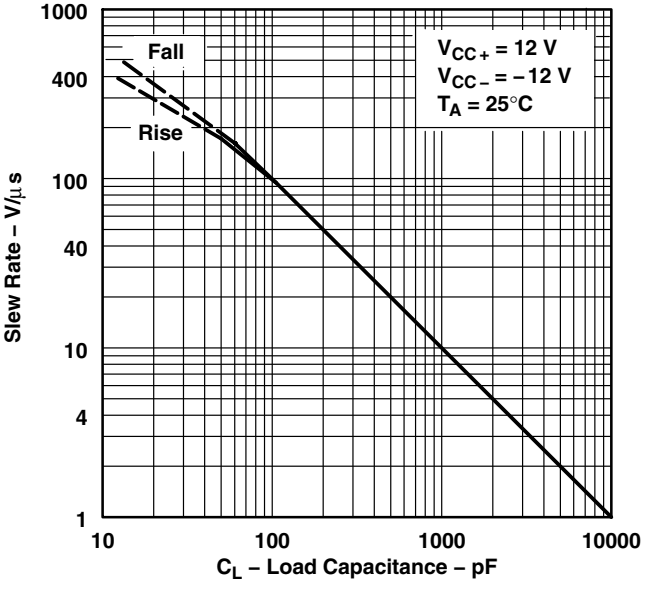


Figure 7

TYPICAL CHARACTERISTICS

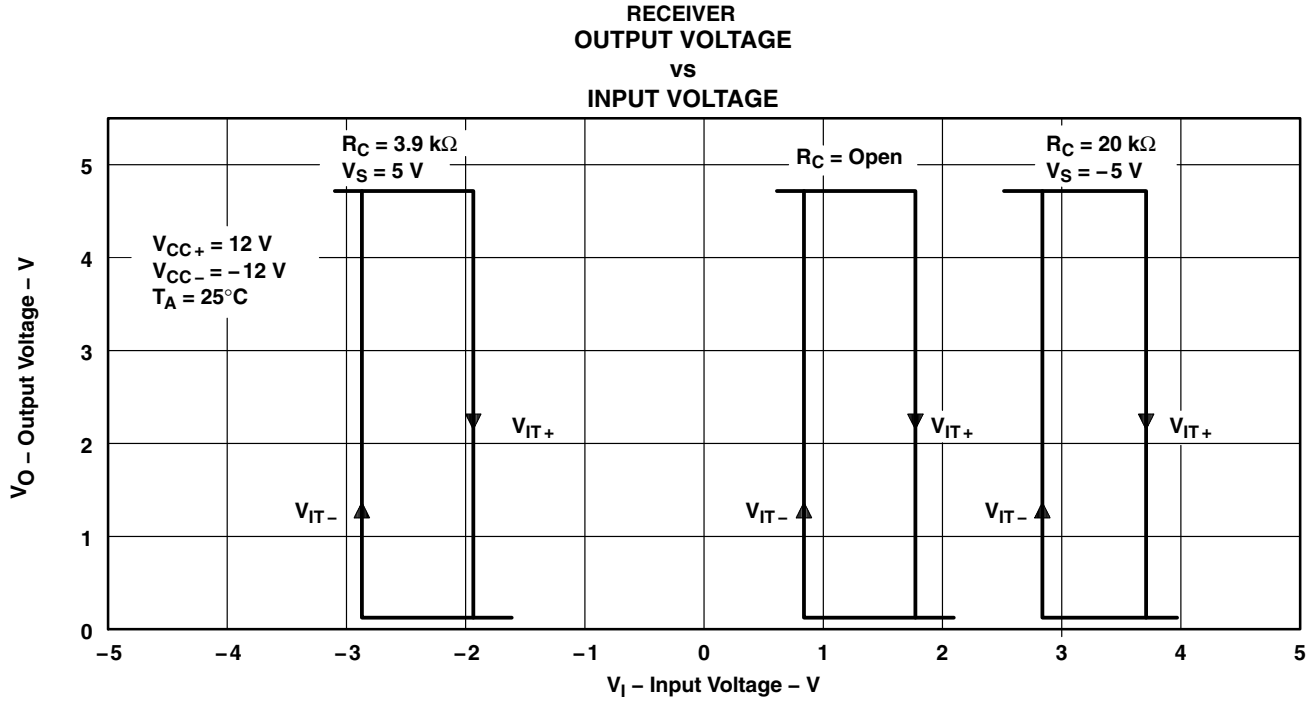


Figure 8

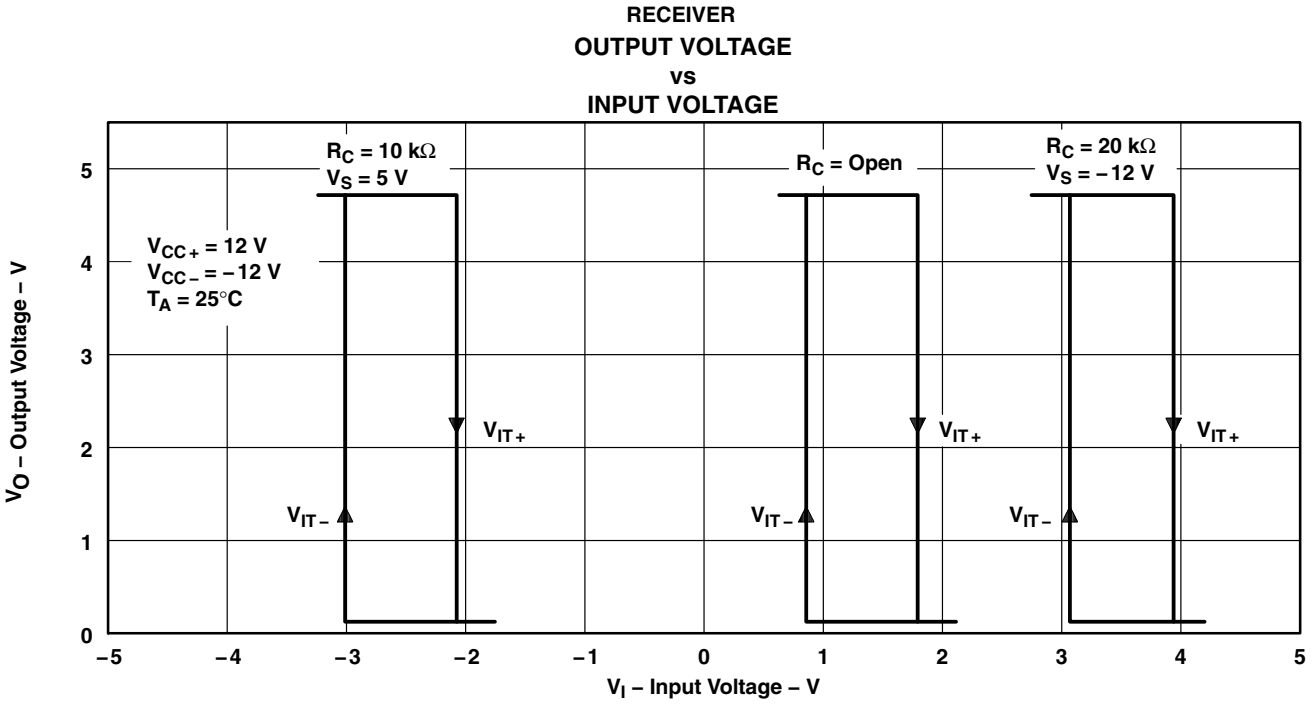


Figure 9

TYPICAL CHARACTERISTICS

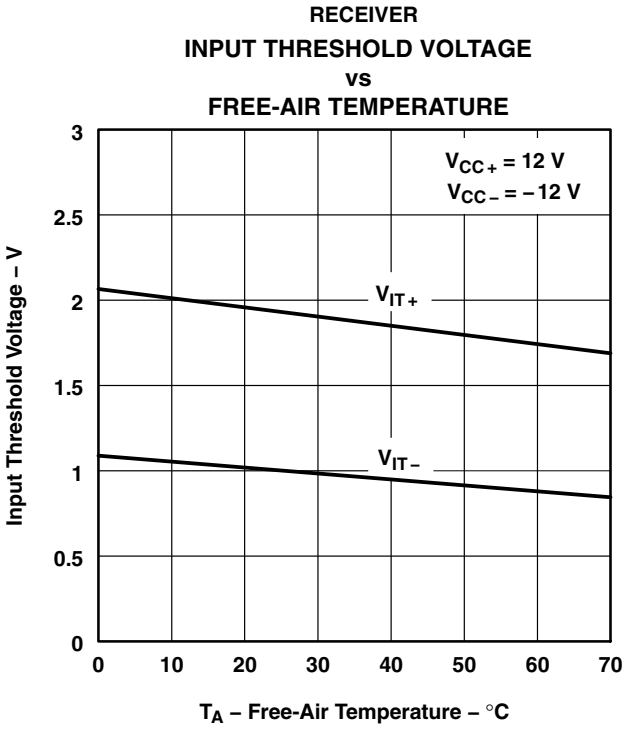


Figure 10

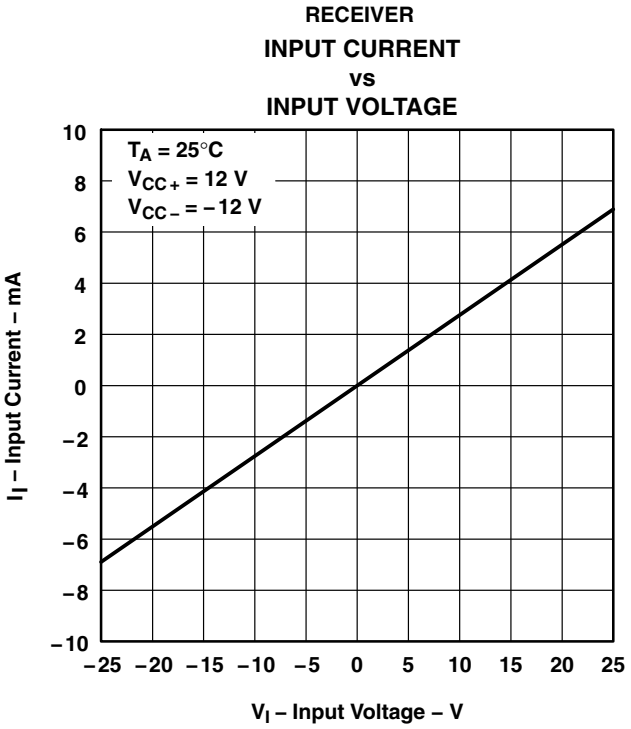


Figure 11

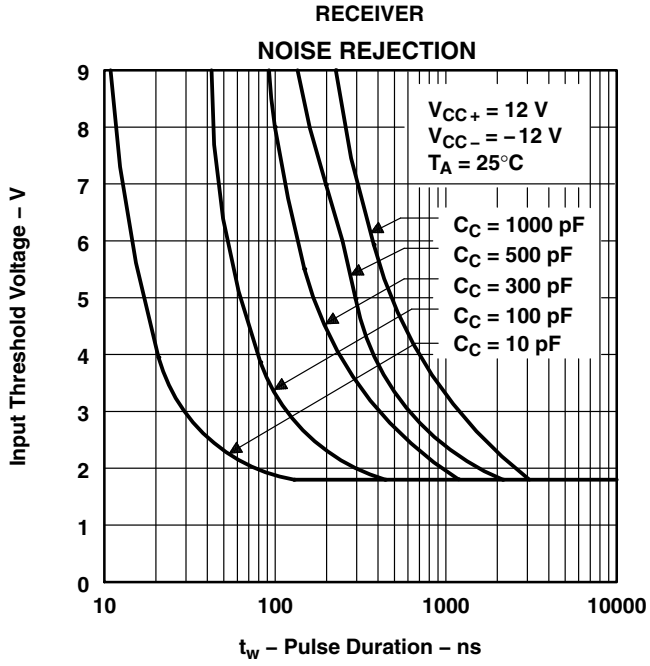


Figure 12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN75155D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75155DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75155DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75155DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75155DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75155DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75155P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75155PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

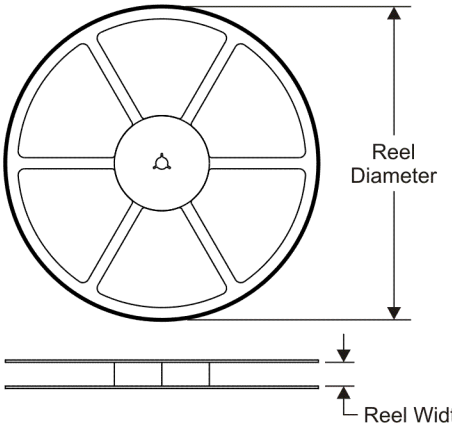
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

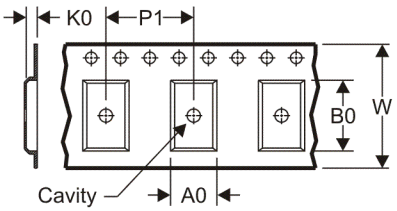
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

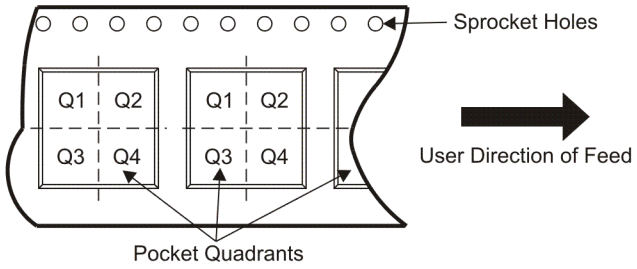


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

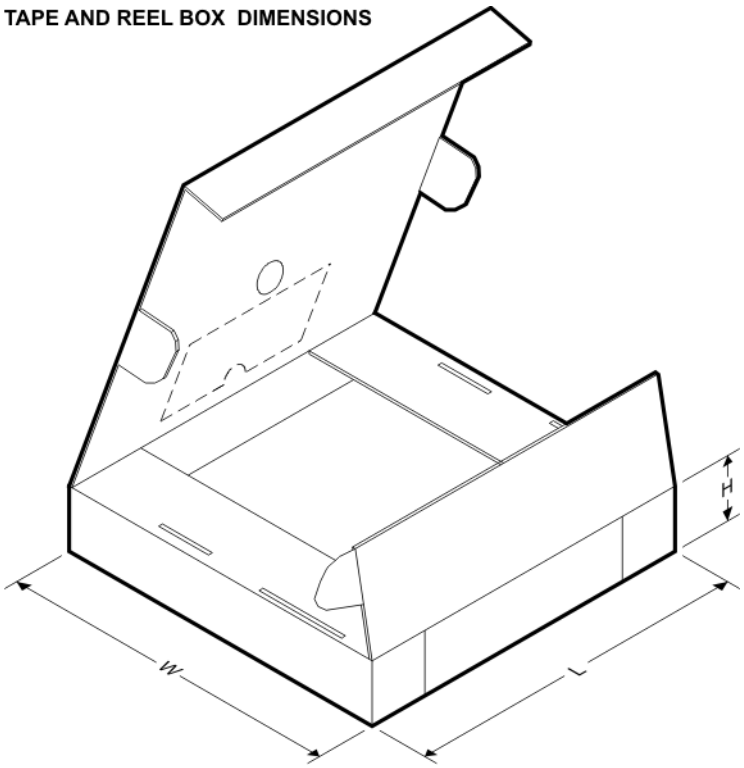
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75155DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

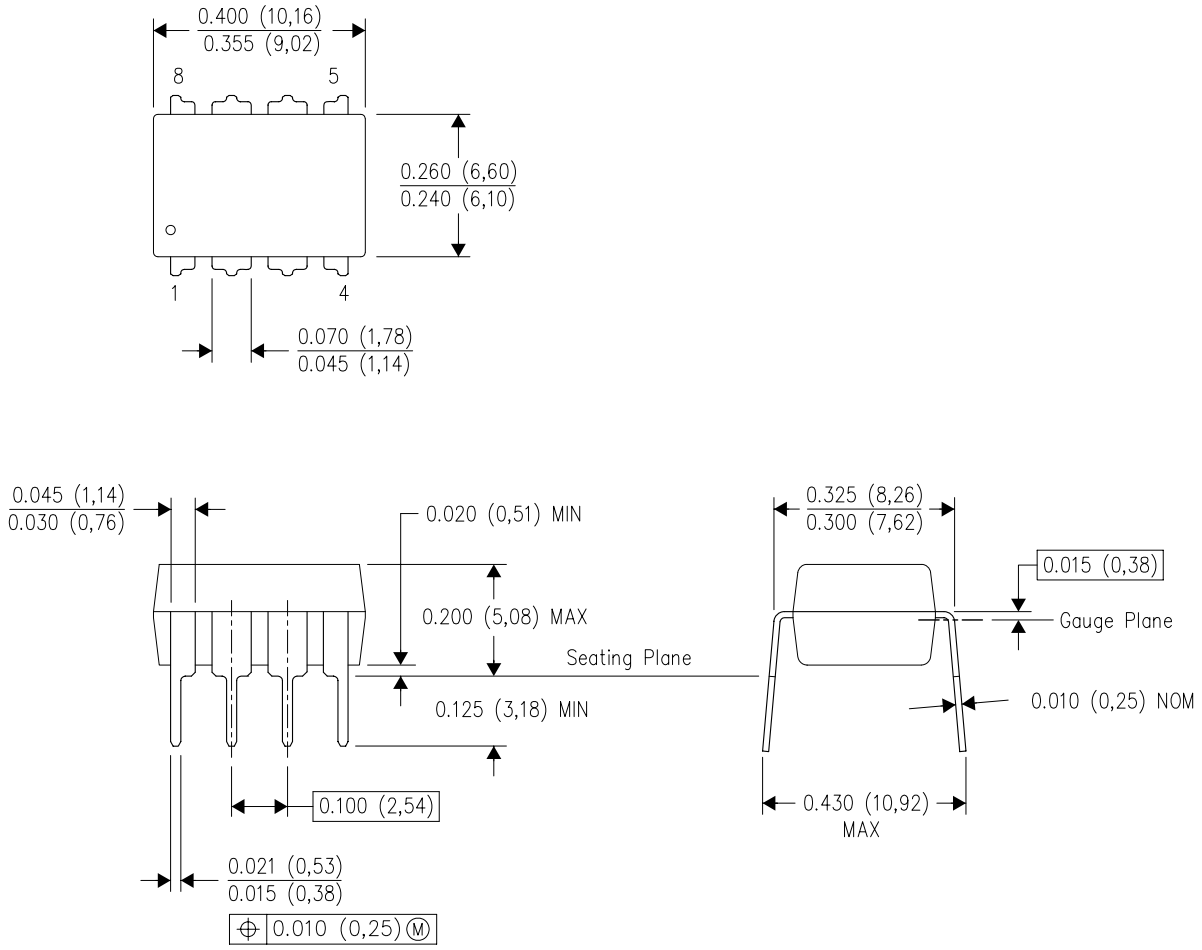
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

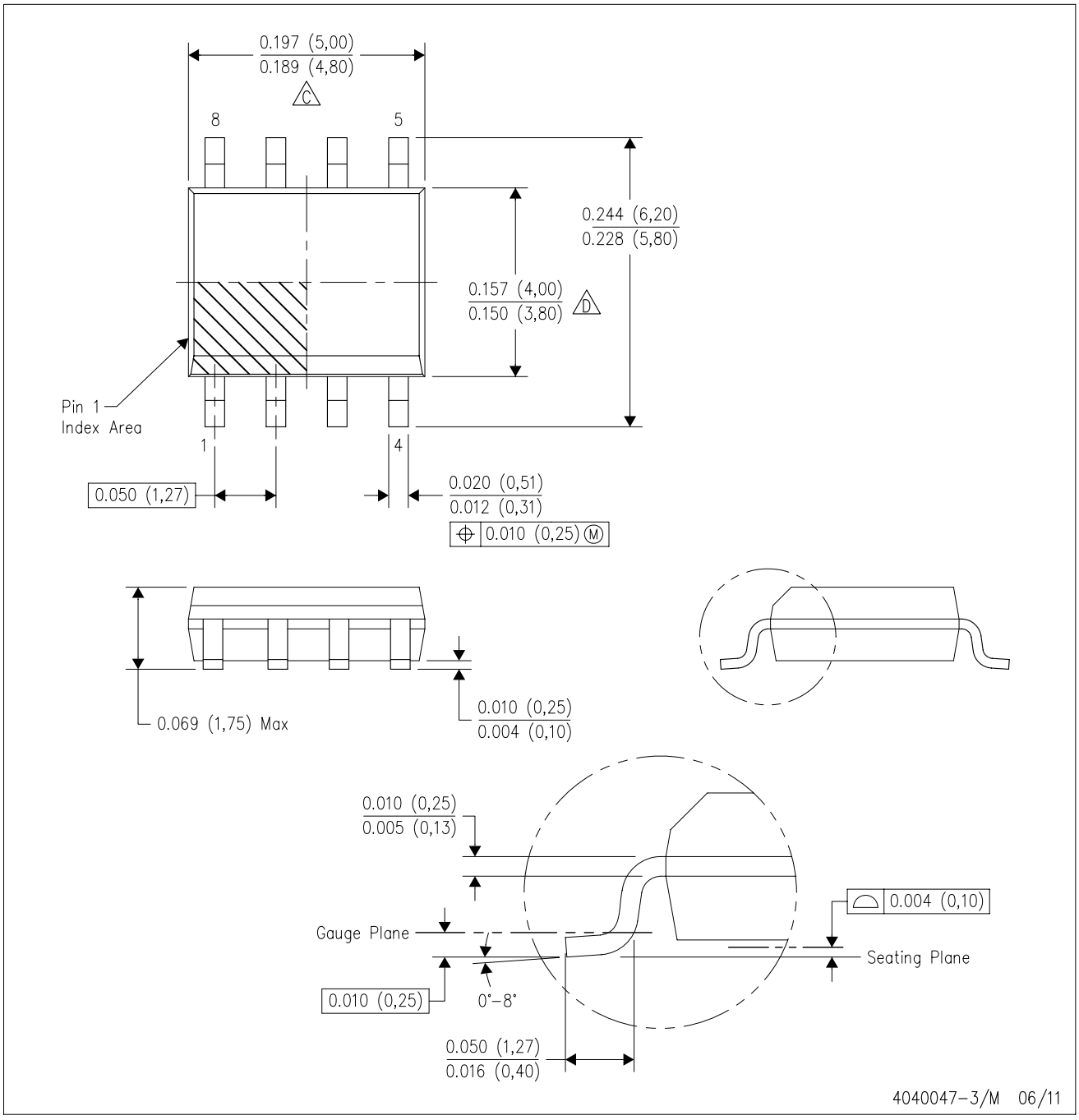
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75155DR	SOIC	D	8	2500	340.5	338.1	20.6

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



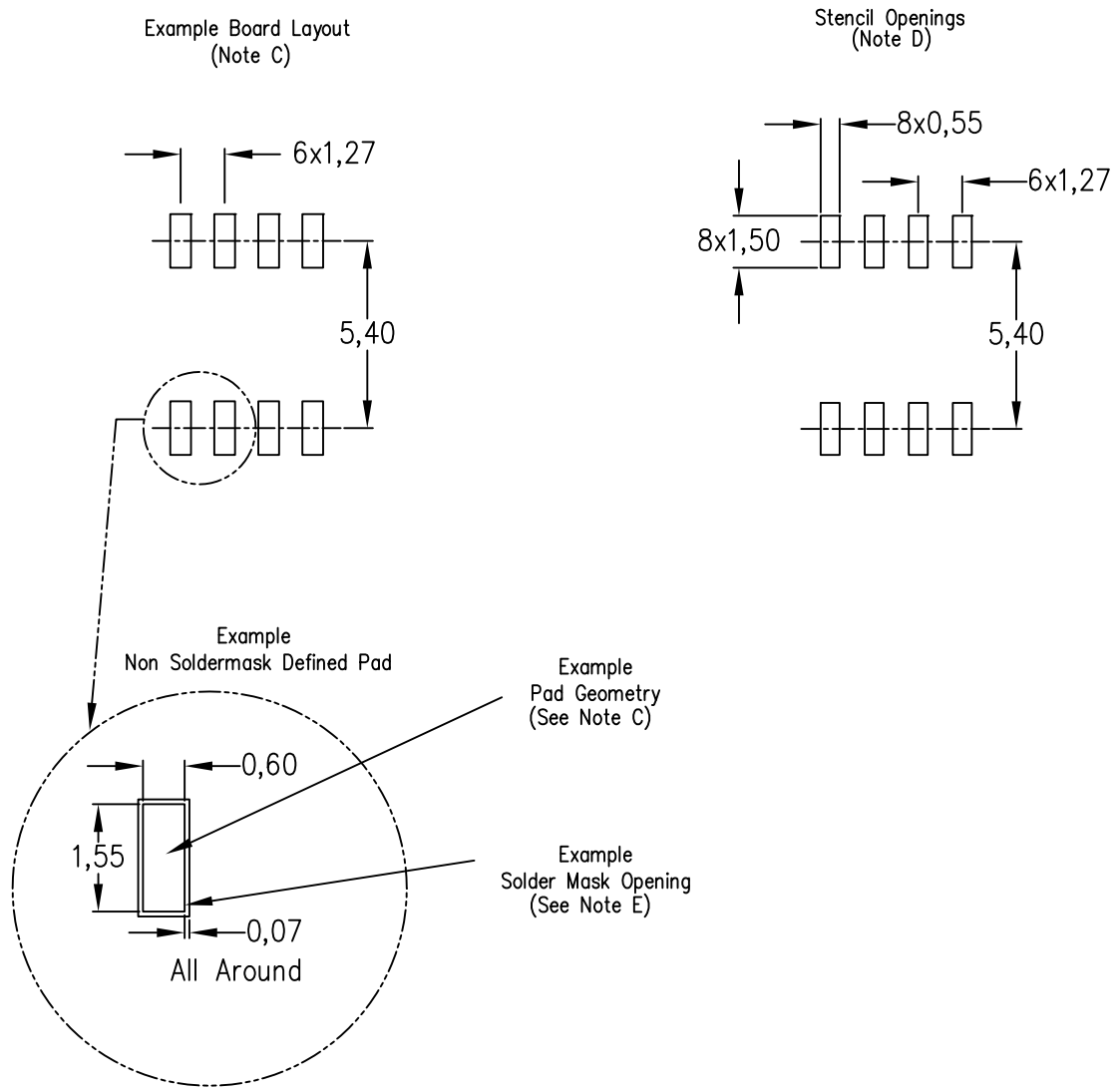
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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