- **Single 5-V Supply**
- **Differential Line Operation**
- **Dual Channels**
- **TTL Compatibility**
- **Short-Circuit Protection of Outputs**
- **Output Clamp Diodes to Terminate Line Transients**
- **High-Current Outputs**
- **Quad Inputs**
- **Single-Ended or Differential AND/NAND Outputs**
- **Designed for Use With Dual Differential Drivers SN55182 and SN75182**
- **Designed to Be Interchangeable With National Semiconductor DS7830 and DS8830**

**SN55183 . . . J OR W PACKAGE**
**SN75183 . . . D OR N PACKAGE**
**DS8830 . . . N PACKAGE**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| 1A | 1 | 14 | $V_{CC}$ |
| 1B | 2 | 13 | 2D |
| 1C | 3 | 12 | 2C |
| 1D | 4 | 11 | 2B |
| 1Y | 5 | 10 | 2A |
| 1Z | 6 | 9 | 2Y |
| GND | 7 | 8 | 2Z |

**SN55183 . . . FK PACKAGE**
**(TOP VIEW)**

Top pins: 1B(3) 1A(2) NC(1) $V_{CC}$(20) 2D(19)

| | | | |
|---|---|---|---|
| 1C | 4 | 18 | 2C |
| NC | 5 | 17 | NC |
| 1D | 6 | 16 | 2B |
| NC | 7 | 15 | NC |
| 1Y | 8 | 14 | 2A |

Bottom pins: 1Z(9) GND(10) NC(11) 2Z(12) 2Y(13)

NC – No internal connection

**THE DS8830 AND SN55183 ARE**
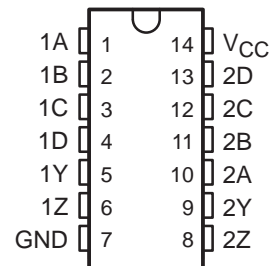**NOT RECOMMENDED FOR NEW DESIGNS**

## description

The DS8830, SN55183, and SN75183 dual differential line drivers are designed to provide differential output signals with high current capability for driving balanced lines, such as twisted pair, at normal line impedances without high power dissipation. These devices can be used as TTL expander/phase splitters, because the output stages are similar to TTL totem-pole outputs.
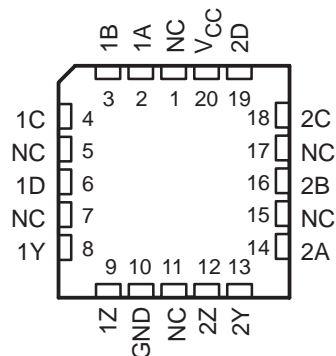
The driver is of monolithic single-chip construction, and both halves of the dual circuits use common power supply and ground terminals.

The SN55183 is characterized for operation over the full military temperature range of –55°C to 125°C. The DS8830 and SN75183 are characterized for operation from 0°C to 70°C.

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**TEXAS INSTRUMENTS**

# DS8830, SN55183, SN75183
# DUAL DIFFERENTIAL LINE DRIVERS

## logic symbol†

1A — 1
1B — 2
1C — 3
1D — 4

2A — 10
2B — 11
2C — 12
2D — 13

& ▷

5 — 1Y
6 — 1Z
9 — 2Y
8 — 2Z
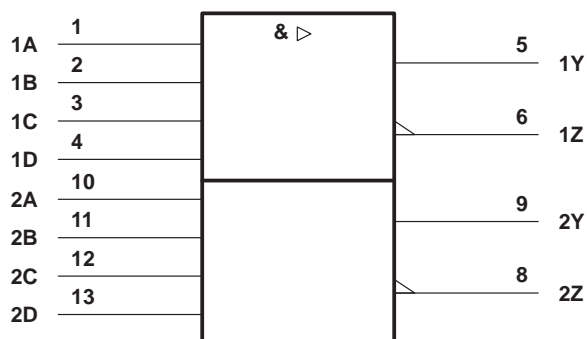
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

## logic diagram (positive logic)

1A — 1
1B — 2
1C — 3
1D — 4

5 — 1Y
6 — 1Z

2A — 10
2B — 11
2C — 12
2D — 13

9 — 2Y
8 — 2Z
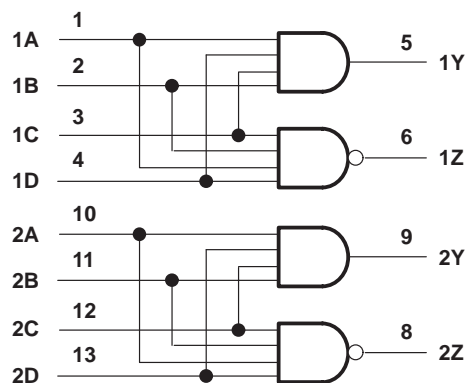
**Positive logic: y = ABCD, Z = $\overline{ABCD}$**

Pin numbers shown are for the D, J, N, and W packages.

## schematic (each driver)
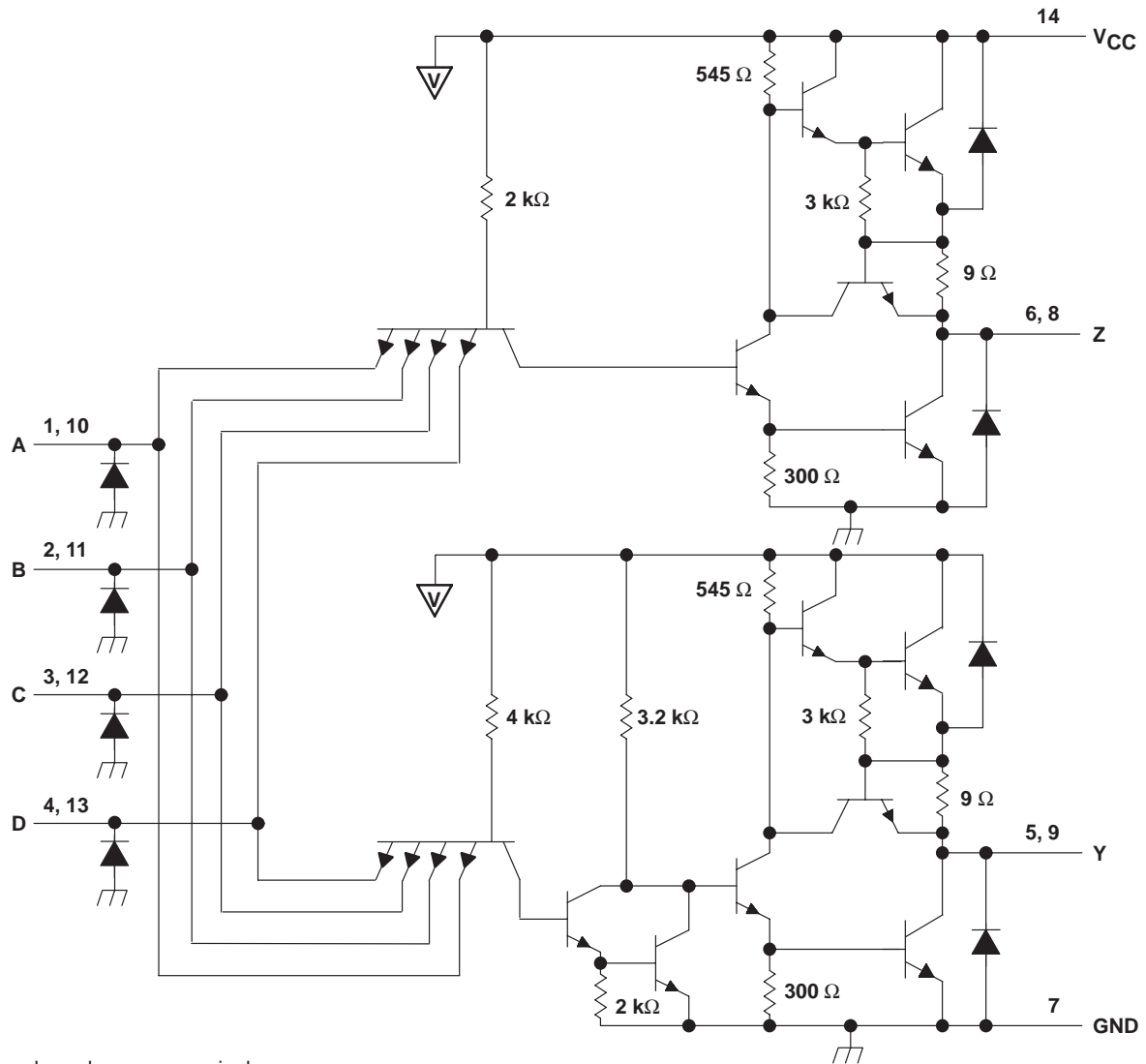


Resistor values shown are nominal.
Pin numbers shown are for the D, J, N, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 7 V
Input voltage, $V_I$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 5.5 V
Duration of output short circuit (see Note 2) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 1 s
Continuous total power dissipation . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . See Dissipation Rating Table
Storage temperature range, $T_{stg}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . . . . . . . . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . . . . . . . . . . . . . . . . . 300°C
Case temperature for 60 seconds, $T_C$: FK package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Not more than one output should be shorted to ground at any one time.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \leq 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 125°C$ POWER RATING |
|---|---|---|---|---|
| D | 950 mW | 7.6 mW/°C | 608 mW | – |
| FK‡ | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J‡ | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW | – |
| W‡ | 1000 mW | 8.0 mW/°C | 640 mW | 200 mW |

‡ In the FK, J, and W packages, SN55183 chips are alloy mounted and SN75183 chips are glass mounted.

## recommended operating conditions

| | SN55183 | | | DS8830, SN75183 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level input voltage, $V_{IH}$ | 2 | | | 2 | | | V |
| Low-level input voltage, $V_{IL}$ | | | 0.8 | | | 0.8 | V |
| High-level output current, $I_{OH}$ | | | –40 | | | –40 | mA |
| Low-level output current, $I_{OL}$ | | | 40 | | | 40 | mA |
| Operating free-air temperature, $T_A$ | –55 | | 125 | 0 | | 70 | °C |

TEXAS
INSTRUMENTS

## electrical characteristics over recommended ranges of $V_{CC}$ and operating free-air temperature (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP[†] | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | Y (AND) outputs | $V_{IH}$ = 2 V | $I_{OH}$ = −0.8 mA | 2.4 | | | V |
| | | | | $I_{OH}$ = −40 mA | 1.8 | 3.3 | | |
| $V_{OL}$ | Low-level output voltage | Y (AND) outputs | $V_{IL}$ = 0.8 V | $I_{OL}$ = 32 mA | | 0.2 | | V |
| | | | | $I_{OL}$ = 40 mA | | 0.22 | 0.4 | |
| $V_{OH}$ | High-level output voltage | Z (NAND) outputs | $V_{IL}$ = 0.8 V | $I_{OH}$ = −0.8 mA | 2.4 | | | V |
| | | | | $I_{OH}$ = −40 mA | 1.8 | 3.3 | | |
| $V_{OL}$ | Low-level output voltage | Z (NAND) outputs | $V_{IH}$ = 2 V | $I_{OL}$ = 32 mA | | 0.2 | | V |
| | | | | $I_{OL}$ = 40 mA | | 0.22 | 0.4 | |
| $I_{IH}$ | High-level input current | | $V_{IH}$ = 2.4 V | | | | 120 | µA |
| $I_I$ | Input current at maximum input voltage | | $V_{IH}$ = 5.5 V | | | | 2 | mA |
| $I_{IL}$ | Low-level input current | | $V_{IL}$ = 0.4 V | | | | −4.8 | mA |
| $I_{OS}$ | Short-circuit output current[‡] | | $V_{CC}$ = 5 V, | $T_A$ =125°C[§] | −40 | −100 | −120 | mA |
| $I_{CC}$ | Supply current (average per driver) | | $V_{CC}$ = 5 V, | All inputs at 5 V, No load | | 10 | 18 | mA |

[†] All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
[‡] Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.
[§] $T_A$ = 125°C is applicable to SN55183 only.

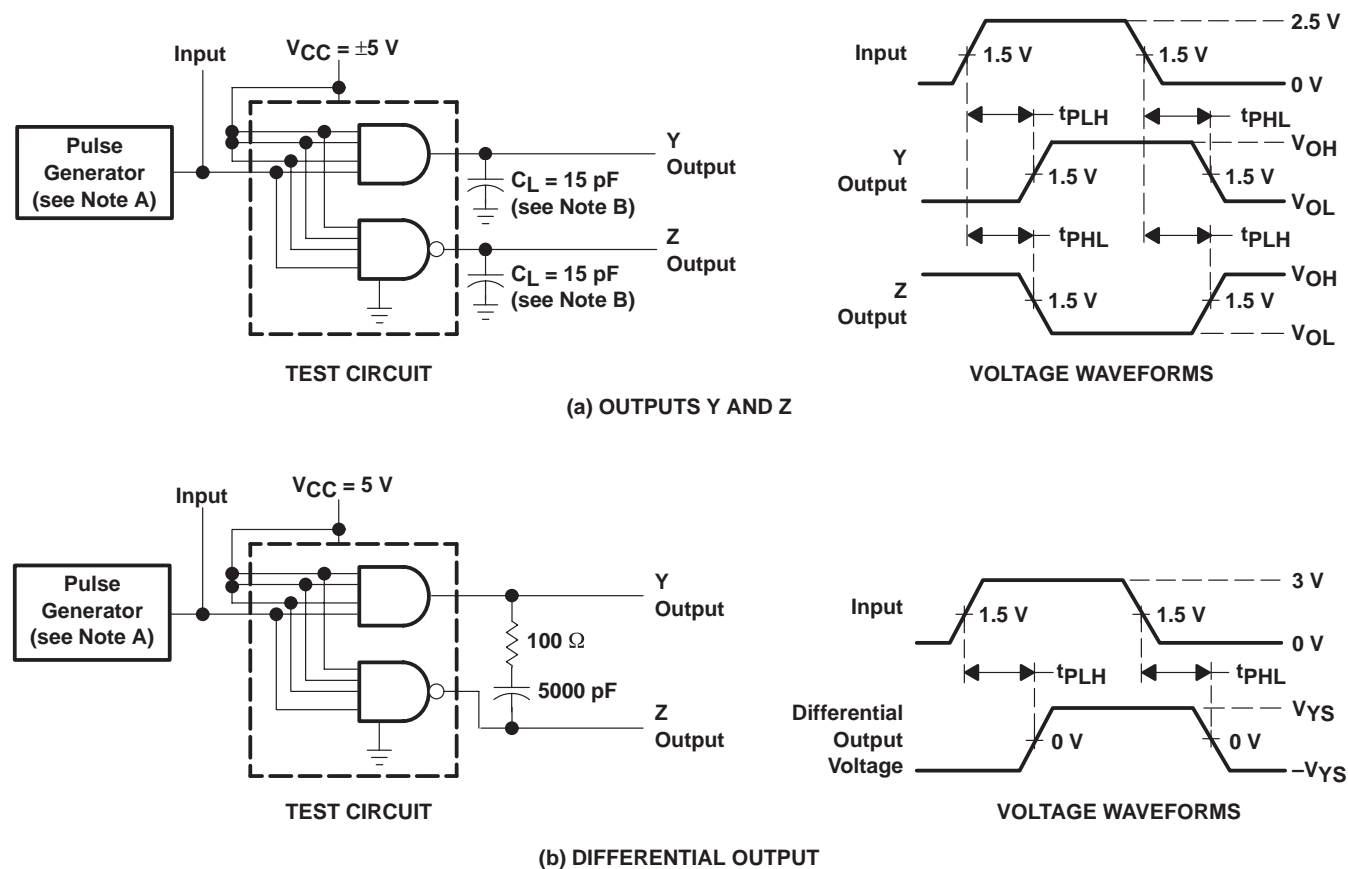## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low- to high-level Y output | AND gates | $C_L$ = 15 pF, See FIgure 1(a) | | 8 | 12 | ns |
| $t_{PHL}$ | Propagation delay time, high- to low-level Y output | AND gates | $C_L$ = 15 pF, See FIgure 1(a) | | 12 | 18 | ns |
| $t_{PLH}$ | Propagation delay time, low- to high-level Z output | NAND gates | $C_L$ = 15 pF, See FIgure 1(a) | | 6 | 12 | ns |
| $t_{PHL}$ | Propagation delay time, high- to low-level Z output | NAND gates | $C_L$ = 15 pF, See FIgure 1(a) | | 6 | 8 | ns |
| $t_{PLH}$ | Propagation delay time, low- to high-level differential output | | Y output with respect to Z output, $R_L$ = 100 Ω in series with 5000 pF, See Figure 1(b) | | 9 | 16 | ns |
| $t_{PHL}$ | Propagation delay time, high- to low-level differential output | | Y output with respect to Z output, $R_L$ = 100 Ω in series with 5000 pF, See Figure 1(b) | | 8 | 16 | ns |

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

## PARAMETER MEASUREMENT INFORMATION

**(a) OUTPUTS Y AND Z**

**TEST CIRCUIT**

Input

$V_{CC} = \pm 5$ V

Pulse Generator (see Note A)

Y Output

$C_L = 15$ pF (see Note B)

Z Output

$C_L = 15$ pF (see Note B)

**VOLTAGE WAVEFORMS**

Input — 2.5 V, 1.5 V, 1.5 V, 0 V

$t_{PLH}$   $t_{PHL}$

Y Output — $V_{OH}$, 1.5 V, 1.5 V, $V_{OL}$

$t_{PHL}$   $t_{PLH}$

Z Output — $V_{OH}$, 1.5 V, 1.5 V, $V_{OL}$

**(b) DIFFERENTIAL OUTPUT**

**TEST CIRCUIT**

Input

$V_{CC} = 5$ V

Pulse Generator (see Note A)

Y Output

100 Ω

5000 pF

Z Output

**VOLTAGE WAVEFORMS**

Input — 3 V, 1.5 V, 1.5 V, 0 V

$t_{PLH}$   $t_{PHL}$

Differential Output Voltage — $V_{YS}$, 0 V, 0 V, $-V_{YS}$

NOTES: A. The pulse generators have the following characteristics: $Z_O = 50$ Ω, $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 0.5$ μs, PRR $\leq 1$ MHz.
B. $C_L$ includes probe and jig capacitance.
C. Waveforms are monitored on an oscilloscope with $r_i \geq 1$ MΩ.

**Figure 1. Test Circuits and Voltage Waveforms**

# TYPICAL CHARACTERISTICS†

**INPUT THRESHOLD VOLTAGE**
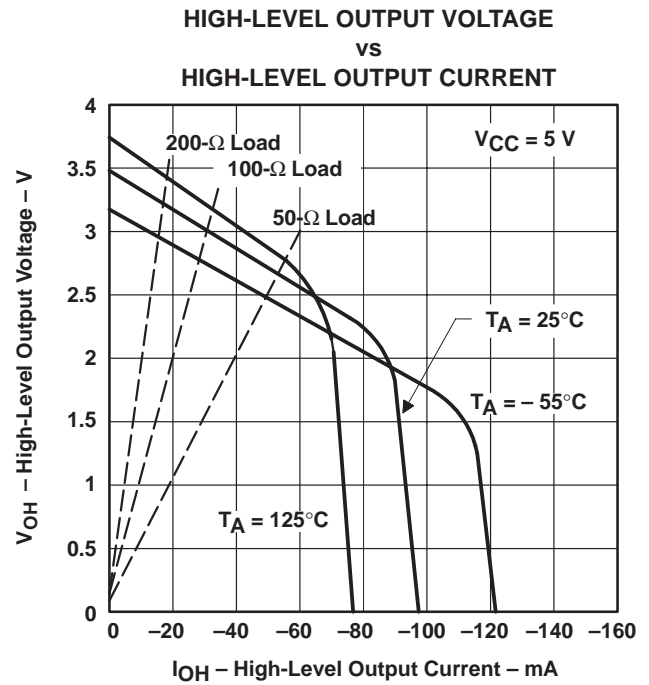**vs**
**FREE-AIR TEMPERATURE**

**Figure 2**

**HIGH-LEVEL OUTPUT VOLTAGE**
**vs**
**HIGH-LEVEL OUTPUT CURRENT**

**Figure 3**

**DIFFERENTIAL OUTPUT VOLTAGE**
**vs**
**DIFFERENTIAL OUTPUT CURRENT**
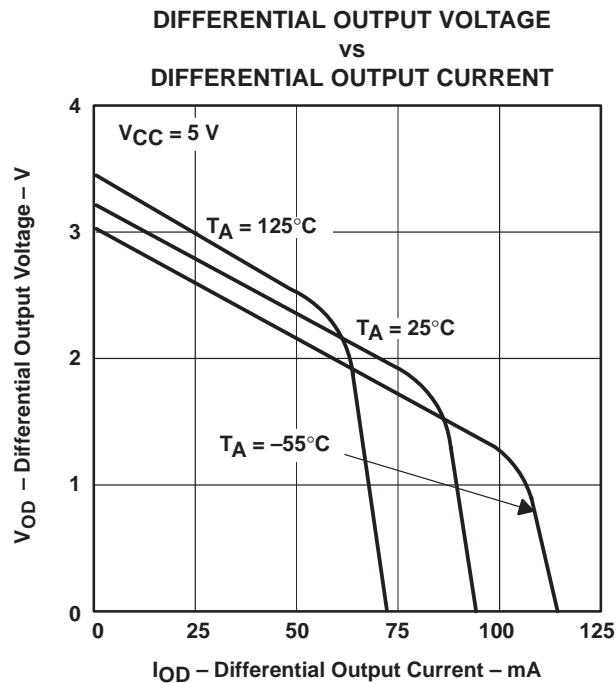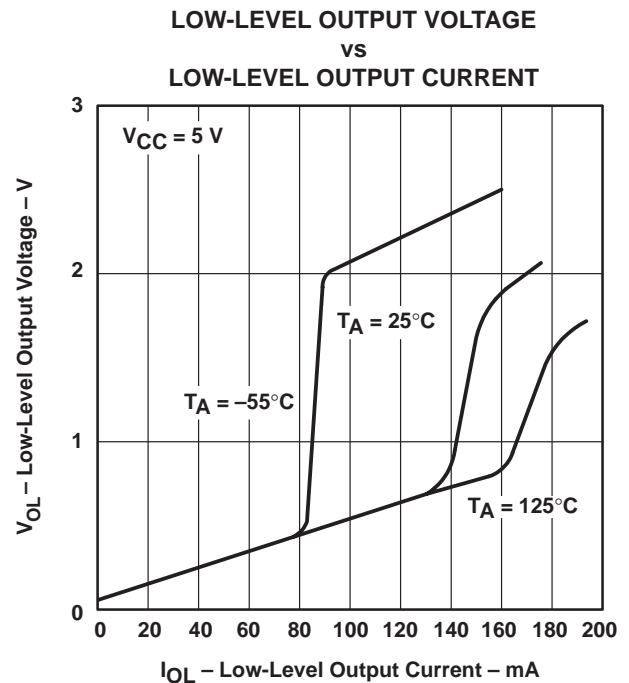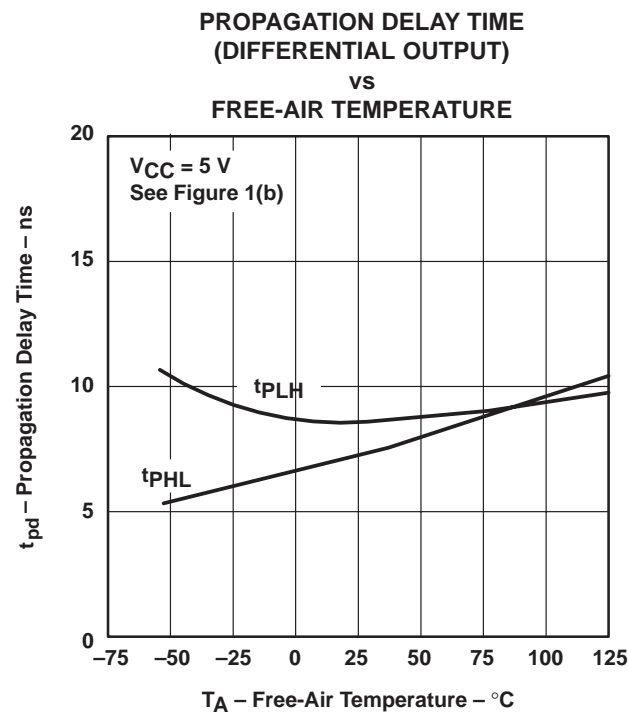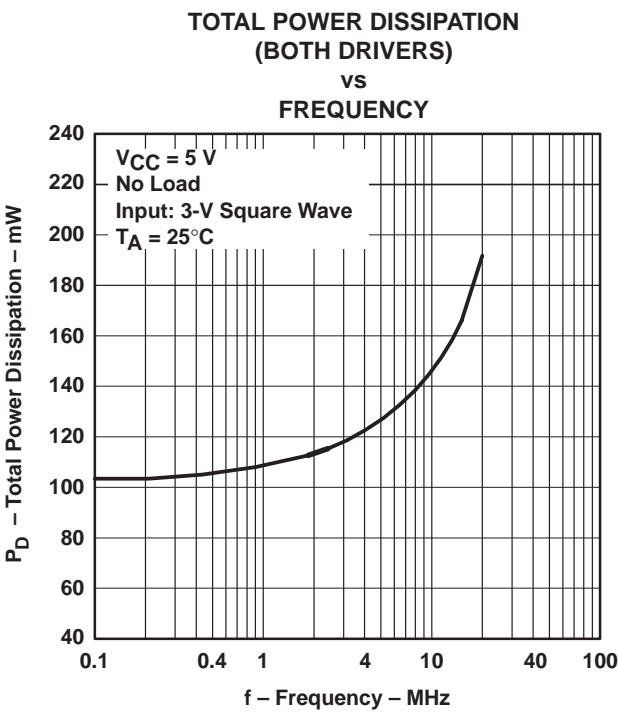
**Figure 4**

**LOW-LEVEL OUTPUT VOLTAGE**
**vs**
**LOW-LEVEL OUTPUT CURRENT**
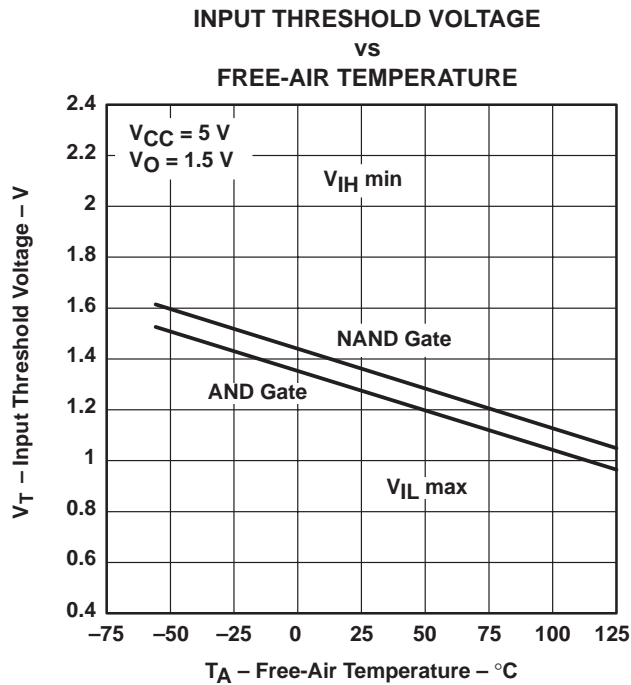
**Figure 5**

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

## TYPICAL CHARACTERISTICS†

**PROPAGATION DELAY TIME**
**(DIFFERENTIAL OUTPUT)**
**vs**
**FREE-AIR TEMPERATURE**



Figure 6

**TOTAL POWER DISSIPATION**
**(BOTH DRIVERS)**
**vs**
**FREQUENCY**



Figure 7

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

## APPLICATION INFORMATION
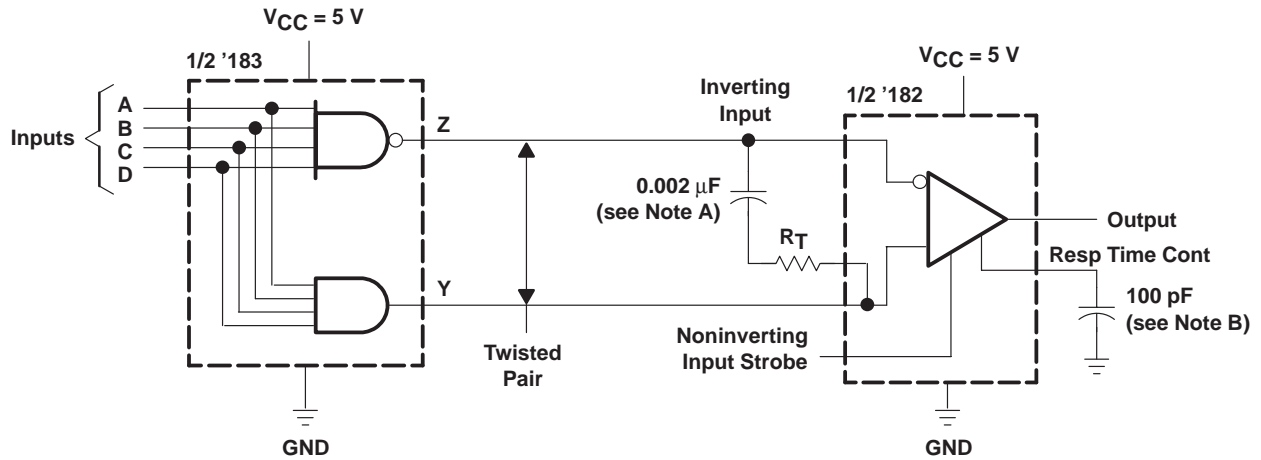


NOTES: A. When the inputs are open circuited, the output is high. A capacitor may be used for dc isolation of the line-terminating resistor. At the frequency of operation, the impedance of the capacitor should be relatively small.

Example: let   f = 5 MHz
C = 0.002 μF

$$Z_{(circuit)} = \frac{1}{2\pi f C} = \frac{1}{2\pi(5 \times 10^6)(0.002 \times 10^{-6})}$$

$$Z_{(circuit)} \approx 16\Omega$$

B. Use of a capacitor to control response time is optional.

**Figure 8. Transmission of Digital Data Over Twisted-Pair Line**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-7900901VCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-7900901VCA SNV55183J | Samples |
| 7900901CA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 7900901CA SNJ55183J | Samples |
| 7900901DA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 7900901DA SNJ55183W | Samples |
| DS8830N | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN55183J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN55183J | Samples |
| SN75183D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75183 | Samples |
| SN75183DE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75183 | Samples |
| SN75183DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75183 | Samples |
| SN75183N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN75183N | Samples |
| SN75183NE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN75183N | Samples |
| SN75183NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75183 | Samples |
| SN75183NSRE4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75183 | Samples |
| SN75183NSRG4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75183 | Samples |
| SNJ55183FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 79009012A SNJ55 183FK | Samples |
| SNJ55183J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 7900901CA SNJ55183J | Samples |
| SNJ55183W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 7900901DA SNJ55183W | Samples |

**(1)** The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN55183, SN55183-SP, SN75183 :**

● Catalog: SN75183, SN55183

● Military: SN55183

● Space: SN55183-SP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN75183NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

**TAPE AND REEL BOX  DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|-----|-------------|------------|-------------|
| SN75183NSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |

J (R−GDIP−T∗∗)                    CERAMIC DUAL IN−LINE PACKAGE
14 LEADS SHOWN

| DIM \ PINS ∗∗ | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | —— | —— | —— | —— |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

B

14                    8

1                    7

0.065 (1,65)
0.045 (1,14)

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°−15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES:    A.  All linear dimensions are in inches (millimeters).
          B.  This drawing is subject to change without notice.
          C.  This package is hermetically sealed with a ceramic lid using glass frit.
          D.  Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
          E.  Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

## W (R–GDFP–F14)                    CERAMIC DUAL FLATPACK



Base and Seating Plane

0.260 (6,60)
0.235 (5,97)

0.045 (1,14)
0.026 (0,66)

0.006 (0,15)
0.004 (0,10)

0.080 (2,03)
0.045 (1,14)

0.280 (7,11) MAX

0.019 (0,48)
0.015 (0,38)

0.050 (1,27)

1                    14

0.390 (9,91)
0.335 (8,51)

0.005 (0,13) MIN
4 Places

7                    8

0.360 (9,14)
0.250 (6,35)

0.360 (9,14)
0.250 (6,35)

4040180–2/D 07/03

NOTES:   A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only.
         E.   Falls within MIL STD 1835 GDFP1–F14 and JEDEC MO–092AB

FK (S−CQCC−N**)                          LEADLESS CERAMIC CHIP CARRIER
28 TERMINAL SHOWN

| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |

0.020 (0,51)
0.010 (0,25)

0.020 (0,51)
0.010 (0,25)

0.080 (2,03)
0.064 (1,63)

0.055 (1,40)
0.045 (1,14)

0.045 (1,14)
0.035 (0,89)

0.028 (0,71)
0.022 (0,54)

0.050 (1,27)

0.045 (1,14)
0.035 (0,89)

4040140/D 01/11

NOTES:   A.  All linear dimensions are in inches (millimeters).
         B.  This drawing is subject to change without notice.
         C.  This package can be hermetically sealed with a metal lid.
         D.  Falls within JEDEC MS−004

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## N (R−PDIP−T**)             PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

| PINS **<br>DIM | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A   MAX | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A   MIN | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS−001<br>VARIATION | AA | BB | AC | AD |

A

16       9

0.260 (6,60)
0.240 (6,10)

1       8

0.070 (1,78)
0.045 (1,14)  D

0.045 (1,14)  D
0.030 (0,76)

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.010 (0,25) NOM

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

0.430 (10,92) MAX

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option  D

4040049/E   12/2002

NOTES:    A.   All linear dimensions are in inches (millimeters).
           B.   This drawing is subject to change without notice.
          C.   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
          D.   The 20 pin end lead shoulder width is a vendor option, either half or full width.

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D (R−PDSO−G14)                                   PLASTIC SMALL OUTLINE



0.344 (8,75)
0.337 (8,55)
C

14                    8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)   D

1                     7

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)        0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−5/M  06/11

NOTES:   A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
         D.   Body width does not include interlead flash.  Interlead flash shall not exceed 0.017 (0,43) each side.
         E.   Reference JEDEC MS−012 variation AB.

D (R−PDSO−G14)                                      PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

|←——12x1,27

|←——14x0,55

|←——12x1,27

14x1,50

5,40

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

Example
Solder Mask Opening
(See Note E)

←——0,60

1,55

——0.07

All Around

4211283−3/E  08/12

NOTES:   A.  All linear dimensions are in millimeters.
         B.  This drawing is subject to change without notice.
         C.  Publication IPC−7351 is recommended for alternate designs.
         D.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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**NS (R-PDSO-G**)**　　　　　　　　　　　　　　　　　　PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



| DIM / PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A　MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A　MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:　A.　All linear dimensions are in millimeters.
　　　　　B.　This drawing is subject to change without notice.
　　　　　C.　Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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