SN75ALS174A
QUADRUPLE DIFFERENTIAL LINE DRIVER

- **Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B and RS-485**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Designed for up to 20-Mbit/s Operation in Both Serial and Parallel Applications**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Low Supply Current Requirements 55 mA Max**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal-Shutdown Protection**
- **Driver Positive- and Negative-Current Limiting**
- **Functionally Interchangeable With SN75174**

N PACKAGE
(TOP VIEW)

1A	1	16	V_{CC}
1Y	2	15	4A
1Z	3	14	4Y
1,2EN	4	13	4Z
2Z	5	12	3,4EN
2Y	6	11	3Z
2A	7	10	3Y
GND	8	9	3A

DW PACKAGE
(TOP VIEW)

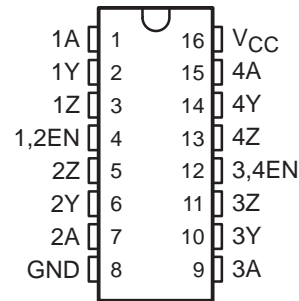|			
1A	1	20	V_{CC}
1Y	2	19	4A
NC	3	18	4Y
1Z	4	17	NC
1,2EN	5	16	4Z
2Z	6	15	3,4EN
NC	7	14	3Z
2Y	8	13	NC
2A	9	12	3Y
GND	10	11	3A

NC – No internal connection

description

The SN75ALS174A is a quadruple line driver with 3-state differential outputs. It is designed to meet the requirements of ANSI Standards EIA/TIA-422-B and RS-485. This device is optimized for balanced multipoint bus transmission at rates of up to 20 Mbit/s. Each driver features wide positive and negative common-mode output voltage ranges that make them suitable for party-line applications in noisy environments.
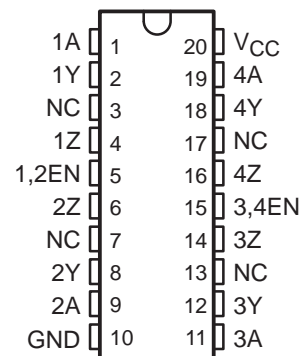
The SN75ALS174A provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C.

The SN75ALS174A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each driver)

INPUT A	ENABLES	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = high level, L = low level, X = irrelevant,
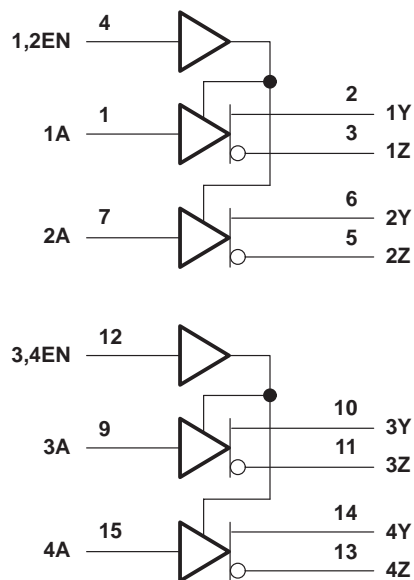Z = high impedance (off)

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SN75ALS174A
QUADRUPLE DIFFERENTIAL LINE DRIVER
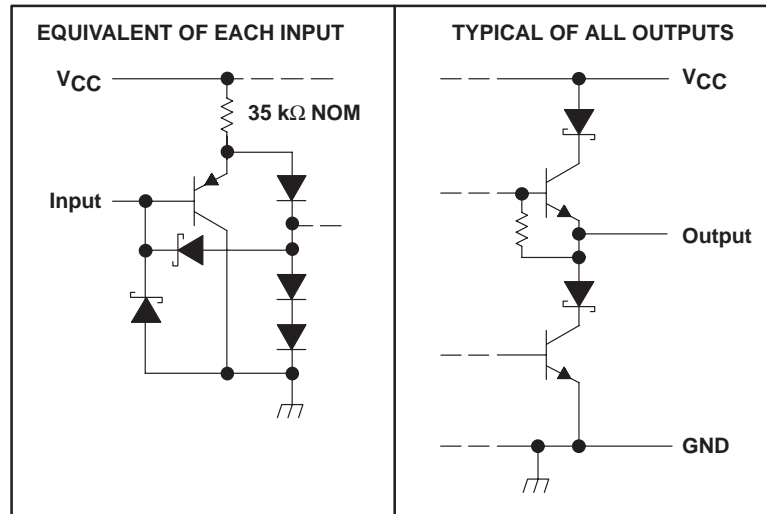
logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

logic diagram (positive logic)

Pin numbers shown are for the N package.

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schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

V_{CC}

35 kΩ NOM

Input

TYPICAL OF ALL OUTPUTS

V_{CC}

Output

GND

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage, V_I . . . . 7 V
Output voltage range, V_O . . . . –9 V to 14 V
Continuous total dissipation . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Common-mode output voltage, V_{OC}				12 −7	V
High-level output current, I_{OH}				−60	mA
Low-level output current, I_{OL}				60	mA
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[†]	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
$|V_{OD1}|$	Differential output voltage	$I_O = 0$		1.5		6	V
$|V_{OD2}|$	Differential output voltage	$R_L = 100\ \Omega$	See Figure 1	$1/2 V_{OD1}$ or 2[‡]			V
		$R_L = 54\ \Omega$		1.5	2.5	5	
$|V_{OD3}|$	Differential output voltage	See Note 2		1.5		5	V
$\Delta|V_{OD}|$	Change in magnitude of differential output voltage[§]	$R_L = 54\ \Omega$ or $100\ \Omega$,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage[¶]	$R_L = 54\ \Omega$ or $100\ \Omega$,	See Figure 1			3 −1	V
$\Delta|V_{OC}|$	Change in magnitude of common-mode output voltage[§]	$R_L = 54\ \Omega$ or $100\ \Omega$,	See Figure 1			±0.2	V
I_O	Output current with power off	$V_{CC} = 0$,	$V_O = -7$ V to 12 V			±100	µA
I_{OZ}	High-impedance-state output current	$V_O = -7$ V to 12 V				±100	µA
I_{IH}	High-level input current	$V_I = 2.7$ V				20	µA
I_{IL}	Low-level input current	$V_I = 0.4$ V				−100	µA
I_{OS}	Short-circuit output current	$V_O = -7$ V to 12 V				±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		36	55	mA
			Outputs disabled		16	30	

[†] All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.
[‡] The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
[§] $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
[¶] In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
NOTE 2: See EIA Standard RS-485, Figure 3-5, Test Termination Measurement 2.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF

PARAMETER		TEST CONDITIONS		MIN	TYP[†]	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	$R_L = 54\ \Omega$,	See Figure 2	9	15	22	ns
t_{PZH}	Output enable time to high level	$R_L = 110\ \Omega$,	See Figure 3	30	45	70	ns
t_{PZL}	Output enable time to low level	$R_L = 110\ \Omega$,	See Figure 4	25	40	65	ns
t_{PHZ}	Output disable time from high level	$R_L = 110\ \Omega$,	See Figure 3	10	20	35	ns
t_{PLZ}	Output disable time from low level	$R_L = 110\ \Omega$,	See Figure 4	10	30	45	ns

[†] All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.
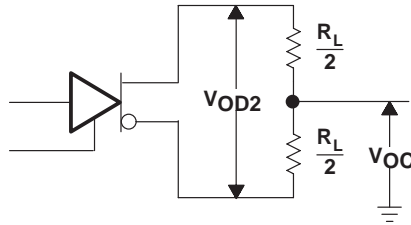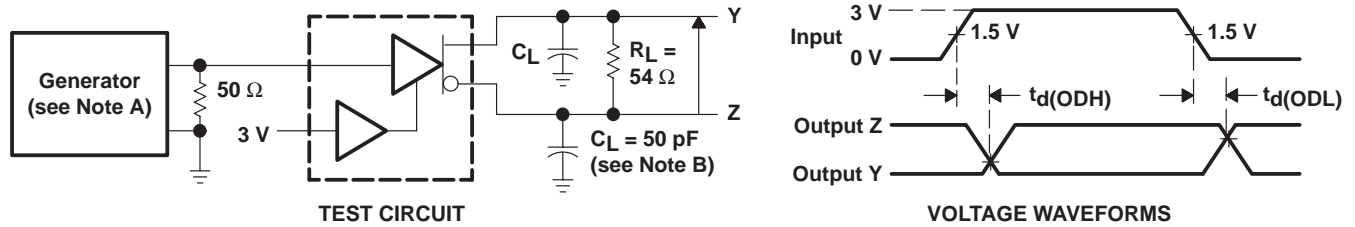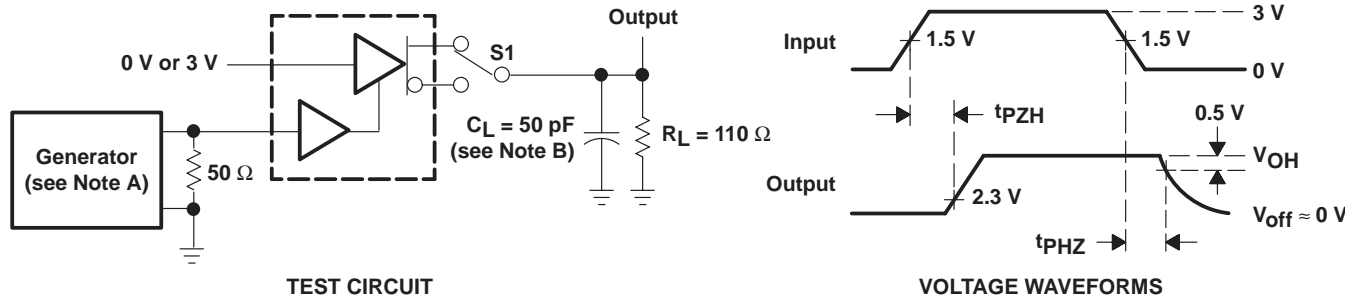
PARAMETER MEASUREMENT INFORMATION

Figure 1. Differential and Common-Mode Output Voltages

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, t_f ≤ 5 ns, t_r ≤ 5 ns.
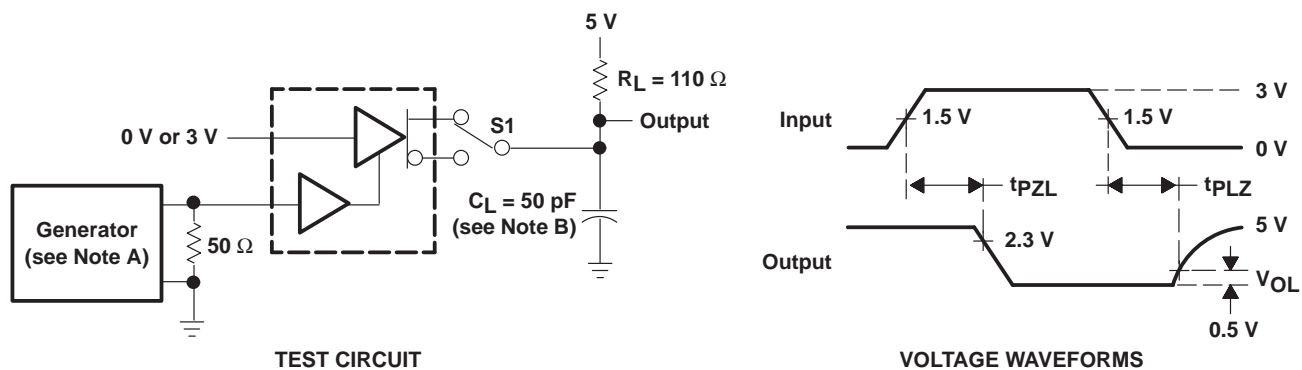B. C_L includes probe and stray capacitance.

Figure 2. Differential-Output Test Circuit and Delay and Transition Times Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, t_f ≤ 5 ns, t_r ≤ 5 ns.
B. C_L includes probe and stray capacitance.

Figure 3. Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}

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PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, $t_f \leq$ 5 ns, $t_r \leq$ 5 ns.

B. C_L includes probe and stray capacitance.

Figure 4. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN75ALS174ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS174A	Samples
SN75ALS174ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS174A	Samples
SN75ALS174ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS174A	Samples
SN75ALS174ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS174A	Samples
SN75ALS174ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS174A	Samples
SN75ALS174ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS174A	Samples
SN75ALS174AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS174AN	Samples
SN75ALS174ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS174AN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
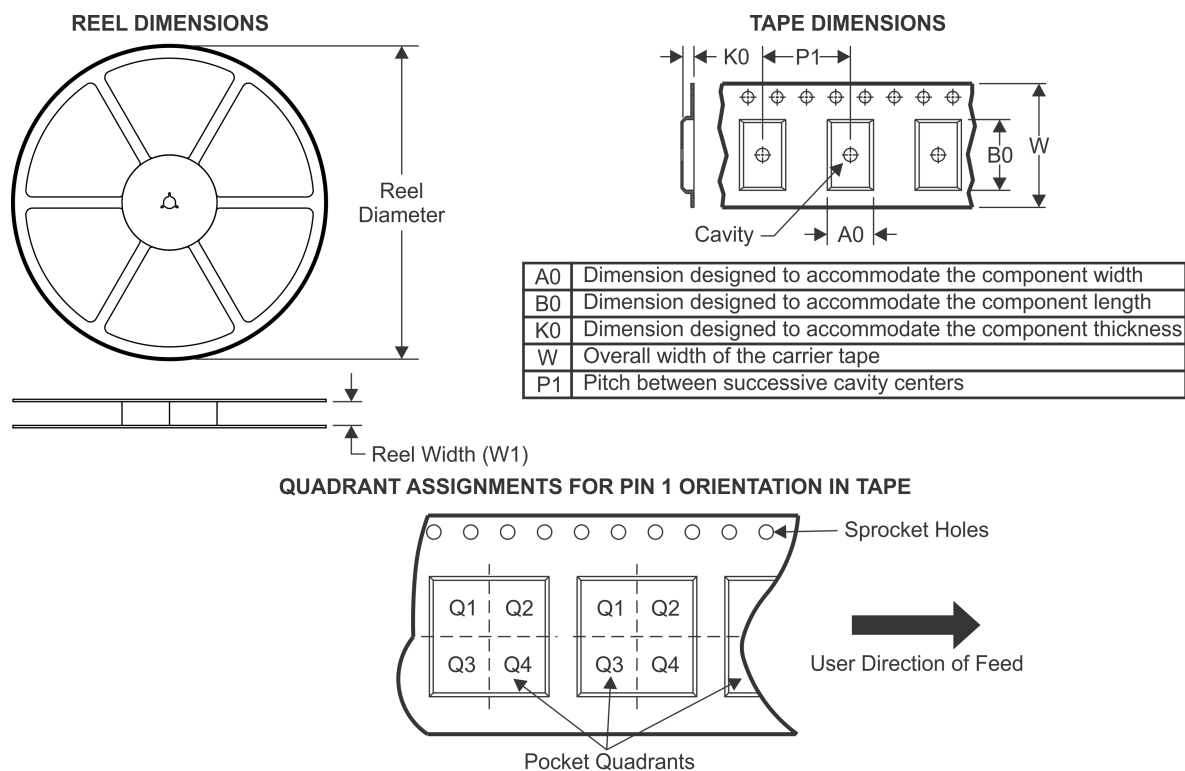
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS174ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS174ADWR	SOIC	DW	20	2000	367.0	367.0	45.0

MECHANICAL DATA

N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) △D

0.045 (1,14) / 0.030 (0,76) △D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option △D

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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DW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0.512 (13,00)
─────────────
0.496 (12,60)

20   11

0.419 (10,63)
─────────────
0.393 (9,97)

0.299 (7,60)
────────────
0.291 (7,40)

1   10

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
────────────
0.012 (0,31)

⌖ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
────────────
0.004 (0,10)

0.013 (0,33)
────────────
0.008 (0,20)

⌂ 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
────────────
0.016 (0,40)

4040000−4/G 01/11

NOTES: A.   All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−013 variation AC.

DW (R-PDSO-G20)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

20x0,6   18x1,27

9,4

20x0,55   18x1,27

20x1,95

9,4

Non Solder Mask Define Pad

0,6

Solder Mask Opening
(Note E)

2,0

Pad Geometry
(Note C)

0,07
All Around

4209202-4/E 07/11

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Refer to IPC7351 for alternate board design.

          D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
               contact their board assembly site for stencil design recommendations. Refer to IPC-7525
          E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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