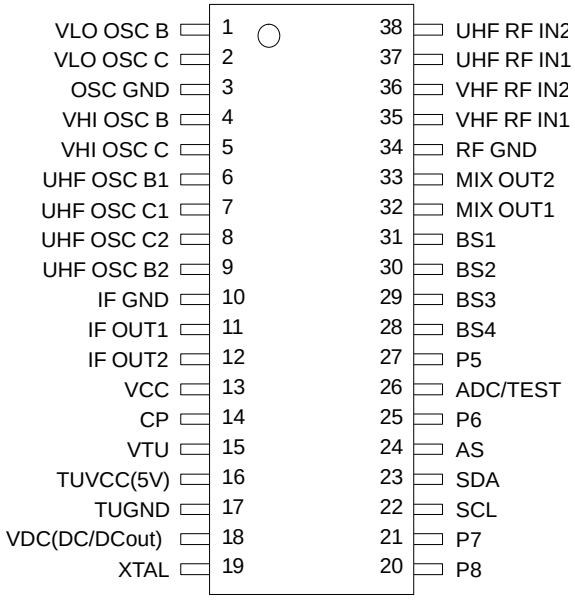
TV/VCR TUNER IC WITH DC/DC CONVERTER

FEATURES

- **Single Chip Mixer/Oscillator, Synthesizer, and 30-V DC/DC Converter for Tuning Amplifier**
- **VHF-L, VHF-H, UHF 3-Band Local Oscillator**
- **I^2C Bus Protocol**
- **Four Data Bytes Transmission**
- **Low Noise DC/DC Converter**
- **4ch NPN Emitter Follower Type Band Switch Drivers**
- **4ch NPN Open Collector Type Ports**
- **Programmable Reference Divider Ratio (31.25 kHz, 50 kHz, or 62 kHz)**
- **5-V Power Supply**
- **38-Pin TSSOP Package**

DA PACKAGE (TOP VIEW)
38-PIN TSSOP (DA)



DESCRIPTION

The SN761677 is a single-chip synthesized tuner IC designed for TV/VCR tuning systems. The circuit consists of a PLL synthesizer, 3-band local oscillators and mixer, 30-V dc/dc converter for tuning the amplifier, four NPN emitter follower band drivers, four NPN open collector ports, and is available in a small package outline. The 15-bit programmable counter and reference divider are controlled by I^2C bus control. Tuning step frequency is selectable by the reference divider ratio for a 4-MHz Xtal oscillator.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		UNIT
Supply voltage (2), V_{CC}	VCC, TUVCC	–0.4 V to 7 V
Input voltage 1 (2), V_{GND}	RF GND, OSC GND, TUGND	–0.4 V to 0.4 V
Input voltage 2 (2), $V_{(VTU)}$	VTU (4)	–0.4 V to 35 V
Input voltage 3 (2), V_{IN}	Other input pins	–0.4 V to 7 V
Continuous total dissipation (3), P_D	$T_A \le 25°C$	1168 mW
Operating free–air temperature, T_A		–20°C to 85°C
Storage temperature range, T_{stg}		–65°C to 150°C
Maximum junction temperature, T_J		150°C
Maximum lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C
Maximum short circuit time, $t_{SC(max)}$	All pins to VCC/TUVCC, IFGND, OSCGND, RFGND, TUGND	10 sec

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to the IF GND of the circuit.
(3) Derating factor is 9.34 mW/°C for $T_A \le 25°C$.
(4) 30 V max, when input from external power supply.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Band switch driver source current, I_{BS}	One port on			10	mA
NPN port sink current, I_{NPN}	One port on		–10	–15	mA
Operating free-air temperature, T_A		–20		85	°C

CAUTION:

It is advised that precautions be taken to avoid damage due to high static voltages or electrostatic fields while handling this device. UHF OSC (pins 6–9) can withstand 1.5 kV and all other pins can withstand 2 kV, according to the Human Body Model (1.5 kΩ, 100 pF).

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5 V to 5.5 V, T_A = –20°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Total Device and Serial Interface						
$I_{CC}1$	Supply current 1 (VCC)			75	95	mA
$I_{CC}2$	Supply current 2 (VCC)	One band switch on (I_{BS} = 10 mA)		85	105	mA
$I_{CC}3$	Supply current 3 (TUVCC)	I_{VDC} = 50 µA		4	10	mA
V_{IH}	High-level input voltage (SCL, SDA)		3			V
V_{IL}	Low-level input voltage (SCL, SDA)				1.5	V
I_{IH}	High-level input current (SCL, SDA)				10	µA
I_{IL}	Low-level input current (SCL, SDA)		–10			µA
V_{POR}	Power-on reset supply voltage	Threshold of supply voltage between reset and operation mode	2.1	3.7	4	V
DC/DC Converter						
$V_{O(VDC)}$	Output voltage (VDC)	I_{VDC} = 50 µA		35		V
$I_{C(VDCM)}$	Output current (VDC)			230		µA
t_S	Output settling time (VDC)	From V_{TUVCC} > 4.5 V to $V_{O(VDC)}$ < 28 V		100		ms
I^2C Interface						
V_{ASH}	Address select high-input voltage (AS)	V_{CC} = 5 V	4.5		5	V
V_{ASM}	Address select mid-input voltage (AS)	V_{CC} = 5 V	2		3	V
V_{ASL}	Address select low-input voltage (AS)	V_{CC} = 5 V			0.5	V
I_{ASH}	Address select high-input current (AS)				10	µA
I_{ASL}	Address select low-input current (AS)		–10			µA
$V_{I(ADC)}$	ADC input voltage	See Table 9	0		V_{CC}	V
$I_{IH(ADH)}$	ADC high-level input current	$V_{I(ADC)}$ = V_{CC}			10	µA
$I_{IL(ADL)}$	ADC low-level input current	$V_{I(ADC)}$ = 0 V	–10			µA
V_{OL}	Low-level output voltage (SDA)	V_{CC} = 5 V, I_{OL} = 3 mA			0.4	V
$I_{lkg(SDA)}$	High-level output leakage current (SDA)	V_{SDA} = 5.5 V			10	µA
F_{SCL}	Clock frequency (SCL)			100	400	kHz
$t_{h(DAT)}$	Data hold time	See timing chart in Figure 1	0			µs
t_{BUF}	Bus free time		1.3			µs
$t_{h(STA)}$	Start hold time		0.6			µs
$t_{h(low)}$	SCL low hold time		0.6			µs
$t_{h(lhigh)}$	SCL high hold time		0.6			µs
$t_{su(STA)}$	Start setup time		0.6			µs
$t_{su(DAT)}$	Data setup time		0.1			µs
t_r	SCL, SDA rise time				0.3	µs
t_f	SCL, SDA fall time				0.3	µs
$t_{su(STO)}$	STOP setup time		0.6			µs

ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 4.5 V to 5.5 V, T_A = –20°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PLL and NPN Port						
N	Divider ratio	14-bit frequent word	256		16383	
		15-bit frequent word	256		32767	
F_{XTAL}	Crystal oscillator	Rxtal = 25 Ω to 300 Ω		4		MHz
Z_{XTAL}	Crystal oscillator input impedance	V_{CC} = 5 V, T_A = 25°C		2.3		kΩ
V_{XTALIN}	External crystal oscillator input amplitude		400			$mV_{p–p}$
$V_{O(TU)}$	Tuning amplifier low-level output voltage	R_L = 27 kΩ		0.4	0.7	V
$I_{IH(CPH)}$	Charge pump high-level input current	CP = 1		40		µA
$I_{IL(CPH)}$	Charge pump low-level input current	CP = 0		10		µA
$V_{O(CP)}$	Charge pump output voltage	In lock		1.95		V
$I_{lkg(CPOFF)}$	Charge pump leakage current	T2 = 0, T1 = 1, $V_{O(CP)}$ = 2 V, T_A = 25°C	–15		15	nA
I_{BS}	Band switch driver source current				10	mA
$V_{O(SBS1)}$	Band switch driver output voltage	I_{BS} = 10 mA	3			V
$V_{O(SBS2)}$		I_{BS} = 10 mA, V_{CC} = 5 V, T_A = 25°C	3.5	3.9		V
$I_{lkg(BSOFF)}$	Band switch driver leakage current	V_{BS} = 0 V			3	µA
I_{NPN}	NPN port sink current				–15	mA
$V_{O(SN1)}$	NPN port output voltage	I_{NPN} = 100 µA			0.2	V
$V_{O(SN2)}$		I_{NPN} = 10 mA			0.5	V
$I_{lkg(NPNOFF)}$	NPN port leakage current	V_{CC} = 5.5 V, V_{NPN} = 1.5 V			1	µA

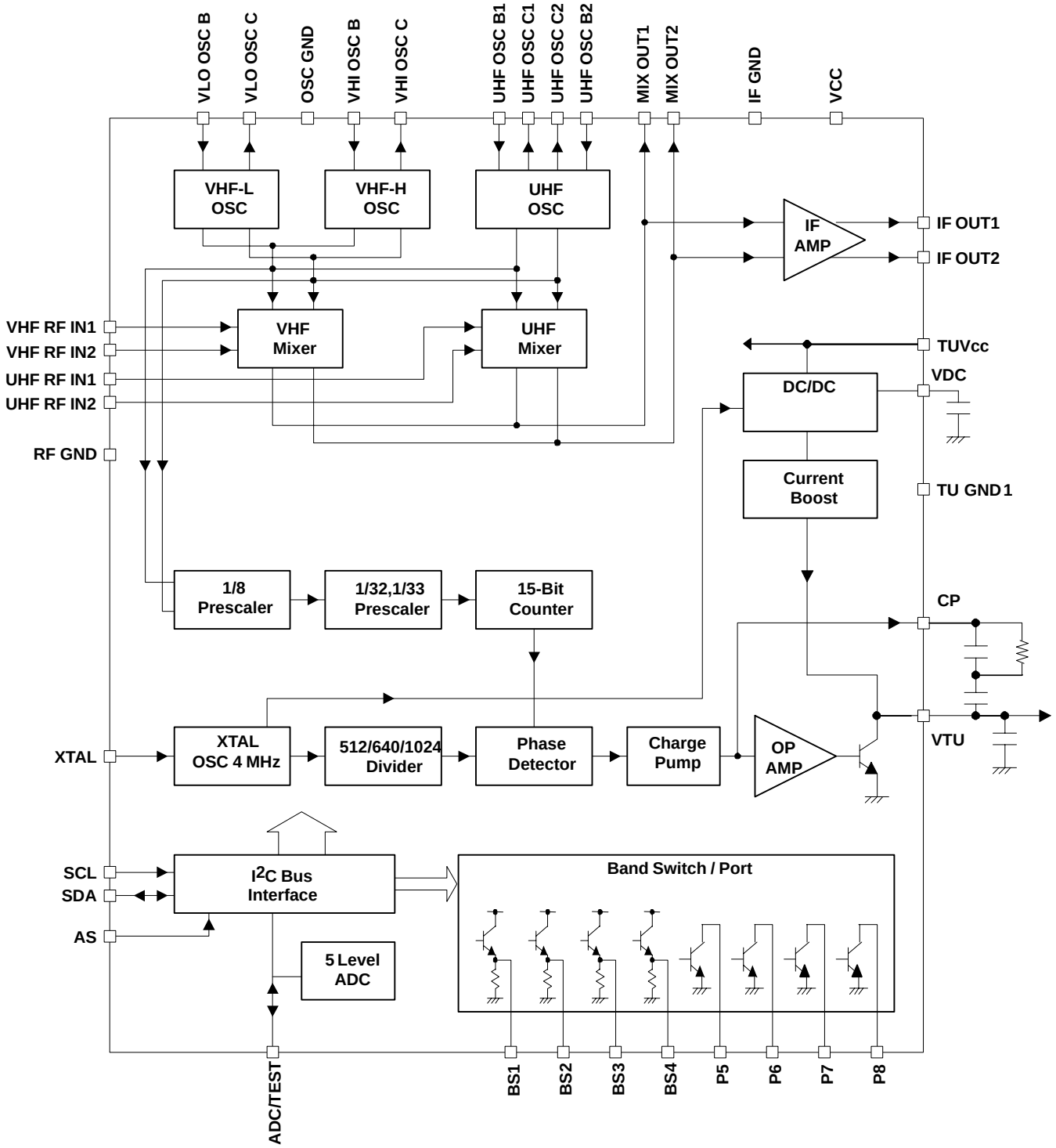
ELECTRICAL CHARACTERISTICS

V_{CC} = 5 V, T_A = –25°C, measured in reference measurement circuit at 50-Ω system, IF filter characteristics: f_{peak} = 43 MHz; (unless otherwise noted)(1)

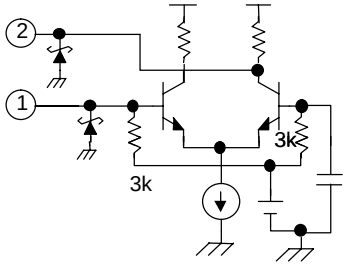
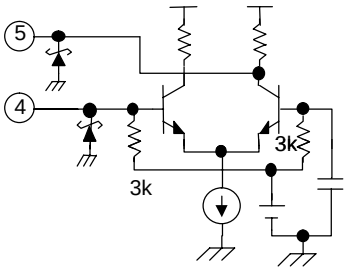
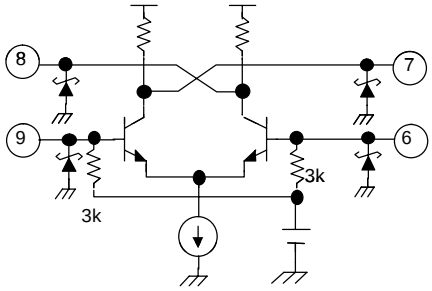
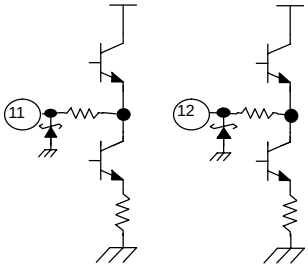
PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
MIXER, OSCILLATOR, IF AMPLIFIER						
G_{c1}	Conversion gain (mixer~IF amplifier) VHF low	F_{in} = 58 MHz(1)	23	26	29	dB
G_{c3}		F_{in} = 130 MHz				
G_{c4}	Conversion gain (mixer~IF amplifier) VHF high	F_{in} = 136 MHz(1)	23	26	29	dB
G_{c6}		F_{in} = 364 MHz				
G_{c7}	Conversion gain (mixer~IF amplifier) VHF–UHF	F_{in} = 370 MHz(1)	24	27	30	dB
G_{c9}		F_{in} = 804 MHz				
NF_1	Noise figure VHF low	F_{in} = 55.25 MHz		11		dB
NF_3		F_{in} = 127.25 MHz				
NF_4	Noise figure VHF high	F_{in} = 133.25 MHz		11		dB
NF_6		F_{in} = 361.25 MHz				
NF_7	Noise figure UHF	F_{in} = 367.25 MHz		10		dB
NF_9		F_{in} = 801.25 MHz		11		
CM_1	1% cross modulation distortion VHF low	F_{in} = 55.25 MHz(2)		89		dBμV
CM_3		F_{in} = 127.25 MHz				
CM_4	1% cross modulation distortion VHF high	F_{in} = 133.25 MHz(2)		86		dBμV
CM_6		F_{in} = 361.25 MHz				
CM_7	1% cross modulation distortion UHF	F_{in} = 367.25 MHz(2)		87		dBμV
CM_9		F_{in} = 801.25 MHz		86		
$V_{O(IF1)}$	IF output voltage VHF low	F_{in} = 55.25 MHz(3)		117		dBμV
$V_{O(IF3)}$		F_{in} = 127.25 MHz				
$V_{O(IF4)}$	IF output voltage VHF high	F_{in} = 133.25 MHz(3)		117		dBμV
$V_{O(IF6)}$		F_{in} = 361.25 MHz				
$V_{O(IF7)}$	IF output voltage UHF	F_{in} = 367.25 MHz(3)		117		dBμV
$V_{O(IF9)}$		F_{in} = 801.25 MHz				

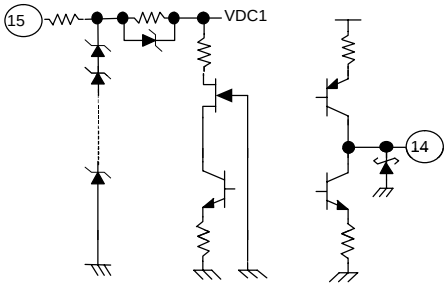
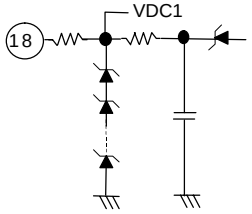
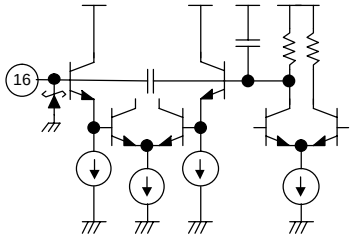
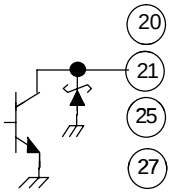
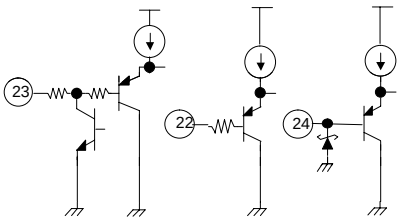
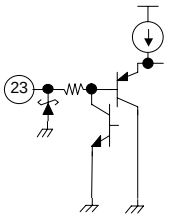
(1) IF = 43 MHz, RF input level = 80 dBμV
(2) $F_{undes} = F_{des} \pm 6$ MHz, pin = 80 dBμV, AM 1 kHz, 30%, DES/CM = S/I = 46 dB
(3) IF = 45.75 MHztop

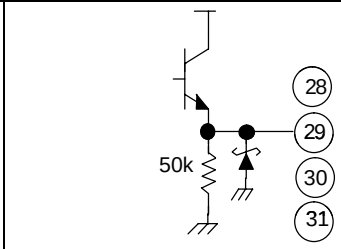
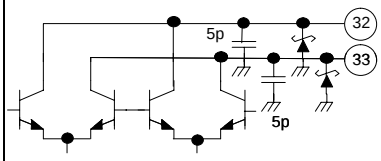
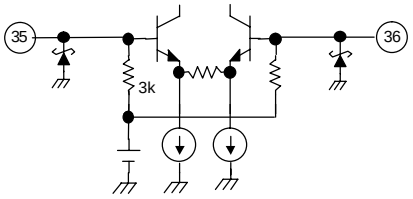
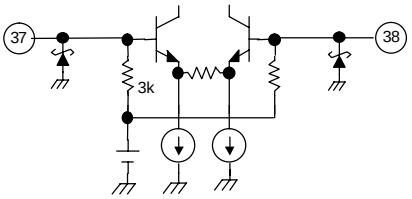
BLOCK DIAGRAM



Terminal Functions

TERMINAL		DESCRIPTION	
NAME	NO.		
VLO OSC B	1	VHF low oscillator input base	
VLO OSC C	2	VHF low oscillator output collector	
OSC GND	3	Oscillator ground	
VHI OSC B	4	VHF hi oscillator input base	
VHI OSC C	5	VHF hi oscillator output collector	
UHF OSC B1	6	UHF oscillator input base1	
UHF OSC C1	7	UHF oscillator output collector1	
UHF OSC C2	8	UHF oscillator output collector2	
UHF OSC B2	9	UHF oscillator input base2	
IF GND	10	IF ground	
IF OUT1	11	IF output	
IF OUT2	12	IF output	
VCC	13	Supply voltage for mixer/oscillator/PLL: 5 V	

TERMINAL		DESCRIPTION	
NAME	NO.		
CP	14	Charge pump output	
VTU	15	Tuning voltage amplifier output	
TUVCC	16	Supply voltage for DC/DC converter: 5 V	
TUGND	17	DC/DC converter ground	
VDC	18	DC/DC converter monitor output. (Do not connect to other terminals or circuits except for the capacitor.)	
XTAL	19	4-MHz crystal oscillator input	
P8	20	Port 8 output (NPN open collector)	
P7	21	Port 7 output (NPN open collector)	
P6	25	Port 6 output (NPN open collector)	
P5	27	Port 5 output (NPN open collector)	
SCL	22	I^2C serial clock input	
SDA	23	I^2C serial data input/output	
AS	24	I^2C address set input	
ADC/TEST	26	ADC input / test output	

TERMINAL		DESCRIPTION	
NAME	NO.		
BS4	28	Band switch4 output (NPN emitter follower)	
BS3	29	Band switch3 output (NPN emitter follower)	
BS2	30	Band switch2 output (NPN emitter follower)	
BS1	31	Band switch1 output (NPN emitter follower)	
MIX OUT1	32	Mixer output	
MIX OUT2	33	Mixer output	
RF GND	34	RF ground	
VHF RF IN1	35	VHF RF input	
VHF RF IN2	36	VHF RF input	
UHF RF IN1	37	UHF RF input	
UHF RF IN2	38	UHF RF input	

FUNCTION DESCRIPTION

The device can be controlled according to the I^2C bus format.

Table 1. Serial Interface Function

PIN	PIN NAME	DESCRIPTION
22	SCL	Clock input
23	SDA	Data input/output
24	AS	Address selection input
26	ADC/TEST	ADC input, test output

I^2C Write Mode (R/W = 0)

Table 2. Write Data Format

	MSB							LSB	
Address byte (ADB)	1	1	0	0	0	MA1	MA0	R/W=0	A
Divider byte 1 (DB1)	0	N14	N13	N12	N11	N10	N9	N8	A
Divider byte 2 (DB2)	N7	N6	N5	N4	N3	N2	N1	N0	A
Control byte (CB)	1	CP	T2	T1	T0	RSA	RSB	OS	A
Ports byte (PB)	P8	P7	P6	P5	BS4	BS3	BS2	BS1	A

Table 3. Description of Data Symbol

SYMBOL	DESCRIPTION	DEFAULT
MA1, MA0	Address set bits (See Table 4)	
N14...N0	Programmable counter set bits N=N14x2^14+N13x2^13+..+N1x2+N0	Nn=0
CP	Charge pump current set bit 10 μA (CP=0) 40 μA (CP=1)	CP=1
T2, T1, T0	Test bits (See Table 5) Normal mode: T2=0, T1=0, T0=1/0	T2=0, T1=0, T0=0
RSA, RSB	Reference divider ratio selection bits (See Table 6)	RSA=0, RSB=1
OS	Tuning amplifier control bit Tuning voltage ON (OS=0) Tuning voltage OFF, high impedance (OS=1)	OS=0
BS4...BS1	Band switch ports control bits BSn=0:Tr=OFF BSn=1:Tr=ON Band selection by BS1, 2, 4 (x: don't care) BS1 BS2 BS4 VHF–Lo 1 0 0 VHF–Hi x 1 0 UHF x x 1	BSn=0
P8...P5	NPN open collector ports control bits Pn=0: Tr=OFF Pn=1: Tr=ON	Pn=0
X	Don't care	

NOTE: A: Acknowledge

Table 4. Address Selection

VOLTAGE APPLIED ON AS INPUT	MA1	MA0
0 V to 0.1 V_{CC}	0	0
Always valid	0	1
0.4 V_{CC} to 0.6 V_{CC}	1	0
0.9 V_{CC} to V_{CC}	1	1

Table 5. Test BIts

T2	T1	T0	FUNCTION	
0	0	0	Normal operation	Default
0	0	1	Normal operation	
0	1	X	Charge pump off	
1	1	0	Charge pump sink	
1	1	1	Charge pump source	
1	0	X	Test mode	Not available ADC

Table 6. Ratio Select Bits

RSA	RSB	REFERENCE DIVIDER RATIO
X	0	640
0	1	1024
1	1	512

I^2C Read Mode (R/W = 1)

Table 7. Read Data Format

	MSB							LSB	
Address byte (ADB)	1	1	0	0	0	MA1	MA0	R/W=1	A
Status byte (SB)	POR	FL	1	1	1	A2	A1	A0	A

NOTE: A: Acknowledge

Table 8. Description of Data Symbol

SYMBOL	DESCRIPTION	DEFAULT
MA1, MA0	Address set bits (see Table 4)	
POR	Power-on reset flag POR Set: Power on POR Reset: End-of-data transmission procedure	POR=1
FL	In-lock flag PLL lock (FL=1) Unlock (FL=0)	
A2...A0	Digital data of ADC (see Table 9)	

Table 9. ADC Level

VOLTAGE APPLIED ON ADC INPUT	A2	A1	A0
0.6 V_{CC} to V_{CC}	1	0	0
0.45 V_{CC} to 0.6 V_{CC}	0	1	1
0.3 V_{CC} to 0.45 V_{CC}	0	1	0
0.15 V_{CC} to 0.3 V_{CC}	0	0	1
0 V_{CC} to 0.15 V_{CC}	0	0	0

(1) Accuracy is 0.03 x V_{CC}.

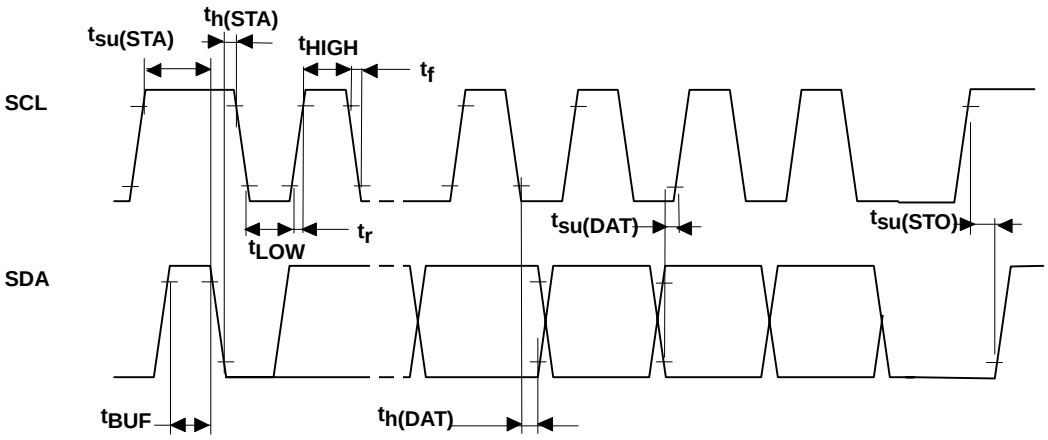
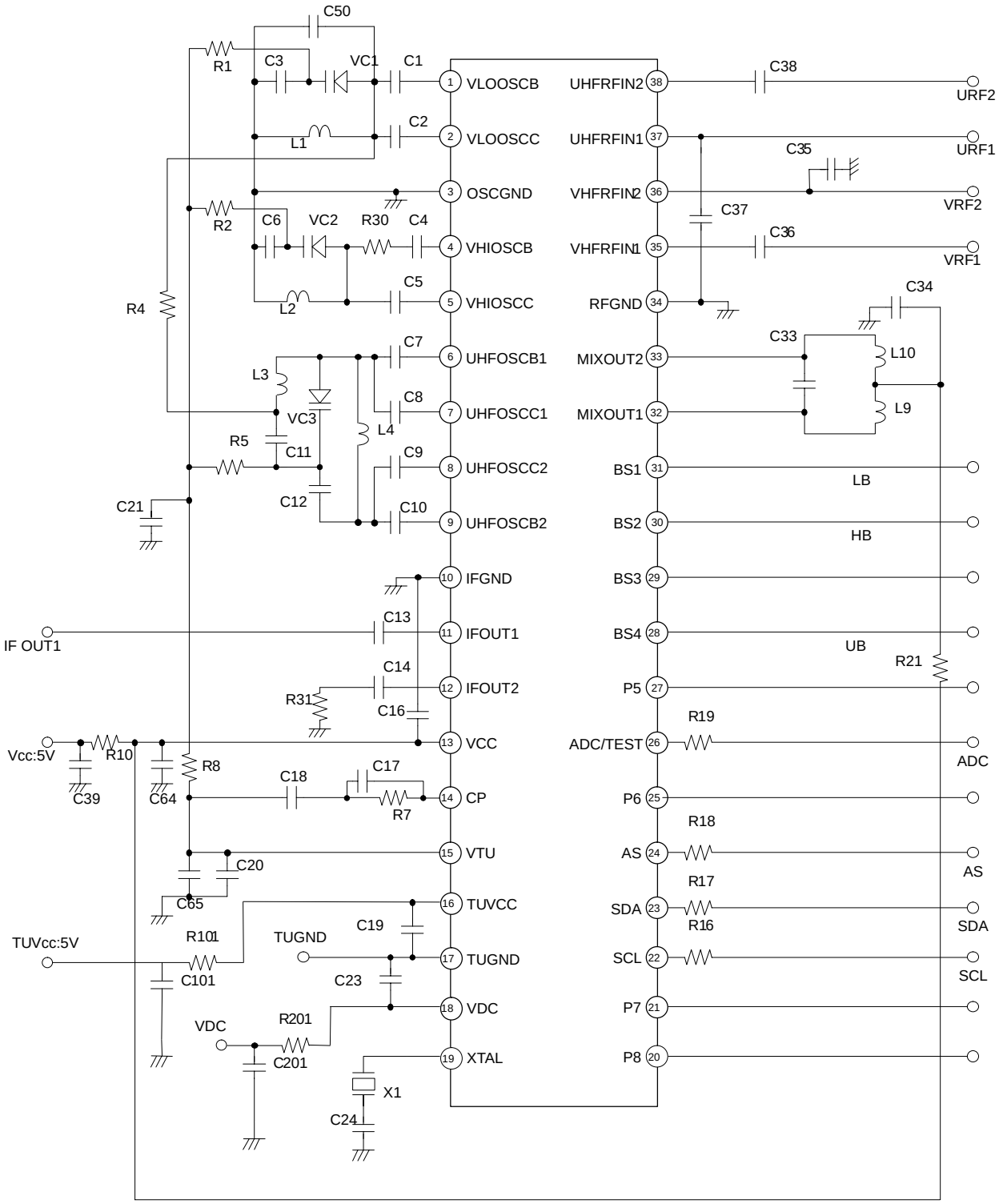


Figure 1. I²C Timing Chart

APPLICATION INFORMATION



(1) It is recommended that designers be careful with the PCB layout and coupling to minimize the effects of the higher harmonics of Xtal oscillation from the dc/dc converter section (pin 16–20) to mixer and oscillator section.

Figure 2. Reference Measurement Circuit

COMPONENT VALUES FOR MEASUREMENT CIRCUIT (TENTATIVE)

PART NAME	VALUE
C1, C2, C4	1 pF
C3	47 pF
C5	1.5 pF
C6	56 pF
C7–C10	1 pF (axial ceramic)
C11	100 pF
C12	13 pF (axial ceramic)
C13, C14, C16, C17, C19–C21, C34–C39, C64, C101	2.2 nF
C18, C23	0.047 μF
C24	68 pF
C33	18 pF
C41, C60, C62, C201	Not mounted
C50	3 pF
R1 , R2, R4, R5, R8	33 kΩ
R7	100 kΩ
R10, R21, R101, R201	0 Ω
R16–R19	330 Ω
R30	20 Ω
R31	50 Ω
L1	2.6ϕ, 8T, wire 0,3 mm
L2	2.4ϕ, 4T, wire 0,4 mm
L3	2.8ϕ, 2T, wire 0,4 mm
L4	2.1ϕ, 3T, wire 0,4 mm
L9, L10	2.5ϕ, 16T, wire 0,25 mm
VC1, VC2, VC3	1T363A
X1	4 MHz

TEST CIRCUIT

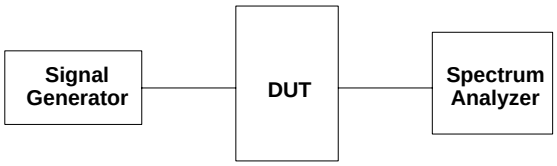


Figure 3. Measurement Circuit of Conversion Gain

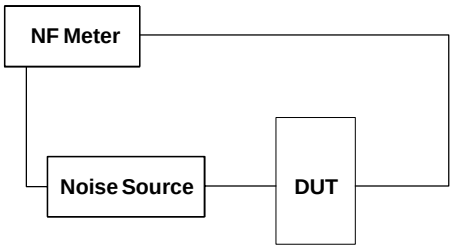


Figure 4. Noise Figure Measurement Circuit

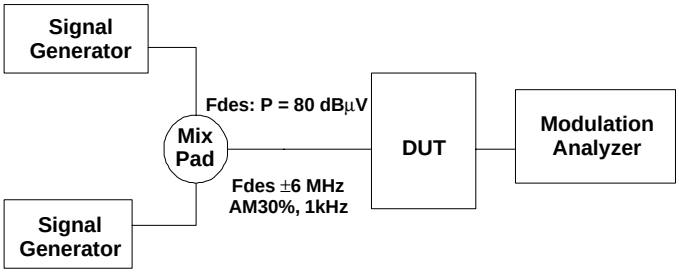


Figure 5. 1% Cross Modulation Distortion Measurement Circuit

S-PARAMETER

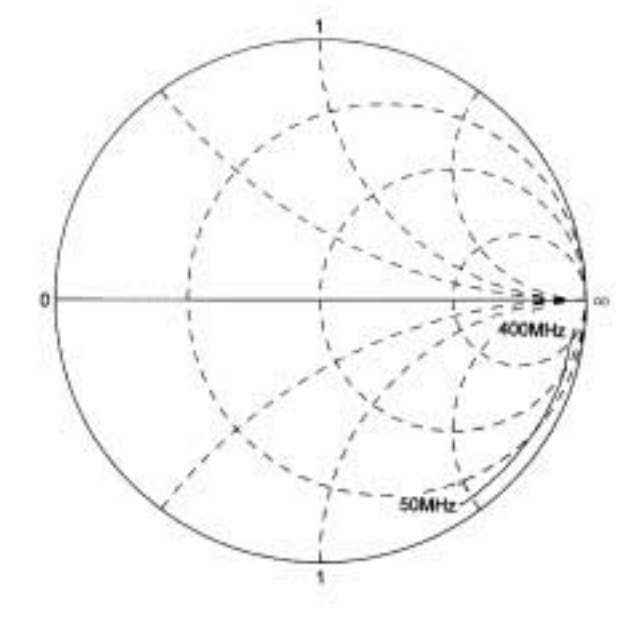


Figure 6. VHF Input

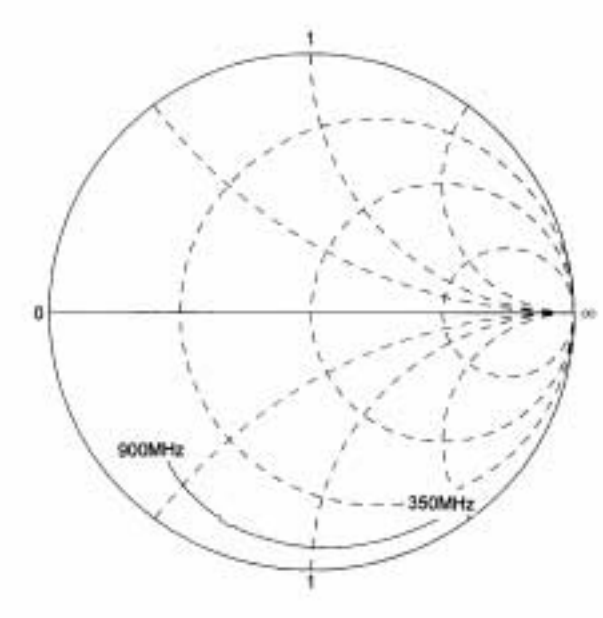


Figure 7. UHF Input

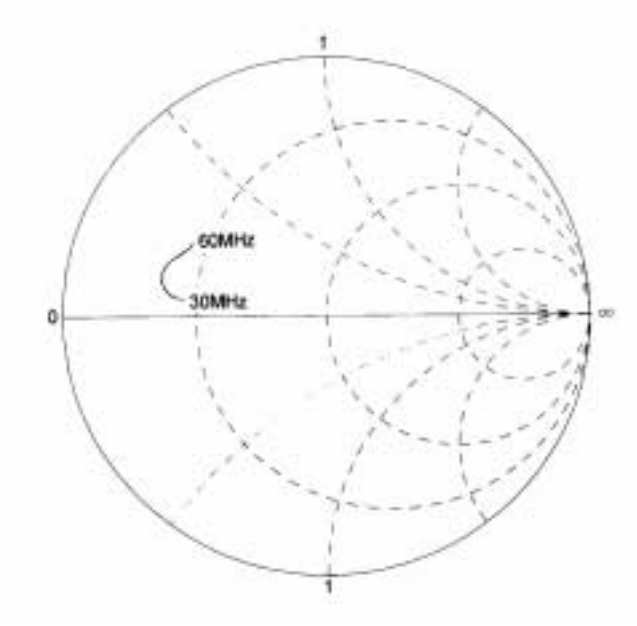


Figure 8. IF Output

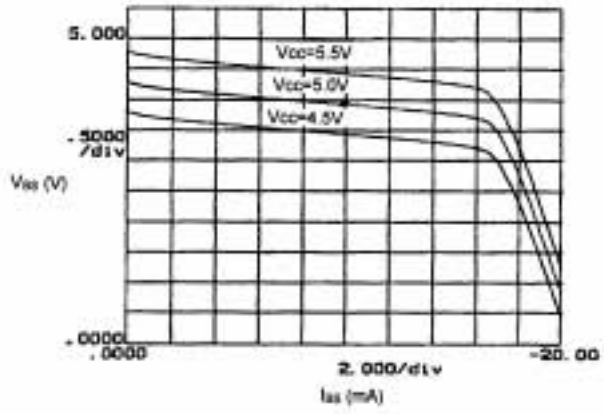


Figure 9. Band Switch Driver Output Voltage (BS1–BS4)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN761677DA	OBSOLETE	TSSOP	DA	38		TBD	Call TI	Call TI	-20 to 85	SN761677	
SN761677DAR	OBSOLETE	TSSOP	DA	38		TBD	Call TI	Call TI	-20 to 85	SN761677	
SN761677DARG4	OBSOLETE	TSSOP	DA	38		TBD	Call TI	Call TI	-20 to 85	SN761677	
SN761677DBTR	OBSOLETE	TSSOP	DBT	38		TBD	Call TI	Call TI		B1677	
SN761677DBTRG4	OBSOLETE	TSSOP	DBT	38		TBD	Call TI	Call TI		B1677	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

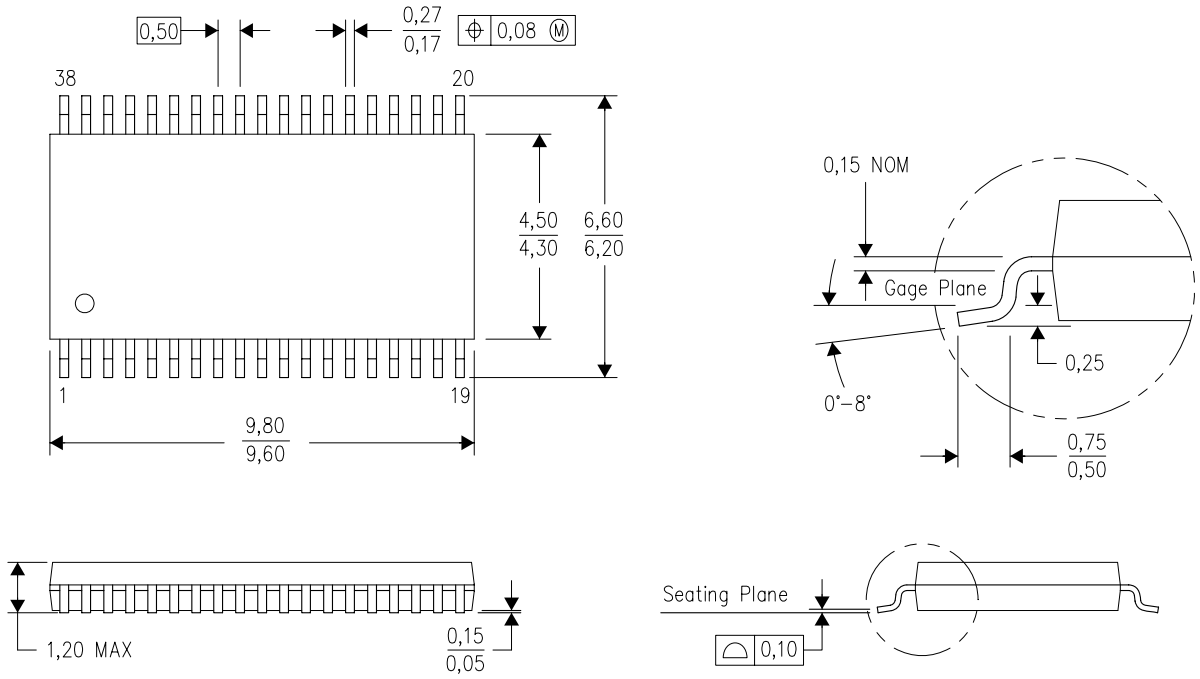
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

DBT (R–PDSO–G38) PLASTIC SMALL OUTLINE

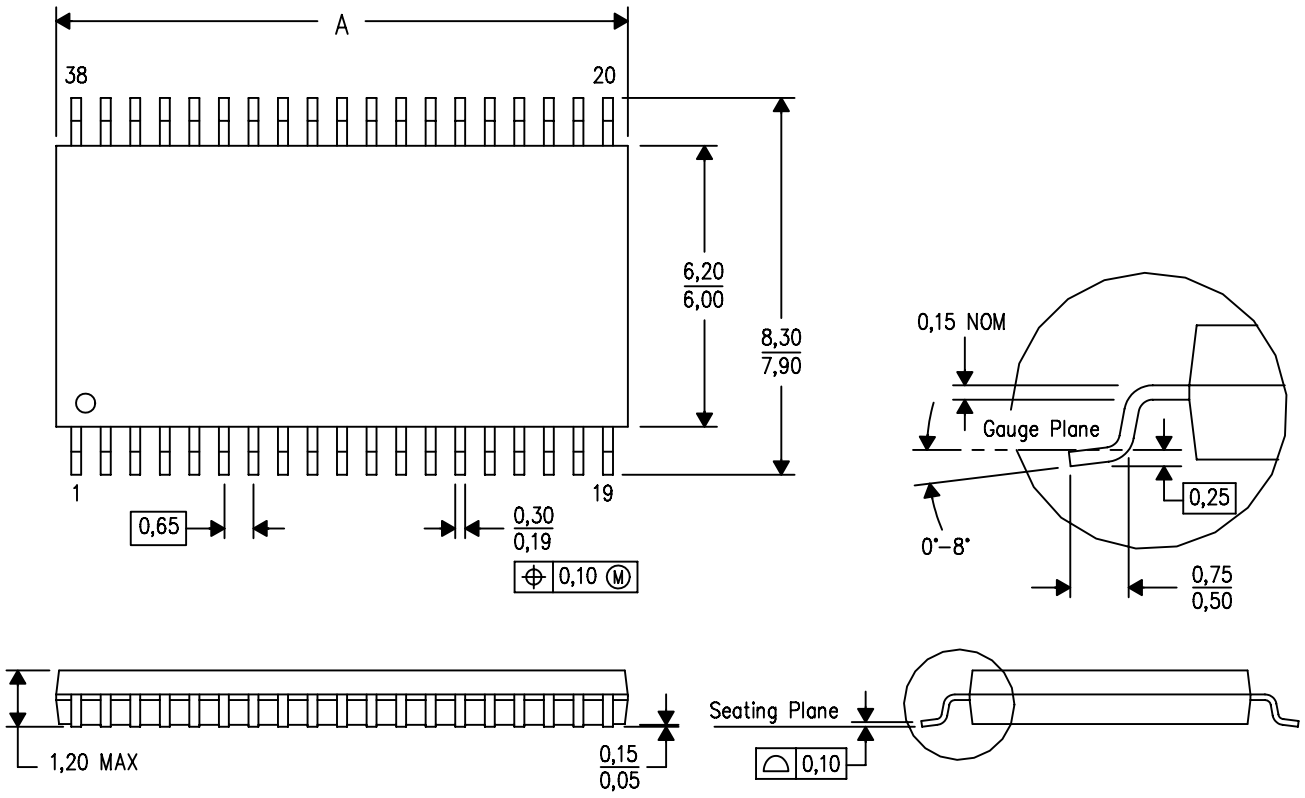


4073252-6/I 03/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–153.

DA (R–PDSO–G**) PLASTIC SMALL–OUTLINE PACKAGE

38 PIN SHOWN



DIM \ PINS **	30	32	38
A MAX	11,10	11,10	12,60
A MIN	10,90	10,90	12,40
△D MO–153 Variation	DB–1	DC	DD–1

4040066/F 01/2009

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
△D Falls within JEDEC MO–153, except 30 pin body length.

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