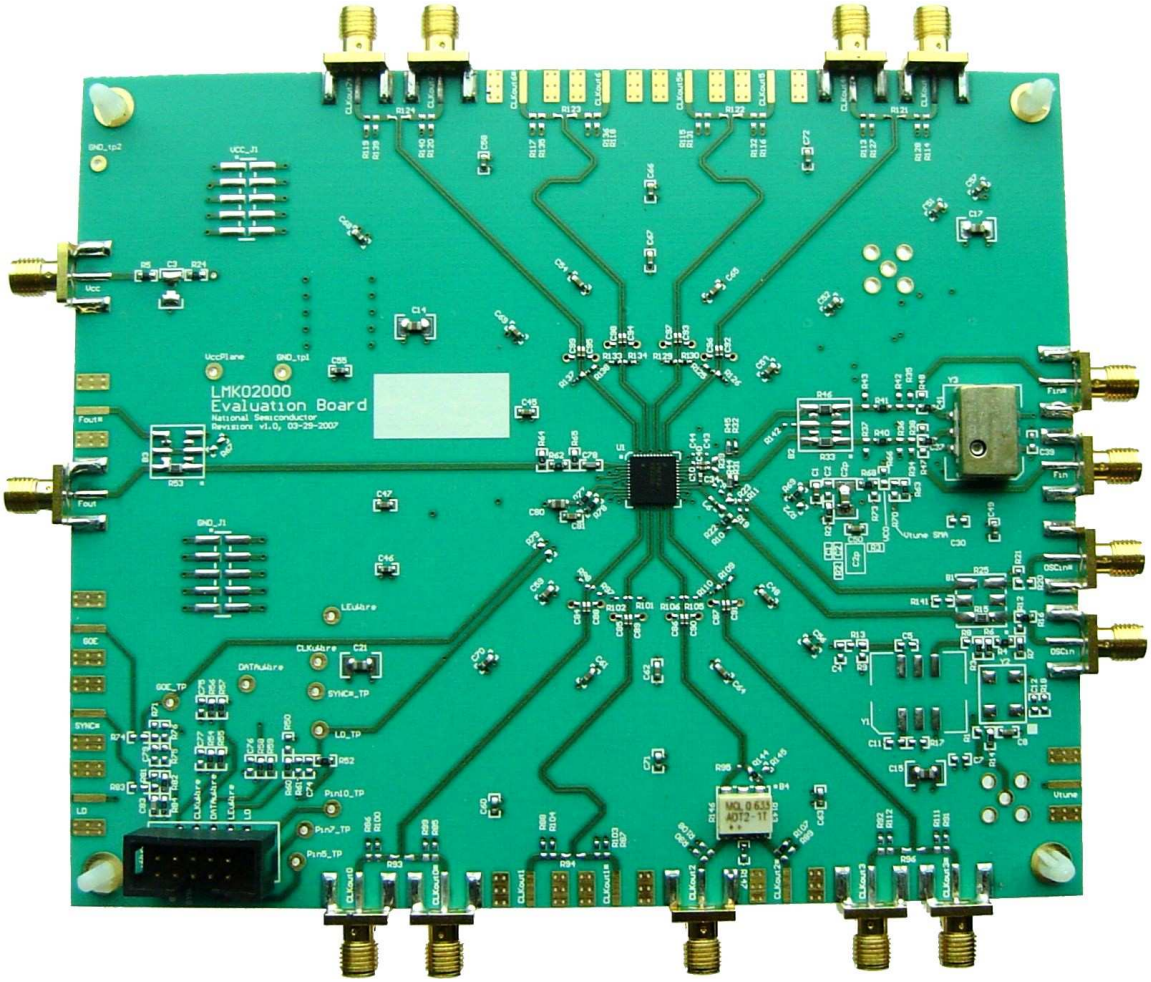
National Semiconductor

LMK02000

Precision Clock Conditioner
Evaluation Board Operating Instructions

5-9-2007



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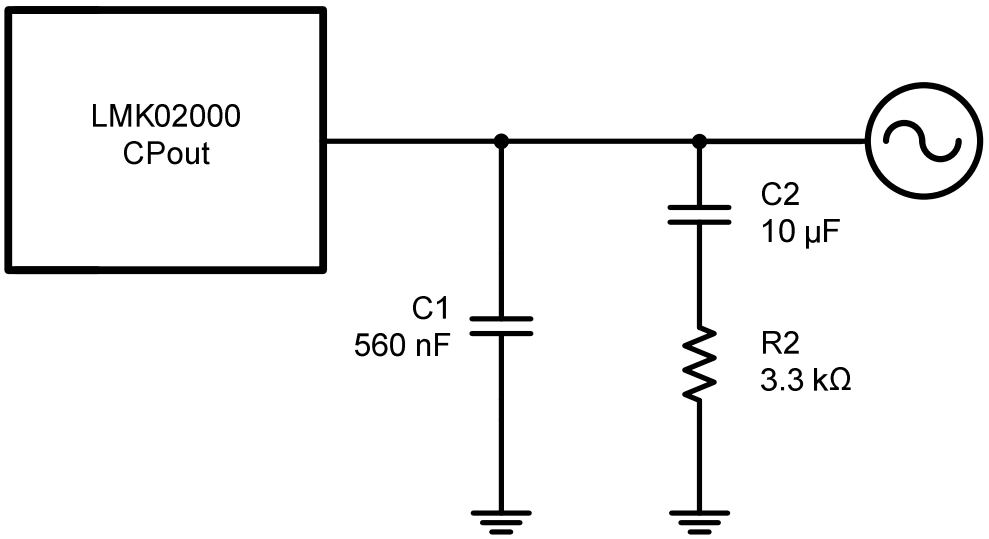
General Description

The LMK02000 Evaluation Board simplifies evaluation of the LMK02000 Precision Clock Conditioner. The package consists of an evaluation board, an LPT to 10 pin uWire cable, and CodeLoader software. The *CodeLoader* software will run on a Windows 2000 or Windows XP PC. The purpose of the *CodeLoader* software is to program the internal registers of the LMK02000 device through a MICROWIRE™ interface.

Loop Filter #1			
Phase Margin	64º	**Kϕ**	400 uA
Loop Bandwidth	20 Hz	**Fcomp**	1.2288 Mhz
Crystal Frequency	12.288 MHz	**Output Frequency**	246.76 MHz
Supply Voltage	3.3 Volts	**VCO Gain**	20 kHz/Volt



Loop filter #1 is selected by placing a 0 ohm resistor on pads R68 and R69.

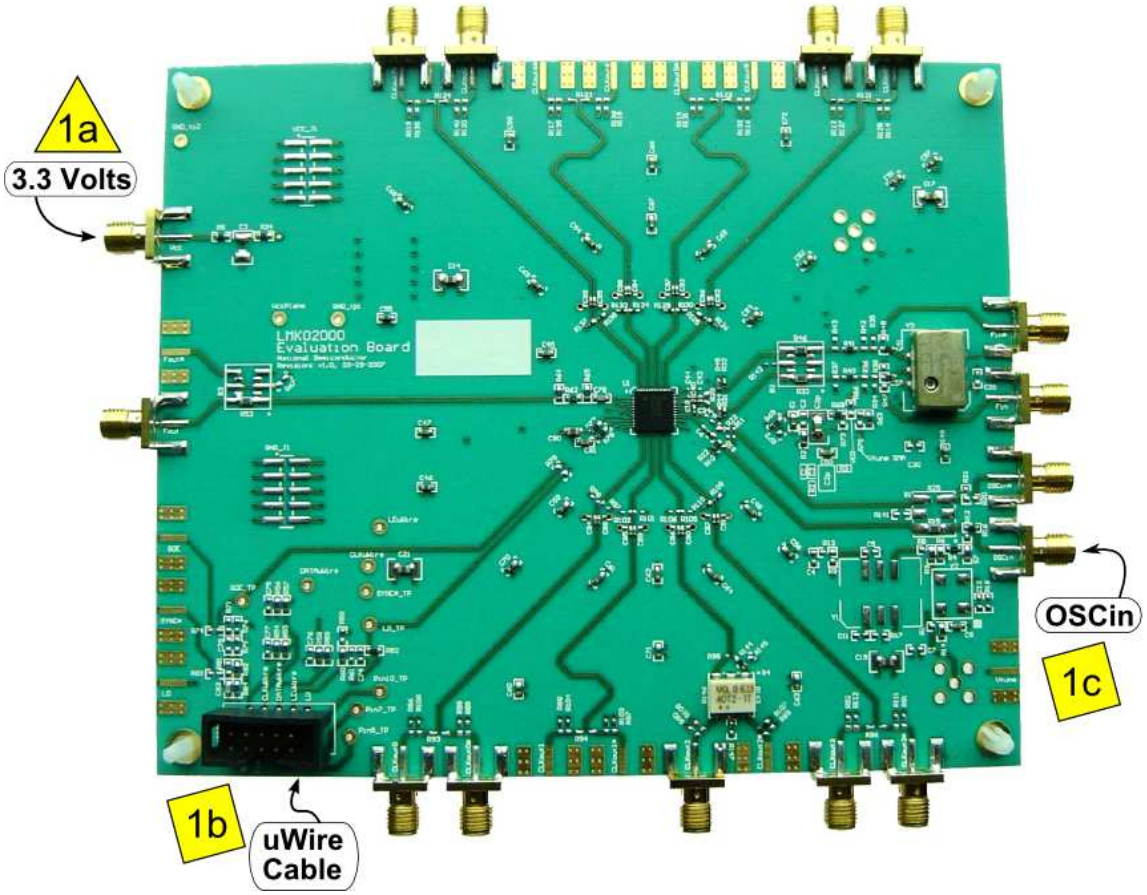
Loop filter #2 is selected by placing a 0 ohm resistor on pads R72 and R73 and is provided for user convenience. That is, to experiment with a new loop filter while not changing the factory default.

Read first, Basic Operation

To prepare the computer for use with the evaluation board CodeLoader4 must be installed. Reference the document, *"Installing CodeLoader 4"* and *"Installing USB Driver"* as needed to assist in this task before continuing with the hardware setup.

For basic operation…

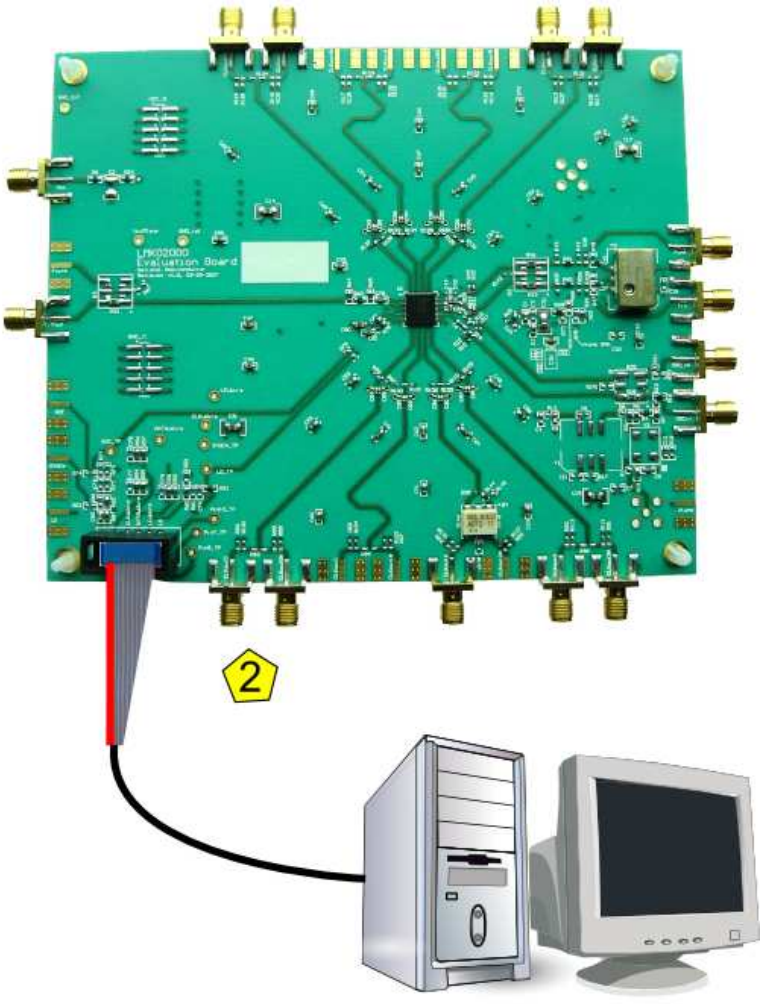
1) Setup hardware
   a) Connect a low noise **3.3 V** power supply to the **Vcc** connector located at the top left of the board
   b) Connect the LPT to 10 pin uWire cable to the **uWire** header located in the lower left.
   c) Connect a suitable reference oscillator to OSCin. The default loop filter expects a 12.288 MHz signal. If a signal generator is used, set the power level on a signal generator to 8 dBm.



Read first, Basic Operation (Continued)

2) Connect…
   - PC directly to the evaluation board with the LPT to 10 pin uWire cable, plugging the cable into an LPT port on the computer. This setup is shown below. **The cable can be removed after programming to minimize noise and EMI.**

     or
   - Available separately, the USB <--> uWire board can be connected to the PC with a USB cable. The board provides a 10 pin ribbon cable to connect to the uWire header on the evaluation board as done in step 1b (instead of the LPT to 10 pin uWire cable).



LPT Cable to PC

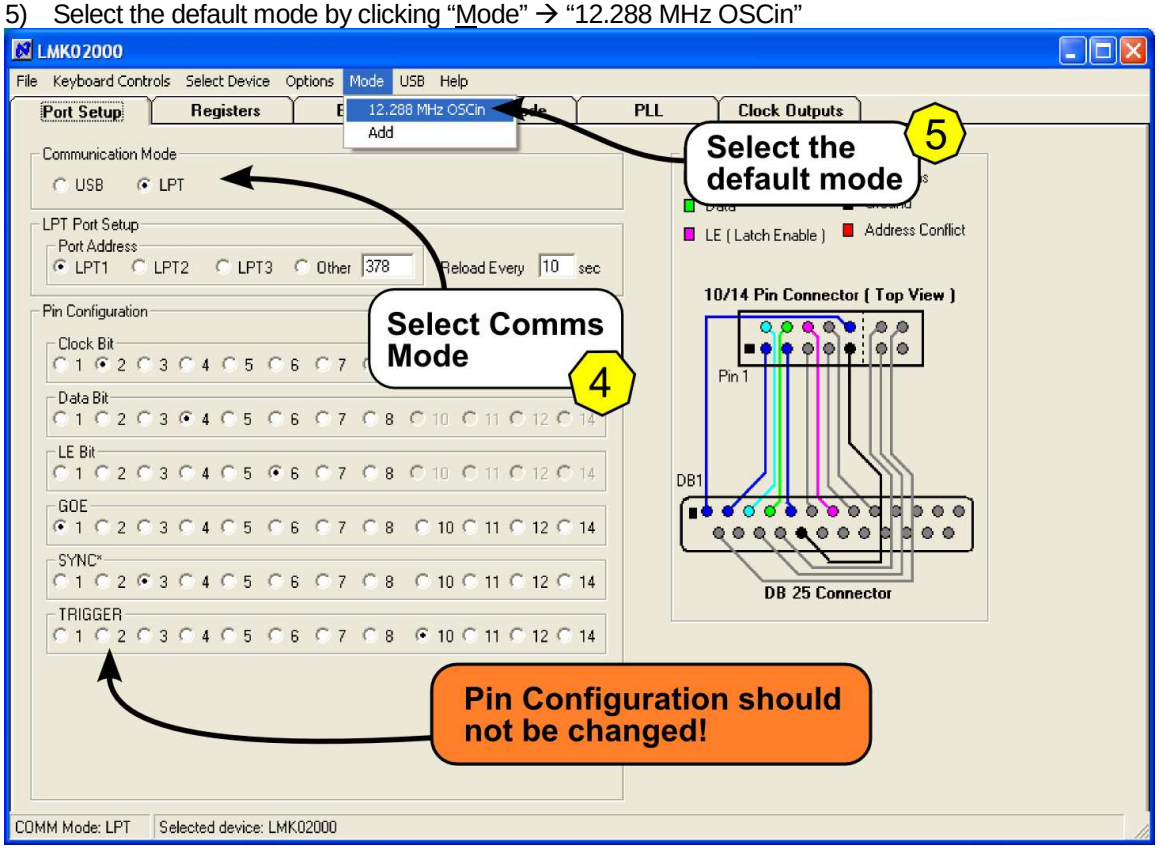
LPT Setup

Read first, Basic Operation (Continued)

3) Start CodeLoader 4.

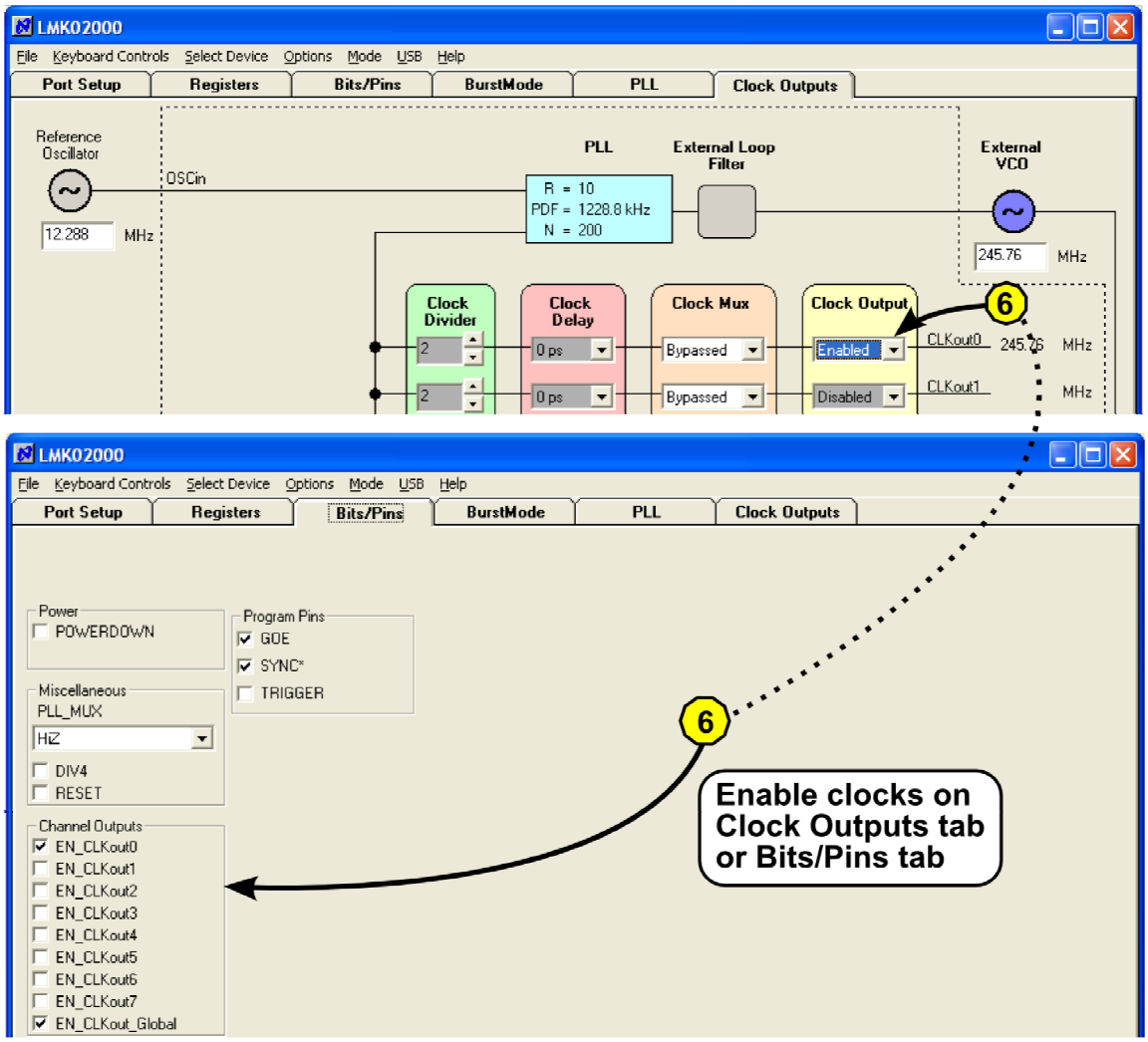
4) Select the USB or LPT Communication Mode on the Port Setup tab as appropriate.

5) Select the default mode by clicking "Mode" → "12.288 MHz OSCin"

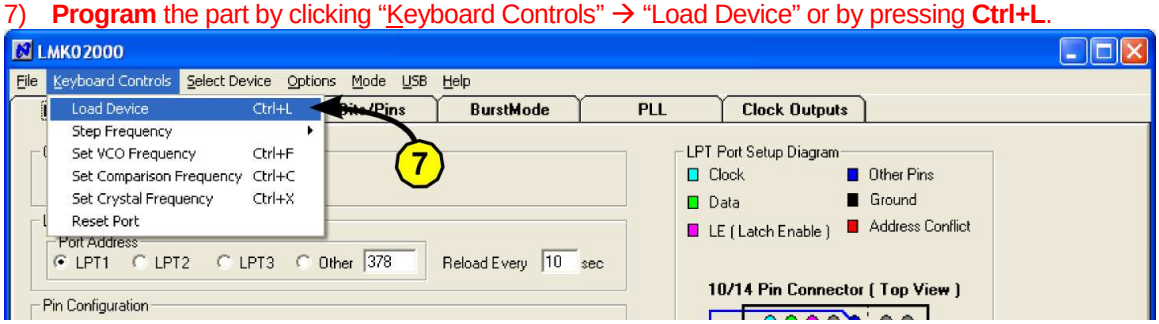


Read first, Basic Operation (Continued)

6) **Enable output to be measured**, any of CLKout(0-7) or EN_Fout from either Clock Outputs or Bits/Pins tab.



7) **Program** the part by clicking "Keyboard Controls" → "Load Device" or by pressing **Ctrl+L**.



8) Make measurements… After programming, the **uWire cable can be unplugged from the evaluation board to minimize noise and EMI.**

Board Information

OSCin

By default the board is configured to use an off board reference. It is also possible to use the board with a single ended or differential reference source at the OSCin port. Below are several possible configurations for driving OSCin.

Single ended OSCin using off board reference [default]	
0 ohm	R15, R16
51 ohm	R22
0.1 uF	C6, C10 (C9 is a 0.1 uF 0402 cap which may be moved to C10)
Open	C9 R12 R9, R13, R1, R14 (if a TCXO is placed, open these resistors to remove power from on-board oscillator for noise reasons)
No Effect	R3, R4, R6, R7, R8

Differential OSCin using off board reference	
0 ohm	R15, R16, R20, R25
100 ohm	R23 (other termination options are possible with R10, R11, R19, R22)
0.1 uF	C6, C9 (C10 is a 0.1 uF 0402 cap which may be moved to C6)
Open	C4, C36 R11, R12, R14, R15, R16, R79 R9, R13, R1, R14 (if a TCXO is placed, open these resistors to remove power from on-board oscillator for noise reasons)
No Effect	R3, R4, R6, R7, R8

Loop Filter

The PCB allows for two separate loop filters to be placed. Loop Filter #1 is the factory default. Loop Filter #2 allows for experimentation with a new loop filter while not altering the factory default loop filter. Four resistors switch loop filter #1 or #2 into the circuit.

Loop Filter	**Resistor Switch**	**Loop Filter Components**	**Default Loop Bandwidth**
Loop Filter #1 [default]	R68 & R69 shorted	C1, C2, C2p, R2	20 Hz
Loop Filter #2 [aux]	R72 & R73 shorted	C1_AUX, C2_AUX, C2p_AUX, R2_AUX	No filter placed

Global Output Enable (GOE) pin

The evaluation board has removed the resistors connecting GOE to the CodeLoader cable so the clock outputs are defaulted on all the time, therefore the GOE pin in CodeLoader has no effect. This way the CodeLoader cable can be removed from the board to reduce noise for measurements. To add GOE functionality, place a 15 k resistor on R76 and a 27 k resistor on R75.

Features of the board

- Either one of two loop filters can be selected by shorting either (R68 & R69 or R72 & R73).
- Test points for each of the uWire lines are scattered in the lower left corner of the board and include: GOE_TP, DATAuWire, CLKuWire, LEuWire, SYNC_TP, and LD_TP.

- **Ground** is located on the unstuffed 10 pin header on the left side of the board.
- **Ground** is located on the GND_tp2 in the upper left corner of the board and GND_tp1 located to the right of the Vcc SMA connector.
- **Ground** is located on the bottom side of the board on each pad of the unstuffed 10 pin header GND_J2.

- **Vcc** is located on the unstuffed 10 pin header on the upper left side of the board.
- **Vcc** is located on VccPlane test point located to the right of the Vcc SMA.
- **Vcc** is located on the bottom side of the board on each pad of the unstuffed 10 pin header VCC_J2

Other Important Notes

- Board v1.0, 3-29-2007 ERRATA: B4 pin 1 is flipped. Pin 1 should be next to CLKout2 SMA. Not B4 label as shown.
- Toggle the SYNC* pin to synchronize the clock outputs when in divided mode.
- For both loop filters, a helper silkscreen is offset from the loop filters to help identify the components according to National Semiconductor's traditional reference designators associated with loop filters.

Recommended Equipment

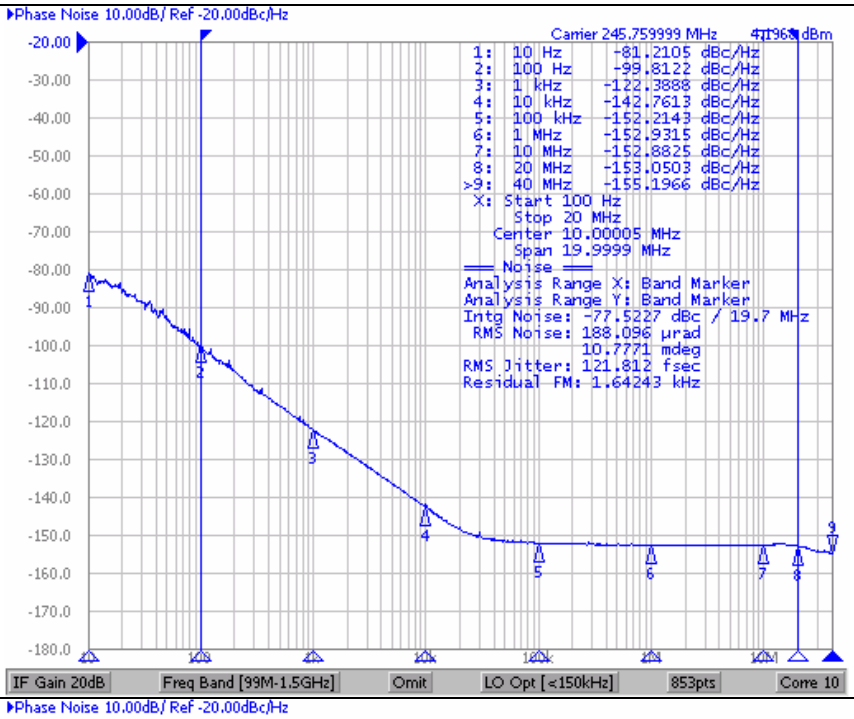
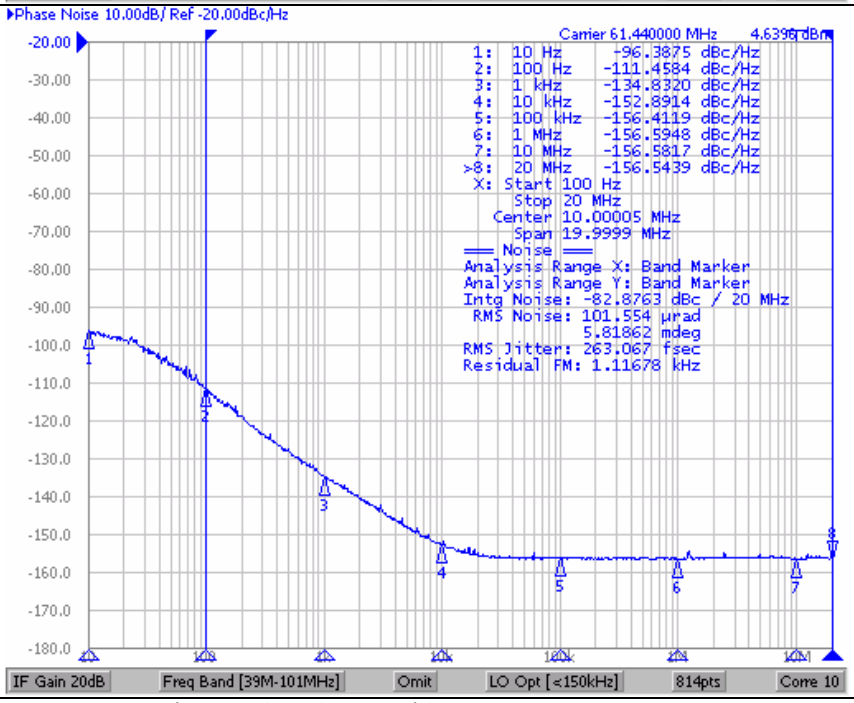
Power Supply
The Power Supply should be a low noise power supply. An Agilent 6623A Triple power supply with external LC filters or an HP E3610A with external LC filters was used in creating these evaluation board instructions. The LC filters on the outputs help to reduce noise from the power supplies.

Phase Noise / Spectrum Analyzer
Due to the high performance of the LMK02000 and VCXO the local oscillator noise of most spectrum analyzers is too high and measurements will be of the local oscillator of the spectrum analyzer, not the LMK02000/VCXO under test. An Agilent E5052A was used for all phase noise measurements in this document.

Oscilloscope
For measuring delay an Agilent Infiniium DSO81204A was used.

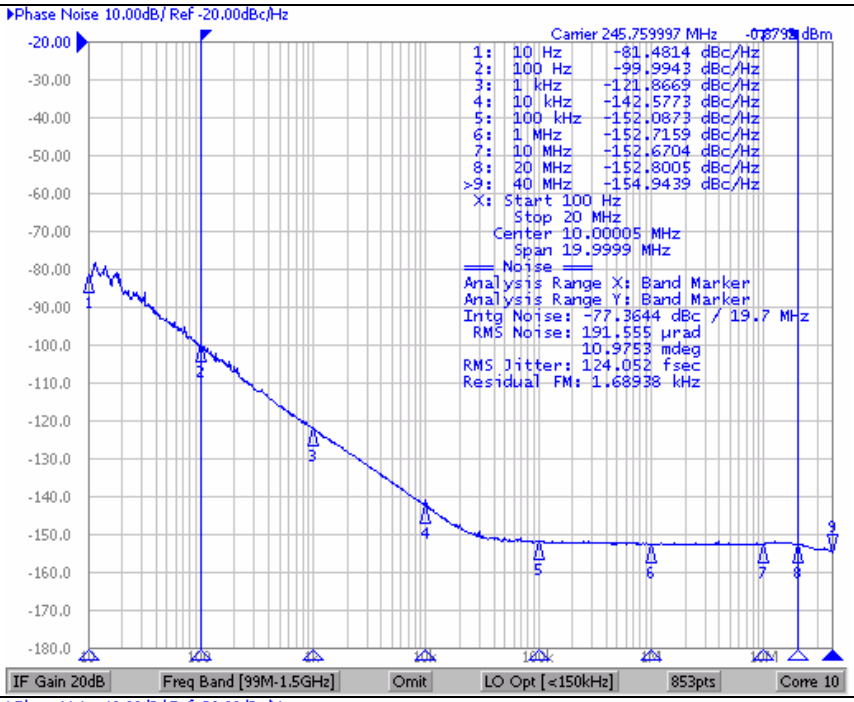
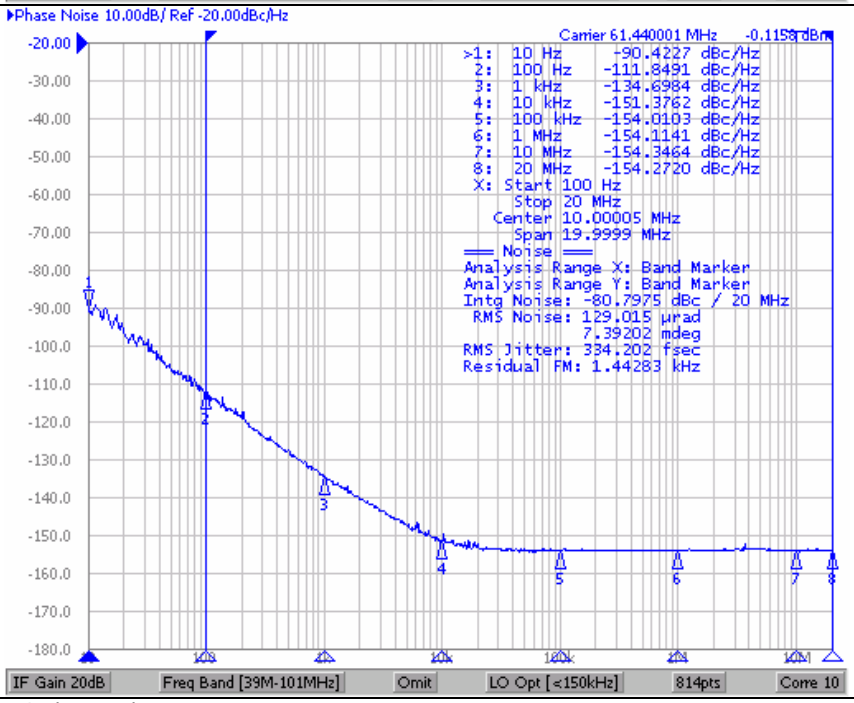
Reference Oscillator
A recovered clock (LVDS or LVPECL) may drive OSCin. If a signal generator (sine wave) is used, program the power to 8 dBm to ensure a fast slew rate.

Phase Noise

CLKout4 LVPECL output, Bypass, 245.76 MHz TCO-2111-AA, 245.76 VCXO		Reference source signal generator at 12.288 MHz at 10 dBm 10 Hz – 20 MHz integrated RMS jitter = 300.8 fs **100 Hz – 20 MHz integrated RMS jitter = 121.8 fs** 1 kHz – 20 MHz integrated RMS jitter = 96.1 fs 10 kHz – 20 MHz integrated RMS jitter = 93.8 fs 100 kHz – 20 MHz integrated RMS jitter = 93.5 fs
LVPECL output CLKout4 VCXO Frequency = 245.76 MHz, CLKout4_div=4 LVPECL output (61.44 MHz)		Reference source signal generator at 12.288 MHz at 10 dBm 10 Hz – 20 MHz integrated RMS jitter = 360.8 fs **100 Hz – 20 MHz integrated RMS jitter = 263.1 fs** 1 kHz – 20 MHz integrated RMS jitter = 251.9 fs 10 kHz – 20 MHz integrated RMS jitter = 251.0 fs 100 kHz – 20 MHz integrated RMS jitter = 250.4 fs

A note on jitter measurements between 245.76 MHz and 61.44 MHz

Theoretically jitter after a divider will be the same as the jitter before the divider because the benefit gained from a lower phase noise curve will be offset by the lower frequency. In the plots above the jitter for 245.76 MHz from 100 Hz to 20 MHz is 121.8 fs. The jitter for 61.44 MHz (after a divide by 4) from 100 Hz to 20 MHz is 263.1 fs. The reason the 61.44 MHz jitter is not also ~121.8 fs is the phase noise curve didn't gain 12 dB along the entire integrated bandwidth because the residual noise floor of the outputs was reached.

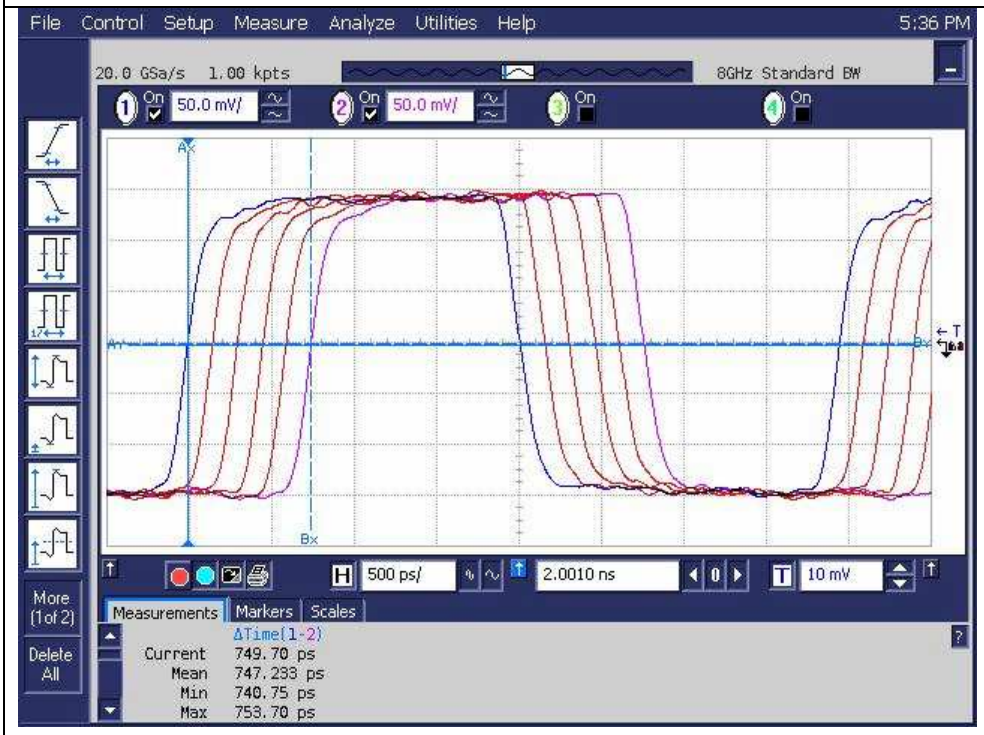
CLKout4 LVDS output, Bypass, 245.76 MHz TCO-2111-AA, 245.76 VCXO		Output is measured with a Minicircuits ADT2-1T balun. Reference source signal generator at 12.288 MHz at 10 dBm 10 Hz – 20 MHz integrated RMS jitter = 335.8 fs **100 Hz – 20 MHz integrated RMS jitter = 124.7 fs** 1 kHz – 20 MHz integrated RMS jitter = 98.8 fs 10 kHz – 20 MHz integrated RMS jitter = 96.6 fs 100 kHz – 20 MHz integrated RMS jitter = 96.2 fs
LVDS output CLKout2 VCXO Frequency = 245.76 MHz, CLKout2_div=4 LVDS output (61.44 MHz)		Output is measured with a Minicircuits ADT2-1T balun. Reference source signal generator at 12.288 MHz at 10 dBm 10 Hz – 20 MHz integrated RMS jitter = 483.8 fs **100 Hz – 20 MHz integrated RMS jitter = 334.2 fs** 1 kHz – 20 MHz integrated RMS jitter = 326.1 fs 10 kHz – 20 MHz integrated RMS jitter = 325.3 fs 100 kHz – 20 MHz integrated RMS jitter = 324.6 fs

A note on LVDS phase noise

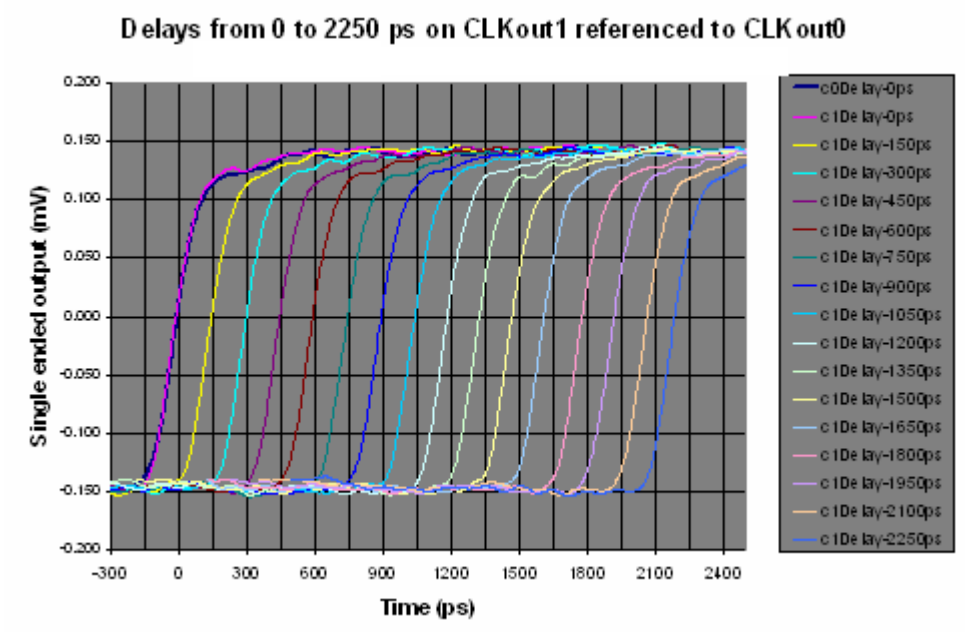
LVDS drivers expect a 100 ohm differential load for optimal phase noise performance. We recommended that a balun be used when making single ended (unbalanced) measurements (like the phase noise measurements above).

Delays

These delay measurements illustrate how skew errors due to different length traces may be tuned out.
The delay may be adjusted in steps of 150 ps.



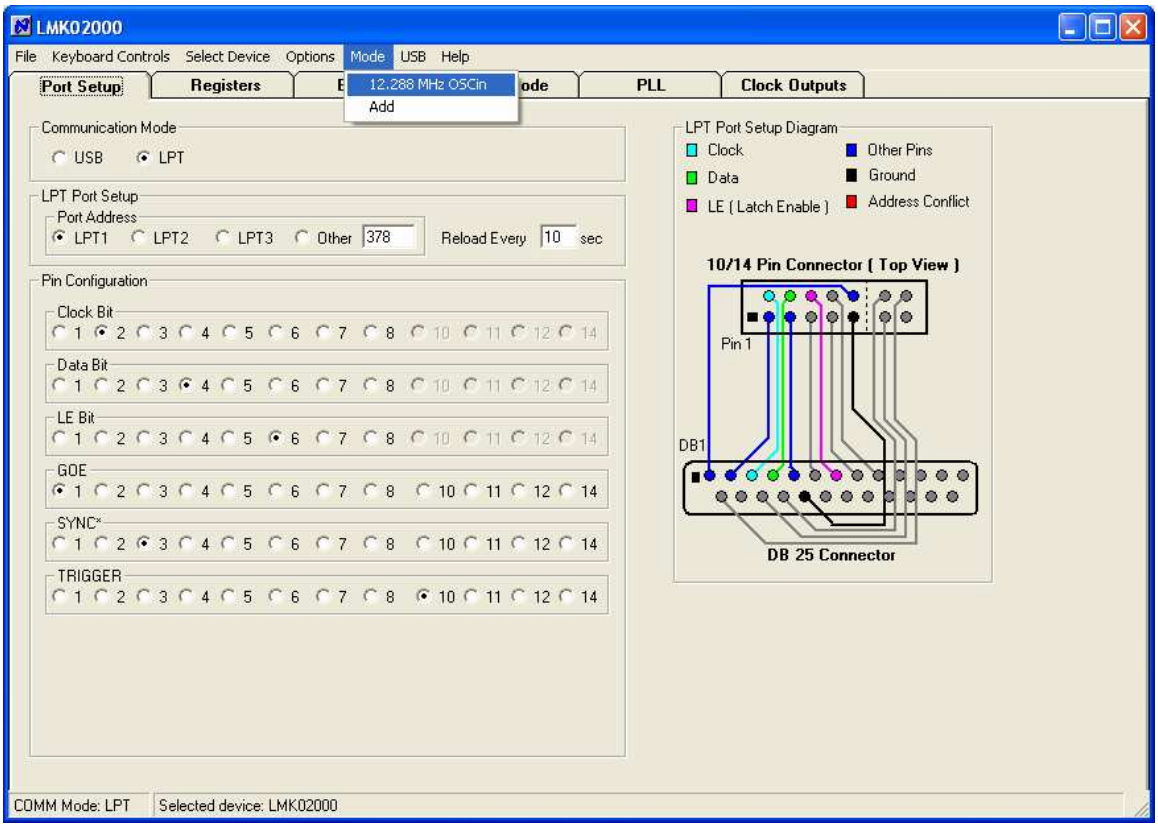
Delays 150, 300, 450, 600, 750



CLKout0_DLY = 0 ps

CLKout1_DLY = all delays programmed: 0, 150, 300, 450, 600, 750, 900, 1050, 1200, 1350, 1500, 1650, 1800, 1950, 2100, and 2250 ps

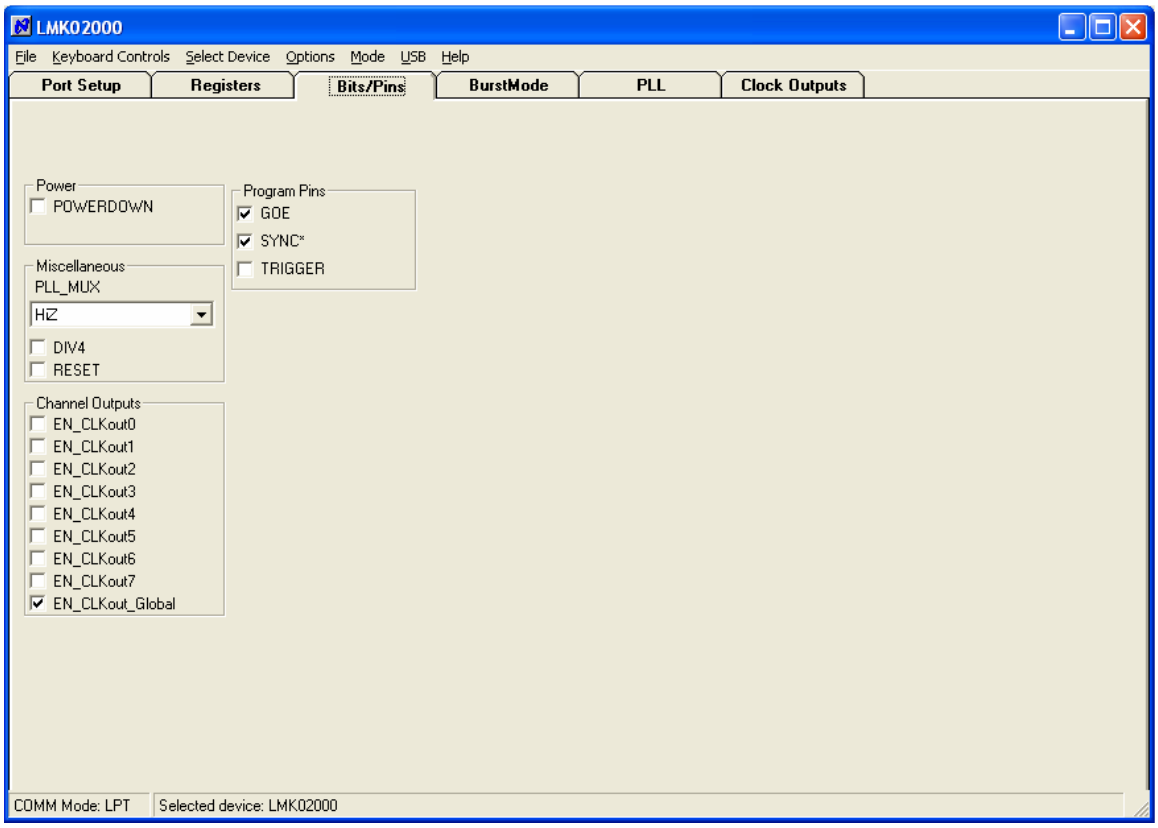
CodeLoader Settings



The Port Setup tab tells CodeLoader what signals are assigned to which pins. If this is wrong, the part will not program.

The default mode for all programming registers can be restored to the default state by clicking Mode → "12.288 MHz OSCin" The default reference oscillator used for these instructions is 12.288 MHz and the restored mode expects a 12.288 MHz OSCin signal. **For the loaded mode to take affect the device must be loaded by pressing Ctrl+L.** However, this will not restore the default Pin Configuration. If any Pin Configuration settings are accidentally changed, refer to the above diagram to fix the Pin Configuration.

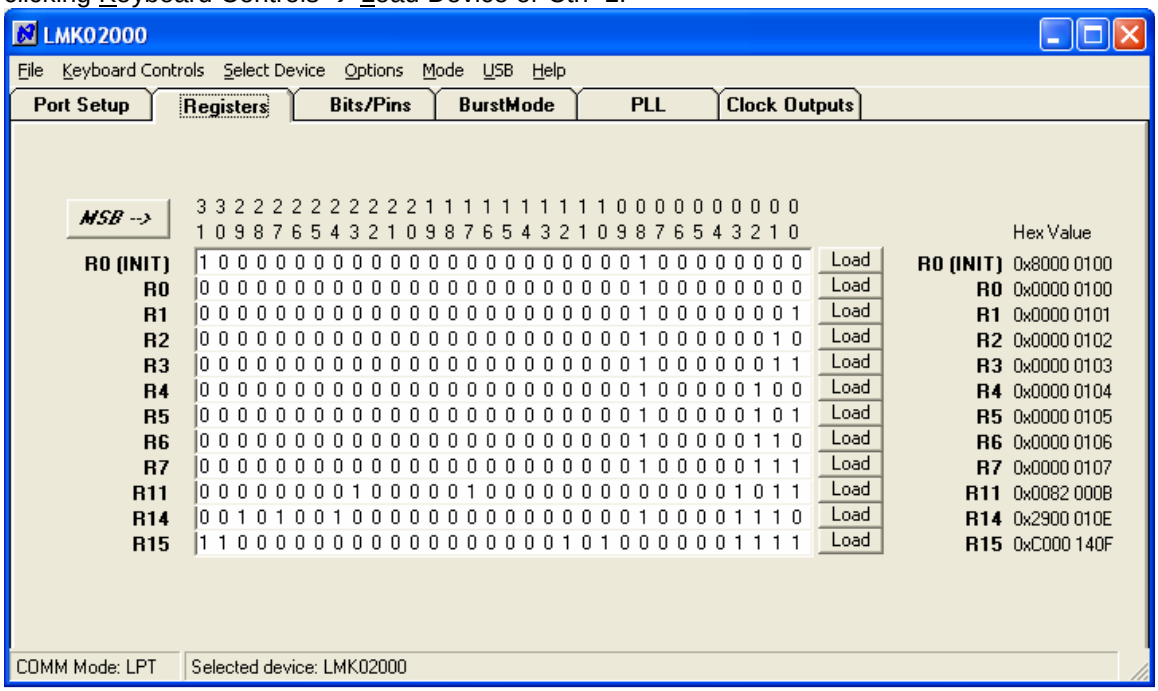
The Bits/Pins tab shows some of the internal registers which are not accessible from any of the other visual tabs like “PLL” and “Clock Outputs.” *Right click on any of the bits for description.*



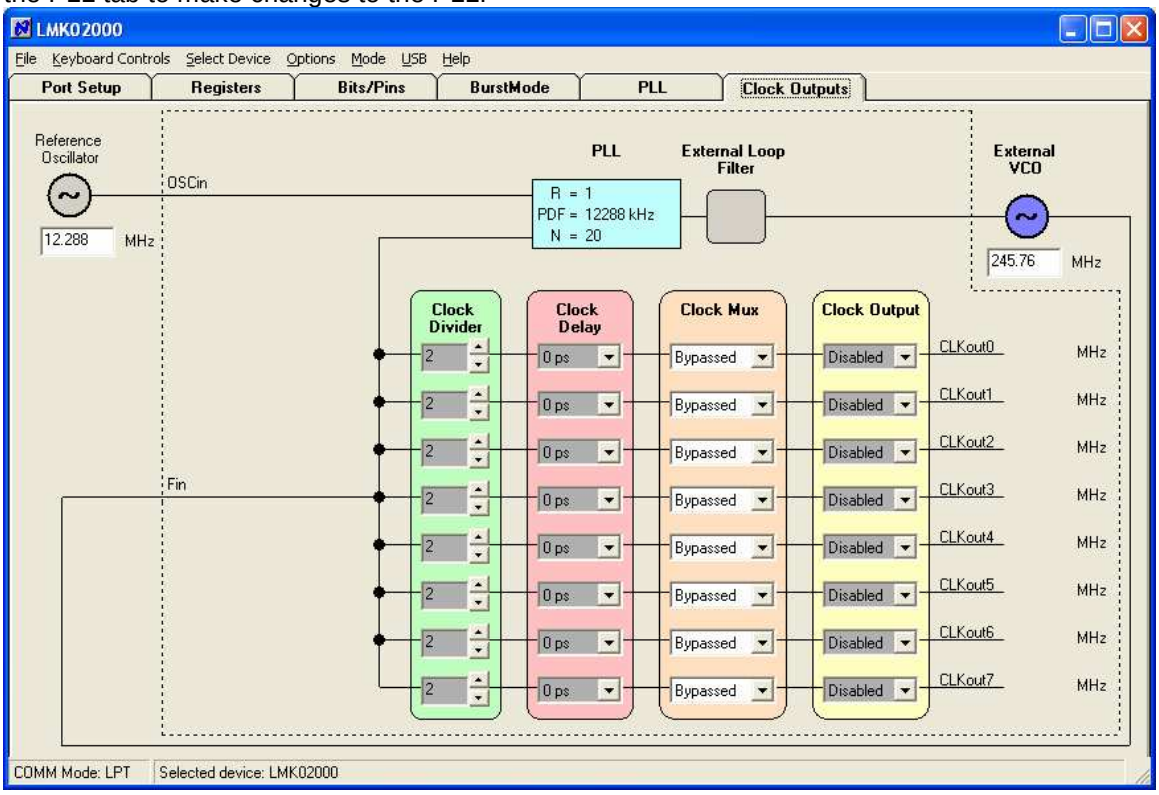
Program Bits	
POWERDOWN	Powers the part down.
PLL_MUX	Programmable to many different values to support Lock Detect or aid troubleshooting.
DIV4	Shall be checked for PDF frequencies greater than 20 MHz.
RESET	The registers can be defaulted by checking and unchecking RESET. Software bits will not reflect this.
EN_CLKout0..7	Enable CLKout bits from CLKout0 to CLKout7. Also accessible from Clock Outputs tab.
EN_CLKout_Global	Enable all clock outs. If unselected then the EN_CLKouts are overridden and the outputs are all disabled.

Program Pins	
GOE	Set Global Output Enable to high or low logic level. **GOE is not used.** See Board Information section for usage of this pin.
SYNC*	Set SYNC* pin to high or low logic level.
TRIGGER	Set auxiliary trigger pin to high or low logic level.

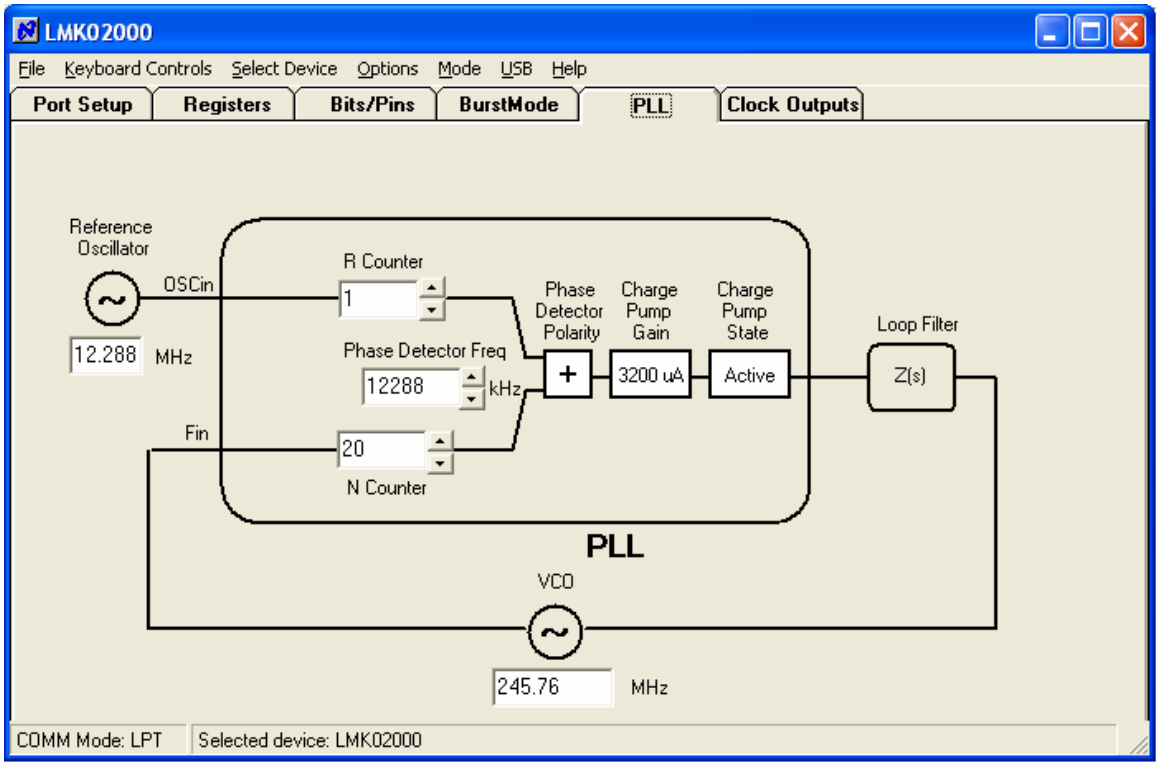
The Registers tab shows the raw bits which will be programmed when device is loaded by clicking Keyboard Controls → Load Device or Ctrl+L.



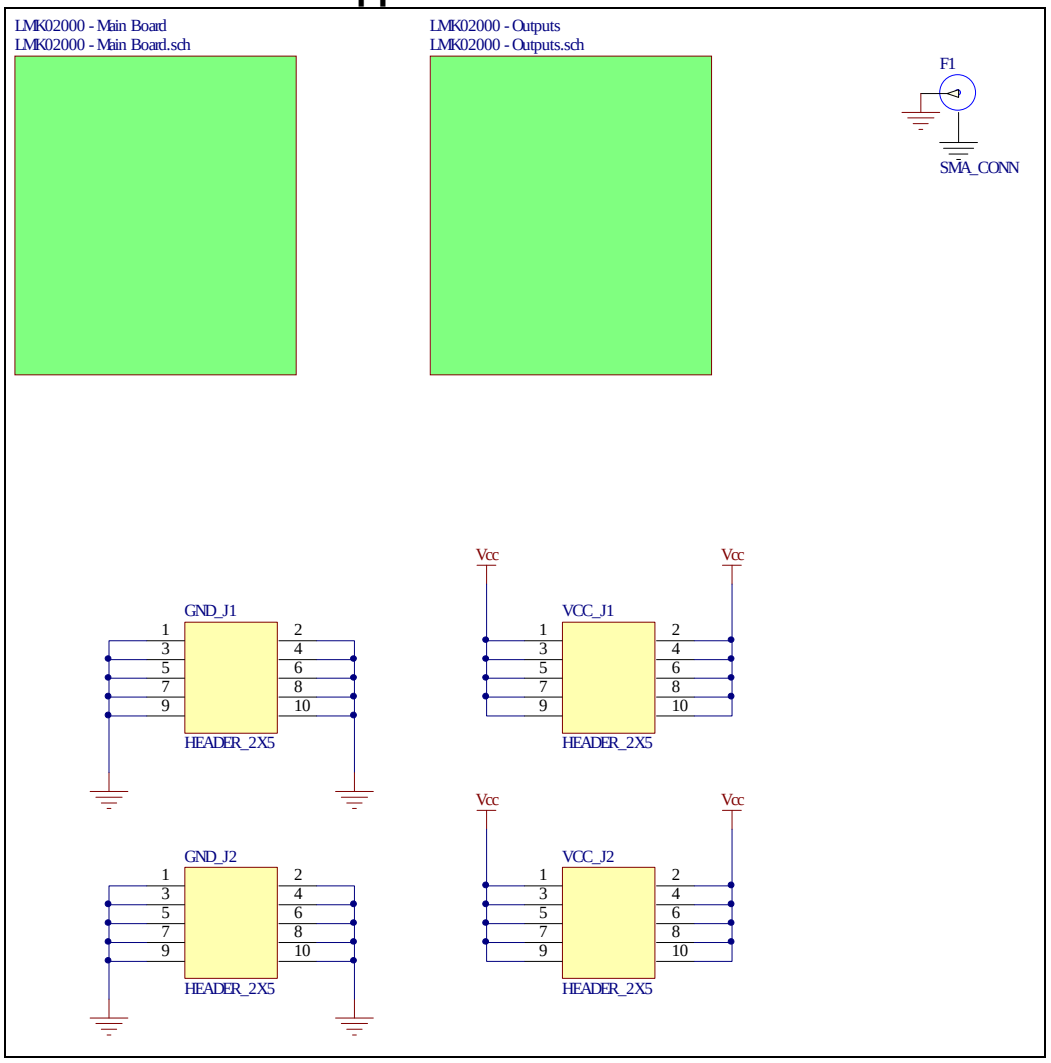
The Clock Outputs tab allows the user to visualize the clock distribution portions of the device. From this tab the device's dividers, delays, clock output muxes, and output drivers can be programmed along with internal loop filter values. The PLL block shows the R and N divider values however to change these values either click on the PLL tab or the blue PLL box to access the PLL tab to make changes to the PLL.

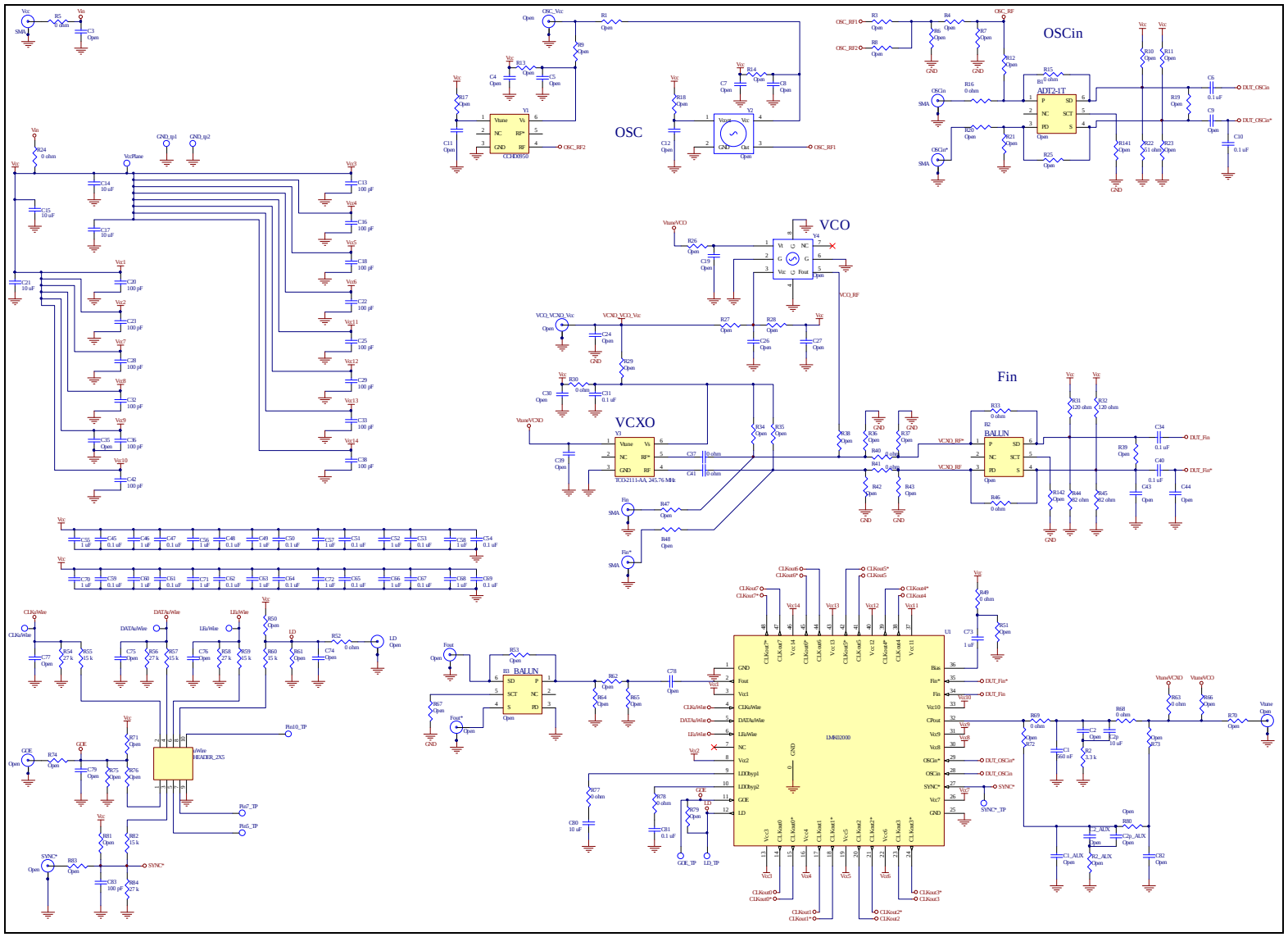


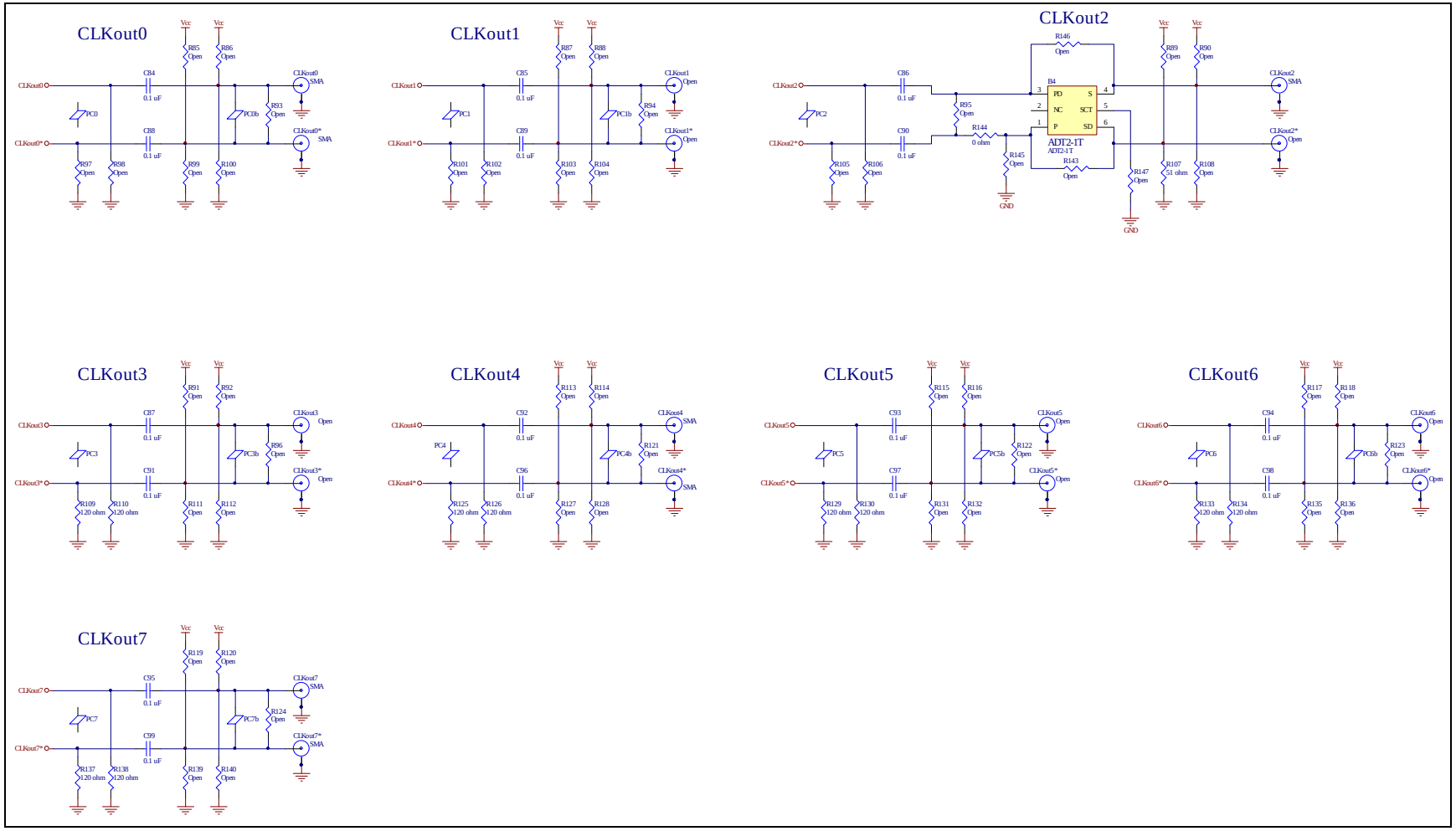
The PLL tab shows a conventional PLL diagram.



Appendix A: Schematic




OSC
OSCin
VCO
VCXO
Fin
LMK02000
ADT2-1T
BALUN
TCO-2111-AA, 245.76 MHz

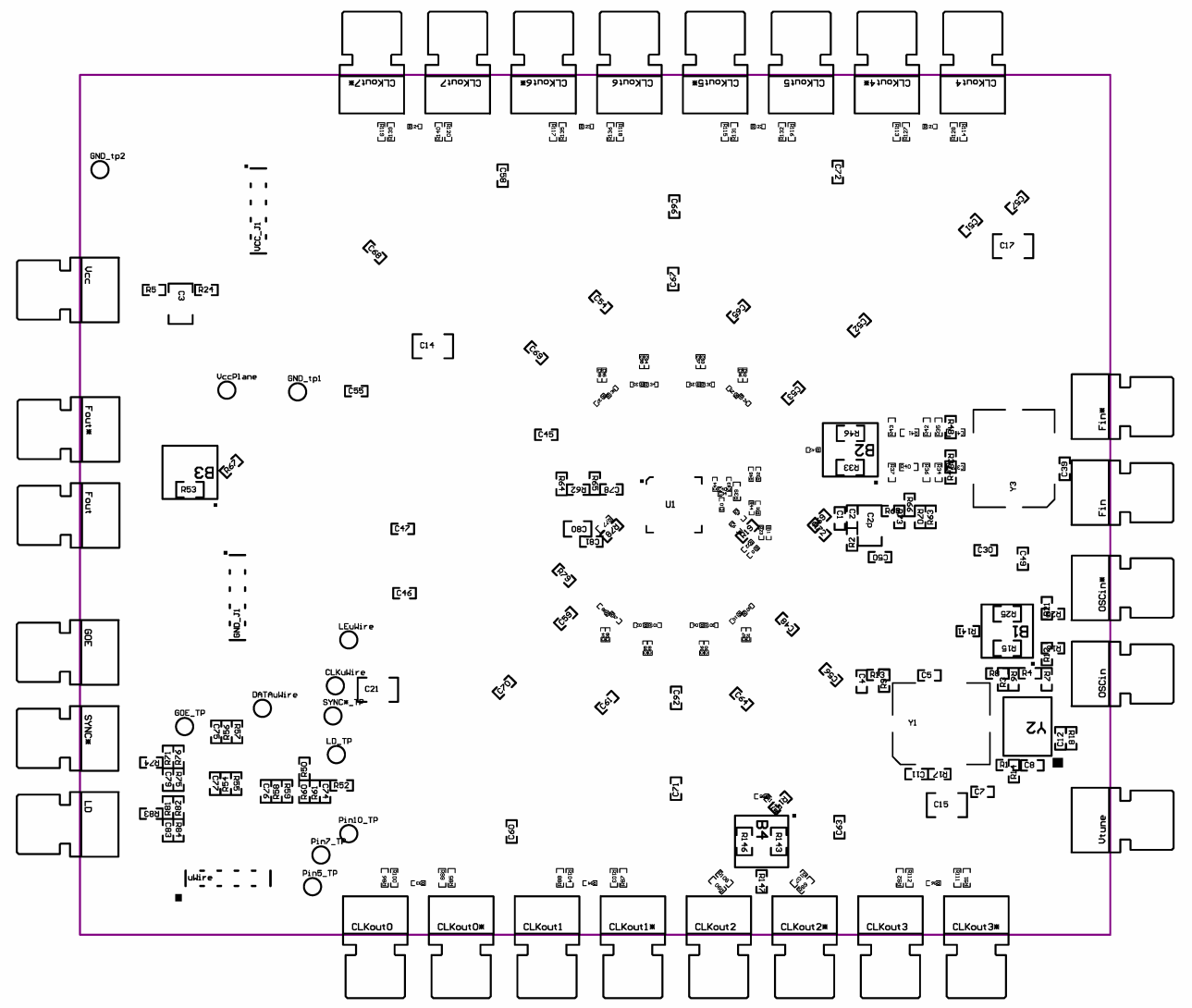

CLKout0
CLKout1
CLKout2
CLKout3
CLKout4
CLKout5
CLKout6
CLKout7
ADT2-1T
Vcc
GND
SMA
Open
0.1 uF
120 ohm
51 ohm
0 ohm

Appendix B: Bill of Materials

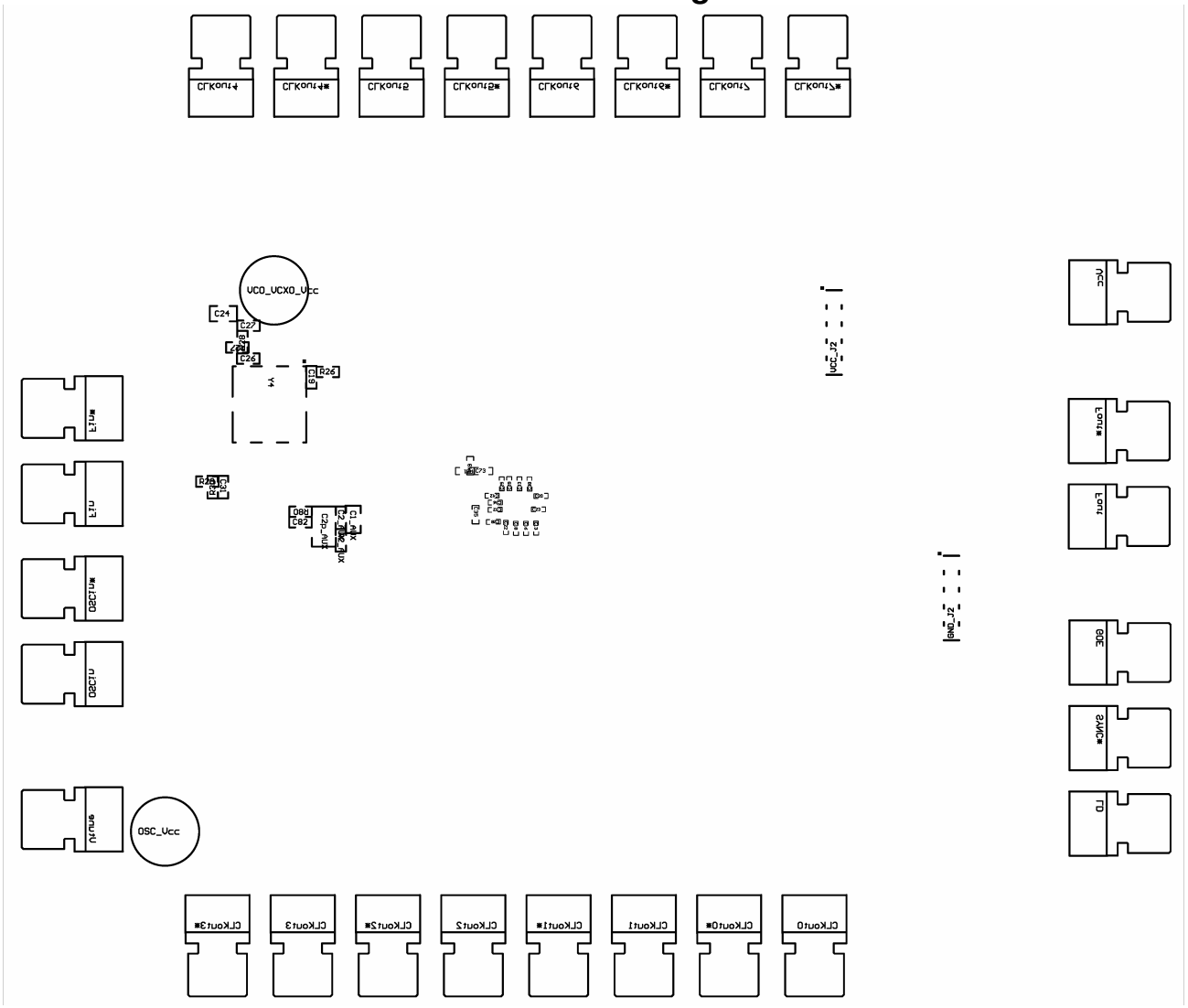
Part	Manufacturer	Part Number	Qnt	Identifier
Capacitors				
100 pF	Kemet	C0402C101J5GAC	14	C13, C16, C18, C20, C22, C23, C25, C28, C29, C32, C33, C36, C38, C42
100 pF	Kemet	C0603C101J5GAC	1	C83
0.1 uF	Kemet	C0402C104J4RAC	20	C6, C10, C34, C40, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99
0.1 uF	Kemet	C0603C104J3RAC	16	C31, C45, C47, C48, C50, C51, C53, C54, C59, C61, C62, C64, C65, C67, C69, C81
560 nF	Kemet	C0603C564K8PACTU	1	C1
1 uF	Kemet	C0603C105K8VAC	14	C46, C49, C52, C55, C56, C57, C58, C60, C63, C66, C68, C70, C71, C72
1 uF	Kemet	C0603C105K8VAC	1	C73
10 uF	Kemet	C0805C106K9PAC	5	C2p, C14, C15, C17, C21
10 uF	Kemet	C0805C106K9PAC	1	C80
Resistors				
0 ohm	Vishay	CRCW0603000ZRT1	7	C37, C41, R40, R41, R49, R77, R144
0 ohm	Vishay	CRCW0603000ZRT1	9	R5, R16, R24, R30, R52, R63, R68, R69, R78
0 ohm	Yageo	RC0805JR-070RL	3	R15, R33, R46
51 ohm	Yageo	CRCW040251R0FKED	1	R22
51 ohm	Vishay/Dale	CRCW060351R0JNEA	1	R107
82 ohm	Vishay/Dale	CRCW040282R0JNED	2	R44, R45
120 ohm	Vishay	CRCW0402120RJNED	12	R31, R32, R109, R110, R125, R126, R129, R130, R133, R134, R137, R138
3.3 k	Vishay/Dale	CRCW06034K70JNEA	1	R2
15 k	Vishay	CRCW0603153JRT1	5	R55, R57, R59, R60, R82
27 k	Vishay	CRCW0603273JRT1	4	R54, R56, R58, R84

Other				
ADT2-1T	Minicircuits	ADT2-1T	1	B4
SMA	Johnson Components	142-0701-851	12	CLKout0, CLKout0*, CLKout2, CLKout4, CLKout4*, CLKout7, CLKout7*, Fin, Fin*, OSCin, OSCin*, Vcc
LMK02000	National Semiconductor	LMK02000 I	1	U1
245.76 VCXO	Epson-Toyocom	TCO-2111-AA, 245.76 MHz	1	Y3
PCB	Printed Circuits Corp	LMK02000_EB_PCB	1	F1
HEADER_2X5	FCI Electronics	52601-S10-8	1	uWire
Open				
Open	-	Open	3	B1, B2, B3
Open	-	0603	64	C2, C2_AUX, C4, C5, C7, C8, C11, C12, C19, C26, C27, C30, C39, C74, C75, C76, C77, C78, C79, C82, R1, R2_AUX, R3, R4, R6, R7, R8, R9, R12, R13, R14, R17, R18, R19, R20, R21, R26, R27, R28, R29, R38, R47, R48, R50, R61, R62, R64, R65, R66, R67, R70, R71, R72, R73, R74, R75, R76, R79, R80, R81, R83, R141, R145, R147
Open	-	Open	4	C1_AUX, C2p_AUX, C3, C24
Open	-	0603	40	C35, R34, R35, R36, R37, R39, R42, R43, R51, R85, R86, R87, R88, R89, R90, R91, R92, R99, R100, R103, R104, R108, R111, R112, R113, R114, R115, R116, R117, R118, R119, R120, R127, R128, R131, R132, R135, R136, R139, R140
Open	-	0402	21	C9, C43, C44, R10, R11, R23, R93, R94, R95, R96, R97, R98, R101, R102, R105, R106, R121, R122, R123, R124, R142
Open	-	Open	15	CLKout1, CLKout1*, CLKout2*, CLKout3, CLKout3*, CLKout5, CLKout5*, CLKout6, CLKout6*, Fout, Fout*, GOE, LD, SYNC*, Vtune
Open	-	Open	4	GND_J1, GND_J2, VCC_J1, VCC_J2
Open	-	Open	2	OSC_Vcc, VCO_VCXO_Vcc
Open	-	0805	4	R25, R53, R143, R146
Open	-	Open	1	Y1, Y2, Y4

Appendix C: Build Diagram



Bottom Build Diagram



IMPORTANT NOTICE

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