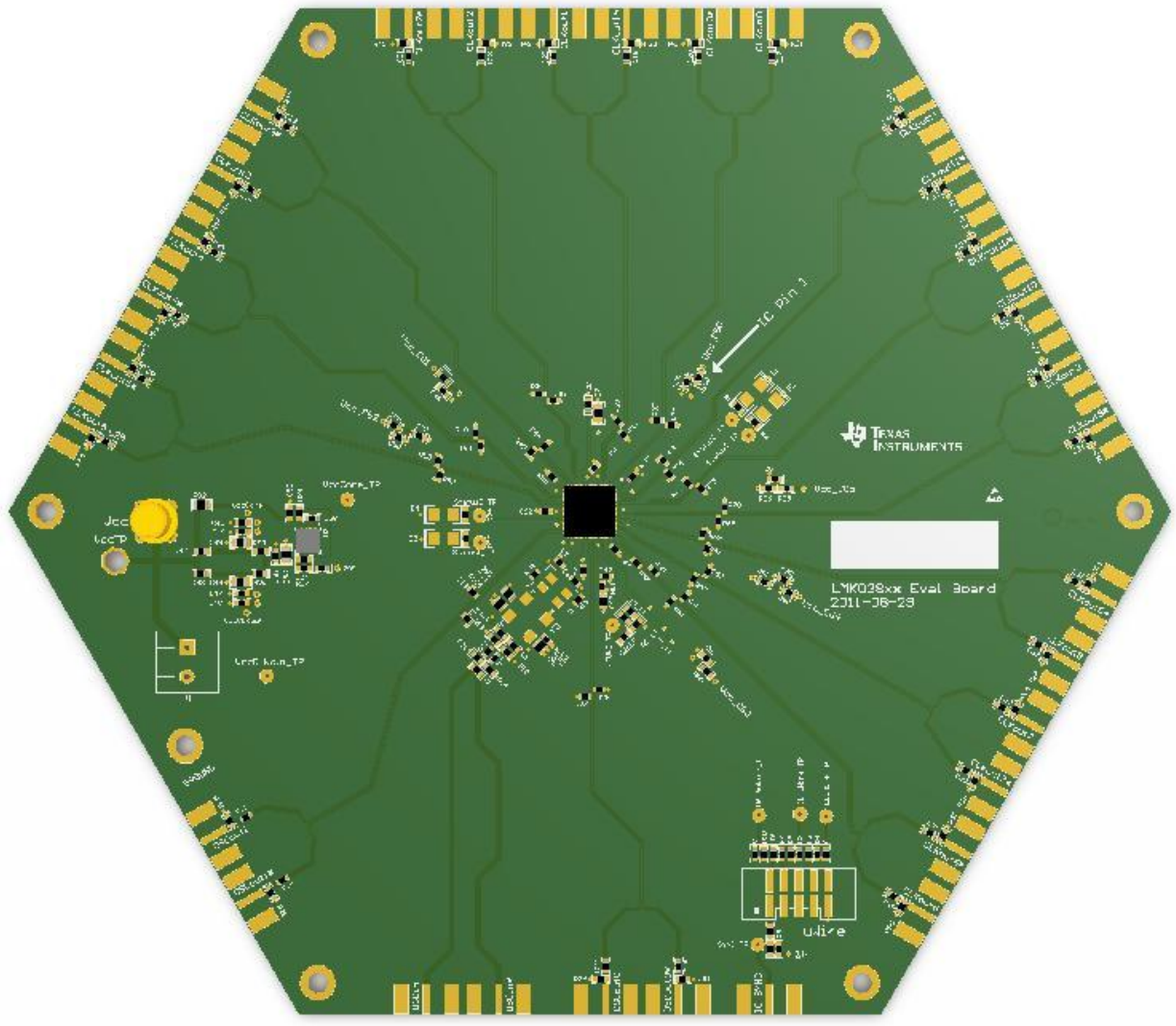
LMK03806BEVAL User's Guide



LMK03806B
Ultra Low Jitter Clock Generator

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1. Introduction

The Texas Instruments LMK03806BEVAL evaluation module (EVM) helps designers evaluate the operation and performance of the LMK03806B high performance, ultra low-jitter, multirate clock generator. Texas Instruments *CodeLoader* software can be used to program the internal registers of the LMK03806B device through the MICROWIRE™ interface. The *CodeLoader* software will run on a Windows 2000 or Windows XP PC and can be downloaded from http://www.ti.com/tool/codeloader

The EVM contains (See Table 1):

Table 1: EVM Contents

QUANTITY	DESCRIPTION
1	LMK03806BEVAL
1	LKM03806 Quick Start Guide
1	CodeLoader uWire cable (LPT to uWire)

2. Quick Start

1. Connect a voltage of **5.0 volts** to the Vcc SMA connector or terminal block. Device operates at 3.3 V using onboard LP3878-ADJ LDO.
2. Connect the uWire header to a computer parallel port with the CodeLoader cable. A USB communication option is also available, search at www.ti.com for: USB2UWIRE-IFACE.
3. Program the device with CodeLoader. CodeLoader is available for download at: www.ti.com/tool/codeloader
   a. Select correct LMK03806B from "Select Device → Clock Conditioners" Menu.
   b. Select a default mode from the "Mode" Menu. For the quick start use, "**100 MHz TCXO/XO Reference**"
   c. **Ctrl-L** must be pressed at least once to load all registers. Alternatively click menu Keyboard Controls → Load Device.
4. Measurements may be made at an active CLKout port via its SMA connector.

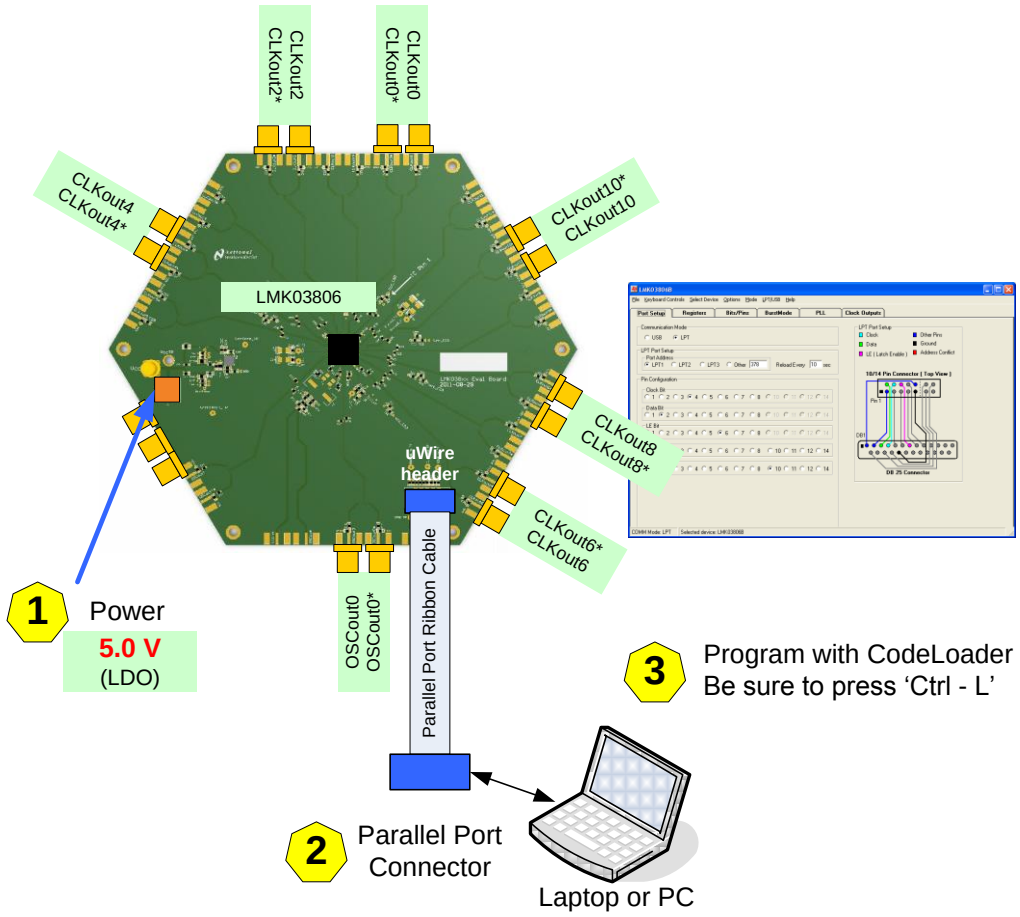

Figure 1: Quick Start Diagram

3. Default CodeLoader Modes for Evaluation Boards

CodeLoader saves the state of the selected LMK03806B device when exiting the software. To ensure a common starting point, the following modes listed in Table 2: Default CodeLoader Modes for LMK03806 may be restored by clicking "Mode" and selecting the appropriate device configuration, as shown in Figure 2 in the case of the LMK03806B device. Similar default modes are available for each LMK03806B device in CodeLoader.

Figure 2: Selecting a Default Mode for the LMK03806B Device

After restoring a default mode, press Ctrl+L to program the device. The default modes also disable certain outputs, so make sure to enable the output under test to make measurements.

Table 2: Default CodeLoader Modes for LMK03806

Default CodeLoader Mode	XO Frequency
LMK03806B, 100 MHz	100 MHz

The next section outlines step-by-step procedures for using the evaluation board with the LMK03806B.

4. Example: Using CodeLoader to Program the LMK03806B

The purpose of this section is to walk the user through using CodeLoader 4 to make some measurements with the LMK03806B device as an example. For more information on CodeLoader refer to CodeLoader Usage or the CodeLoader 4 instructions located at http://www.ti.com/tool/codeloader.

Before proceeding, be sure to follow the Quick Start section to ensure proper connections.

1. Start CodeLoader 4 Application

Click "Start" → "Programs" → "CodeLoader 4" → "CodeLoader 4"

The CodeLoader 4 program is installed by default to the CodeLoader 4 application group.

2. Select Device

Click "Select Device" → "Clock Conditioners" → "LMK03806B"

Once started CodeLoader 4 will load the last used device. To load a new device click "Select Device" from the menu bar, then select the subgroup and finally device to load. For this example, the LMK03806B is chosen. Selecting the device does cause the device to be programmed.

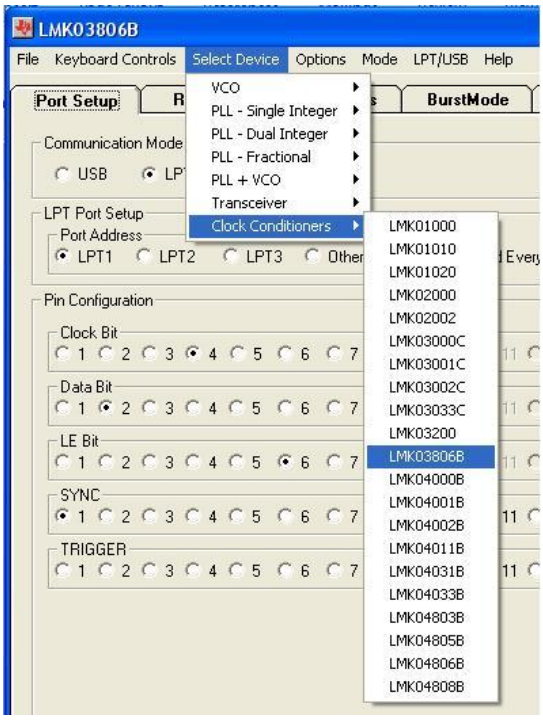

Figure 3: Selecting the LMK03806B Device

5. Program/Load Device

Assuming the Port Setup settings are correct, press the "Ctrl+L" shortcut or click "Keyboard Controls" → "Load Device" from the menu to program the device to the current state of the newly loaded LMK03806 file.

Figure 4: Loading the Device

Once the device has been initially loaded, CodeLoader will automatically program changed registers so it is not necessary to re-load the device upon subsequent changes in the device configuration. It is possible to disable this functionality by ensuring there is no checkmark by the "Options" → "AutoReload with Changes."

Because a default mode will be restored in the next step, this step isn't really needed but included to emphasize the importance of pressing "Ctrl+L" to load the device at least once after starting CodeLoader, restoring a mode, or restoring a saved setup using the File menu.

See CodeLoader Usage or the CodeLoader 4 instructions located at http://www.ti.com/tool/codeloader for more information on Port Setup. Troubleshooting Information contains information on troubleshooting communications.

6. Restoring a Default Mode

Click "Mode" → "**100 MHz XO/TCXO Reference**"; then press Ctrl+L.

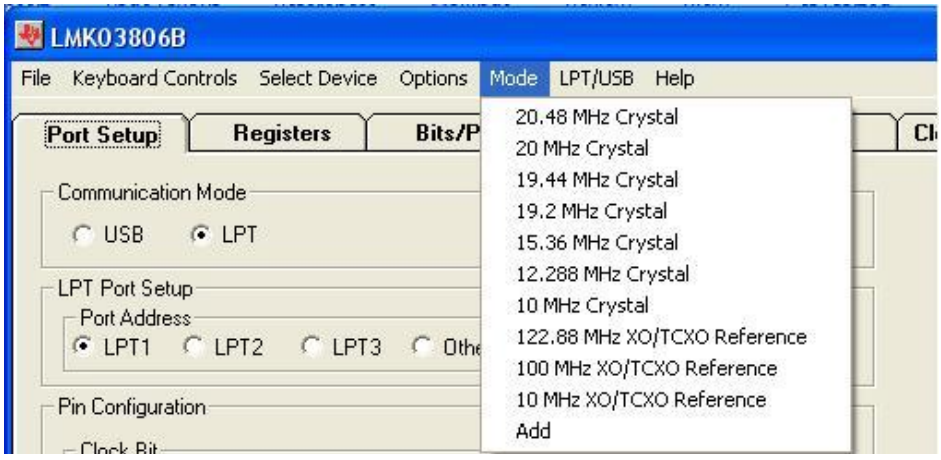

Figure 5: Setting the Default mode for LMK03806

For the purpose of this walkthrough, a default mode will be loaded to ensure a common starting point. This is important because when CodeLoader is closed, it remembers the last settings used for a particular device. Again, remember to press Ctrl+L as the first step after loading a default mode.

7. Visual Confirmation of Frequency Lock

After a default mode is restored and loaded, LED D4, should illuminate red when the PLL is locked to the reference crystal.

8. Enable Clock Outputs

While the LMK03806B offers programmable clock output buffer formats, the evaluation board is shipped with preconfigured output terminations to match the default buffer type for each output. Refer to the CLKout port description in the Evaluation Board Inputs and Outputs section.

To measure phase noise at one of the clock outputs, for example, CLKout0:

1. Click on the **Clock Outputs** tab,
2. Uncheck "Powerdown" in the Divider Powerdown box to enable the channel,
3. Set the following settings as needed:
    a. Clock Divider value
    b. Clock Output type.

Figure 6: Setting Digital Delay, Clock Divider, Analog Delay, and Output Format for CLKout0

4. Depending on the configured output type, the clock output SMAs can be interfaced to a test instrument with a single-ended 50-ohm input as follows.
    a. For LVDS:
        i. A balun (like ADT2-1T) is recommended for differential-to-single-ended conversion.
    b. For LVPECL:
        i. A balun can be used, or
        ii. One side of the LVPECL signal can be terminated with a 50-ohm load and the other side can be run single-ended to the instrument.
    c. For LVCMOS:
        i. There are two single-ended outputs, CLKoutX and CLKoutX*, and each output can be set to Normal, Inverted, or Off. There are nine (9) combinations of LVCMOS modes in the Clock Output list.
        ii. One side of the LVCMOS signal can be terminated with a 50-ohm load and the other side can be run single-ended to the instrument.
        iii. A balun may also be used. Ensure CLKoutX and CLKoutX* states are complementary, i.e.: Norm/Inv or Inv/Norm.

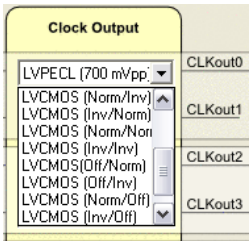

Figure 7: Setting LVCMOS

5. The phase noise may be measured with a spectrum analyzer or signal source analyzer.

See Typical Phase Noise Performance Plots for phase noise plots of the clock outputs. TI's Clock Design Tool can be used to calculate divider values to achieve desired clock output frequencies. See: http://www.ti.com/tool/codeloader.

9. PLL Loop Filters and Loop Parameters

The default loop filter for the PLL has been configured for a 60 kHz bandwidth. The following table contains the parameters for the PLL.

TI's Clock Design Tool can be used to optimize PLL phase noise/jitter for given specifications. See: http://www.ti.com/tool/codeloader.

PLL Loop Filter

Table 3: PLL Loop Filter Parameters for LMK03806B

	Integrated VCO PLL		
	20 MHz Reference	**100 MHz Reference**	
C1_LF	0.022	.022	nF
C2_LF	18	18	nF
C3 (internal)	0.01	0.01	nF
C4 (internal)	0.01	0.01	nF
R2_A2	0.82	0.82	kΩ
R3 (internal)	0.2	0.2	kΩ
R4 (internal)	0.2	0.2	kΩ
Charge Pump Current, Kϕ	3.2	3.2	mA
Phase Detector Frequency	20	100	MHz
Frequency	2500	2400	MHz
Kvco	19	19	MHz/V
N	25	12	
P	5	2	
Phase Margin	75	70	degrees
Loop Bandwidth	63	60	kHz

Note: PLL Loop Bandwidth is a function of Kϕ, Kvco, N as well as loop components. Changing Kϕ and N will change the loop bandwidth.

10. Evaluation Board Inputs and Outputs

The following table contains descriptions of the inputs and outputs for the evaluation board. Unless otherwise noted, the connectors described can be assumed to be populated by default. Additionally, some applicable CodeLoader programming controls are noted for convenience.

Table 4: Evaluation Board Inputs and Outputs

<table>
<tr><th>Connector Name</th><th>Signal Type, Input/Output</th><th>Description</th></tr>
<tr>
<td><u>SMAs Populated:</u>
CLKout0, CLKout0*,
CLKout2, CLKout2*,
CLKout4, CLKout4*,
CLKout6, CLKout6*,
CLKout8, CLKout8*,
CLKout10, CLKout10*

<u>SMAs Not Populated:</u>
CLKout1, CLKout1*,
CLKout3, CLKout3*,
CLKout5, CLKout5*,
CLKout7, CLKout7*,
CLKout9, CLKout9*,
CLKout11, CLKout11*</td>
<td>Analog, Output</td>
<td>Clock outputs with programmable output buffers.

The output terminations by default on the evaluation board are shown below, and the output type selected by default in CodeLoader is indicated by an asterisk (*):

<table>
<tr><th>Clock output pair</th><th>Default Board Termination</th></tr>
<tr><td>CLKout0</td><td>LVPECL*</td></tr>
<tr><td>CLKout1</td><td>LVPECL</td></tr>
<tr><td>CLKout2</td><td>LVPECL*</td></tr>
<tr><td>CLKout3</td><td>LVPECL</td></tr>
<tr><td>CLKout4</td><td>LVDS* / LVCMOS</td></tr>
<tr><td>CLKout5</td><td>LVDS / LVCMOS</td></tr>
<tr><td>CLKout6</td><td>LVDS* / LVCMOS</td></tr>
<tr><td>CLKout7</td><td>LVDS / LVCMOS</td></tr>
<tr><td>CLKout8</td><td>LVDS* / LVCMOS</td></tr>
<tr><td>CLKout9</td><td>LVDS / LVCMOS</td></tr>
<tr><td>CLKout10</td><td>LVPECL*</td></tr>
<tr><td>CLKout11</td><td>LVPECL</td></tr>
</table>

Each CLKout pair has a programmable LVDS, LVPECL, or LVCMOS buffer. The output buffer type can be selected in CodeLoader in the Clock Outputs tab via the CLKoutX_TYPE control.

All clock outputs are AC-coupled to allow safe testing with RF test equipment.

All LVPECL clock outputs are source-terminated using 240-ohm resistors.

If an output pair is programmed to LVCMOS, each output can be independently configured (normal, inverted, or off/tri-state).</td>
</tr>
</table>

<table>
<tr><th>Connector Name</th><th>Signal Type, Input/Output</th><th>Description</th></tr>
<tr><td>OSCout0, OSCout0*, OSCout1, OSCout1*</td><td>Analog, Output</td><td>Buffered outputs of OSCin port.

The output terminations on the evaluation board are shown below, the output type selected by default in CodeLoader is indicated by an asterisk (*):
<table>
<tr><th>OSC output pair</th><th>Default Board Termination</th></tr>
<tr><td>OSCout0</td><td>LVPECL* (fixed)</td></tr>
<tr><td>OSCout1</td><td>LVPECL* (fixed)</td></tr>
</table>
Only OSCout0 has a programmable LVDS, LVPECL, or LVCMOS output buffer. The OSCout0 buffer type can be selected in CodeLoader on the Clock Outputs tab via the OSCout0_TYPE control. OSCout1 has LVPECL buffer only but has programmable swing amplitude.

Both OSCout pairs are AC-coupled to allow safe testing with RF test equipment.

The OSCout0 and OSCout1 outputs are source-terminated using 240-ohm resistors.

If OSCout0 is programmed as LVCMOS, each output can be independently configured (normal, inverted, inverted, and off/tri-state).</td></tr>
<tr><td>Vcc</td><td>Power, Input</td><td>Main power supply input for the evaluation board.

A 3.9 V DC power source applied to this SMA will, by default, source the onboard LDO regulators that power the inner layer planes that supply the LMK03806B.

The LMK03806B contains internal voltage regulators for the VCO, PLL and other internal blocks. The clock outputs do not have an internal regulator, so a clean power supply with sufficient output current capability is required for optimal performance.

On-board LDO regulators and 0 Ω resistor options provide flexibility to supply and route power to various devices. See schematics for more details.</td></tr>
</table>

Connector Name	Signal Type, Input/Output	Description
J1	Power, Input	Alternative power supply input for the evaluation board using two unshielded wires (Vcc and GND). Apply power to either Vcc SMA or J1, but not both.
OSCin, OSCin*	Analog, Input	By default, these SMAs are not connected to the traces going to the OSCin/OSCin* pins of the LMK03806B. Instead, the onboard crystal drives the OSCin input of the device. A single-ended or differential signal may be used to drive the OSCin/OSCin* pins and must be AC coupled. If operated in single-ended mode, the unused input must be connected to GND with 0.1 uF. Refer to the LMK03806 Datasheet section "Electrical Characteristics" for PLL Reference Input (OSCin) specifications.
uWire	CMOS, Input/Output	10-pin header for uWire programming interface and programmable logic I/O pins for the LMK03806B. The uWire interface includes CLKuWire, DATAuWire, and LEuWire signals. The programmable logic I/O signals accessible through this header include: SYNC. SYNC also has a dedicated SMA and test point.

Connector Name	Signal Type, Input/Output	Description
SYNC	CMOS, Input/Output	Programmable status I/O pin. By default, set as an input pin for synchronize the clock outputs with a fixed and known phase relationship between each clock output selected for SYNC. In the default CodeLoader mode, SYNC will asserted when the SYNC pin is low and the outputs to be synchronized will be held in a logic low state. When SYNC is unasserted, the clock outputs to be synchronized are activated and will be initially phase aligned with each other except for outputs programmed with different digital delay values. A SYNC event can also be programmed by toggling the SYNC_POL_INV bit in the **Bits/Pins** tab in CodeLoader. Refer to the LMK03806 Datasheet section "Clock Output Synchronization" for more information.

11. Recommended Test Equipment

Power Supply

The Power Supply should be a low noise power supply, particularly when the devices on the board are being directly powered (onboard LDO regulators bypassed).

Phase Noise / Spectrum Analyzer

To measure phase noise and RMS jitter, an Agilent E5052 Signal Source Analyzer is recommended. An Agilent E4445A PSA Spectrum Analyzer with the Phase Noise option is also usable although the architecture of the E5052 is superior for phase noise measurements. At frequencies less than 100 MHz the local oscillator noise of the E4445A is too high and measurements will reflect the E4445A's internal local oscillator performance, not the device under test.

Oscilloscope

To measure the output clocks for AC performance, such as rise time or fall time, propagation delay, or skew, it is suggested to use a real-time oscilloscope with at least 1 GHz analog input bandwidth (2.5+ GHz recommended) with 50 ohm inputs and 10+ Gsps sample rate. To evaluate clock synchronization or phase alignment between multiple clock outputs, it's recommended to use phase-matched, 50-ohm cables to minimize external sources of skew or other errors/distortion that may be introduced if using oscilloscope probes.

12. CodeLoader Usage

Code Loader is used to program the evaluation board with either an LPT port using the included CodeLoader cable or with a USB port using the optional USB-to-uWire cable available from http://www.ti.com/tool/usb2uwire-iface#buy. The part number is USB2UWIRE-IFACE.

Port Setup Tab

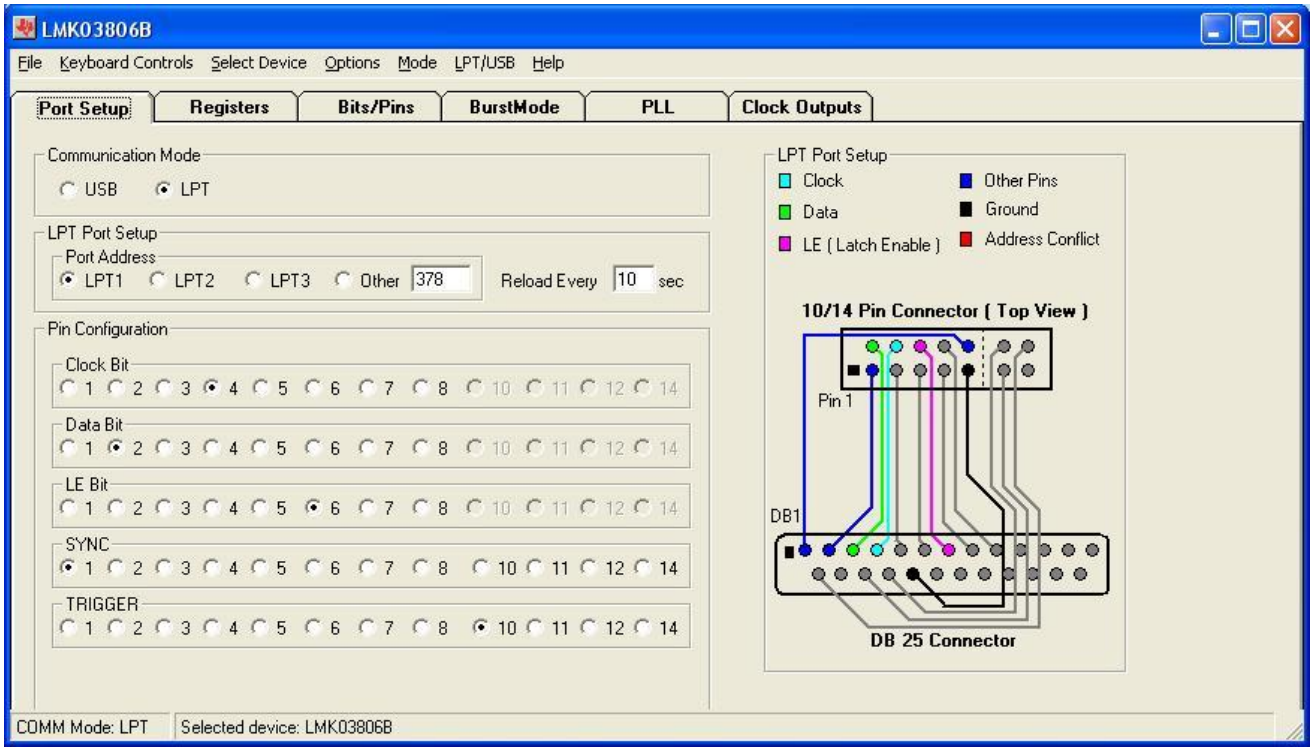

Figure 8: Port Setup Tab

On the Port Setup tab, the user may select the type of communication port (USB or Parallel) that will be used to program the device on the evaluation board. If parallel port is selected, the user should ensure that the correct port address is entered.

The Pin Configuration field is hardware dependent and normally **does not** need to be changed by the user. Figure 8: Port Setup Tab shows the default settings.

Clock Outputs Tab

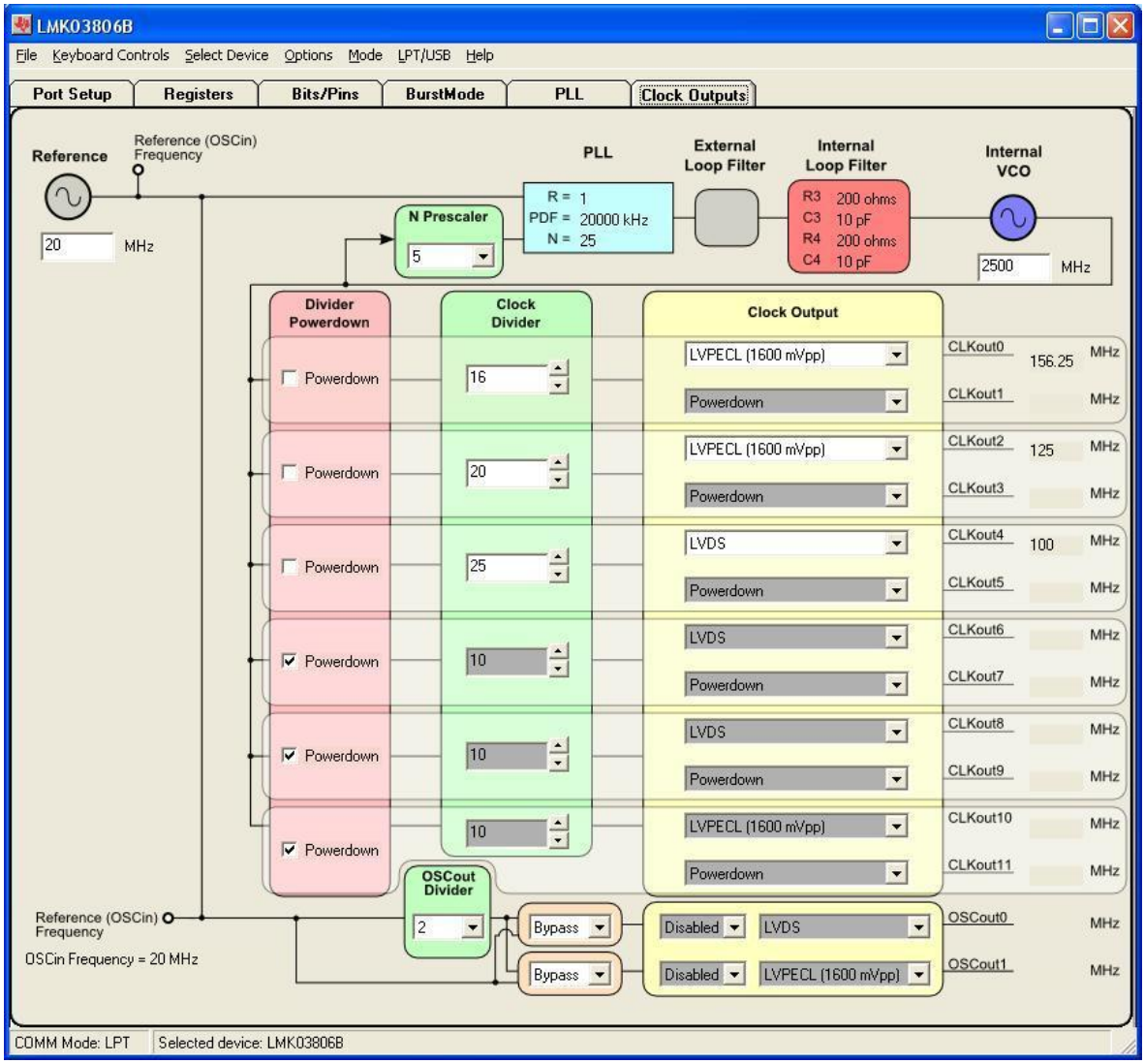

Figure 9: Clock Outputs Tab

The **Clock Outputs** tab allows the user to control the output channel blocks, including:

- Clock Group Source from either Crystal or OSCin
- Channel Powerdown (affects clock divider, and buffer blocks)
- Clock Divide value
- Clock Output format (per output)

Clicking on the cyan-colored PLL block that contains R, PDF and N values will bring the **PLL** tab into focus where these values may be modified, if needed.

Clicking on the values in the box containing the Internal Loop Filter component (R3, C3, R4, C4) allow one to step through the possible values. Left click to increase the component value, and right click to decrease the value. These values can also be changed in the **Bits/Pins** tab.

The Reference Oscillator value field may be changed in either the **Clock Outputs** tab or the **PLL** tab. The PLL Reference frequency should match the frequency of the onboard Crystal.

PLL Tab

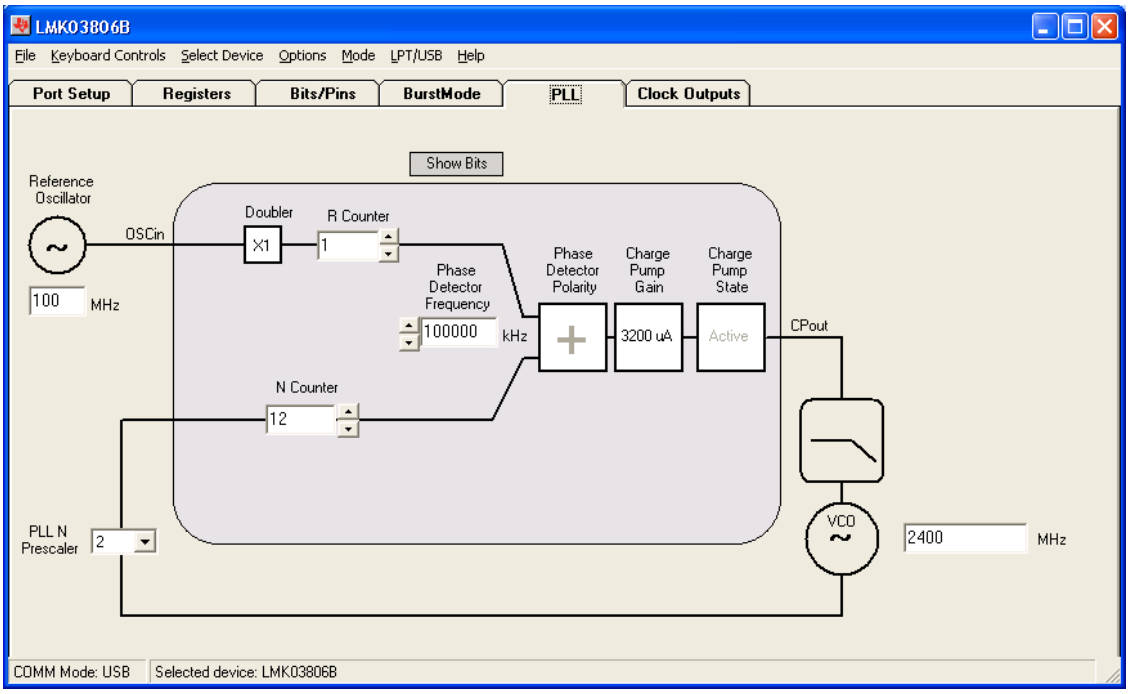

Figure 10: PLL Tab

The PLL tab allows the user to change the following parameters in Table 5.

Table 5: Registers Controls and Descriptions in PLL Tab

Control Name	Register Name	Description
Reference Oscillator Frequency (MHz)	OSCin_FREQ	OSCin frequency from the External OSCin connector or Crystal.
Phase Detector Frequency (MHz)	n/s	PLL Phase Detector Frequency (PDF). This value is calculated as: PLL PDF = OSCin Frequency *($2^{EN\_PLL\_REF\_2X}$) / (PLL_R).
VCO Frequency (MHz)	n/a	Internal VCO Frequency should be within the allowable range of the LMK03806B device. This value is calculated as: VCO Frequency = PLL PDF * (PLL_N * PLL_P).

Doubler	EN_PLL_REF_2X	PLL Doubler. 0 = Bypass Doubler 1 = Enable Doubler
R Counter	PLL_R	PLL R Counter value (1 to 4095).
N Counter	PLL_N	PLL N Counter value (1 to 49140).
OSCout Divider	PLL_P	PLL N Prescaler value (2 to 8).
Phase Detector Polarity	PLL_CP_POL	PLL Phase Detector Polarity. Click on the polarity sign to toggle polarity "+" or "–".
Charge Pump Gain	PLL_CP_GAIN	PLL Charge Pump Gain. Left-click/right-click to increase/decrease charge pump gain (100, 400, 1600, 3200 uA).
Charge Pump State	PLL_CP_TRI	PLL Charge Pump State. Click to toggle between Active and Tri-State.

Changes made on this tab will be reflected in the **Clock Outputs** tab. The VCO Frequency should conform to the specified internal VCO frequency range for the LMK03806B.

Bits/Pins Tab

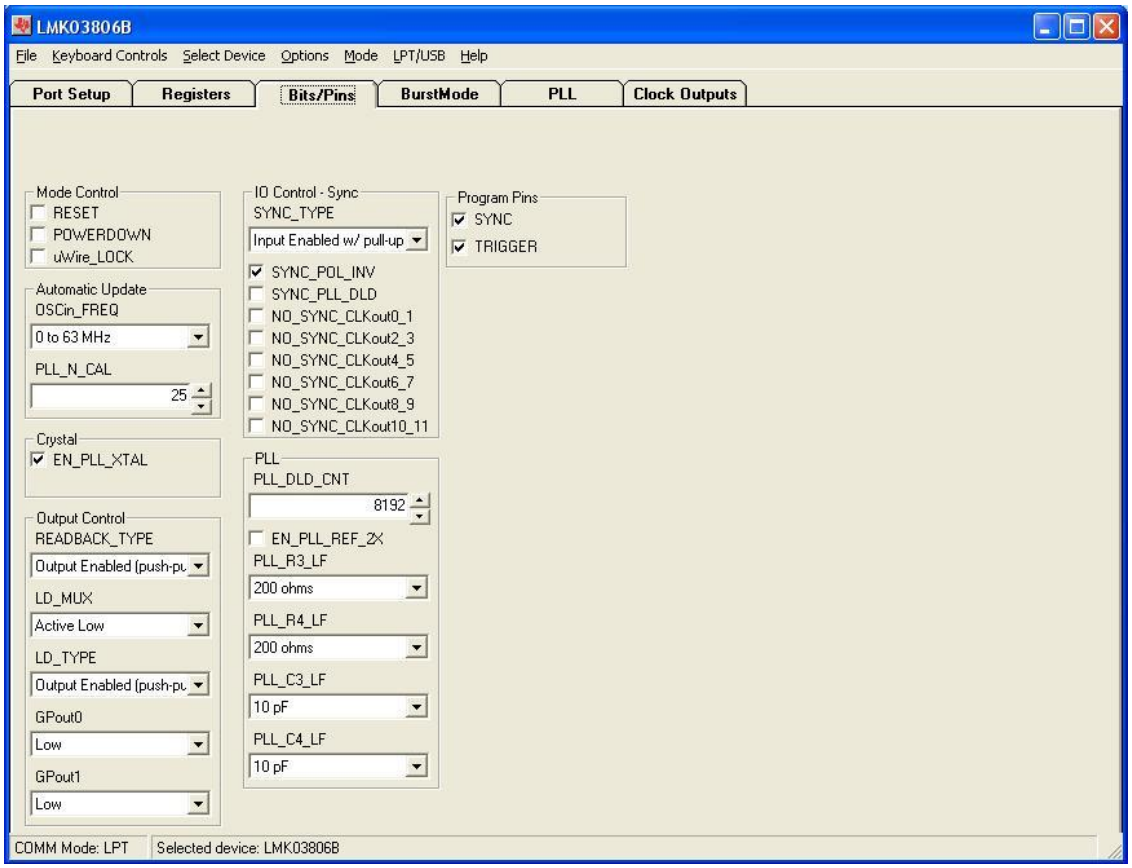

Figure 11: Bits/Pins Tab

The **Bits/Pins** tab allows the user to program bits directly, many of which are not available on other tabs. Brief descriptions for the controls on this tab are provided in Table 7: Register Controls and Descriptions on Bits/Pins Tab to supplement the datasheet. Refer to the LMK03806 Datasheet for more information.

TIP: Right-clicking any register name in the **Bits/Pins** tab will display a Help prompt with the register address, data bit location/length, and a brief register description.

Note: Table 6 shows some differences between the datasheet names and PCB names for -002 PCB's:

Table 6: Datasheet to PCB Silkscreen Updates

Datasheet Name	PCB Silkscreen Identifier
Readback (pin 27)	Status0
Ftest/LD (pin 33)	Status1
GPout0 (pin 62)	Status2
GPout1 (pin 63)	Status3

Table 7: Register Controls and Descriptions on Bits/Pins Tab

Group	Register Name	Description
Mode Control	RESET	Resets the device to default register values. RESET must be cleared for normal operation to prevent an unintended reset every time R0 is programmed.
	POWERDOWN	Places the device in powerdown mode.
	uWire_LOCK	When checked, no other uWire programming will have effect. Must be unchecked to enable uWire programming of registers R0 to R30.
Automatic Update	OSCin_FREQ	Sets the OSCin frequency range.
	PLL_N_CAL	Sets the PLL_N value.
Crystal	EN_PLL_XTAL	Enables Crystal Oscillator.
Output Control	READBACK_TYPE	Readback pin type. (Labeled Stats0 on PCB)
	LD_MUX	Ftest/LD pin selection when output. (Ftest/LD output labeled Status1 on PCB)
	LD_TYPE	Sets I/O pin type on the LD pin.
	GPO0	Sets logic level on the GPO0 pin. (Labeled Status2 on PCB)
	GPO1	Sets logic level on the GPO1 pin. (Labeled Status3 on PCB)
IO Control – Sync	SYNC_TYPE	Sets I/O pin type on the SYNC pin.
	SYNC_POL_INV	Sets polarity on SYNC input to active low when checked. Toggling this bit will initiate a SYNC event.
	SYNC_PLL_DLD	Engage SYNC mode until PLL DLD is true
	NO_SYNC_CLKoutX_Y	Synchronization will not affect selected clock outputs, where X = even-numbered output and Y = odd-numbered output.
PLL	PLL_DLD_CNT	The reference and feedback of PLL must be within the window of phase error as specified by PLL_WND_SIZE for this many cycles before PLL digital lock detect is asserted.
	EN_PLL_REF_2X	Enables the doubler block to doubles the reference frequency into the PLL R counter. This can allow for frequency of 2/3, 2/5, etc. of OSCin to be used at the phase detector of PLL.
	PLL_R3_LF	Set the corresponding integrated PLL loop filter values: R3, R4, C3, and C4. It is also possible to set these values by clicking on the loop filter values on the **Clock Outputs** tab.
	PLL_R4_LF	
	PLL_C3_LF	
	PLL_C4_LF	
Program Pins	SYNC	Sets these pins on the uWire header to logic high (checked) or logic low (unchecked).
	TRIGGER	

Registers Tab

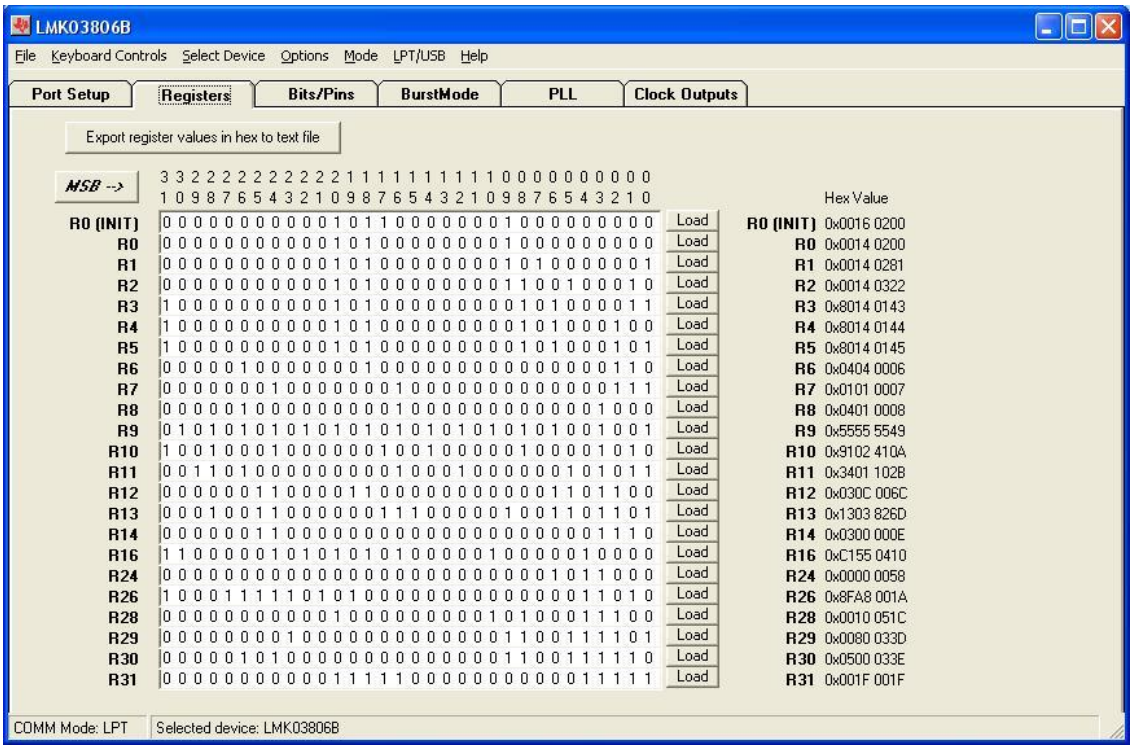

Figure 12: Registers Tab

The Registers tab shows the value of each register. This is convenient for programming the device to the desired settings, then exporting to a text file the register values in hexadecimal for use in your own application.

By clicking in the "bit field" it is possible to manually change the value of registers by typing '1' and '0.'

13. Typical Phase Noise Performance Plots

PLL

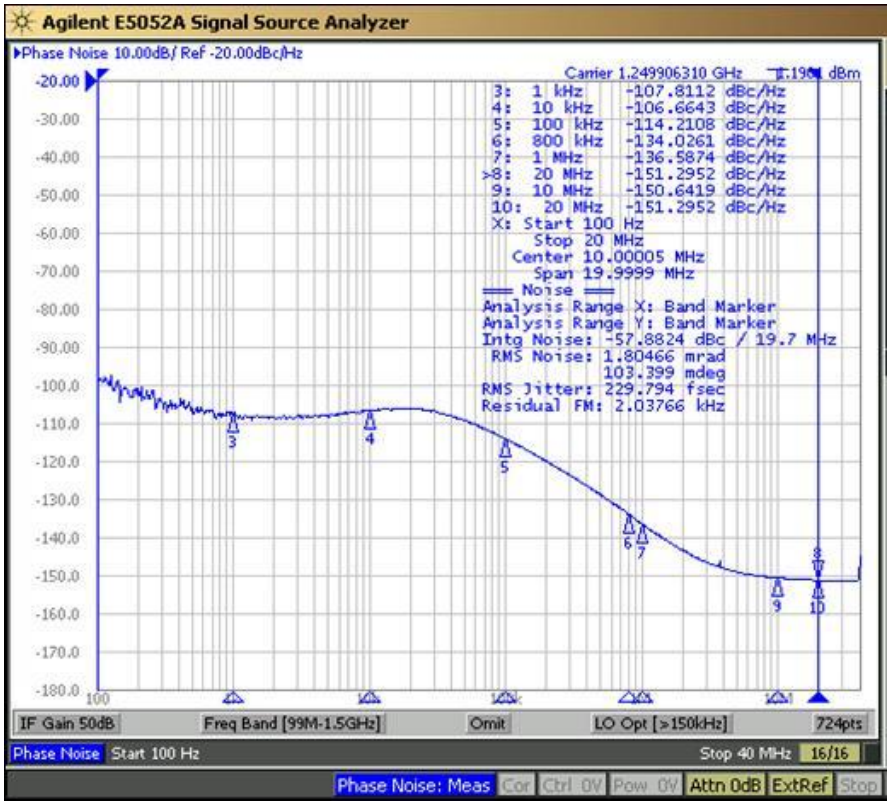

Figure 13: LMK03806B PLL VCO div2 LVPECL Phase Noise

Table 8: LMK03806B PLL VCO div2 Phase Noise and RMS Jitter (fs)

Offset	Phase Noise (dBc/Hz)
100 Hz	-98.3
1 kHz	-107.8
10 kHz	-106.6
100 kHz	-114.2
1 MHz	-136.6
10 MHz	-150.6
20 MHz	-151.3
RMS Jitter (fs) 12 kHz to 20 MHz	215
RMS Jitter (fs) 100 Hz to 20 MHz	229

Clock Outputs (CLKout)

The LMK03806 Family features programmable LVDS, LVPECL, and LVCMOS buffer modes for the CLKoutX and OSCout0 output pairs. The OSCout1 output pair has a LVPECL buffer. Included below are various phase noise measurements for each output format.

CLKout Phase Noise (div8 and div16)

For the LMK03806B, the internal VCO frequency is 2400 MHz. The divide-by-8 CLKout frequency is 312.5 MHz, and the divide-by-16 CLKout frequency is 156.25 MHz.

Table 9: Typical Phase Noise Performance Plot Setup

Parameter	Condition
LMK03806B Mode	**100 MHz TCXO/XO Reference**
Loop Filter Parameters	As shown under "100 MHz Reference" in Table 3
CLKout for LVDS/LVCMOS	CLKout8, with CLKout8* terminated in to 50 Ω
CLKout for LVPECL	CLKout10, with CLKout10* terminated in to 50 Ω

Table 10: LMK03806B Phase Noise and RMS Jitter for Different CLKout Output Formats and Frequencies

Offset	div8 LVPECL	div8 LVDS	div8 LVCMOS	div16 LVPECL	div16 LVDS	div16 LVCMOS
100 Hz	-91.9	-92.0	-93.2	-98.6	-98.8	-97.1
1 kHz	-113.8	-113.2	-113.4	-119.8	-119.3	-119.0
10 kHz	-122.6	-122.7	-122.5	-128.7	-128.4	-128.4
100 kHz	-128.7	-128.9	-128.4	-134.8	-134.9	-134.4
1 MHz	-148.1	-147.7	-148.2	-153.7	-153.0	-153.7
10 MHz	-157.6	-155.0	-157.2	-160.5	-158.0	-160.4
20 MHz	-157.7	-155.1	-157.2	-160.7	-158.1	-160.4
RMS Jitter (fs) 12 kHz to 20 MHz	141.1	144.0	143.2	145.3	155.4	149.8
RMS Jitter (fs) 100 Hz to 20 MHz	206.1	210.5	210.2	208.8	217.1	224.4

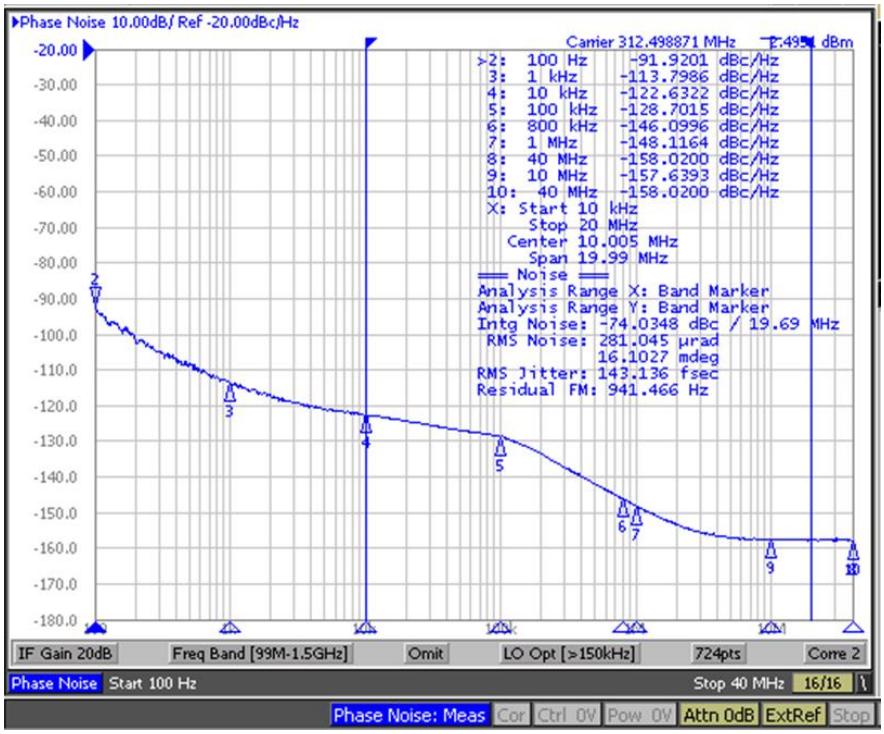

Figure 14: LMK03806B div8 CLKout LVPECL Phase Noise

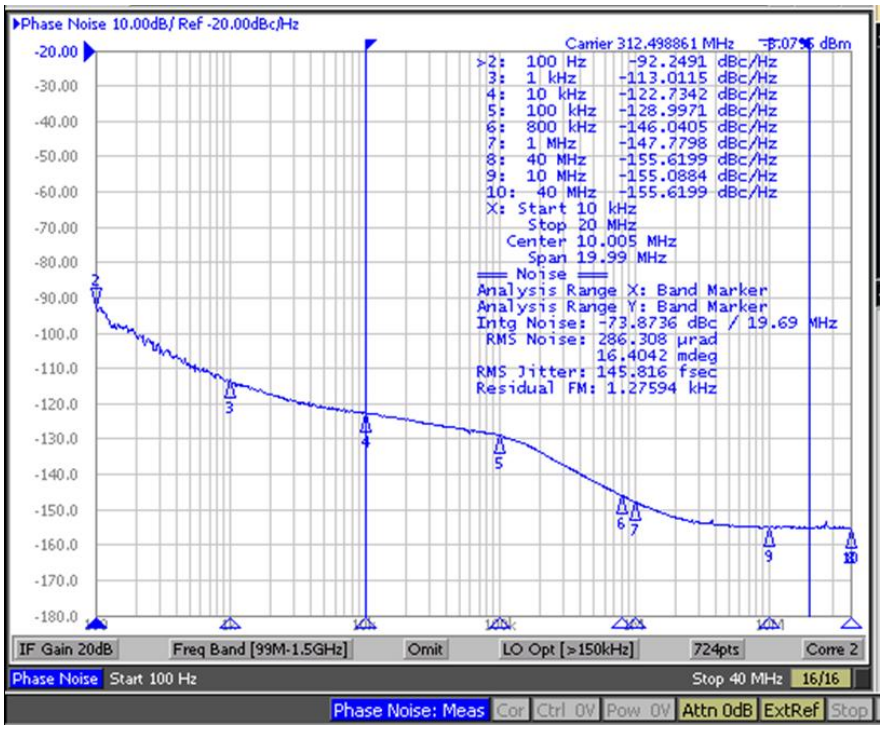

Figure 15: LMK03806B div8 CLKout LVDS Phase Noise

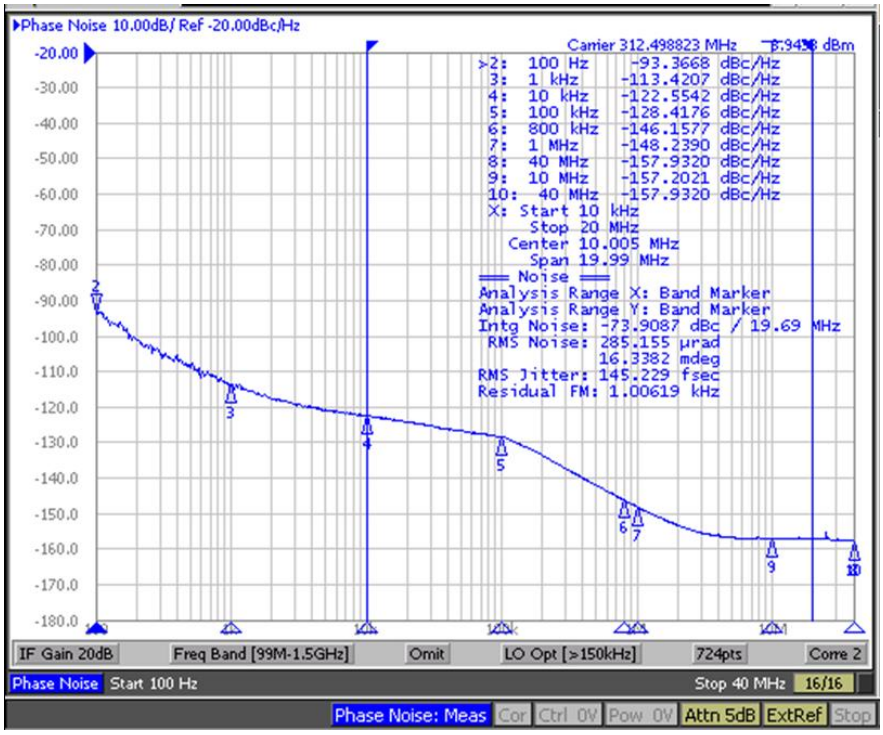

Figure 16: LMK03806B div8 CLKout LVCMOS Phase Noise

14. Schematics

Power Supplies

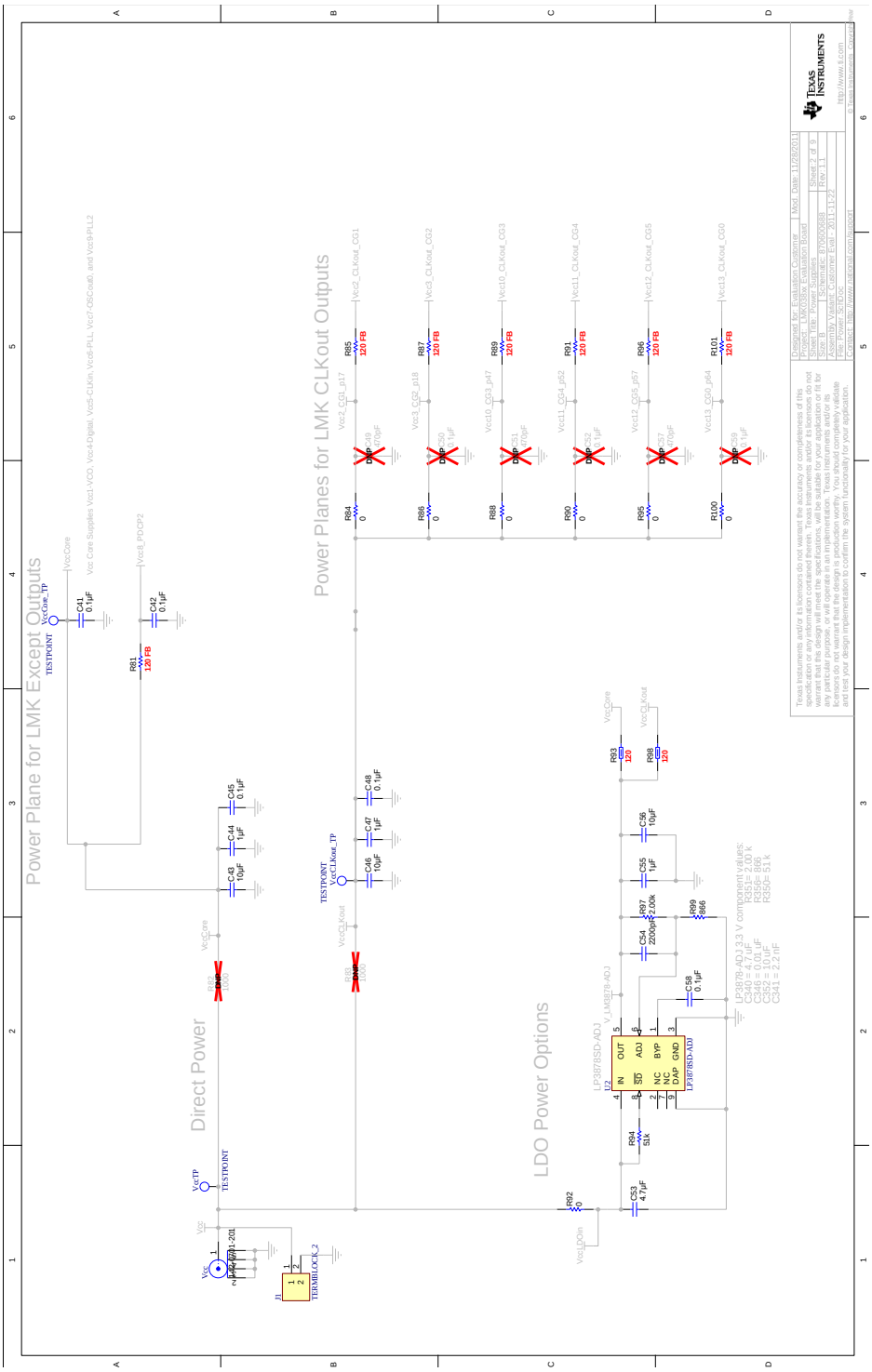

Figure 17 - LMK03806 Power Supply Schematic

LMK03806B Device with Loop Filter and Crystal Circuits

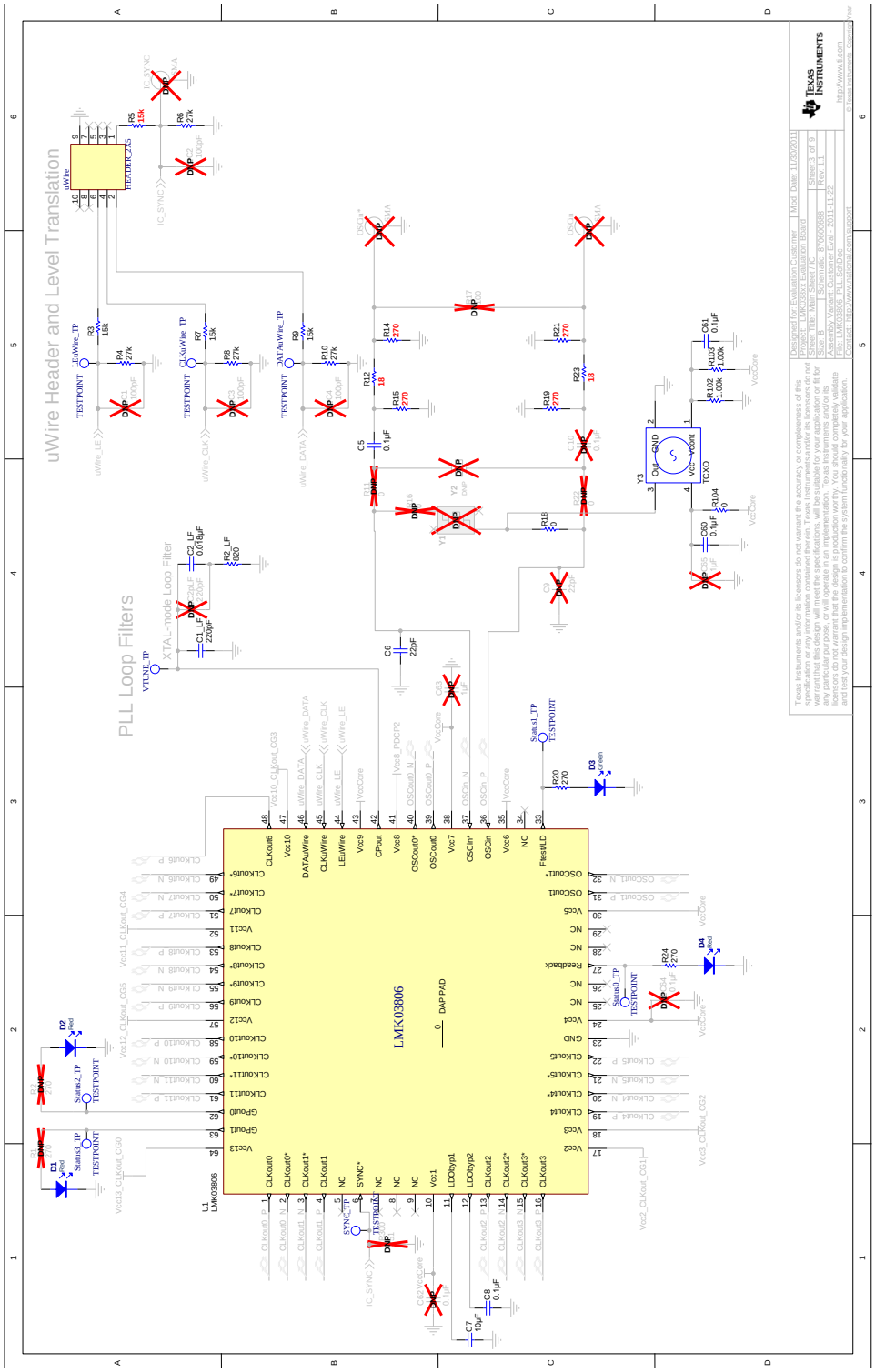

Figure 18 - LMK03806 Device Schematic

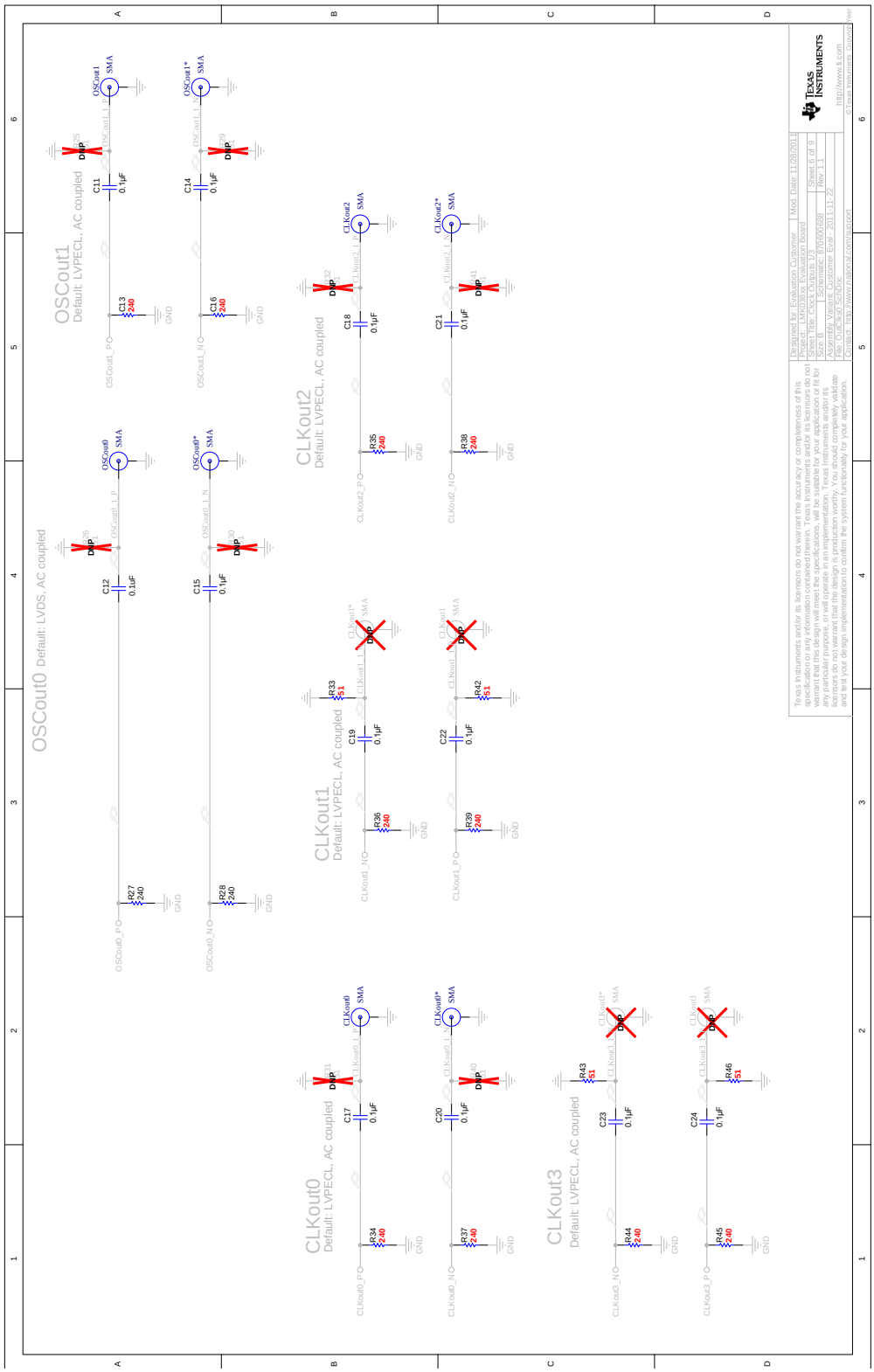

Figure 19 - Outputs, (OSCout, CLKout0/1/2/3) Schematics

Clock Outputs (CLKout 4/5/6/7)

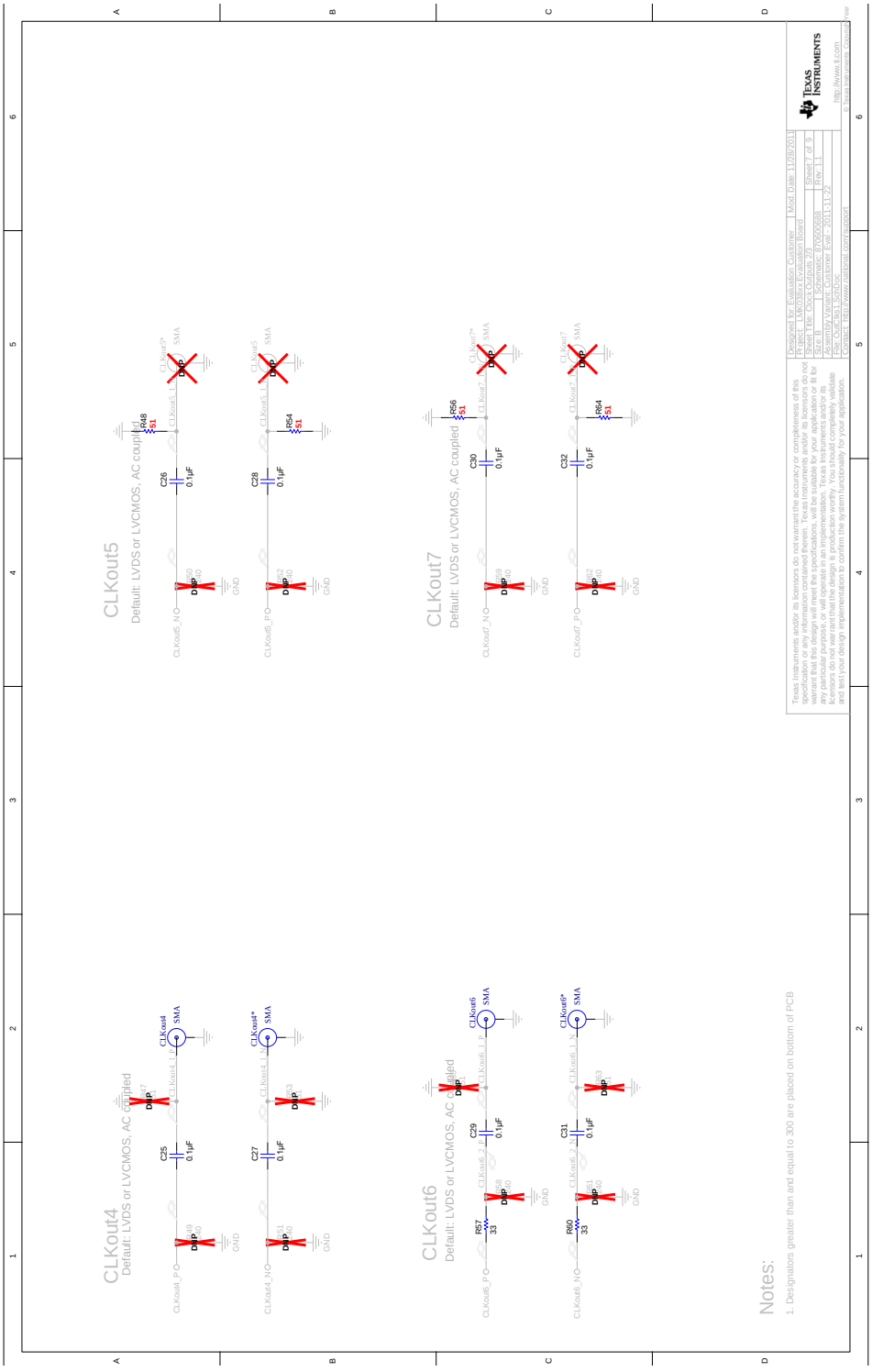

Figure 20 - LMK03806 Clock Outputs 4 through 7 Schematics

Clock Outputs (CLKout8/9/10/11)

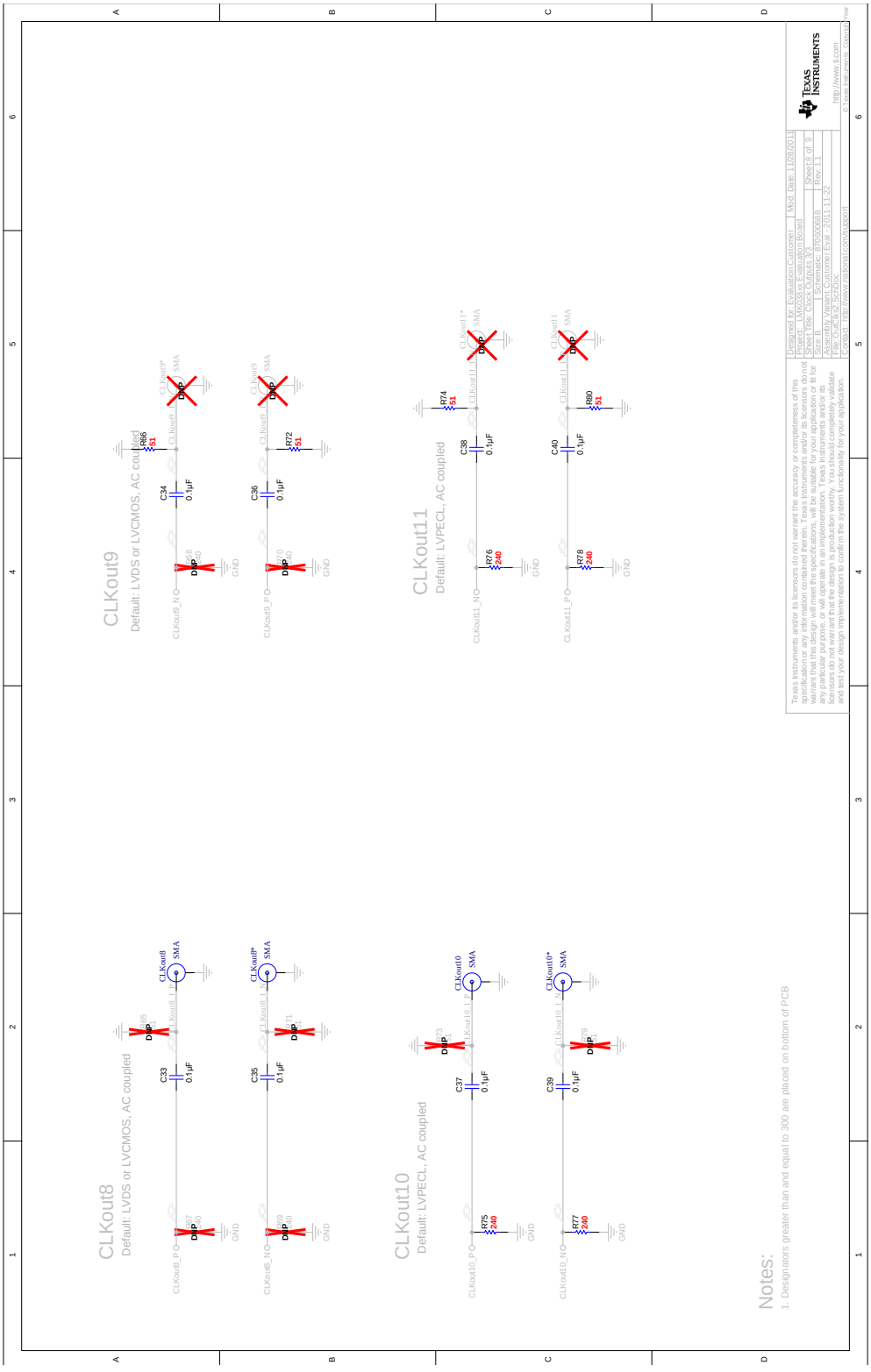

Figure 21 - LMK03806 Clock Outputs 8 through 11 Schematics

15. Bill of Materials

Table 11: Bill of Materials for LMK03806BEVAL Boards

Item	Description	Qty	Designator	Manufacturer	PartNumber
1	CAP, CERM, 47pF, 50V, +/-5%, C0G/NP0, 0603	1	C1_LF	Kemet	C0603C470J5GACTU
2	CAP, CERM, 3900pF, 50V, +/-10%, X7R, 0603	1	C2_LF	MuRata	GRM188R71H392KA01D
3	CAP, CERM, 0.1uF, 25V, +/-5%, X7R, 0603	33	C5, C8, C12, C15, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C45, C48, C60, C61	Kemet	C0603C104J3RACTU
4	CAP, CERM, 22pF, 50V, +/-5%, C0G/NP0, 0603	1	C6	AVX	06035A220JAT2A
5	CAP, CERM, 10uF, 10V, +/-10%, X5R, 0805	4	C7, C43, C46, C56	Kemet	C0805C106K8PACTU
6	RES, 0 ohm, 5%, 0.1W, 0603	10	C11, C14, R18, R84, R86, R88, R90, R95, R100, R104	Vishay-Dale	CRCW06030000Z0EA
7	RES, 240 ohm, 5%, 0.1W, 0603	16	C13, C16, R27, R28, R34, R35, R36, R37, R38, R39, R44, R45, R75, R76, R77, R78	Vishay-Dale	CRCW0603240RJNEA
8	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603	1	C31	Kemet	C0603C104K3RACTU
9	CAP, CERM, 1uF, 10V, +/-10%, X5R, 0603	3	C44, C47, C55	Kemet	C0603C105K8PACTU
10	CAP, CERM, 4.7uF, 10V, +/-10%, X5R, 0603	1	C53	Kemet	C0603C475K8PACTU
11	CAP, CERM, 2200pF, 50V, +/-10%, X7R, 0603	1	C54	Kemet	C0603C222K5RACTU
12	CAP, CERM, 0.1uF, 16V, +/-10%, X7R, 0603	1	C58	Kemet	C0603C104K4RACTU
13	Connector, SMT, End launch SMA 50 Ohm	16	CLKout0, CLKout0*, CLKout2, CLKout2*, CLKout4, CLKout4*, CLKout6, CLKout6*, CLKout8, CLKout8*, CLKout10, CLKout10*, OSCout0, OSCout0*, OSCout1, OSCout1*	Emerson Network Power	142-0701-851
14	LED 2.8X3.2MM 565NM RED CLR SMD	3	D1, D2, D4	Lumex Opto/Components Inc.	SML-LX2832IC
15	LED 2.8X3.2MM 565NM GRN CLR SMD	1	D3	Lumex Opto/Components Inc.	SML-LX2832GC
16	CONN TERM BLK PCB 5.08MM 2POS OR	1	J1	Weidmuller	1594540000

17	RES, 620 ohm, 5%, 0.1W, 0603	1	R2_LF	Vishay-Dale	CRCW0603620RJNEA
18	RES, 15k ohm, 5%, 0.1W, 0603	4	R3, R5, R7, R9	Vishay-Dale	CRCW060315K0JNEA
19	RES, 27k ohm, 5%, 0.1W, 0603	4	R4, R6, R8, R10	Vishay-Dale	CRCW060327K0JNEA
20	RES, 18 ohm, 5%, 0.1W, 0603	2	R12, R23	Vishay-Dale	CRCW060318R0JNEA
21	RES, 270 ohm, 5%, 0.1W, 0603	6	R14, R15, R19, R20, R21, R24	Vishay-Dale	CRCW0603270RJNEA
22	RES, 51 ohm, 5%, 0.1W, 0603	12	R33, R42, R43, R46, R48, R54, R56, R64, R66, R72, R74, R80	Vishay-Dale	CRCW060351R0JNEA
23	RES, 33 ohm, 5%, 0.1W, 0603	2	R57, R60	Vishay-Dale	CRCW060333R0JNEA
24	FB, 120 ohm, 500 mA, 0603	9	R81, R85, R87, R89, R91, R93, R96, R98, R101	Murata	BLM18AG121SN1D
25	RES, 0 ohm, 5%, 0.125W, 0805	1	R92	Vishay-Dale	CRCW08050000Z0EA
26	RES, 51k ohm, 5%, 0.1W, 0603	1	R94	Vishay-Dale	CRCW060351K0JNEA
27	RES, 2.00k ohm, 1%, 0.1W, 0603	1	R97	Vishay-Dale	CRCW06032K00FKEA
28	RES, 866 ohm, 1%, 0.1W, 0603	1	R99	Vishay-Dale	CRCW0603866RFKEA
29	RES, 1.00k ohm, 1%, 0.1W, 0603	2	R103	Vishay-Dale	CRCW06031K00FKEA
30	0.875" Standoff	6	S1, S2, S3, S4, S5, S6	VOLTREX	SPCS-14
31	LMK03806	1	U1	Texas Instruments	LMK03806BISQ
32	Micropower 800mA Low Noise 'Ceramic Stable' Adjustable Voltage Regulator for 1V to 5V Applications	1	U2	Texas Instruments	LP3878SD-ADJ
33	Low Profile Vertical Header 2x5 0.100"	1	uWire	FCI	52601-G10-8LF
34	Connector, TH, SMA	1	Vcc	Emerson Network Power	142-0701-201
35	100 MHz TCXO	1	Y3	Connor Winfield	CWX813-100.00M
36	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603	0	C1, C2, C3, C4	Kemet	C0603C101J5GACTU
37	CAP, CERM, 220pF, 50V, +/-5%, C0G/NP0, 0603	0	C2pLF	MuRata	GRM1885C1H221JA01D
38	CAP, CERM, 22pF, 50V, +/-5%, C0G/NP0, 0603	0	C9	AVX	06035A220JAT2A
39	CAP, CERM, 0.1uF, 25V, +/-5%, X7R, 0603	0	C10, C62, C64	Kemet	C0603C104J3RACTU
40	CAP, CERM, 470pF, 50V, +/-10%, X7R, 0603	0	C49, C51, C57	Kemet	C0603C471K5RACTU
41	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603	0	C50, C52, C59	Kemet	C0603C104K3RACTU
42	CAP, CERM, 1uF, 25V, +/-	0	C63, C65	AVX	08053D105KAT2A

	10%, X5R, 0805				
43	Connector, SMT, End launch SMA 50 Ohm	0	CLKout1, CLKout1*, CLKout3, CLKout3*, CLKout5, CLKout5*, CLKout7, CLKout7*, CLKout9, CLKout9*, CLKout11, CLKout11*, IC_SYNC, OSCin, OSCin*	Emerson Network Power	142-0701-851
44	RES, 270 ohm, 5%, 0.1W, 0603	0	R1, R2	Vishay-Dale	CRCW0603270RJNEA
45	RES, 0 ohm, 5%, 0.1W, 0603	0	R11, R16, R22	Vishay-Dale	CRCW06030000Z0EA
46	RES, 100 ohm, 5%, 0.1W, 0603	0	R17	Vishay-Dale	CRCW0603100RJNEA
47	RES, 51 ohm, 5%, 0.1W, 0603	0	R25, R26, R29, R30, R31, R32, R40, R41, R47, R53, R55, R63, R65, R71, R73, R79, R300	Vishay-Dale	CRCW060351R0JNEA
48	RES, 240 ohm, 5%, 0.1W, 0603	0	R49, R50, R51, R52, R58, R59, R61, R62, R67, R68, R69, R70	Vishay-Dale	CRCW0603240RJNEA
49	RES, 1.00k ohm, 1%, 0.1W, 0603	0	R102	Vishay-Dale	CRCW06031K00FKEA
50	FB, 1000 ohm, 600 mA, 0603	0	R82, R83	Murata	BLM18HE102SN1D
51		0	Y1, Y2	ECS	DNP_XTAL, ECS-200-20-30B-DU

16. PCB Layers Stackup

6-layer PCB Stackup includes:

- Top Layer for high-priority high-frequency signals (2 oz.)
- FR4 Dielectric, 19 mils
- RF Ground plane (1 oz.)
- FR4, 14.5 mils
- Power plane (1 oz.)
- FR4, 19 mils
- Bottom Layer copper clad for thermal relief (2 oz.)

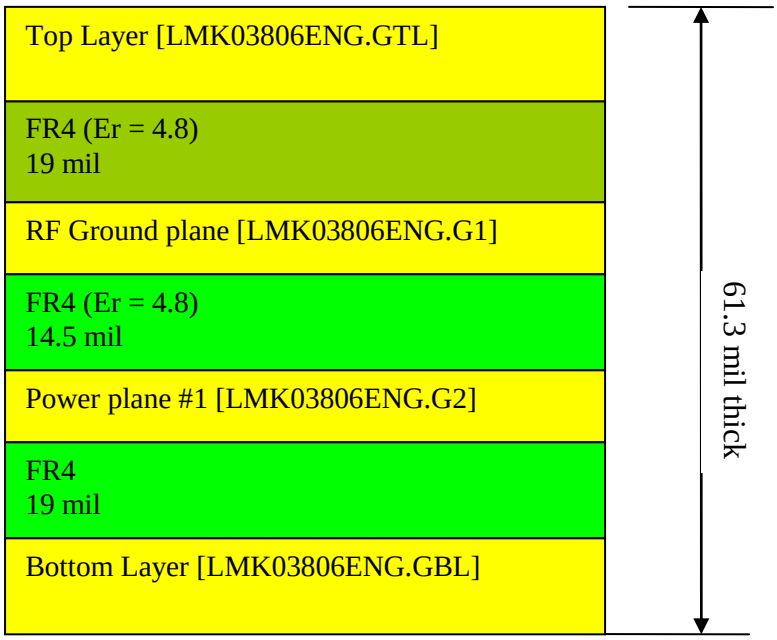

Figure 22: PCB Stackup

17. PCB Layout

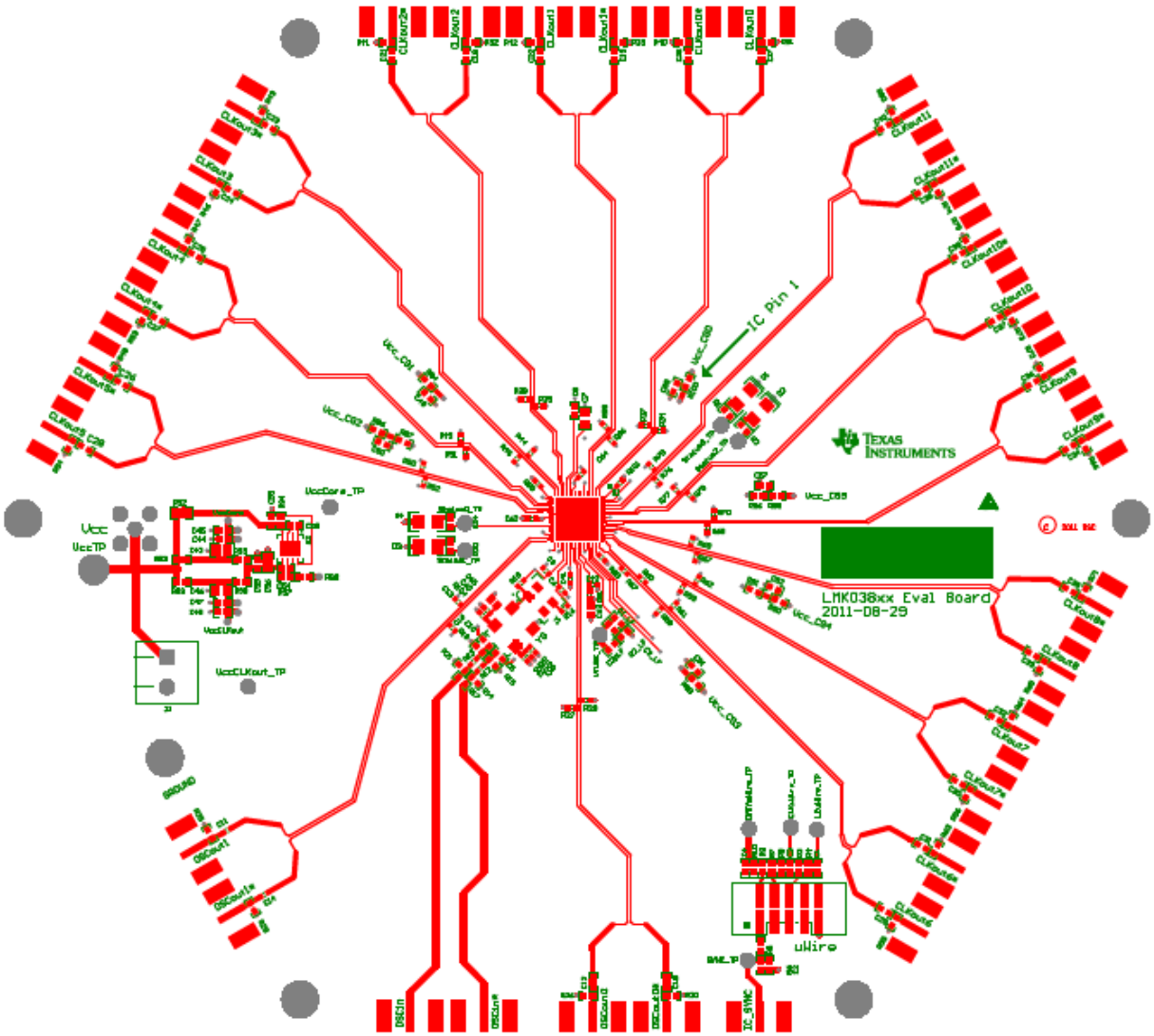

Figure 23: Layer 1 - Top

Figure 24: Layer 2 – RF Ground Plane

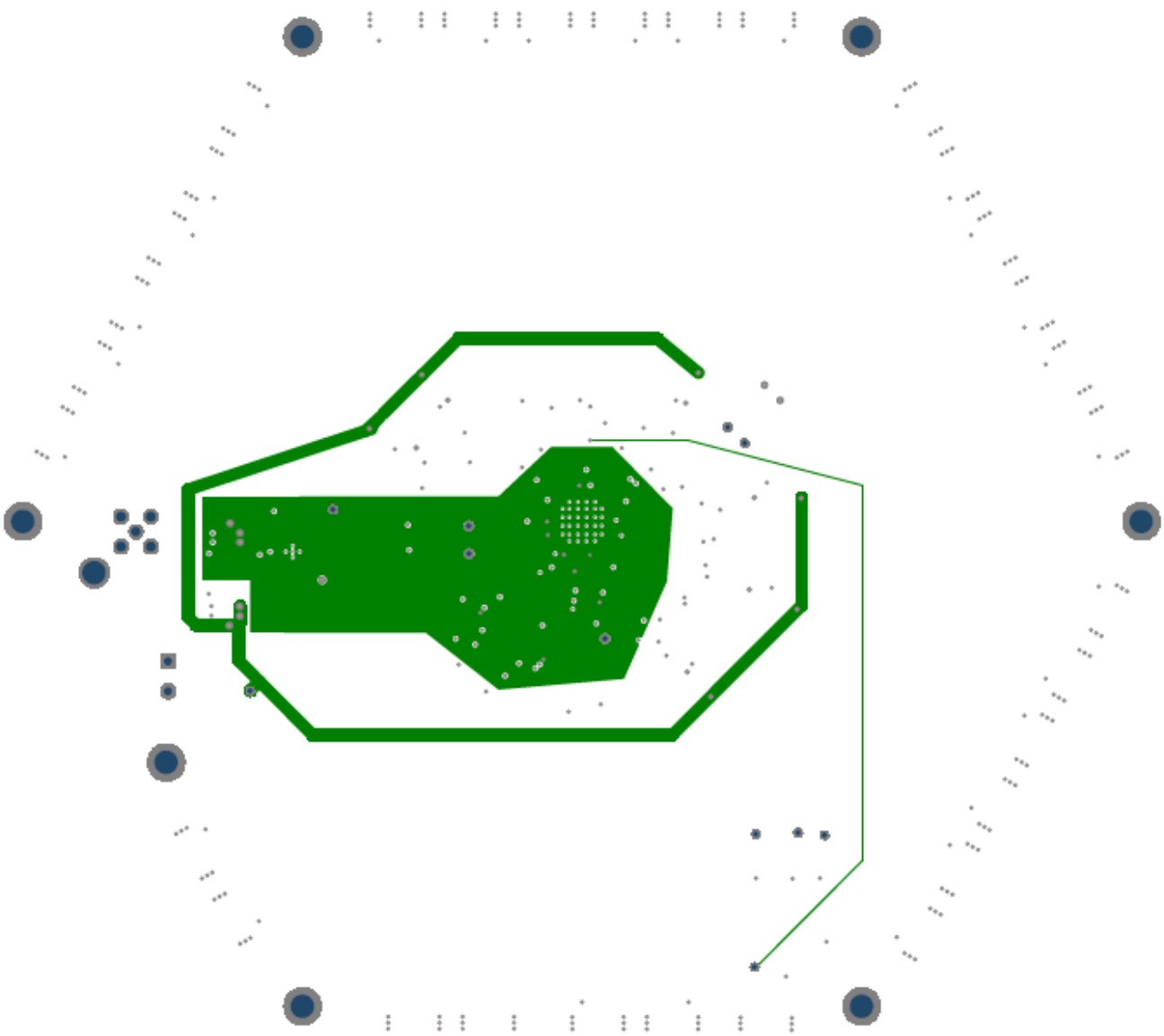

Figure 25: Layer 3 – Vcc Planes

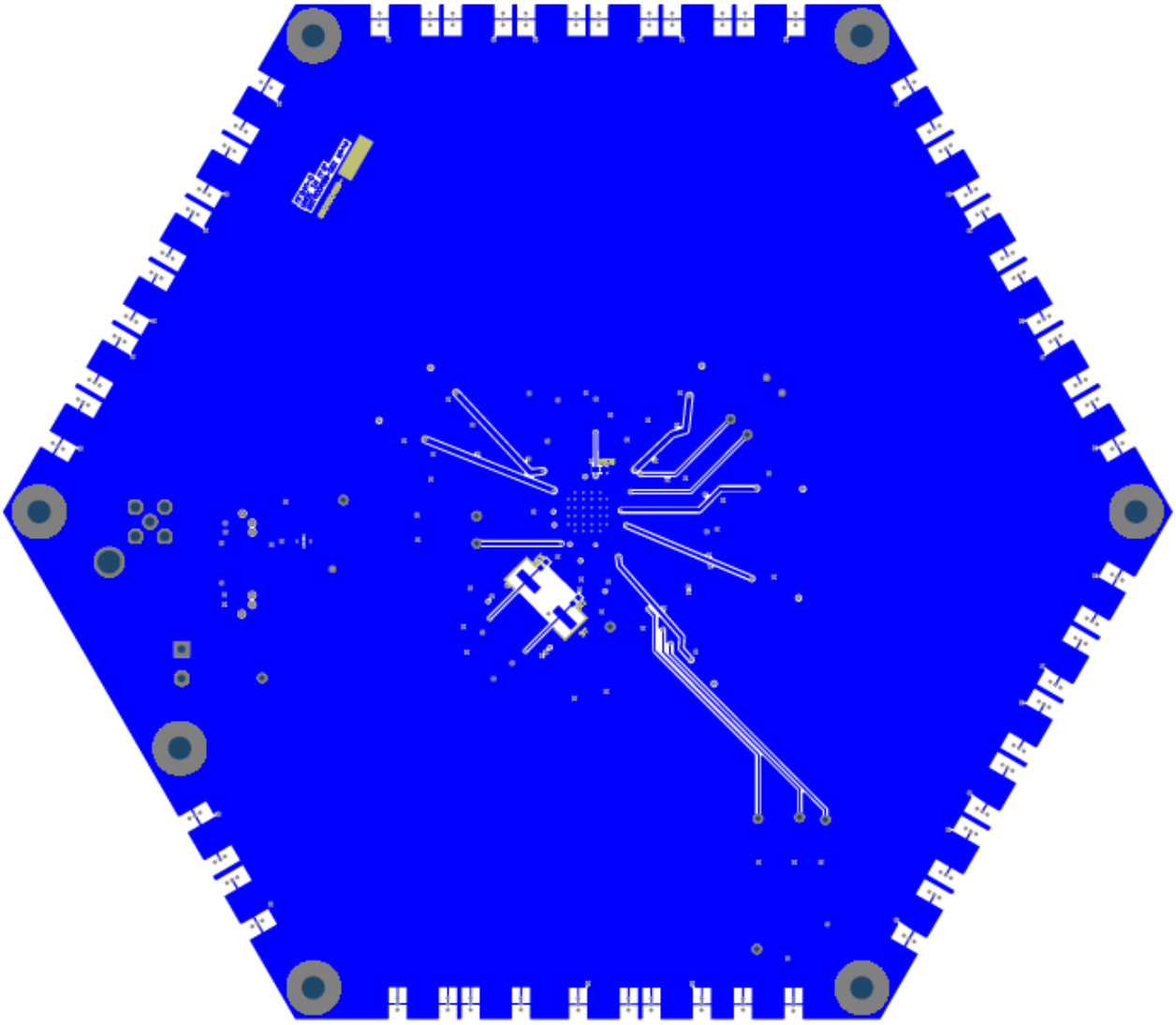

Figure 26: Layer 4 - Bottom

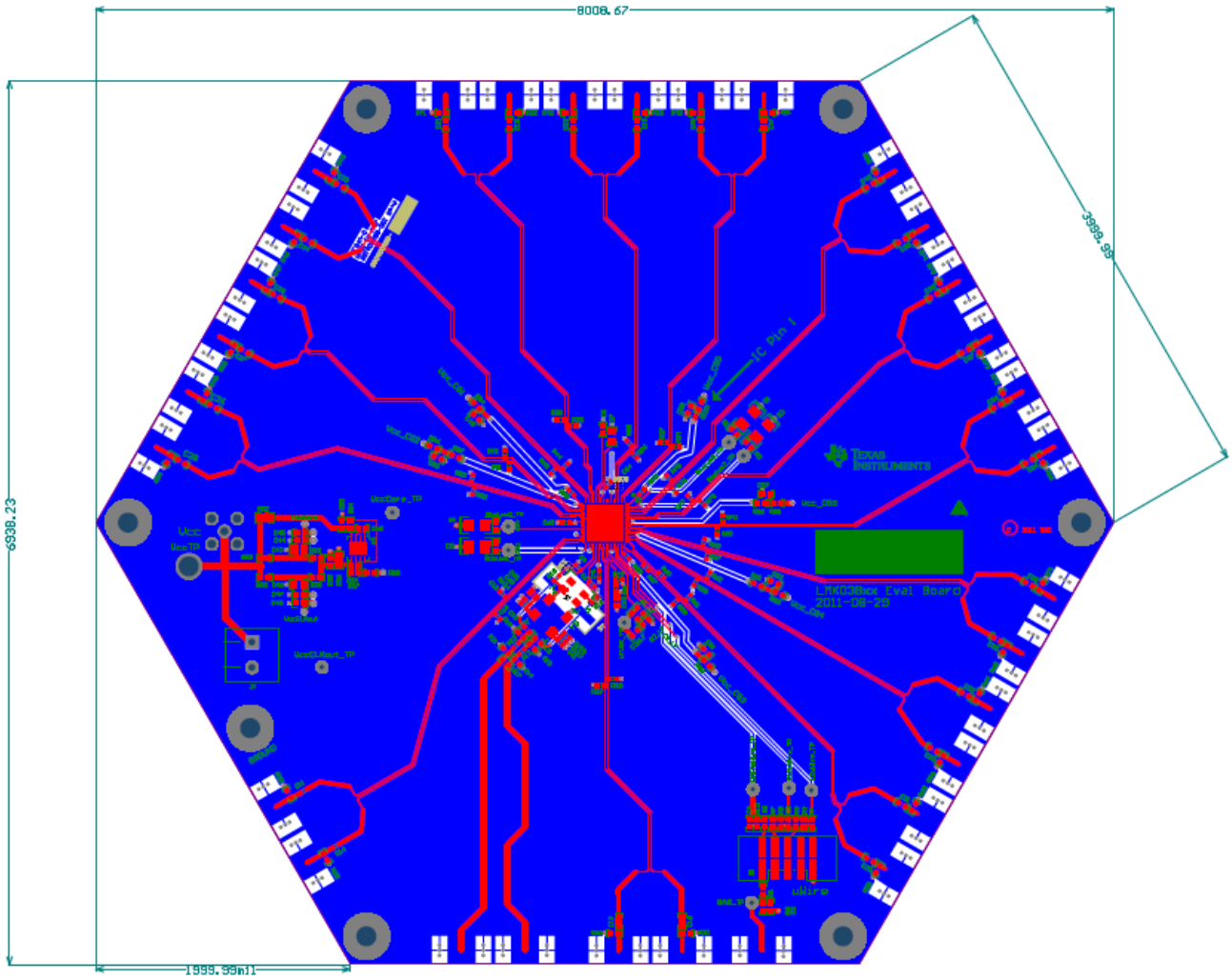

Figure 27: Top and Bottom (Composite)

18. Properly Configuring the LPT Port

When trying to solve any communications issue, it is most convenient to verify communication by programming the POWERDOWN bit to confirm normal or low supply current consumption of the evaluation board.

LPT Driver Loading

The parallel port must be configured for proper operation. To confirm that the LPT port driver is successfully loading click "LPT/USB" → "Check LPT." If the driver properly loads then the following message is displayed:

Figure 28: Successfully Opened LPT Driver

Successful loading of LPT driver does not mean LPT communications in CodeLoader are setup properly. The proper LPT port must be selected and the LPT port must not be in an improper mode.

The PC must be rebooted after install for LPT support to work properly.

Correct LPT Port/Address

To determine the correct LPT port in Windows, open the device manager (On Windows XP, Start → Settings → Control Panel → System → Hardware tab → Device Manager) and check the LPT port under the Ports (COM & LPT) node of the tree. It can be helpful to confirm that the LPT port is mapped to the expected port address, for instance to confirm that LPT1 is really mapped to address 0x378. This can be checked by viewing the Properties of the LPT1 port and viewing Resources tab to verify that the I/O Range starts at 0x378. CodeLoader expects the traditional port mapping:

Table 12: LPT Port Addresses

Port	Address
LPT1	0x378
LPT2	0x278
LPT3	0x3BC

If a non-standard address is used, use the "Other" port address in CodeLoader and type in the port address in hexadecimal. It is possible to change the port address in the computer's BIOS settings. The port address can be set in CodeLoader in the Port Setup tab as shown in Figure 29.

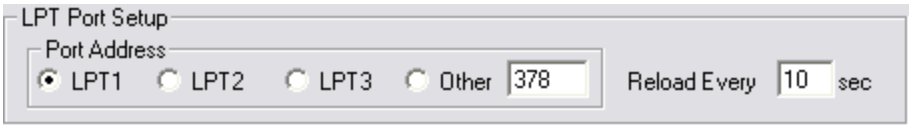

Figure 29: Selecting the LPT Port Address

Correct LPT Mode

If communications are not working, then it is possible the LPT port mode is set improperly. It is recommended to use the simple, Output-only mode of the LPT port. This can be set in the BIOS of the computer. Common terms for this desired parallel port mode are "Normal," "Output," or "AT." It is possible to enter BIOS setup during the initial boot up sequence of the computer.

19. Troubleshooting Information

If the evaluation board is not behaving as expected, the most likely issues are…

1) Board communication issue
2) Incorrect Programming of the device
3) Setup Error

Refer to this checklist for a practical guide on identifying/exposing possible issues.

Confirm Communications

Refer to Properly Configuring the LPT Port to troubleshoot this item.

Remember to load device with Ctrl+L.

EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/ kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.

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As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this is strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user’s authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.
~

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

Important Notice for Users of this Product in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan!

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

(1) Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,

(2) Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or

(3) Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product.

Also, please do not transfer this product, unless you give the same notice above to the transferee.

Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

Texas Instruments Japan Limited
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http://www.tij.co.jp

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EVALUATION BOARD/KIT/MODULE (EVM)

WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.

2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.

3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.

4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60^{o}C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

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