LMK04826/28 User's Guide

1 Introduction

These evaluation board instructions describes how to set up and operate the LMK04828/6 evaluation module (EVM). The LMK04828/6 is the industry's highest performance clock conditioner with JEDEC JESD204B support.

2 Evaluation Board Kit Contents

The evaluation board kit includes. -002 and -003 are currently available:

Table 1. EVM Contents

SV600788	-001	-002	-003
Evaluation Board	(1) LMK04828B Evaluation Board		(1) LMK04826B Evaluation Board
USB Communications	(1) USB2UWIRE-IFACE	(1) USB2ANY	
LPT Communicaitions	(1) CodeLoader uWire cable	-	

3 Quick Start

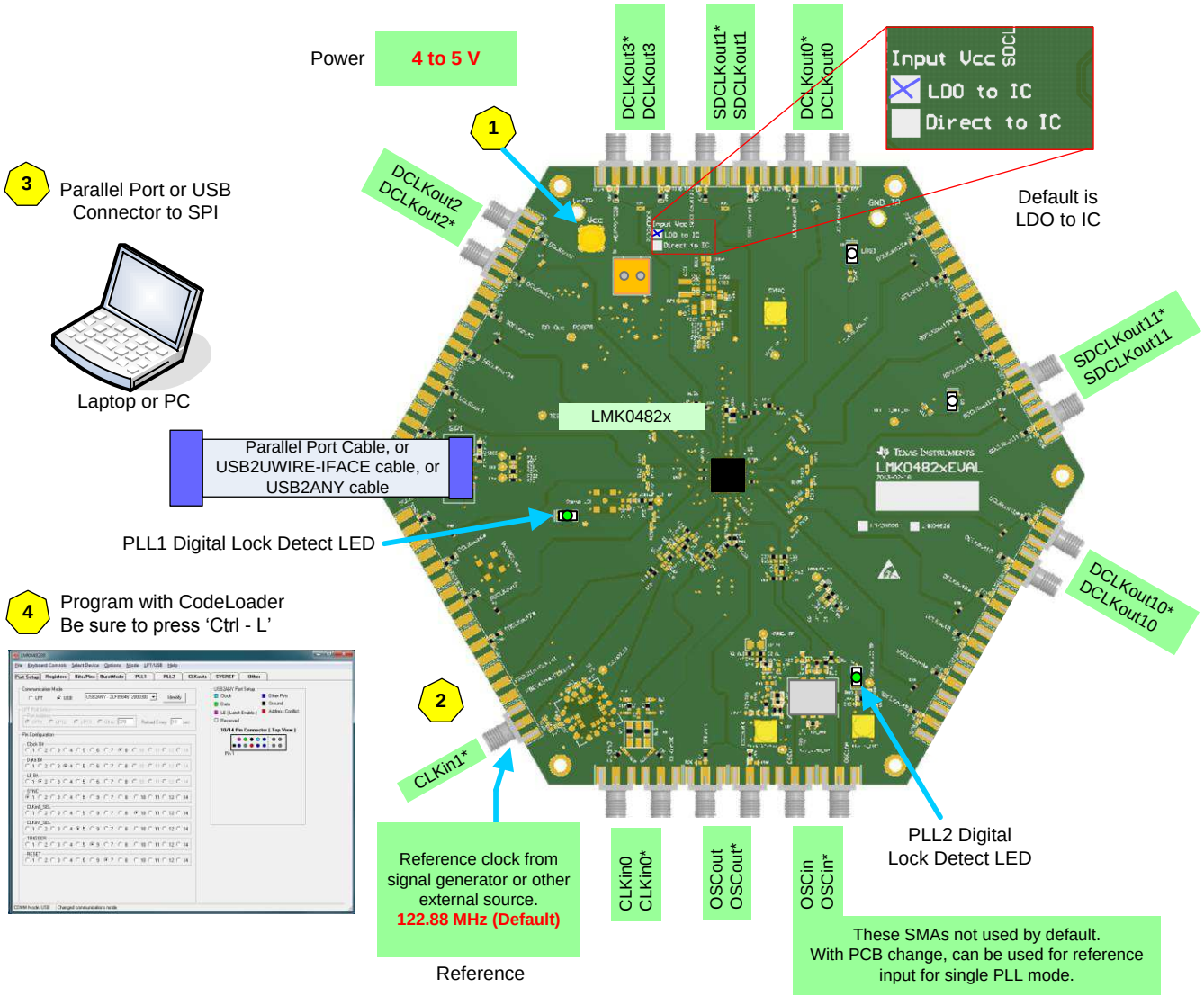

Figure 1. Quick Start Diagram

3.1 Quick Start Description

The LMK04828/6 EVM allows full verification of the device functionality and performance specifications. To quickly set up and operate the board with basic equipment, refer to the quick start procedure below and test setup shown in Figure 1.

1. Connect a voltage of **4.5** volts to the Vcc SMA connector or terminal block. Device operates at 3.3 V using onboard LP3878-ADJ LDO. VCXO operates at 3.3 V using onboard LP5900 LDO.
2. Connect a reference clock to the CLKin1 port from a signal generator or other source. Use **122.88 MHz** for default. Exact frequency and input port (CLKin0/CLKin1) depends on programming.
3. Connect the SPI header to a computer using USB2ANY, USB2UWIRE-IFACE, *or* parallel port with the CodeLoader cable.
4. Program the device with CodeLoader. CodeLoader is available for download at: http://www.ti.com/tool/codeloader.
   (a) Select LMK04828B or LMK04826B from “Select Device → Clock Conditioners” Menu.
   (b) **Select LPT or USB mode** from the Port Setup tab as required. If USB is selected, confirm that USB device being used to communicate with EVM is chosen from list of available USB devices.
   (c) Select a default mode from the “Mode” Menu. For the quick start use, “**CLKin1 122.88 MHz, OSCin 122.88 MHz**”
   (d) **Ctrl-L** must be pressed at least once to load all registers. Alternatively click menu Keyboard Controls → Load Device.
5. Measurements may be made at an active CLKout port via its SMA connector.

NOTE: New REV C boards dated 02-18-2013 have an updated Pin Configuration which is defaulted.

For older pre-release boards, Pin Configuration must manually be changed and only work with USB2UWIRE-IFACE or LPT cable.

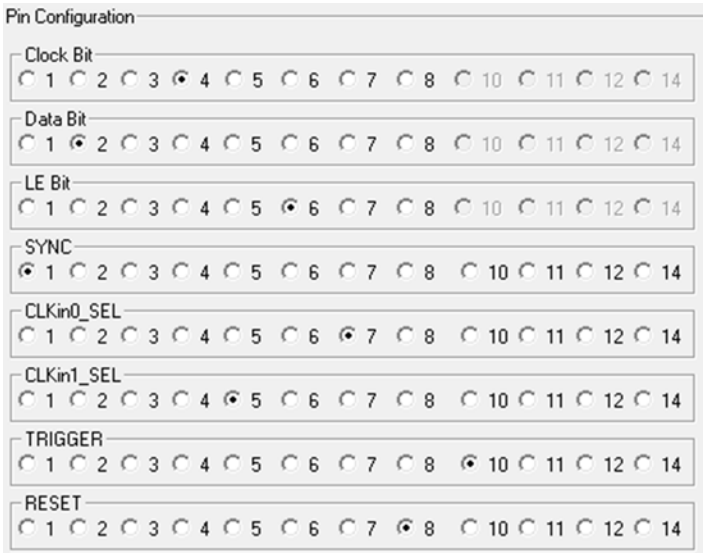

Figure 2. Pin Configuration for Pre-Release Boards

3.1.1 CLKout Tab Description

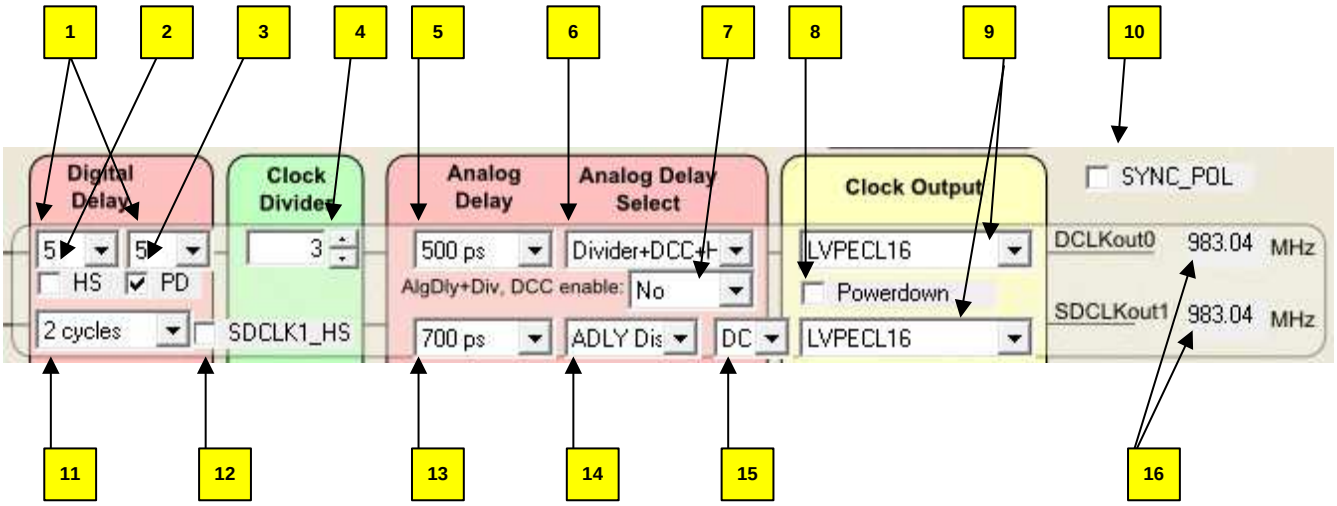

Figure 3. CLKout Tab Description Diagram

Device Clock Controls

1. CLKoutX_Y_CNTL/CNTH for controlling digital delay.
2. Half step bit (must have a HS mode selected by #6 or #7).
3. Power down digital delay for DCLKoutX.
4. DCLKoutX_DIV, divider for the output channel.
5. Analog delay (if enabled with #6).
6. Select source for output. Can be divider only, divider w/ DCC+HS (duty cycle correction and half step), bypass, or analog delay w/ Divider (and DCC/HS if selected by #7).
7. Select DCC/HS or not when using analog delay mode.
8. Powerdown the entire CLKoutX_Y block. Both outputs will be off.

Device Clock/SYSREF Controls

9. Select output type for each output.
10. SYNC_POL bit, will allow SYNC when in default configuration (SYNC_MODE / SYSREF_MUX setup for normal SYNC).

SYSREF Controls

11. SYSREF clock digital delay.
12. SYSREF clock half step
13. SYSREF analog delay (if enabled by #14)
14. Enable analog delay
15. Select Device Clock or SYSREF clock for output to SDCLKoutY clock.
16. Calculated output frequency.

3.1.2 CodeLoader Tips

- On Bits/Pins tab right-clicking any register name in the Bits/Pins tab will display a Help prompt with the register address, data bit location/length, and a brief register description.
- On PLL tabs clicking Show Bits will show register info.
- On other tabs, pressing ~ with a control focused will show help.

3.2 SYSREF Quick Start

The LMK0482x EVK allows for verification of the LMK0482x's implementation of JESD 204B SYSREF functionality. To quickly setup and operate the SYSREF functions refer to the following procedures.

3.2.1 Continuous SYSREF

1. Set SDCLKoutY_PD = 0 (where Y is the desired SDCLKout)
2. Set SDCLKoutY_MUX = 1 (Set to "SR" for desired SDCLKout)
3. Set SYSREF_PD and SYSREF_DDLY_PD = 0
4. Set SYNC_DISX and SYNC_DISSYSREF = 0 (where X is the desired DCLKout)
5. Perform a SYNC event (toggle SYNC_POL on/off/on)
6. Set SYNC_DISX = 1 (for desired DCLKout's) and SYNC_DISSYSREF = 1
7. Set SYSREF_MUX = 3 (SYSREF Continuous)
8. Ensure SYSREF_CLR = 0 (SYSREF tab, location: right side, below clock output pic)

In Figure 2 and Figure 4 the Blue trace is DCLKout6 at 245.76 MHz and the Green trace is SDCLKout7 (SYSREF) at 24.475 MHz. Figure 5 shows the configuration of the LMK0482xB outputs.

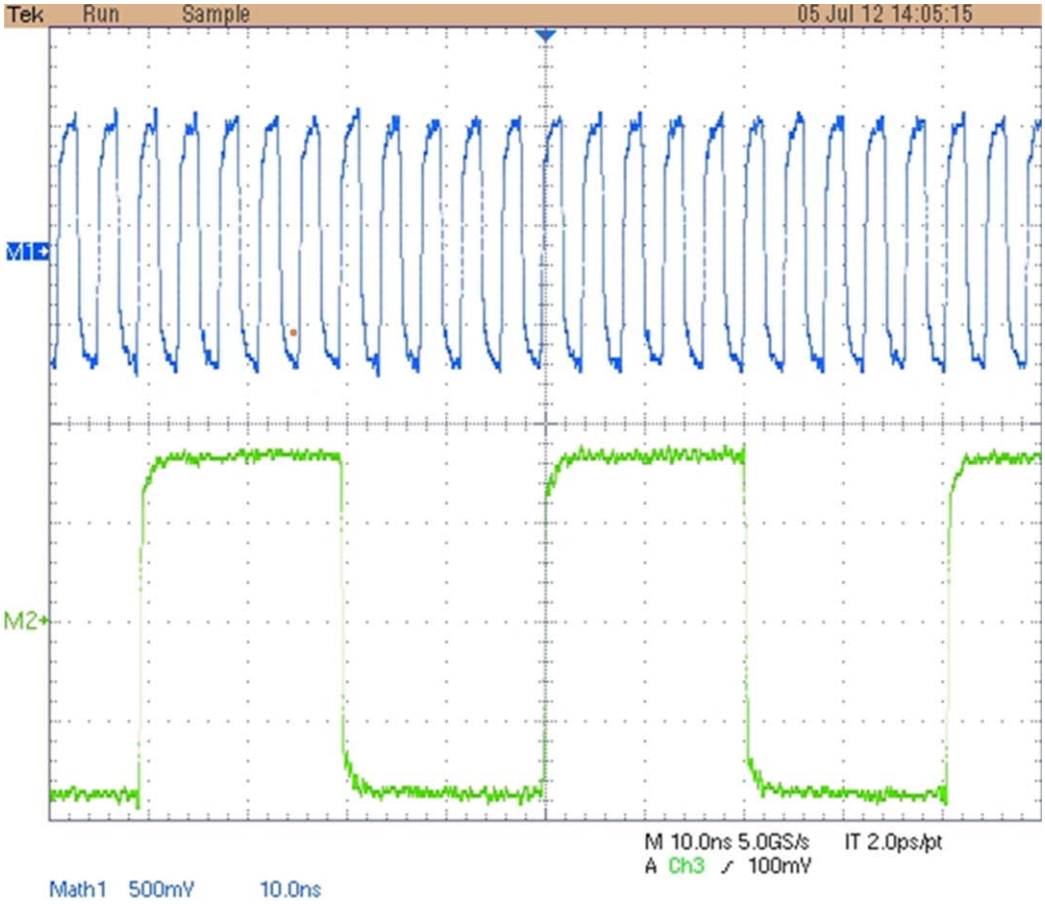

Figure 4. Continuous SYSREF Output

3.2.2 Pulsed SYSREF

1. Set SDCLKoutY_PD = 0 (where Y is the desired SDCLKout)
2. Set SDCLKoutY_MUX = 1 (Set to "SR" for desired SDCLKout)
3. Set SYSREF_PD and SYSREF_DDLY_PD = 0
4. Set SYNC_DISX and SYNC_DISSYSREF = 0 (where X is the desired DCLKout)

5. Perform a SYNC event (toggle SYNC_POL on/off/on)
6. Set SYNC_DISX = 1 (for desired DCLKout's) and SYNC_DISSYSREF = 1
7. Set SYSREF_MUX = 2 (SYSREF Pulses)
8. Set SYSREF_PULSE_CNT = 1, 2, 4, or 8 as desired
9. Generate a SYNC event (i.e. toggle SYNC_POL on/off/on)
10. Ensure SYSREF_CLR = 0 (SYSREF tab, location: right side, below clock output pic)

Figure 5. Pulsed SYSREF Output

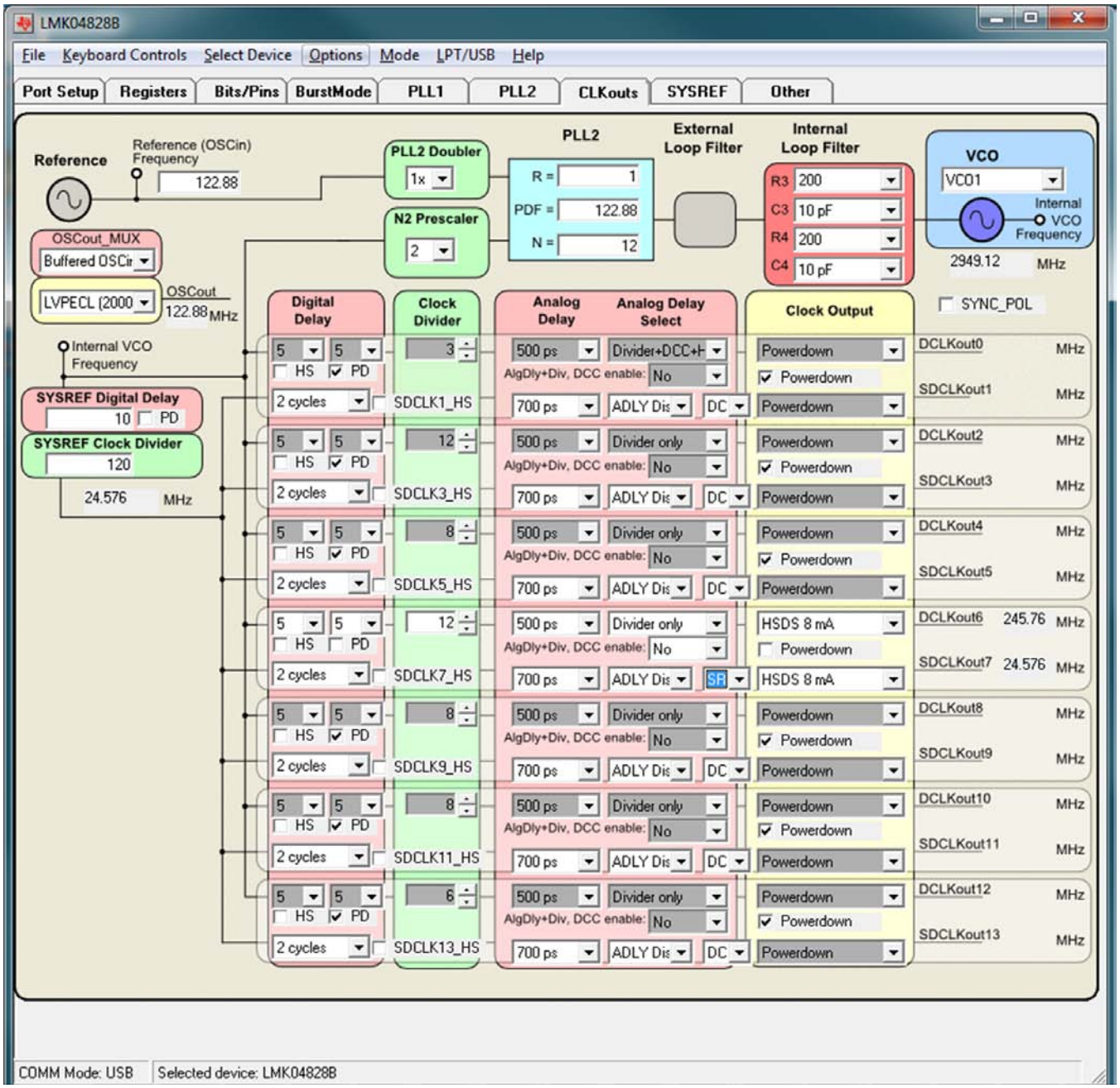

Figure 6. Clock Outputs Tab Setup for SYSREF Output on SDCLKout7

4 PLL Loop Filters and Loop Parameters

In jitter cleaning applications that use a cascaded or dual PLL architecture, the first PLL's purpose is to substitute the phase noise of a low-noise oscillator (VCXO or crystal resonator) for the phase noise of a "dirty" reference clock. The first PLL is typically configured with a narrow loop bandwidth in order to minimize the impact of the reference clock phase noise. The reference clock consequently serves only as a frequency reference rather than a phase reference.

The loop filters on the LMK048xx evaluation board are setup using the approach above. The loop filter for PLL1 has been configured for a narrow loop bandwidth (> 100 kHz). The specific loop bandwidth values depend on the phase noise performance of the oscillator mounted on the board. The following tables (Table 2 and Table 3) contain the parameters for PLL1 and PLL2 for each oscillator option.

TI's Clock Design Tool can be used to optimize PLL phase noise/jitter for given specifications. See: http://www.ti.com/tool/clockdesigntool

4.1 PLL1 Loop Filter

Table 2. PLL1 Loop Filter Parameters for Crystek 122.88 MHz VCXO(1)

122.88 MHz VCXO PLL			
Phase Margin	50˚	**Kφ (Charge Pump)**	450 uA
Loop Bandwidth	14 Hz	**Phase Detector Freq**	1.024 MHz
		VCO Gain	2.5 kHz/V
Reference Clock Frequency	122.88 MHz	**Output Frequency**	122.88 MHz (To PLL 2)
Loop Filter Components	C1_A1 = 100 nF	C2_A1 = 680 nF	R2_A1 = 39 kΩ

(1) Loop Bandwidth is a function of Kφ, Kvco, N as well as loop components. Changing Kφ and N will change the loop bandwidth.

4.2 PLL2 Loop Filter

Table 3. Integrated VCO PLL(1)

	LMK04826		LMK04828		
	VCO0	VCO1	VCO0	VCO1	
C1_A2	0.047				nF
C2_A2	3.9				nF
C3 (internal)	0.01				nF
C4 (internal)	0.01				nF
R2_A2	0.62				kΩ
R3 (internal)	0.2				kΩ
R4 (internal)	0.2				kΩ
Charge Pump Current, Kφ	3.2				mA
Phase Detector Frequency	122.88				MHz
Frequency	1966.08	2457.6	2457.6	2949.12	MHz
Kvco	15.3	8.9	21.9	17.4	MHz/V
N	16	20	20	24	
Phase Margin	73	64	73	70	degrees
Loop Bandwidth	303	151	344	233	kHz

(1) PLL Loop Bandwidth is a function of Kφ, Kvco, N as well as loop components. Changing Kφ and N will change the loop bandwidth.

5 Default CodeLoader Modes for the LMK0482x

CodeLoader saves the state of the selected LMK0482x device when exiting the software. To ensure a common starting point, the following modes listed in Table 4 may be restored by clicking “Mode” and selecting the appropriate device configuration.

Table 4. Default CodeLoader Modes for the LMK0482x

Default CodeLoader Mode	Device Mode	CLKin Frequency	OSCin Frequency
CLKin1 122.88 MHz, OSCin 122.88 MHz	Dual PLL, Internal VCO	122.88 MHz	122.88 MHz

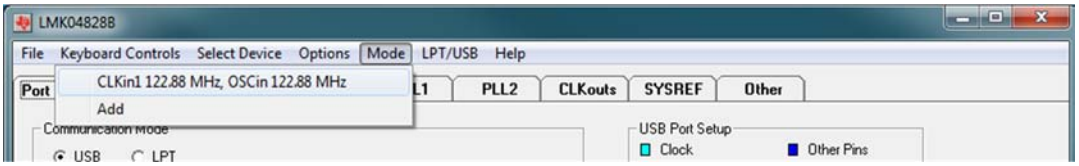

Figure 7. Selecting a Default Mode for the LMK04828 Device

6 Using CodeLoader to Program the LMK04828

The purpose of this section is to walk the user through using CodeLoader 4 to make some measurements with the LMK04828B device as an example. For more information on CodeLoader refer to CodeLoader 4 instructions located at http://www.ti.com/tool/codeloader

Before proceeding, be sure to follow the Section 3 section above to ensure proper connections. To program the LMK04826B the procedure would be the same but select the LMK04826B as the device.

6.1 Start CodeLoader Application

Click “Start” → “Programs” → “CodeLoader 4” → “CodeLoader 4”

The CodeLoader 4 program is installed by default to the CodeLoader 4 application group.

6.2 Select Device

Click “Select Device” → “Clock Conditioners” → “LMK04828B”

Once started CodeLoader 4 will load the last used device. To load a new device click “Select Device” from the menu bar, then select the subgroup and finally device to load. For this example, the LMK04828B is chosen. Selecting the device does cause the device to be programmed.

6.3 Program/Load Device

Assuming the Port Setup settings are correct, press the “Ctrl+L” shortcut or click “Keyboard Controls” → “Load Device” from the menu to program the device to the current state of the newly loaded LMK04828 file.

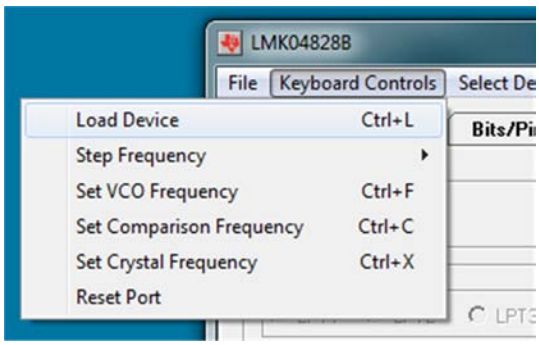

Figure 8. Loading the Device

Once the device has been initially loaded, CodeLoader will automatically program changed registers so it is not necessary to re-load the device upon subsequent changes in the device configuration. It is possible to disable this functionality by ensuring there is no checkmark by the “Options” → “AutoReload with Changes.”

Because a default mode will be restored in the next step, this step isn’t really needed but included to emphasize the importance of pressing “Ctrl+L” to load the device at least once after starting CodeLoader, restoring a mode, or restoring a saved setup using the File menu.

See CodeLoader 4 instructions located at http://www.ti.com/tool/codeloader/ for more information on Port Setup. This contains information on troubleshooting communications.

6.4 Restoring a Default Mode

Click “Mode” → “CLKin1 122.88 MHz, OSCin 122.88 MHz”; then press Ctrl+L.

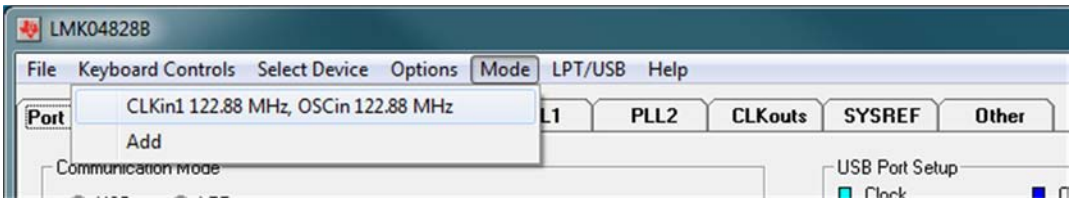

Figure 9. Setting the Default Mode for LMK04828

For the purpose of this walkthrough, a default mode will be loaded to ensure a common starting point. This is important because when CodeLoader is closed, it remembers the last settings used for a particular device. Again, remember to press Ctrl+L as the first step after loading a default mode.

6.5 Visual Confirmation of Frequency Lock

After a default mode is restored and loaded, LED D4, and D5 should illuminate when PLL1 and PLL2 are locked to the reference clock applied to CLKin1. This assumes PLL1_LD_MUX = PLL1_DLD, PLL2_LD_MUX = PLL2_DLD and PLLX_LD_TYPE = Output (Push-Pull).

6.6 Enable Clock Outputs

While the LMK0482x offers programmable clock output buffer formats, the evaluation board is shipped with preconfigured output terminations to match the default buffer type for each output.

To measure Phase noise at one of the clock outputs, for example DCLKout0:

1. 1. Click on the Distribution tab,
2. 2. Uncheck “Powerdown” in the Clock output box to enable the channel,
3. 3. Set the following settings as needed:
   (a) Digital Delay value
   (b) Clock Divider value
   (c) Analog delay select and Analog Delay value (if not “Analog Delay and Divider” is selected in the Analog Delay Select box,

Figure 10. Setting Digital Delay, Clock Divider, Analog Delay and Output Format

4. Depending on the configured output type, the clock output SMAs can be interfaced to a test instrument with a single-ended 50-ohm input as follows.
   (a) For LVDS:
      (i) A balun (like ADT2-1T or high quality Prodyn BIB-100G) is recommended for differential-to-single-ended conversion.
   (b) For LVPECL:
      (i) A balun can be used, or
      (ii) One side of the LVPECL signal can be terminated with a 50-ohm load and the other side can be run single-ended to the instrument.
   (c) For HSDS:
      (i) A balun (like ADT2-1T or high quality Prodyn BIB-100G) is recommended for differential-to-single-ended conversion.
5. The phase noise may be measured with a spectrum analyzer or signal source analyzer.

TI’s Clock Design Tool can be used to calculate divider values to achieve desired clock output frequencies. See: http://www.ti.com/tool/clockdesigntool

7 Evaluation Board Inputs and Outputs

The following table (Table 5) contains descriptions of the inputs and outputs for the evaluation board. Unless otherwise noted, the connectors described can be assumed to be populated by default. Additionally, some applicable CodeLoader programming controls are noted for convenience.

Table 5. Description of Evaluation Board Inputs and Outputs

<table>
<tr><th>Connector Name</th><th>Signal Type, Input/Output</th><th>Description</th></tr>
<tr><td rowspan="18">Populated:
DCLKout0,
DCLKout0*,
SDCLKout1,
SDCLKout1*,
DCLKout2,
DCLKout2*,
SDCLKout3,
SDCLKout3*,
DCLKout10,
DCLKout10*
SDCLKout11,
SDCLKout11*</td><td rowspan="18">Analog,
Output</td><td colspan="2">Clock outputs with programmable output buffers.

The output terminations by default on the evaluation board are shown below:</td></tr>
<tr><td>Clock Output Pair</td><td>Default Board Termination</td></tr>
<tr><td>DCLKout0</td><td>240 Ω</td></tr>
<tr><td>SDCLKout1</td><td>240 Ω</td></tr>
<tr><td>DCLKout2</td><td>240Ω</td></tr>
<tr><td>SDCLKout3</td><td>240 Ω</td></tr>
<tr><td>DCLKout4</td><td>HSDS / LVDS</td></tr>
<tr><td>SDCLKout5</td><td>HSDS / LVDS</td></tr>
<tr><td>DCLKout6</td><td>HSDS / LVDS</td></tr>
<tr><td>SDCLKout7</td><td>HSDS / LVDS</td></tr>
<tr><td>DCLKout8</td><td>HSDS / LVDS</td></tr>
<tr><td>SDCLKout9</td><td>HSDS / LVDS</td></tr>
<tr><td>DCLKout10</td><td>HSDS / LVDS</td></tr>
<tr><td>SDCLKout11</td><td>HSDS / LVDS</td></tr>
<tr><td>DCLKout12</td><td>HSDS / LVDS</td></tr>
<tr><td>SDCLKout13</td><td>HSDS / LVDS</td></tr>
<tr><td colspan="2">Each CLKout pair has a programmable LVDS, LVPECL, or HSDS buffer. The output buffer type can be selected in CodeLoader in the Clock Outputs tab via the CLKoutX_TYPE control.

All clock outputs are AC-coupled to allow safe testing with RF test equipment.

All LVPECL clock outputs are terminated using 240 Ω emitter-resistors.

If an output pair is programmed to LVCMOS, each output can be independently configured (normal, inverted, or off/tri-state).</td></tr>
<tr><td rowspan="6">Populated:
OSCout, OSCout*</td><td rowspan="6">Analog,
Output</td><td colspan="2">Buffered outputs of OSCin port.</td></tr>
<tr><td colspan="2">The output terminations on the evaluation board are shown below.:</td></tr>
<tr><td>OSC output pair</td><td>Default Board Termination</td></tr>
<tr><td>OSCout</td><td>LVPECL</td></tr>
<tr><td colspan="2">OSCout has a programmable LVDS, LVPECL, or LVCMOS output buffer. The OSCout buffer type can be selected in CodeLoader on the Distribution tab via the OSCout_FMT control.

OSCout is AC-coupled to allow safe testing with RF test equipment.

The OSCout output is terminated using 240 Ω emitter-resistors.

If OSCout is programmed as LVCMOS, each output can be independently configured (normal, inverted, inverted, and off/tri-state).</td></tr>
<tr><td colspan="2">Best performance/EMI reduction is achieved by using a complementary output mode like Norm/Inv. It is NOT recommended to use Norm/Norm or Inv/Inv mode.</td></tr>
<tr><td>Vcc</td><td>Power,
Input</td><td colspan="2">Main power supply input for the evaluation board.

The LMK0482x contains internal voltage regulators for the VCO, PLL and other internal blocks. The clock outputs do not have an internal regulator, so a clean power supply with sufficient output current capability is required for optimal performance.

On-board LDO regulators and 0 Ω resistor options provide flexibility to supply and route power to various devices. See the schematics in section Section 11 for more details.</td></tr>
</table>

Table 5. Description of Evaluation Board Inputs and Outputs (continued)

Connector Name	Signal Type, Input/Output	Description
Populated: J1	Power, Input	Alternative power supply input for the evaluation board using two unshielded wires (Vcc and GND). Apply power to either Vcc SMA or J1, but not both.
VccVCXO/Aux	Power, Input	Optional Vcc input to power the VCXO circuit if separated voltage rails are needed. The VccVCXO/Aux input can power these circuits directly or supply the on-board LDO regulators. 0 Ω resistor options provide flexibility to route power.
Populated: CLKin0, CLKin0*, CLKin1* Not Populated: CLKin1	Analog, Input	Reference Clock Inputs for PLL1 (CLKin0, 1). CLKin1 can alternatively be used as an External Feedback Clock Input (FBCLKin) in 0-delay mode or an RF Input (Fin) in External VCO mode. **Reference Clock Inputs for PLL1 (CLKin0, 1)** FBCLKin/CLKin1* is configured by default for a single-ended reference clock input from a 50-ohm source.The non-driven input pin (FBCLKin/CLKin1) is connected to GND with a 0.1 uF. CLKin0/CLKin0* is configured by default for a differential reference clock input from a 50-ohm source. CLKin1* is the default reference clock input selected in CodeLoader. The clock input selection mode can be programmed on the **Bits/Pins** tab via the Clock Inputs control. **External Feedback Input (FBCLKin) for 0-Delay** CLKin1 is shared for use with FBCLKin as an external feedback clock input to PLL1 for 0-delay mode. See the LMK04820 family datasheet (literature number SNAS605) for more details on using 0-delay mode with the evaluation board and the evaluation board software.
Populated: OSCin, OSCin*	Analog, Input	Feedback VCXO clock input to PLL1 and Reference clock input to PLL2. The single-ended output of the onboard VCXO (U4) drives the OSCin* input of the device and the OSCin input of the device is connected to GND with 0.1 uF. A VCXO add-on board may be optionally attached via these SMA connectors with minor modification to the components going to the OSCin/OSCin* pins of device. This is useful if the VCXO footprint does not accommodate the desired VCXO device or if the user desires to use the LMK0482xB in single loop mode. A single-ended or differential signal may be used to drive the OSCin/OSCin* pins and must be AC coupled. If operated in single-ended mode, the unused input must be connected to GND with 0.1 uF. Refer to the LMK04820 family datasheet section “Electrical Characteristics” for PLL2 Reference Input (OSCin) specifications (literature number SNAS605).
Test point: VTUNE1_TP	Analog, Input	Tuning voltage output from the loop filter for PLL1. If a VCXO add-on board is used, this tuning voltage can be connected to the voltage control pin of the external VCXO when this SMA connector is installed and connected through R72 by the user.
Test point: VTUNE2_TP	Analog, Input	Tuning voltage output from the loop filter for PLL2.
Test points: SDIO SCK CS*	CMOS, Input/Output	10-pin header for SPI programming interface and programmable logic I/O pins for the LMK0482x.
Populated: SPI		10-pin header for SPI programming interface and programmable logic I/O pins for the LMK0482x. The programmable logic I/O signals accessible through this header include: RESET, SYNC, Status_LD1, Status_LD2, CLKin_SEL0, and CLKin_SEL1. These logic I/O signals also have dedicated SMAs and test points.

Table 5. Description of Evaluation Board Inputs and Outputs (continued)

<table>
<tr><th>Connector Name</th><th>Signal Type, Input/Output</th><th>Description</th></tr>
<tr><td>Test point:
Status_LD1_TP

Status_LD</td><td>CMOS,
Input/Output</td><td>Programmable status output pin. By default, set to output the digital lock detect status signal for PLL1.

In the default CodeLoader modes, LED D5 will illuminate green when PLL1 lock is detected by the LMK0482x (output is high) and turn off when lock is lost (output is low).

The status output signal for the Status_LD1 pin can be selected on the Bits/Pins tab via the PLL1_LD_MUX control.</td></tr>
<tr><td>Test point:
Status_LD2_TP

Status_LD2</td><td>CMOS,
Input/Output</td><td>Programmable status output pin. By default, set to output the digital lock detect status signal for PLL2.

In the default CodeLoader modes, LED D4 will illuminate green when PLL1 lock is detected by the LMK0482x (output is high) and turn off when lock is lost (output is low).

The status output signal for the Status_LD1 pin can be selected on the Bits/Pins tab via the PLL2_LD_MUX control.</td></tr>
<tr><td>Test points:
CLKin0_SEL_TP
CLKin1_SEL_TP</td><td>CMOS,
Input/Output</td><td>Programmable status I/O pins. By default, set as input pins for controlling input clock switching of CLKin0 and CLKin1.

These inputs will not be functional because CLKin_SEL_MODE is set to 0 (CLKin0 Manual) by default in the Bits/Pins tab in CodeLoader. To enable input clock switching, CLKin_SEL_MODE must be 3 and Status_CLKinX_TYPE must be 0 to 3 (pin enabled as an input).

Input Clock Switching – Pin Select Mode
When CLKin_SEL_MODE is 3, the Status_CLKinX pins select which clock input is active as follows:
<table>
<tr><th>Status_CLKin1</th><th>Status_CLKin0</th><th>Active Clock</th></tr>
<tr><td>0</td><td>0</td><td>CLKin0</td></tr>
<tr><td>0</td><td>1</td><td>CLKin1</td></tr>
<tr><td>1</td><td>0</td><td>CLKin2</td></tr>
<tr><td>1</td><td>1</td><td>Holdover</td></tr>
</table></td></tr>
<tr><td>Test point:
SYNC_TP

Populated:
SYNC</td><td>CMOS,
Input/Output</td><td rowspan="2">Programmable status I/O pin. By default, set as an input pin for synchronize the clock outputs with a fixed and known phase relationship between each clock output selected for SYNC. A SYNC event also causes the digital delay values to take effect.

SYNC/SYSREF_REQ pin forces the SYSREF_MUX into SYSREF Continuous mode (0x03) when SYSREF_REQ_EN = 1.

SYNC/SYSREF_REQ pin can hold outputs in a low state, depending on system configuration. SYNC_POL adjusts for active low or active high control.

A SYNC event can also be programmed by toggling the SYNC_POL_INV bit in the Bits/Pins tab in CodeLoader.

Programmable status I/O pin.</td></tr>
<tr><td>Test point:
RESET_TP</td><td>CMOS,
Input/Output</td></tr>
</table>

8 Recommended Test Equipment

Power Supply

The Power Supply should be a low noise power supply, particularly when the devices on the board are being directly powered (onboard LDO regulators bypassed).

Phase Noise / Spectrum Analyzer

To measure phase noise and RMS jitter, an Agilent E5052 Signal Source Analyzer is recommended. An Agilent E4445A PSA Spectrum Analyzer with the Phase Noise option is also usable although the architecture of the E5052 is superior for phase noise measurements. At frequencies less than 100 MHz the local oscillator noise of the E4445A is too high and measurements will reflect the E4445A's internal local oscillator performance, not the device under test.

Oscilloscope

To measure the output clocks for AC performance, such as rise time or fall time, propagation delay, or skew, it is suggested to use a real-time oscilloscope with at least 1 GHz analog input bandwidth (2.5+ GHz recommended) with 50 ohm inputs and 10+ Gsps sample rate. To evaluate clock synchronization or phase alignment between multiple clock outputs, it's recommended to use phase-matched, 50-ohm cables to minimize external sources of skew or other errors/distortion that may be introduced if using oscilloscope probes.

9 Appendix A: CodeLoader Usage

Code Loader is used to program the evaluation board with either an LPT port using the included CodeLoader cable or with a USB port using the included USB2UWIRE-IFACE.

9.1 Port Setup Tab

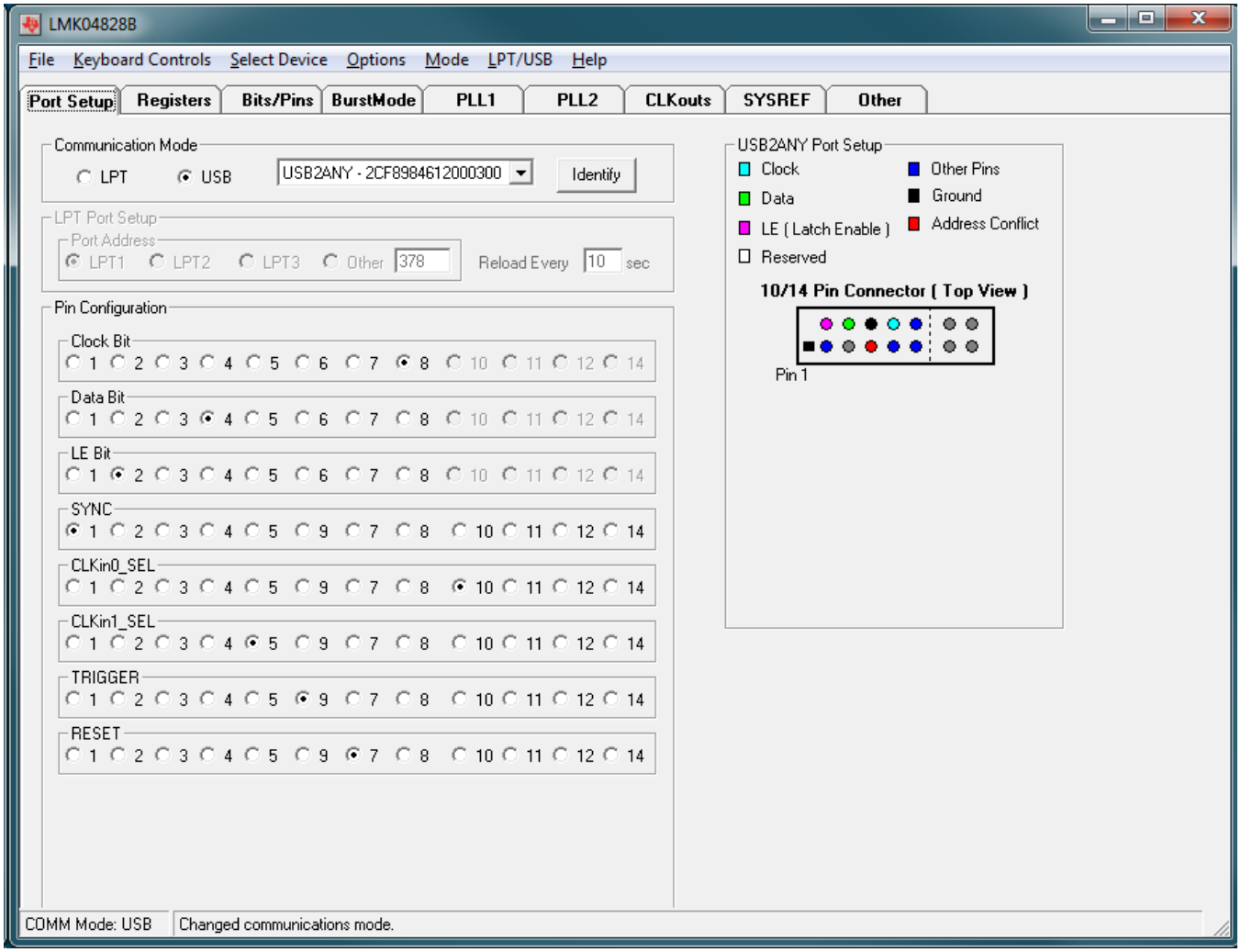

Figure 11. Port Setup Tab

On the Port Setup tab, the user may select the type of communication port (USB or Parallel) that will be used to program the device on the evaluation board. If parallel port is selected, the user should ensure that the correct port address is entered. If USB mode is selected, identify the correct target device by clicking the Identify button - the selected USB2ANY will blink the onboard LED 5 times.

The Pin Configuration field is hardware dependent and normally **does not** need to be changed by the user (except for pre-release boards). For information on this configuration, refer to Figure 2.

9.2 PLL1 Tab

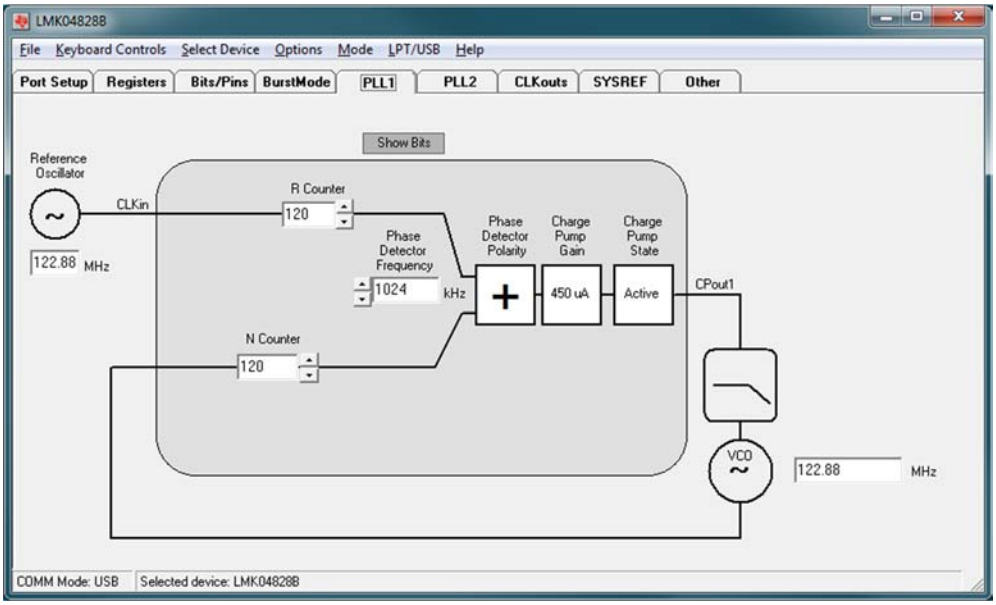

Figure 12. PLL1 Tab

The PLL1 tab allows the user to change the following parameters in Table 6.

Table 6. Registers Controls and Descriptions in PLL1 Tab

Control Name	Register Name	Description
Reference Oscillator Frequency (MHz)	n/a	CLKin frequency of the selected reference clock.
Phase Detector Frequency (MHz)	n/a	PLL1 Phase Detector Frequency (PDF). This value is calculated as: PLL1 PDF = CLKin Frequency / (PLL1_R)
VCO Frequency (MHz)	n/a	The VCO Frequency should be the OSCin frequency, except when operating in Dual PLL with 0-delay feedback. This value is calculated as: VCO Freq (OSCin freq) = PLL1 PDF * PLL1_N.
R Counter	PLL1_R	PLL1 R Counter value (1 to 16383).
N Counter	PLL1_N	PLL1 N Counter value (1 to 16383).
Phase Detector Polarity	PLL1_CP_POL	PLL1 Phase Detector Polarity. Click on the polarity sign to toggle polarity "+" or "–".
Charge Pump Gain	PLL1_CP_GAIN	PLL1 Charge Pump Gain. Left-click/right-click to increase/decrease charge pump gain (50,150, 250, 1550 uA).
Charge Pump State	PLL1_CP_TRI	PLL1 Charge Pump State. Click to toggle between Active and Tri-State.

9.3 PLL2 Tab

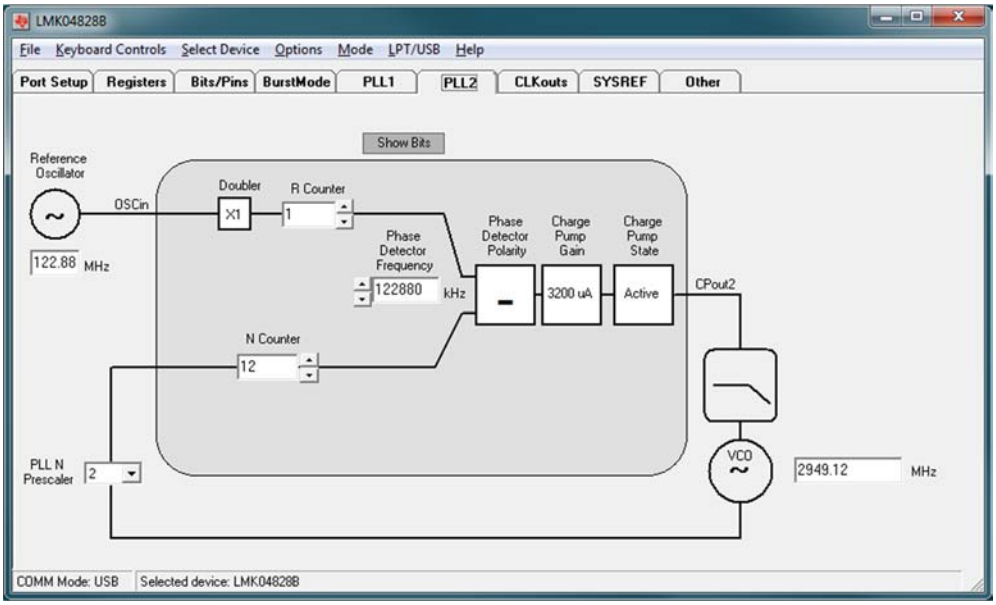

Figure 13. PLL2 Tab

The PLL2 tab allows the user to change the following parameters in Table 7.

Table 7. Registers Controls and Descriptions in PLL2 Tab(1)

Control Name	Register Name	Description
Reference Oscillator Frequency (MHz)	OSCin_FREQ	OSCin frequency from the External VCXO or Crystal.
Phase Detector Frequency (MHz)	n/a	PLL2 Phase Detector Frequency (PDF). This value is calculated as: PLL2 PDF = OSCin Frequency *(2EN_PLL2_REF_2X) / PLL2_R.
VCO Frequency (MHz)	n/a	Internal VCO Frequency should be within the allowable range of the LMK048xxB device. This value is calculated as: VCO Frequency = PLL2 PDF * (PLL2_N * PLL2_P * VCO divider value).
Doubler	EN_PLL2_REF_2X	PLL2 Doubler. 0 = Bypass Doubler 1 = Enable Doubler
R Counter	PLL2_R	PLL2 R Counter value (1 to 4095).
N Counter	PLL2_N	PLL2 N Counter value (1 to 262143).
PLL Prescaler	PLL2_P	PLL2 N Prescaler value (2 to 8).
Phase Detector Polarity	PLL2_CP_POL	PLL2 Phase Detector Polarity. Click on the polarity sign to toggle polarity “+” or “–”.
Charge Pump Gain	PLL2_CP_GAIN	PLL2 Charge Pump Gain. Left-click/right-click to increase/decrease charge pump gain (100, 400, 1600, 3200 uA).
Charge Pump State	PLL2_CP_TRI	PLL2 Charge Pump State. Click to toggle between Active and Tri-State.

(1) Changes made on this tab will be reflected in the **Clock Outputs** tab. The VCO Frequency should conform to the specified internal VCO frequency range.

9.4 Distribution Tab

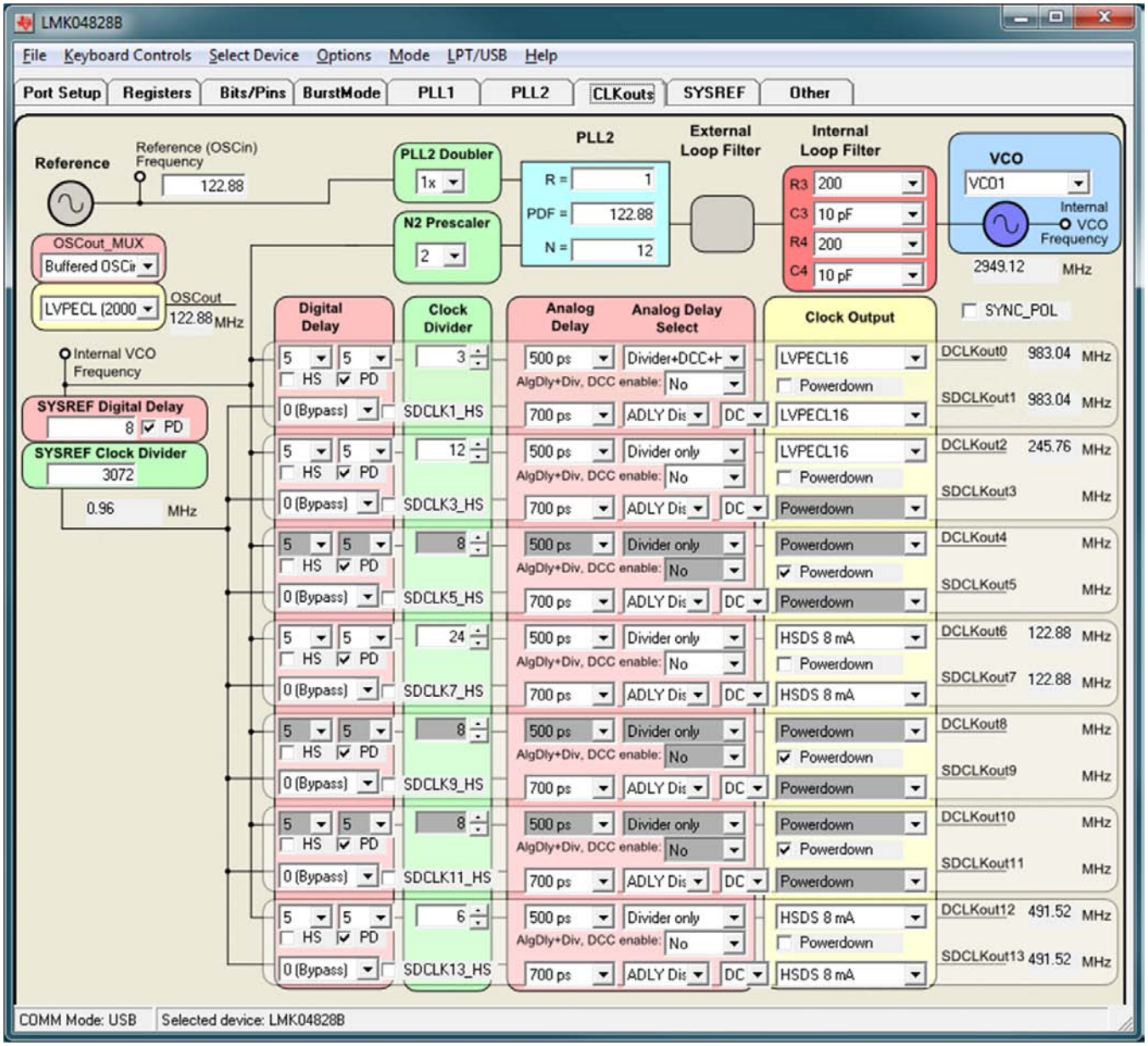

Figure 14. Distribution Tab

The **Distribution tab** allows the user to control the output channel blocks.

Note that the total PLL2 N divider value is the product of the VCO Divider value and the PLL N Prescaler and N Counter values (shown in the **PLL2** tab), and is given by:

PLL2 N Total = PLL2 N Prescaler * PLL2 N Counter (1)

Clicking on the cyan-colored PLL2 block that contains R, PDF and N values will bring the **PLL2** tab into focus where these values may be modified, if needed.

Clicking on the values in the box containing the Internal Loop Filter component (R3, C3, R4, C4) allow one to step through the possible values. Left click to increase the component value, and right click to decrease the value. These values can also be changed in the **Bits/Pins** tab.

9.5 SYSREF Tab

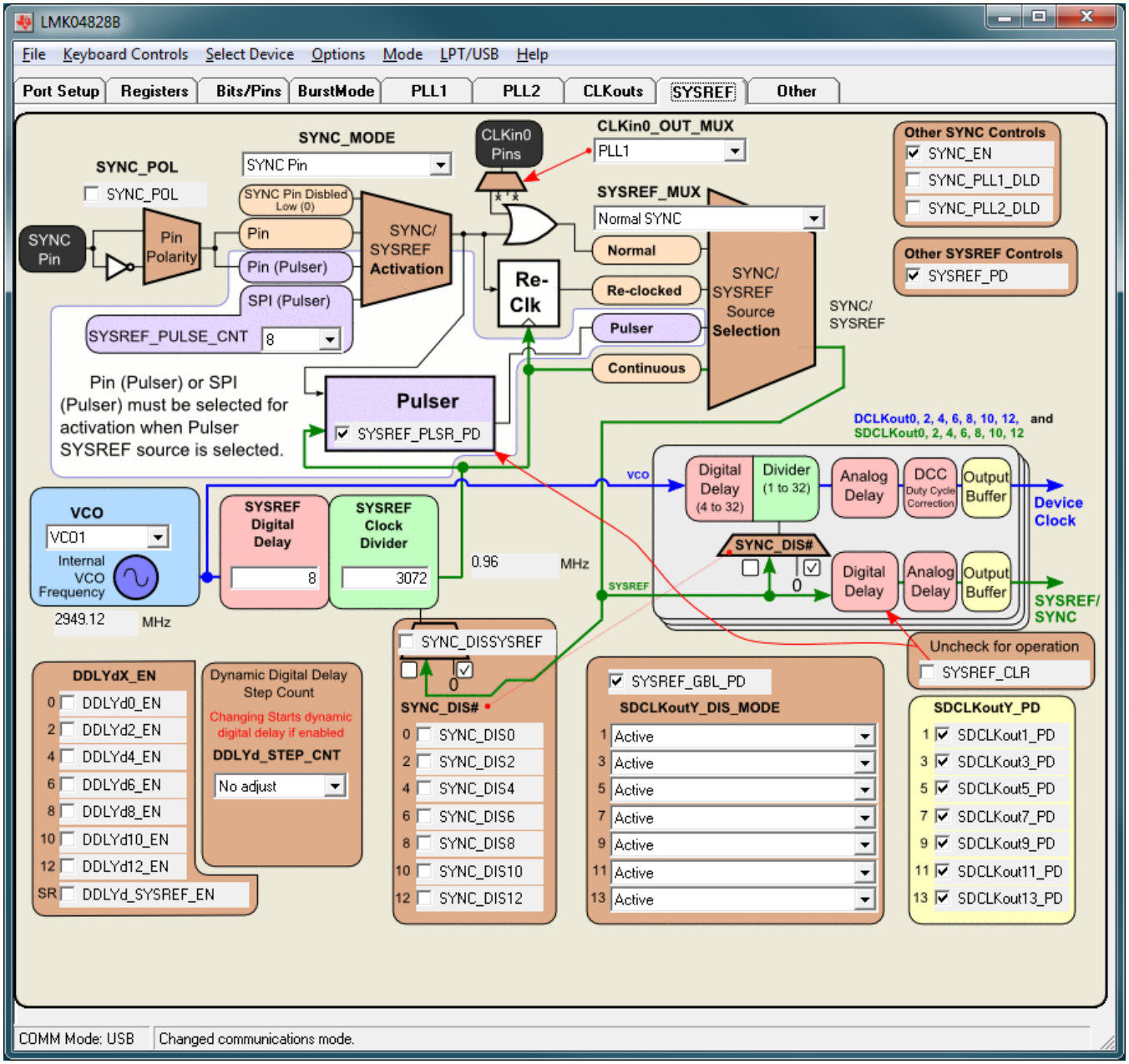

Figure 15. SYSREF Tab

The **SYSREF tab** show the controls for SYSREF functionality as well as Dynamic Digital Delay enable.

9.6 Bits/Pins Tab

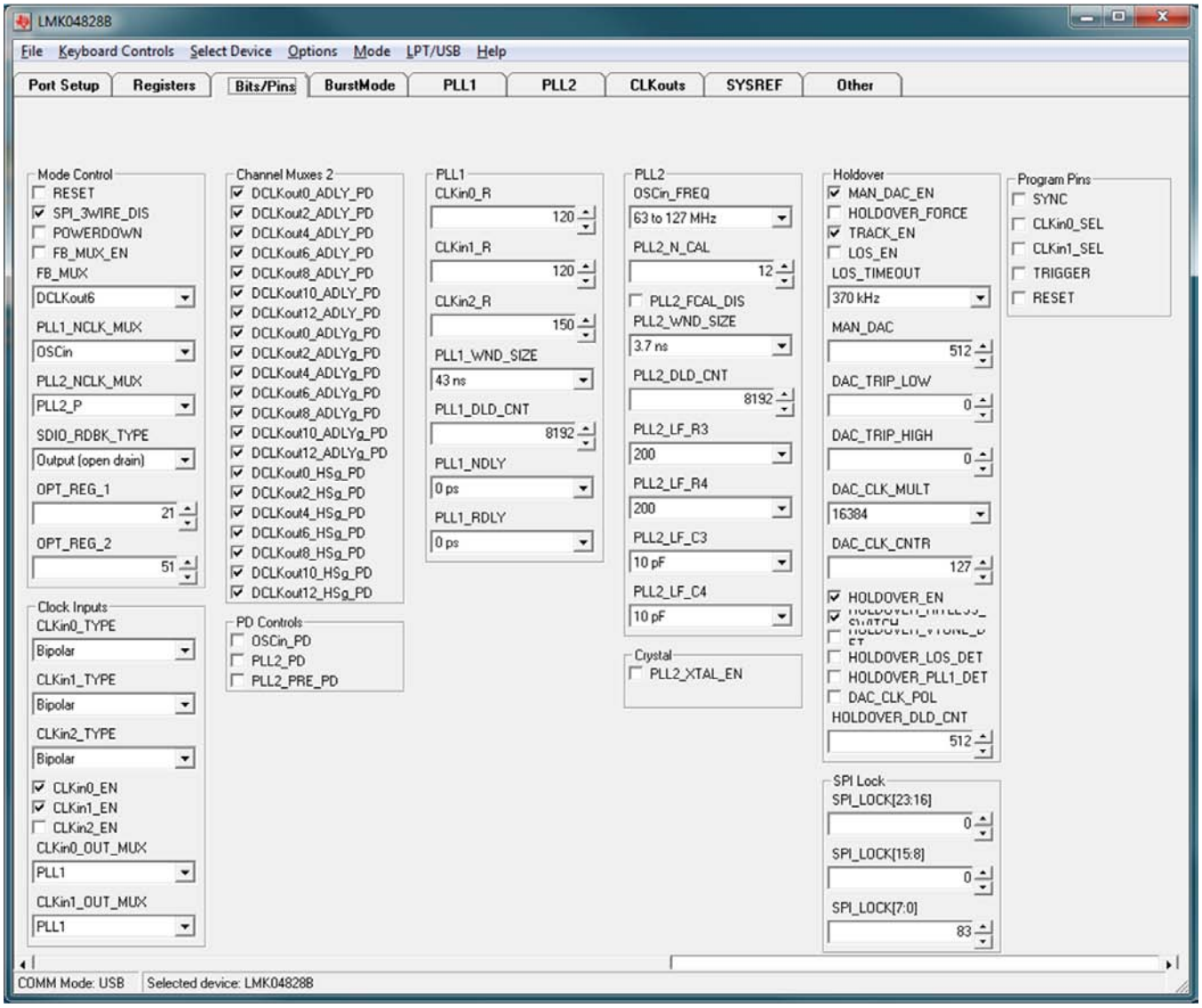

Figure 16. Bits/Pins Tab

The **Bits/Pins** tab allows the user to program bits not available on other tabs.

NOTE: Right-clicking any register name in the **Bits/Pins** tab will display a Help prompt with the register address, data bit location/length, and a brief register description.

10 Appendix B: Typical Phase Noise Performance Plots

The LMK0482x's dual PLL architecture achieves ultra low jitter and phase noise by allowing the external VCXO or Crystal's phase noise to dominate the final output phase noise at low offset frequencies and the internal VCO's phase noise to dominate the final output phase noise at high offset frequencies. This results in the best overall noise and jitter performance.

Table 8 lists the test conditions used for output clock phase noise measurements with the Crystek 122.88 MHz VCXO.

Table 8. LMK0482x Test Conditions

Parameter	Value
PLL1 Reference clock input	CLKin1* single-ended input, CLKin1 AC-coupled to GND
PLL1 Reference Clock frequency	122.88 MHz
PLL1 Phase detector frequency	1024 kHz
PLL1 Charge Pump Gain	450 uA
VCXO frequency	122.88 MHz
PLL2 phase detector frequency	122.88 MHz
PLL2 Charge Pump Gain	3200 uA
PLL2 REF2X mode	Enabled

10.1 122.88 MHz VCXO Phase Noise

The phase noise of the reference is masked by the phase noise of this VCXO by using a narrow loop bandwidth for PLL1 while retaining the frequency accuracy of the reference clock input. This VCXO sets the reference noise to PLL2. Figure 17 shows the open loop typical phase noise performance of the CVHD-950-122.88 Crystek VCXO.

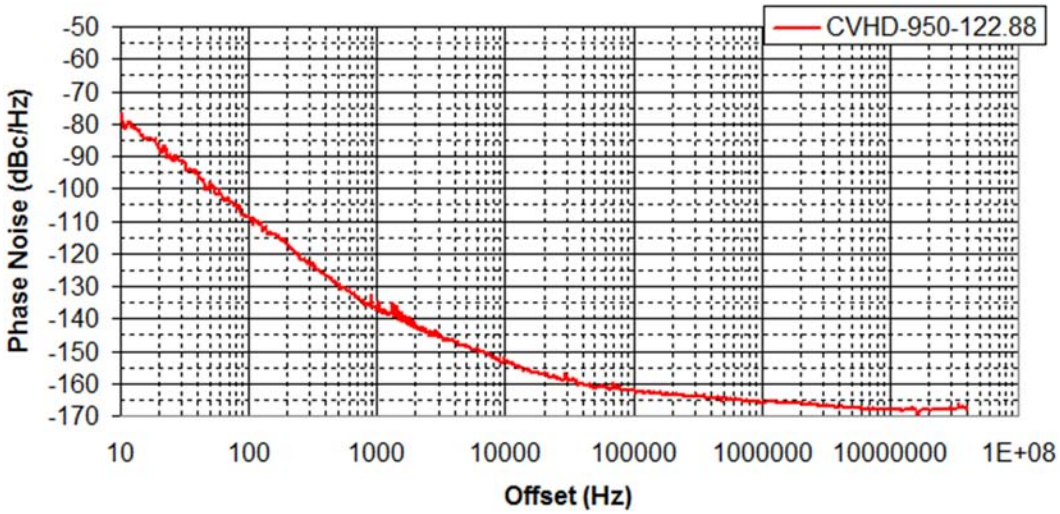

Figure 17. Crystek CVHD-950-122.88 MHz VCXO Phase Noise at 122.88 MHz

Table 9. VCXO Phase Noise and Jitter

Offset	VCXO Phase Noise at 122.88 MHz (dBc/Hz)	VCXO RMS Jitter to high offset of 20 MHz at 122.88 MHz (rms fs)
10 Hz	-76.6	60.5
100 Hz	-108.9	36.2
1 kHz	-137.4	35
10 kHz	-153.3	34.5
100 kHz	-162	32.9
1 MHz	-165.7	22.7
10 MHz	-168.1	515.4
40 MHz	-168.1	60.5

10.2 Output Measurement Technique

The same technique was used to measure phase noise for all three output types available on the programmable OSCout and CLKout buffers. This was achieved by terminating one side of the LVPECL, LVDS, or LVCMOS output with a 50-ohm load, and measuring the other side single-ended using an Agilent E5052B Source Signal Analyzer.

10.3 Clock Outputs (DCLKout and SDCLKout)

The LMK0482x features programmable HSDS, LVDS, LVPECL buffer modes for the DCLKoutX, SDCLKout pairs. Below is a phase noise measurement of DCLKout2 (best phase noise clock output) using both a balun and single ended.

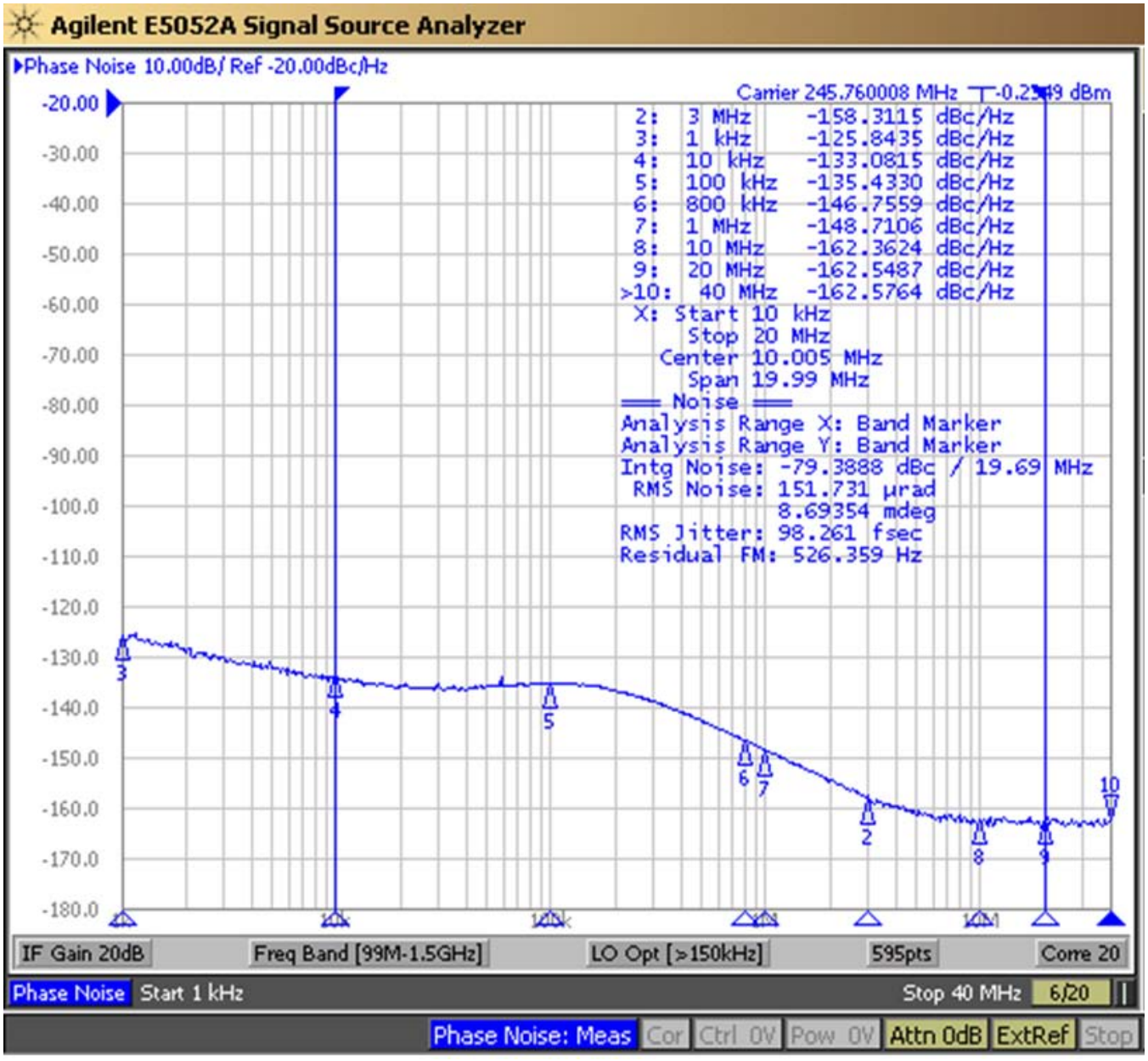

Figure 18. LMK04826 DCLKout2, VCO0, 245.76 MHz, Div8, LVPECL20 /w 240 ohm emitter resistor, DCLKoutX_MUX=Divider, IDL=1, ODL=0, Balun = Prodyn BIB-100G

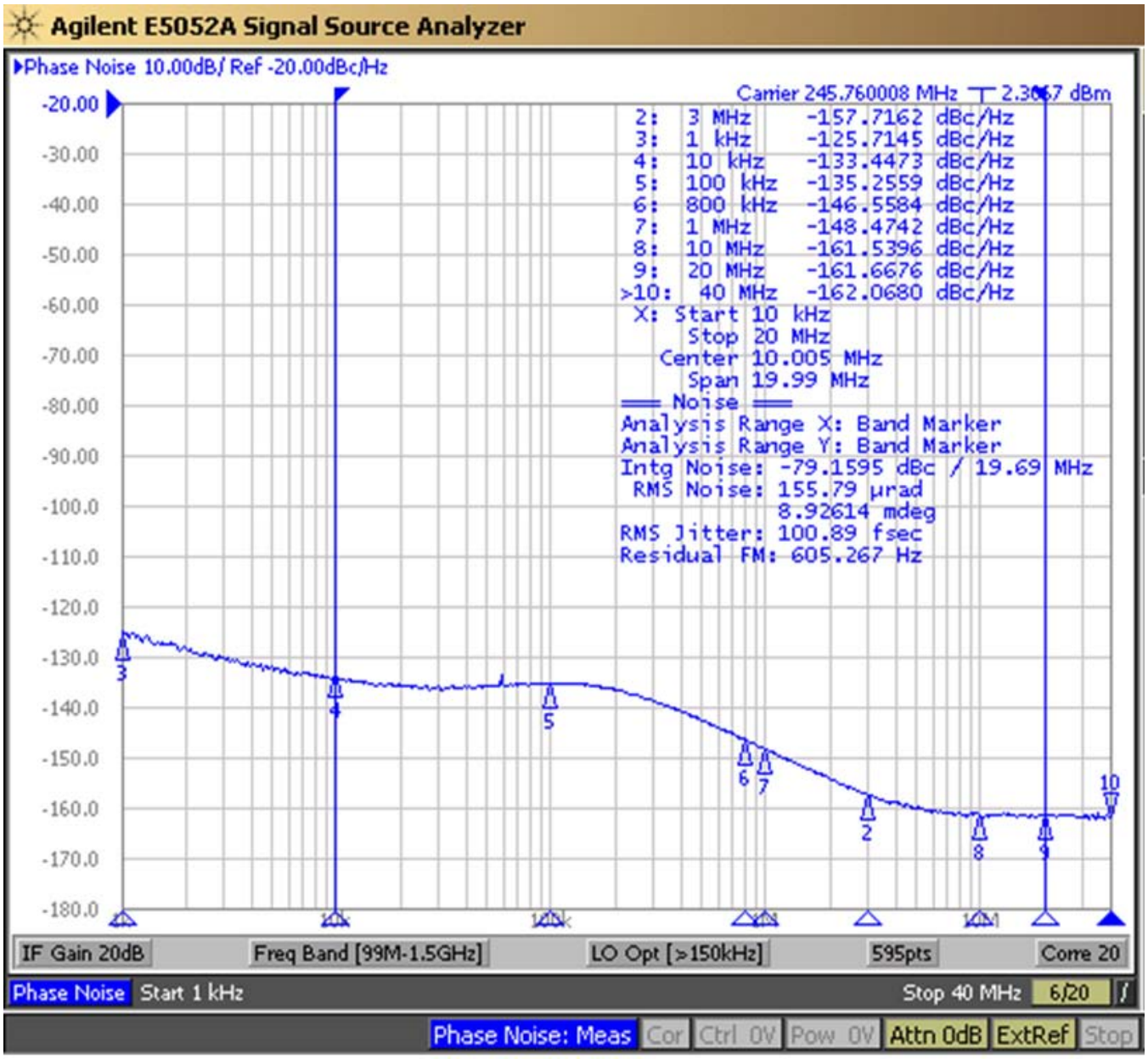

Figure 19. LMK04826 DCLKout2, VCO0, 245.76 MHz, Div8, LVPECL20 /w 240 ohm emitter resistor, DCLKoutX_MUX=Divider, IDL=1, ODL=0, Single Ended

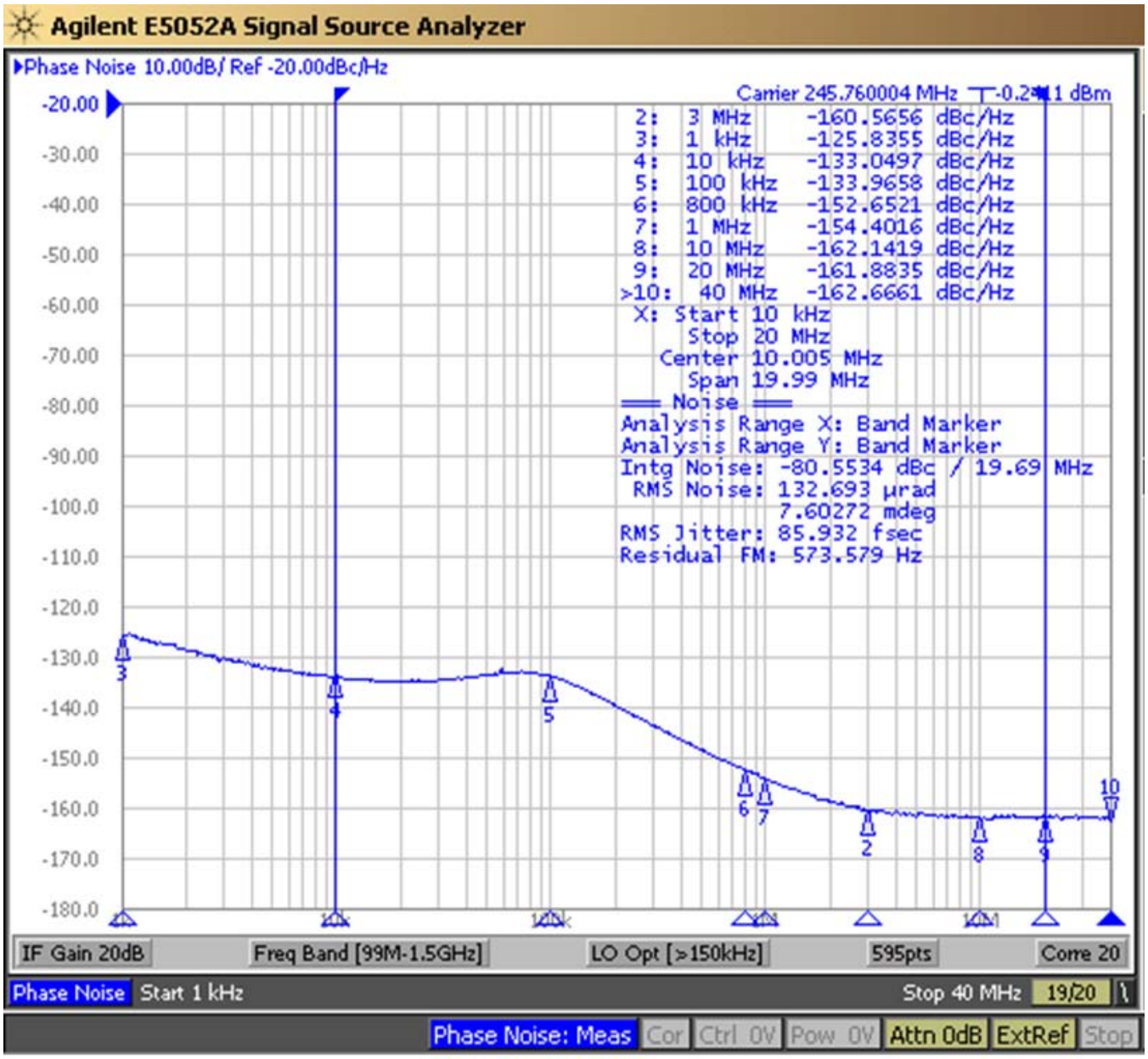

Figure 20. LMK04826 DCLKout2, VCO1, 245.76 MHz, Div10, LVPECL20 /w 240 ohm emitter resistor, DCLKoutX_MUX=Divider, IDL=1, ODL=0, Balun = Prodyn BIB-100G

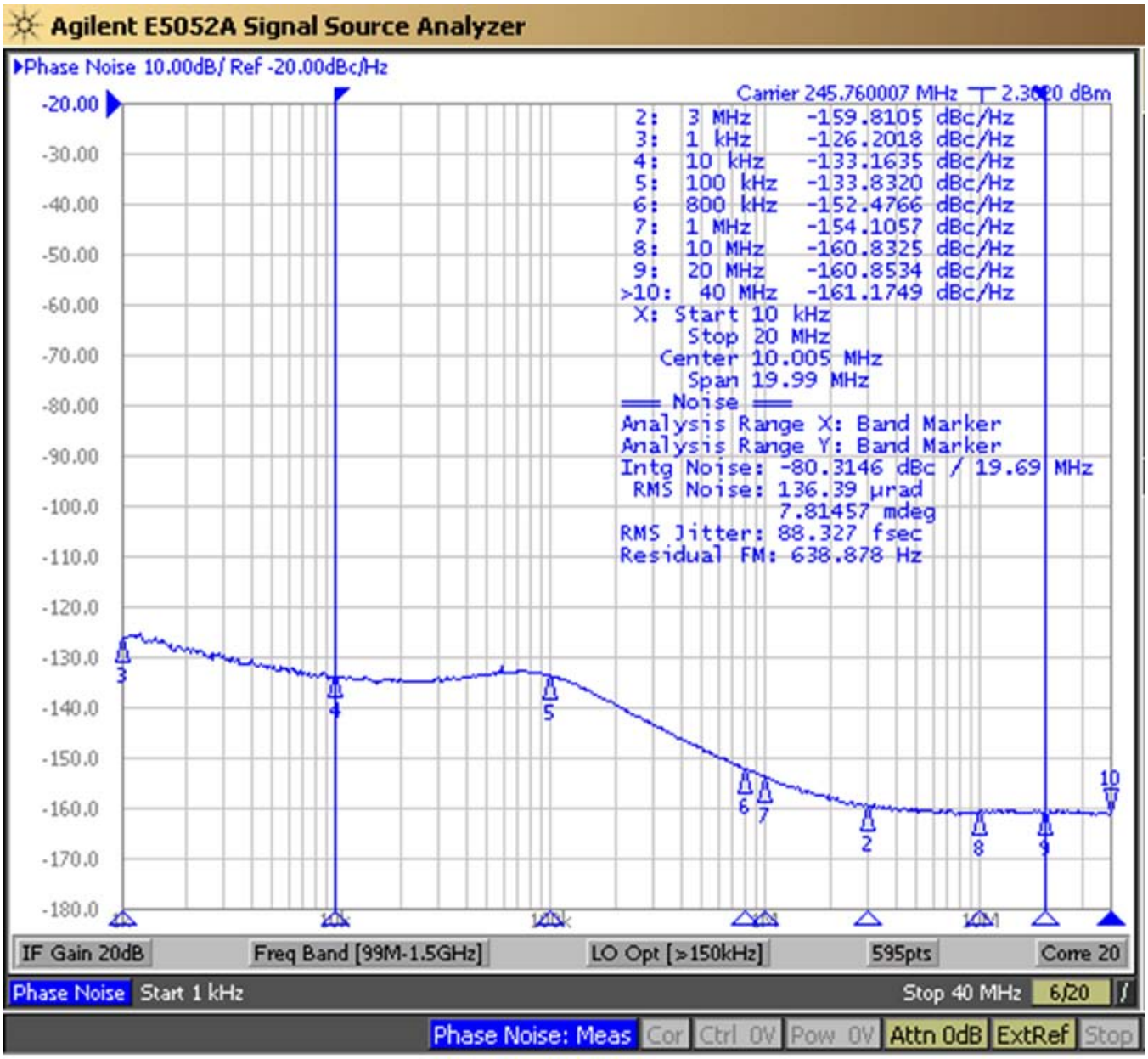

Figure 21. LMK04826 DCLKout2, VCO1, 245.76 MHz, Div10 , LVPECL20 /w 240 ohm emitter resistor, DCLKoutX_MUX=Divider, IDL=1, ODL=0, Single Ended

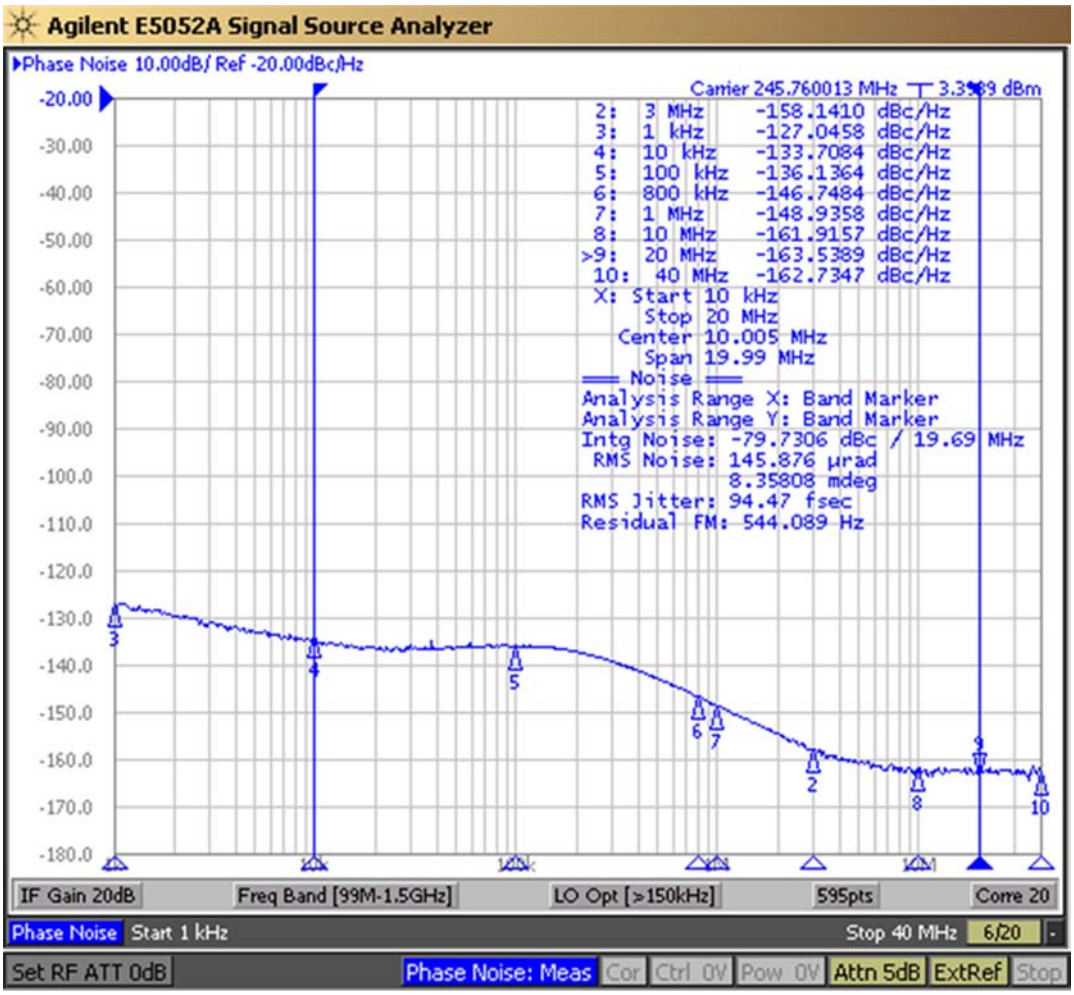

Figure 22. LMK04828 DCLKout2, VCO0, 245.76 MHz, Div10, LVPECL20 /w 240 ohm emitter resistor, DCLKoutX_MUX=Divider, IDL=1, ODL=0, Balun = ADT2-1T

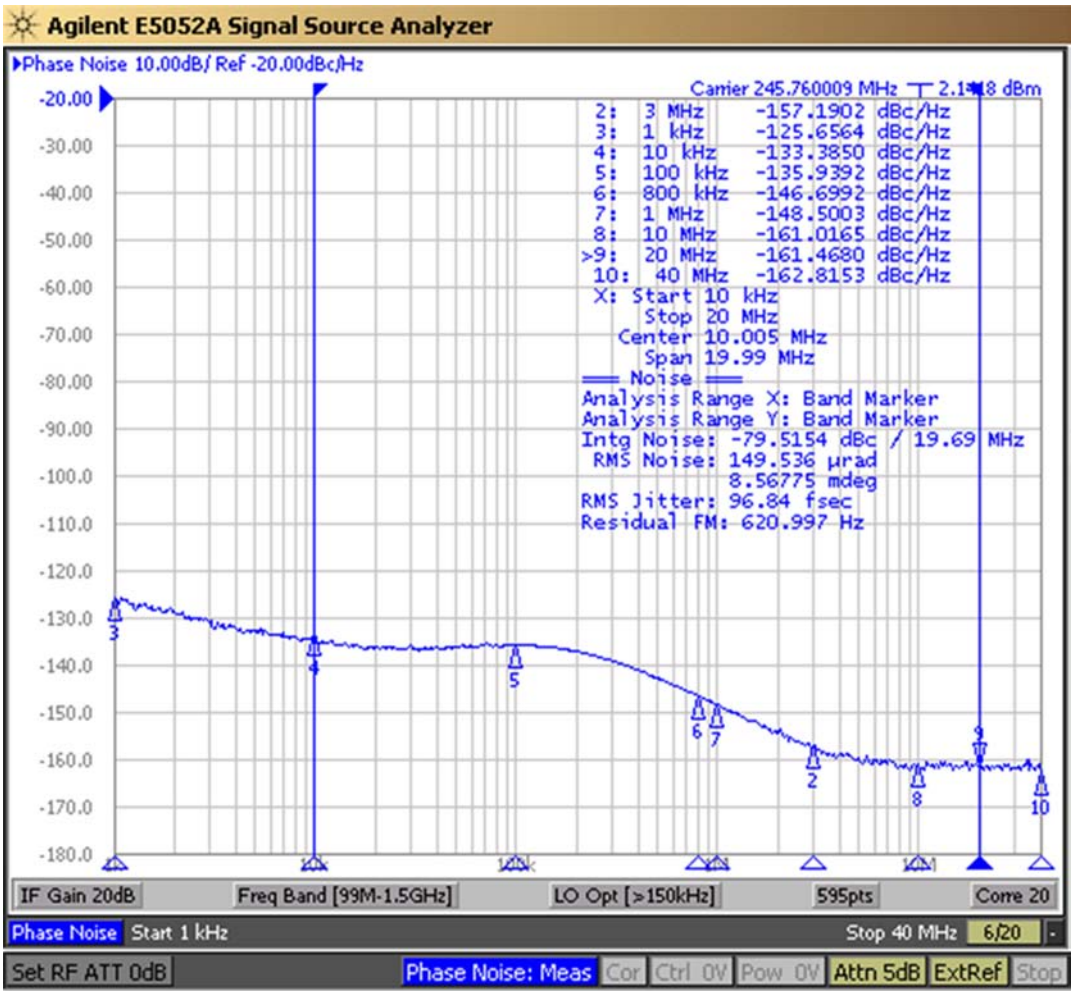

Figure 23. LMK04828 DCLKout2, VCO0, 245.76 MHz, Div10, LVPECL20 /w 240 ohm emitter resistor, DCLKoutX_MUX=Divider, IDL=1, ODL=0, Single Ended

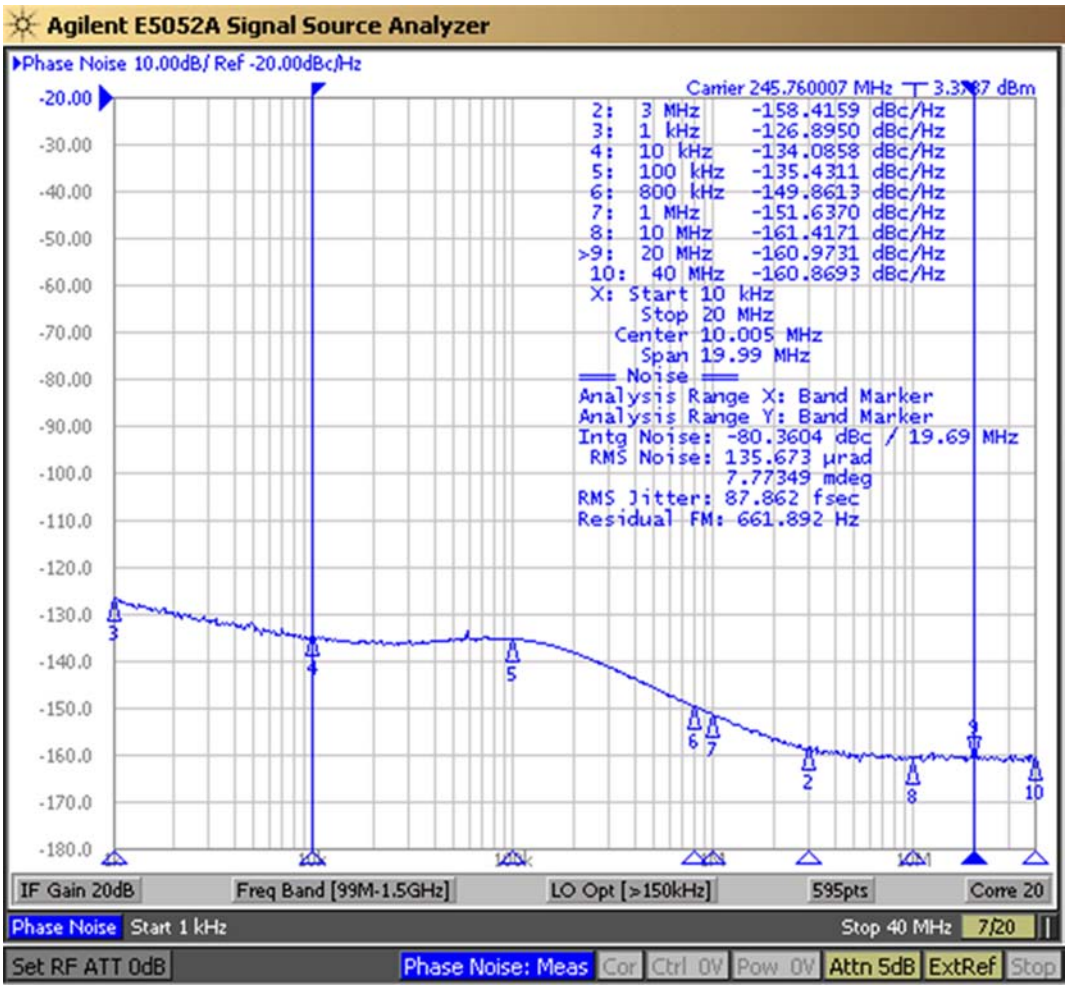

Figure 24. LMK04828 DCLKout2, VCO1, 245.76 MHz, Div12, LVPECL20 /w 240 ohm emitter resistor, DCLKoutX_MUX=Divider, IDL=1, ODL=0, Balun = ADT2-1T

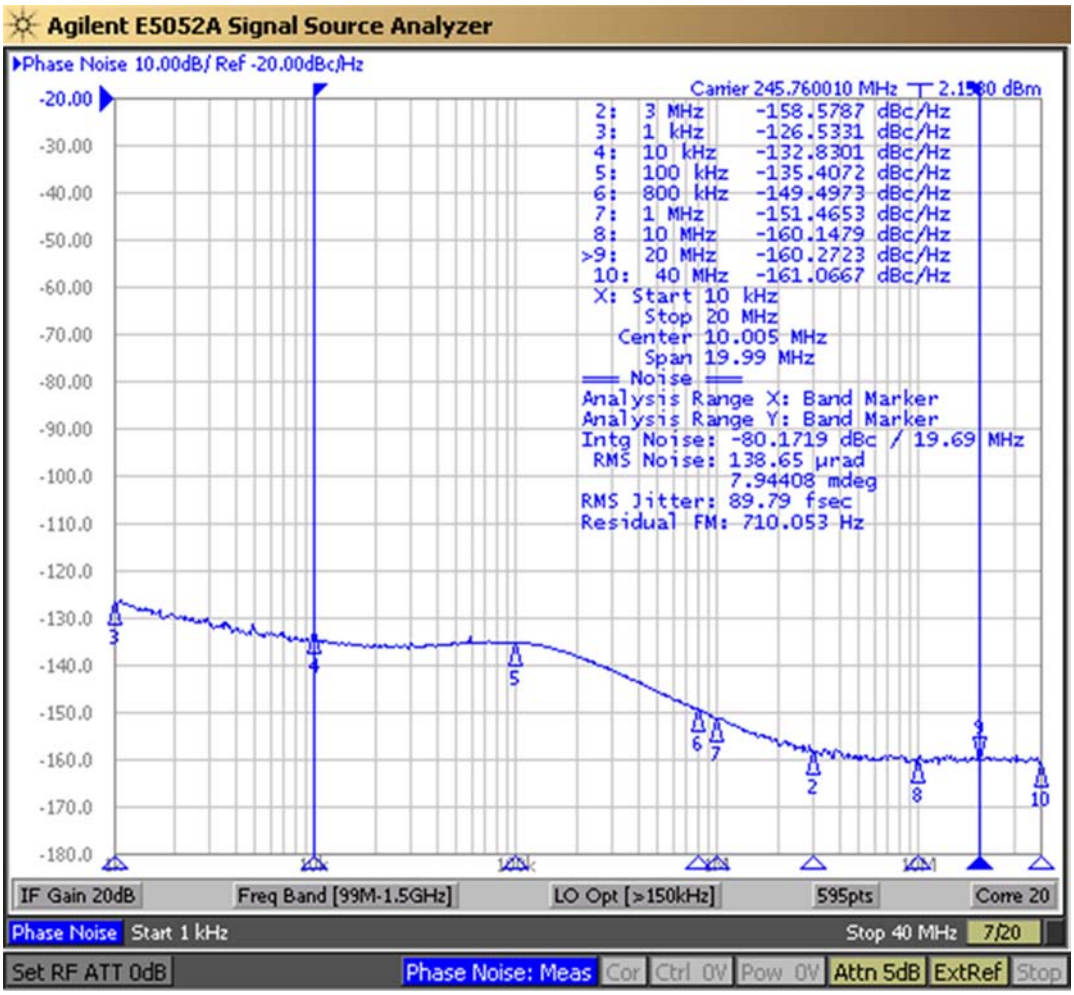

Figure 25. LMK04828 DCLKout2, VCO1, 245.76 MHz, Div12, LVPECL20 /w 240 ohm emitter resistor, DCLKoutX_MUX=Divider, IDL=1, ODL=0, Single Ended

11 Appendix C: Schematics

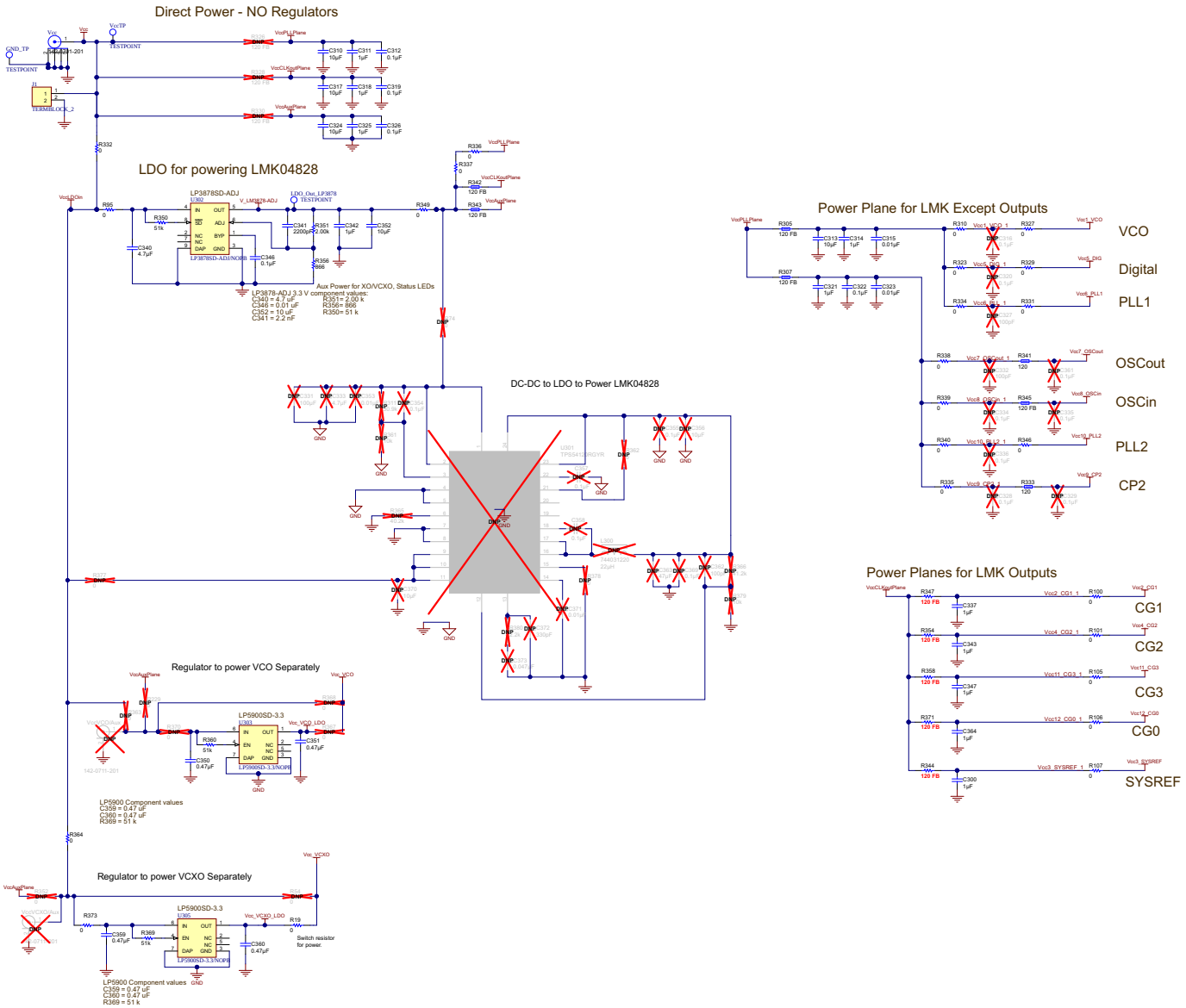

Figure 26. Power Supply

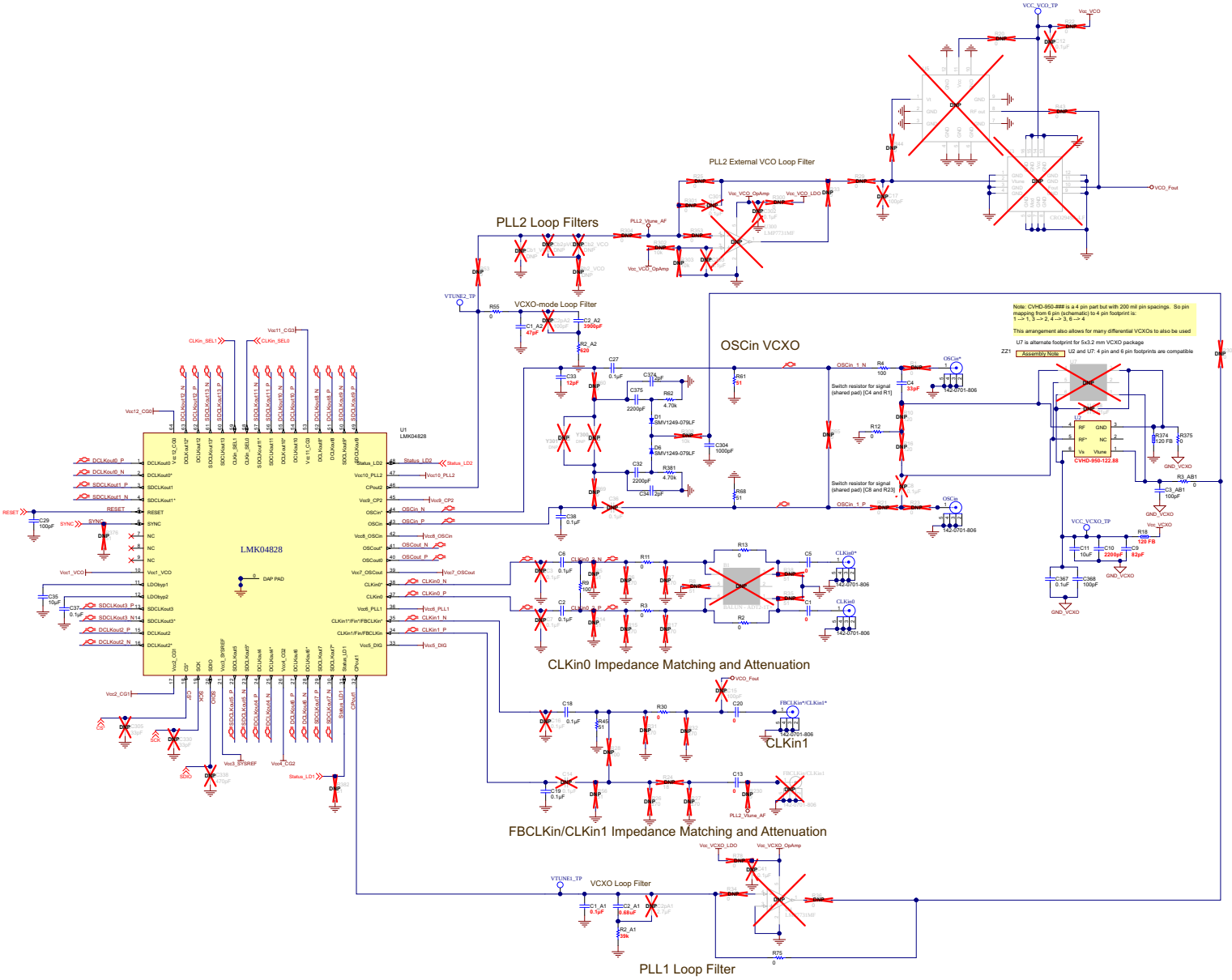

Figure 27. LMK04828B

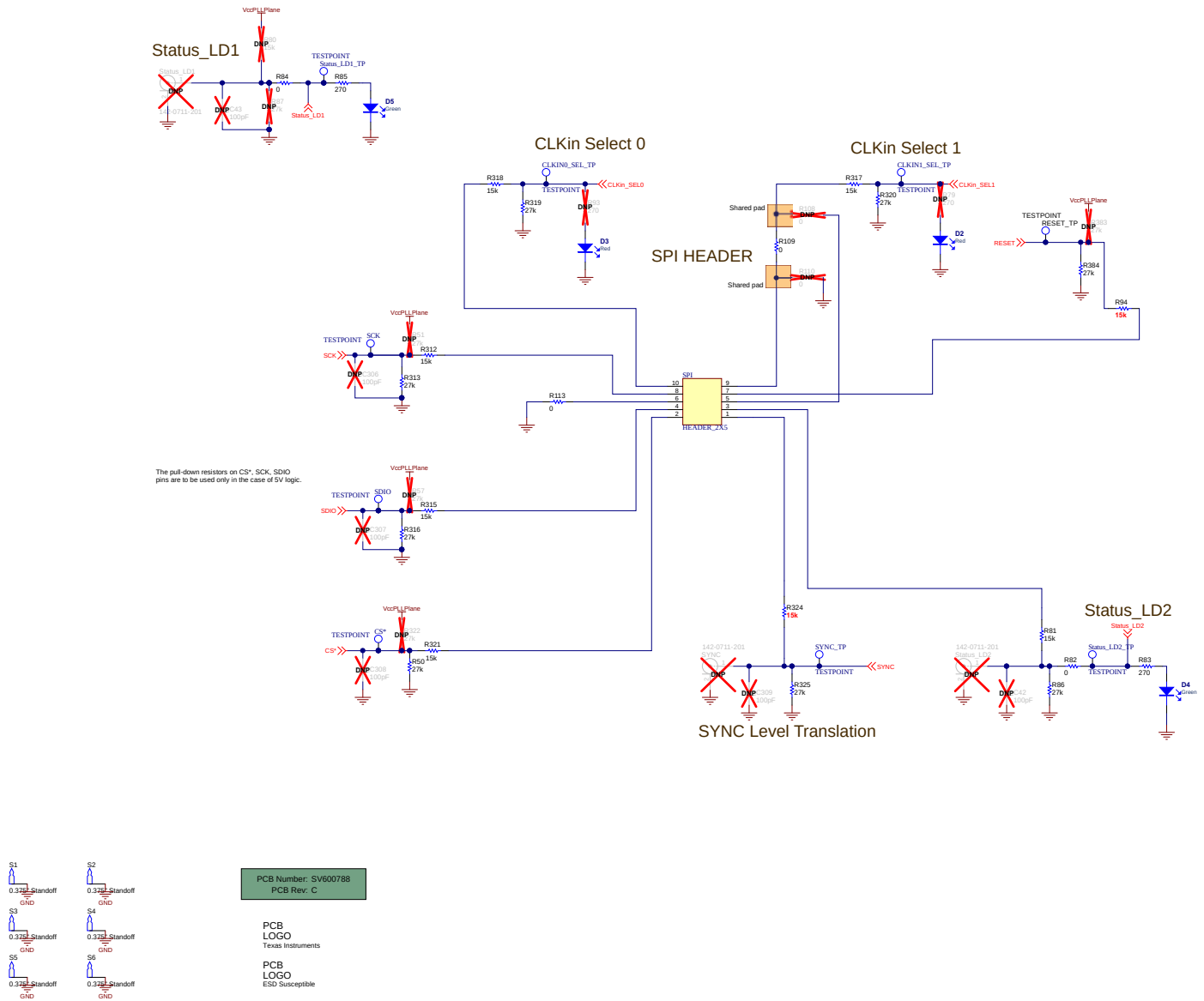

Figure 28. Digital

SYSREF CLOCK OUTPUTS

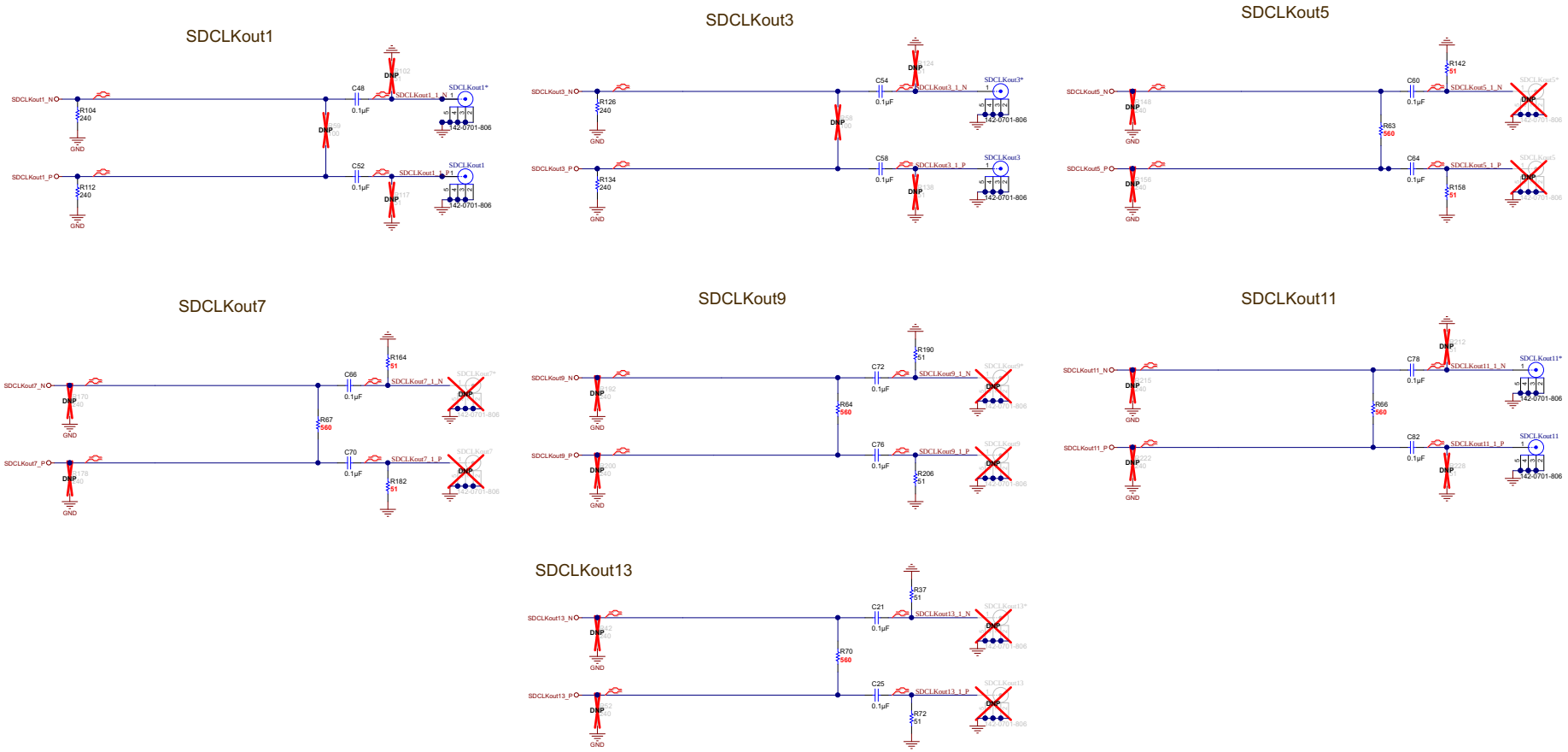

Figure 29. Clock Outputs 1 of 2

DEVICE CLOCK OUTPUTS AND OSCout

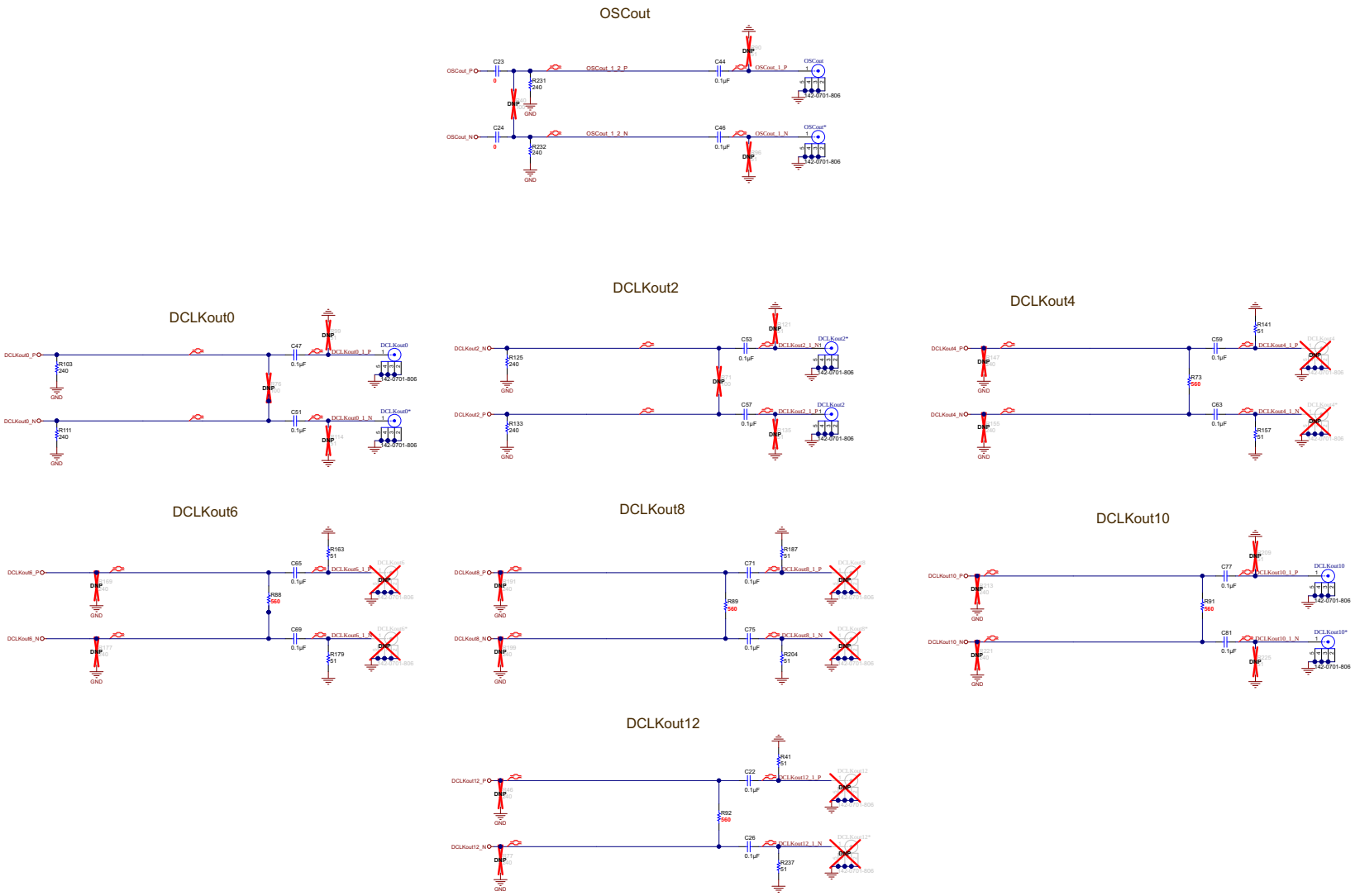

Figure 30. Clock Outputs 2 of 2

12 Appendix D: Bill of Materials

Table 10. Bill of Materials

Item	Designator	Description	Manufacturer	PartNumber	Quantity
1	PCB	Printed Circuit Board	Any	SV600788C	1
2	C1, C5, C13, C20, C23, C24, R3, R3_AB1, R11, R12, R19, R30, R55, R75, R82, R84, R95, R109, R113, R310, R323, R327, R329, R331, R334, R335, R336, R337, R338, R339, R340, R346, R349, R364, R373, R375	RES, 0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06030000Z0EA	36
3	C1_A1, C2, C6, C18, C19, C21, C22, C25, C26, C27, C38, C37, C44, C46, C47, C48, C51, C52, C53, C54, C57, C58, C59, C60, C63, C64, C65, C66, C70, C71, C72, C75, C76, C77, C78, C81, C82, C312, C319, C346	CAP, CERM, 0.1uF, 25V, +/-5%, X7R, 0603	Kemet	C0603C104J3RACTU	40
4	C1_A2	CAP, CERM, 47pF, 50V, +/-5%, C0G/NP0, 0603	Kemet	C0603C470J5GACTU	1
5	C2_A1	CAP, CERM, 0.68uF, 10V, +/-10%, X5R, 0603	Kemet	C0603C684K8PACTU	1
6	C2_A2	CAP, CERM, 3900pF, 50V, +/-10%, X7R, 0603	MuRata	GRM188R71H392KA01D	1
7	C3_AB1, C29, C368	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603	Kemet	C0603C101J5GACTU	3
8	C4	CAP, CERM, 33pF, 100V, +/-5%, C0G/NP0, 0603	AVX	06031A330JAT2A	1
9	C9	CAP, CERM, 82pF, 50V, +/-10%, C0G/NP0, 0603	Kemet	C0603C820K5GACTU	1
10	C10, C32, C341, C375	CAP, CERM, 2200pF, 50V, +/-10%, X7R, 0603	Kemet	C0603C222K5RACTU	4
11	C11	CAP, CERM, 10uF, 10V, +/-20%, X5R, 0805	Kemet	C0805C106M8PACTU	1
12	C33	CAP, CERM, 12pF, 50V, +/-5%, C0G/NP0, 0603	AVX	06035A120JAT2A	1
13	C34, C374	CAP, CERM, 2pF, 50V, +/-12.5%, C0G/NP0, 0603	Kemet	C0603C209C5GACTU	2
14	C35, C310, C317, C324, C352	CAP, CERM, 10uF, 10V, +/-10%, X5R, 0805	Kemet	C0805C106K8PACTU	5

Table 10. Bill of Materials (continued)

Item	Designator	Description	Manufacturer	PartNumber	Quantity
15	C69, C322, C326, C367	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603	Kemet	C0603C104K3RACTU	4
16	C300, C311, C314, C318, C321, C325, C337, C342, C343, C347, C364	CAP, CERM, 1uF, 10V, +/-10%, X5R, 0603	Kemet	C0603C105K8PACTU	11
17	C304	CAP, CERM, 1000pF, 50V, +/-5%, C0G/NP0, 0603	Kemet	C0603C102J5GACTU	1
18	C313	CAP, CERM, 10uF, 6.3V, +/-20%, X5R, 0603	Kemet	C0603C106M9PACTU	1
19	C315, C323	CAP, CERM, 0.01uF, 100V, +/-10%, X7R, 0603	Kemet	C0603C103K1RACTU	2
20	C340	CAP, CERM, 4.7uF, 10V, +/-10%, X5R, 0603	Kemet	C0603C475K8PACTU	1
21	C350, C351, C359, C360	CAP, CERM, 0.47uF, 16V, +/-10%, X7R, 0603	Kemet	C0603C474K4RACTU	4
22	CLKin0, CLKin0*, DCLKout0, DCLKout0*, DCLKout2, DCLKout2*, DCLKout10, DCLKout10*, FBCLKin*/CLKin1*, OSCin, OSCin*, OSCout, OSCout*, SDCLKout1, SDCLKout1*, SDCLKout3, SDCLKout3*, SDCLKout11, SDCLKout11*	Connector, SMT, End launch SMA 50 ohm	Emerson Network Power	142-0701-806	23
23	D1, D6	DIODE VARACTOR 15V 20MA SC-79	Skyworks Inc	SMV1249-079LF	2
24	D2, D3	LED 2.8X3.2MM 565NM RED CLR SMD	Lumex Opto/Components Inc.	SML-LX2832IC	2
25	D4, D5	LED 2.8X3.2MM 565NM GRN CLR SMD	Lumex Opto/Components Inc.	SML-LX2832GC	2
26	J1	CONN TERM BLK PCB 5.08MM 2POS OR	Weidmuller	1594540000	1
27	R2, R13, R332	RES, 0 ohm, 5%, 0.125W, 0805	Vishay-Dale	CRCW08050000Z0EA	3
28	R2_A1	RES, 39k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060339K0JNEA	1
29	R2_A2	RES, 620 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603620RJNEA	1
30	R4, R9	RES, 100 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603100RJNEA	2
31	R18, R305, R307, R342, R343, R344, R345, R347, R354, R358, R371, R374	FB, 120 ohm, 500 mA, 0603	Murata	BLM18AG121SN1D	12

Table 10. Bill of Materials (continued)

Item	Designator	Description	Manufacturer	PartNumber	Quantity
32	R37, R41, R45, R61, R68, R72, R141, R142, R157, R158, R163, R164, R179, R182, R237	RES, 51 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060351R0JNEA	15
33	R50, R86, R313, R316, R319, R320, R325, R384	RES, 27k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060327K0JNEA	8
34	R62, R381	RES, 4.70k ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-074K7L	2
35	R63, R64, R66, R67, R70, R73, R88, R89, R91, R92	RES, 560 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603560RJNEA	10
36	R81, R94, R312, R315, R317, R318, R321, R324	RES, 15k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060315K0JNEA	8
37	R83, R85	RES, 270 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603270RJNEA	2
38	R100, R101, R105, R106, R107	RES, 0 ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW04020000Z0ED	5
39	R103, R104, R111, R112, R125, R126, R133, R134, R231, R232	RES, 240 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603240RJNEA	10
40	R333, R341	FB, 120 ohm, 500 mA, 0402	TDK	MMZ1005Y121C	2
41	R350, R360, R369	RES, 51k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060351K0JNEA	3
42	R351	RES, 2.00k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06032K00FKEA	1
43	R356	RES, 866 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603866RFKEA	1
44	S1, S2, S3, S4, S5, S6	0.375" Standoff	VOLTREX	SPCS-6	6
45	SPI	Low Profile Vertical Header 2x5 0.100"	FCI	52601-G10-8LF	1
46	U1	LMK04826	Texas Instruments	LMK04826BISQ	1
		LMK04828		LMK04828BISQ	
47	U2	122.88 MHz VCXO	Crystek	CVHD-950-122.88	1
48	U302	Micropower 800mA Low Noise "Ceramic Stable" Adjustable Voltage Regulator for 1V to 5V Applications, 8-pin LLP, Pb-Free	Texas Instruments	LP3878SD-ADJ/NOPB	1
49	U303, U305	Ultra Low Noise, 150mA Linear Regulator for RF/Analog Circuits Requires No Bypass Capacitor, 6-pin LLP, Pb-Free	Texas Instruments	LP5900SD-3.3/NOPB	2
50	Vcc	Connector, TH, SMA	Emerson Network Power	142-0701-201	1

13 Appendix E: Properly Configuring LPT Port

When trying to solve any communications issue, it is most convenient to verify communication by programming the POWERDOWN bit to confirm normal or low supply current consumption of the evaluation board.

13.1 LPT Driver Loading

The parallel port must be configured for proper operation. To confirm that the LPT port driver is successfully loading click “LPT/USB” → “Check LPT.” If the driver properly loads then the following message is displayed in Figure 31:

Figure 31. Successfully Opened LPT Driver

Successful loading of LPT driver does not mean LPT communications in CodeLoader are setup properly. The proper LPT port must be selected and the LPT port must not be in an improper mode.

NOTE: The PC must be re-booted after install for LPT support to work properly.

13.2 Correct LPT Port/Address

To determine the correct LPT port in Windows, open the device manager (On Windows XP, Start → Settings → Control Panel → System → Hardware tab → Device Manager) and check the LPT port under the Ports (COM & LPT) node of the tree. It can be helpful to confirm that the LPT port is mapped to the expected port address, for instance to confirm that LPT1 is really mapped to address 0x378. This can be checked by viewing the Properties of the LPT1 port and viewing Resources tab to verify that the I/O Range starts at 0x378. CodeLoader expects the traditional port mapping, shown in Table 11:

Table 11. LPT Port Addresses

Port	Address
LPT1	0x378
LPT2	0x278
LPT3	0x3BC

If a non-standard address is used, use the “Other” port address in CodeLoader and type in the port address in hexadecimal. It is possible to change the port address in the computer’s BIOS settings. The port address can be set in CodeLoader in the Port Setup tab as shown in Figure 31.

Figure 32. Selecting the LPT Port Address

13.3 Correct LPT Mode

If communications are not working, then it is possible the LPT port mode is set improperly. It is recommended to use the simple, Output-only mode of the LPT port. This can be set in the BIOS of the computer. Common terms for this desired parallel port mode are “Normal,” “Output,” or “AT.” It is possible to enter BIOS setup during the initial boot up sequence of the computer.

14 Appendix F: USB2UWIRE-IFACE under Windows 7

USB2ANY provides native support for Windows 7. In order to operate in Windows 7 using the USB2UWIRE-IFACE , reference the following instrucions to use a Windows XP Virtual Machine.

14.1 (One-time step) Download and install Microsoft Windows XP mode for Windows 7

Download and install Microsoft’s Windows XP Mode for the Windows 7 operating system by following this link: http://www.microsoft.com/windows/virtual-pc/download.aspx

Follow all of the installation steps listed on Microsoft’s website, as shown below.

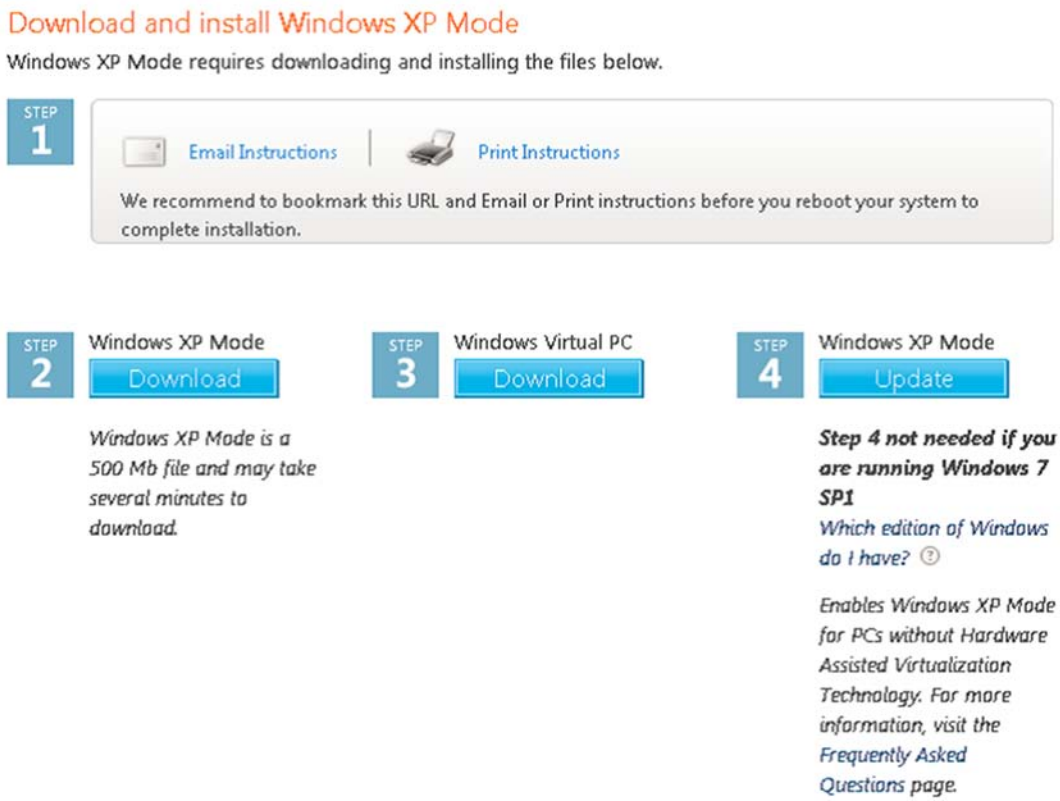

Figure 33. Installation Steps for Microsoft Windows XP Mode for Windows 7

14.2 Launch Microsoft XP Mode

Launch Microsoft XP Mode by clicking on Start > All Programs > Windows Virtual PC > Windows XP Mode, as shown below.

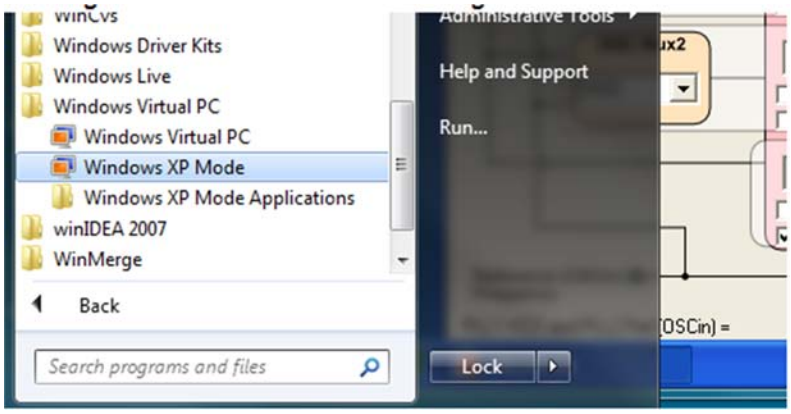

Figure 34. Launch Microsoft XP Mode

14.3 (One-time step) Install the ALP software from within Windows XP

Once Windows XP is running, install the CodeLoader software by running the executable file.

14.4 Attach the USB device to your computer

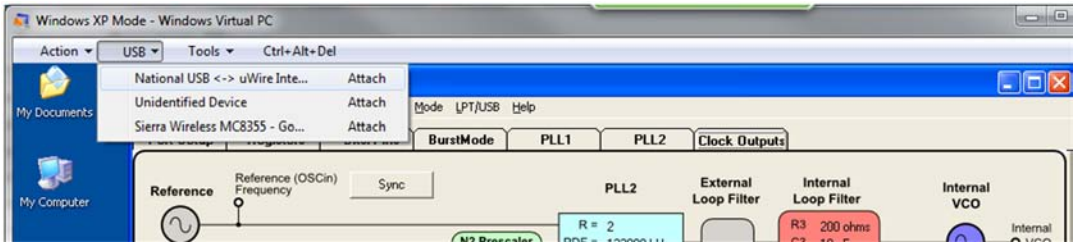

Figure 35. Attach USB

EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used. TI currently deals with a variety of customers for products, and therefore our arrangement with the user is not exclusive. TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.

REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of EVMs for RF Products in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

Texas Instruments Japan Limited
(address) 24-1, Nishi-Shinjuku 6 chome, Shinjuku-ku, Tokyo, Japan

http://www.tij.co.jp

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】

本開発キットは技術基準適合証明を受けておりません。

本製品のご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。

日本テキサス・インスツルメンツ株式会社
東京都新宿区西新宿６丁目２４番１号
西新宿三井ビル
http://www.tij.co.jp

EVALUATION BOARD/KIT/MODULE (EVM)
WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. Since the EVM is not a completed product, it may not meet all applicable regulatory and safety compliance standards (such as UL, CSA, VDE, CE, RoHS and WEEE) which may normally be associated with similar items. You assume full responsibility to determine and/or assure compliance with any such standards and related certifications as may be applicable. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM’s electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI’s recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265