SERDES Demonstration Kit User Manual

Rev 0.2

NSID: SERDESUR-43USB

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Introduction:

National Semiconductor's SERDES evaluation kit contains one (1) DS90UR241 Serializer (Tx) board, one (1) DS90UR124 De-serializer (Rx) board, and one (1) generic two (2) meter USB 2.0 Hi-SPEED cable assembly. National is not recommending using the USB 2.0 Hi-SPEED cable assembly but is provided in this kit as a generic solution to show the robustness of the chipset.
Note: the demo boards are not for EMI testing. The demo boards were designed for easy accessibility to device pins with tap points for monitoring or applying signals, additional pads for termination, and multiple connector options.

The DS90UR241/124 chipset supports a variety of display applications. The single LVDS interface is well-suited for any display system interface. Typical applications include: navigation displays, automated teller machines (ATMs), POS, video cameras, global positioning systems (GPS), portable equipment/instruments, factory automation, etc.

The DS90UR241 and DS90UR124 can be used as a 24-bit general purpose LVDS Serializer and De-serializer chipset designed to transmit data at clocks speeds ranging from 5 to 43 MHz.

The DS90UR241 serializer board accepts LVCMOS input signals. The LVDS Serializer converts the LVCMOS parallel lines into a single serialized LVDS data pair with an embedded LVDS clock. The serial data stream toggles at 28 times the base clock rate. With an input clock at 43 MHz, the transmission rate for the LVDS line is 1.204Gbps.

The DS90UR124 de-serializer board accepts the LVDS serialized data stream with embedded clock and converts the data back into parallel LVCMOS signals and clock. Note that NO reference clock is needed to prevent harmonic lock as with other devices currently on the market.

Suggested equipment to evaluate the chipset, an LVCMOS signal source such as a video generator or word generator or pulse generator and oscilloscope with a bandwidth of at least 43 MHz will be needed.

The user needs to provide the proper LVCMOS/RGB inputs and LVCMOS/clock to the serializer and also provide a proper interface from the de-serializer output to an LCD panel or test equipment. The serializer and de-serializer boards can also be used to evaluate device parameters. A cable conversion board or harness scramble may be necessary depending on type of cable/connector interface used on the input to the DS90UR241 and to the output of the DS90UR124.

Example of suggested display setup:

1) video generator with LVCMOS output
2) 6-bit LCD panel with a LVCMOS input interface.

Contents of the Evaluation Kit:

1) One Serializer board with the DS90UR241
2) One De-serializer board with the DS90UR124
3) One 2-meter USB 2.0 Hi-SPEED cable assembly
4) Evaluation Kit Documentation (this manual)
5) DS90UR241/124 Datasheet

SERDES Typical Application:

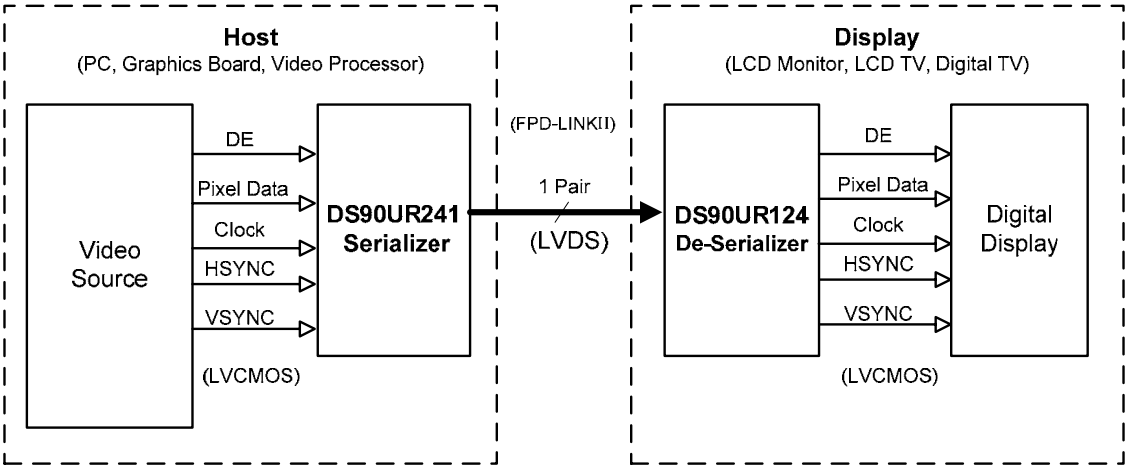


Figure 1a. Typical SERDES Application (18-bit RGB Color)

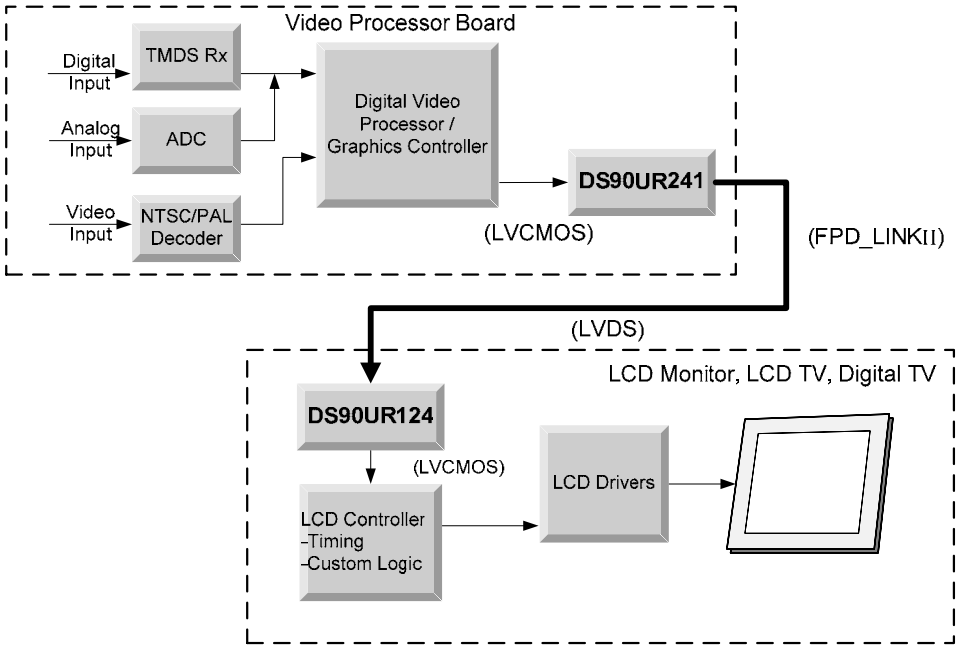


Figure 1b. Typical SERDES System Diagram

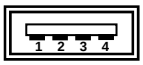
Figures 1a and 1b illustrate the use of the Chipset (Tx/Rx) in a Host to Flat Panel Interface.

The chipsets support up to 18-bit color depth TFT LCD Panels.

Refer to the proper datasheet information on Chipsets (Tx/Rx) provided on each board for more detailed information.

How to set up the Evaluation Kit:

The PCB routing for the serializer input pins (DIN) have been laid out to accept incoming LVCMOS signals from a 50-pin IDC connector. The TxOUT/RxIN (DOUT/RIN) interface uses a USB connector/cable assembly (provided). The PCB routing for the Rx output pins (ROUT) are accessed through a 50-pin IDC connector. Please follow these steps to set up the evaluation kit for bench testing and performance measurements:

1) A two (2) meter USB connector/cable assembly has been included in the kit. Connect 4-pin USB A 

A side of cable harness to the serializer board and the other side 5-pin mini USB jack 

MIN to the de-serializer board. This completes the LVDS interface connection.
NOTE: The DS90C241 and DS90C124 are NOT USB compliant and should not be plugged into a USB device nor should a USB device be plugged into the demo boards.

2) Jumpers and switches have been configured at the factory; they should not require any changes for immediate operation of the chipset. See text on Configuration settings for more details. From the Video Decoder board, connect a flat cable (not supplied) to the Serializer board and connect another flat cable (not supplied) from the De-serializer board to the panel. Caution: The LVCMOS input levels should be within the specified range for optimal performance, not to exceed the absolute maximum rating of -0.3V to (VCC +0.3V).
Note: For 50 ohm LVCMOS input signal sources, add 50 ohm parallel termination resistors R1-R25 on the DS90UR241 Serializer board and provide appropriate 3.3V LVCMOS input signal levels into DIN[23:0] and TCLK.

3) Power for the Tx and Rx boards must be supplied externally through Power Jack (VDD). Grounds for both boards are connected through Power Jack (VSS) (see section below).

Power Connection:

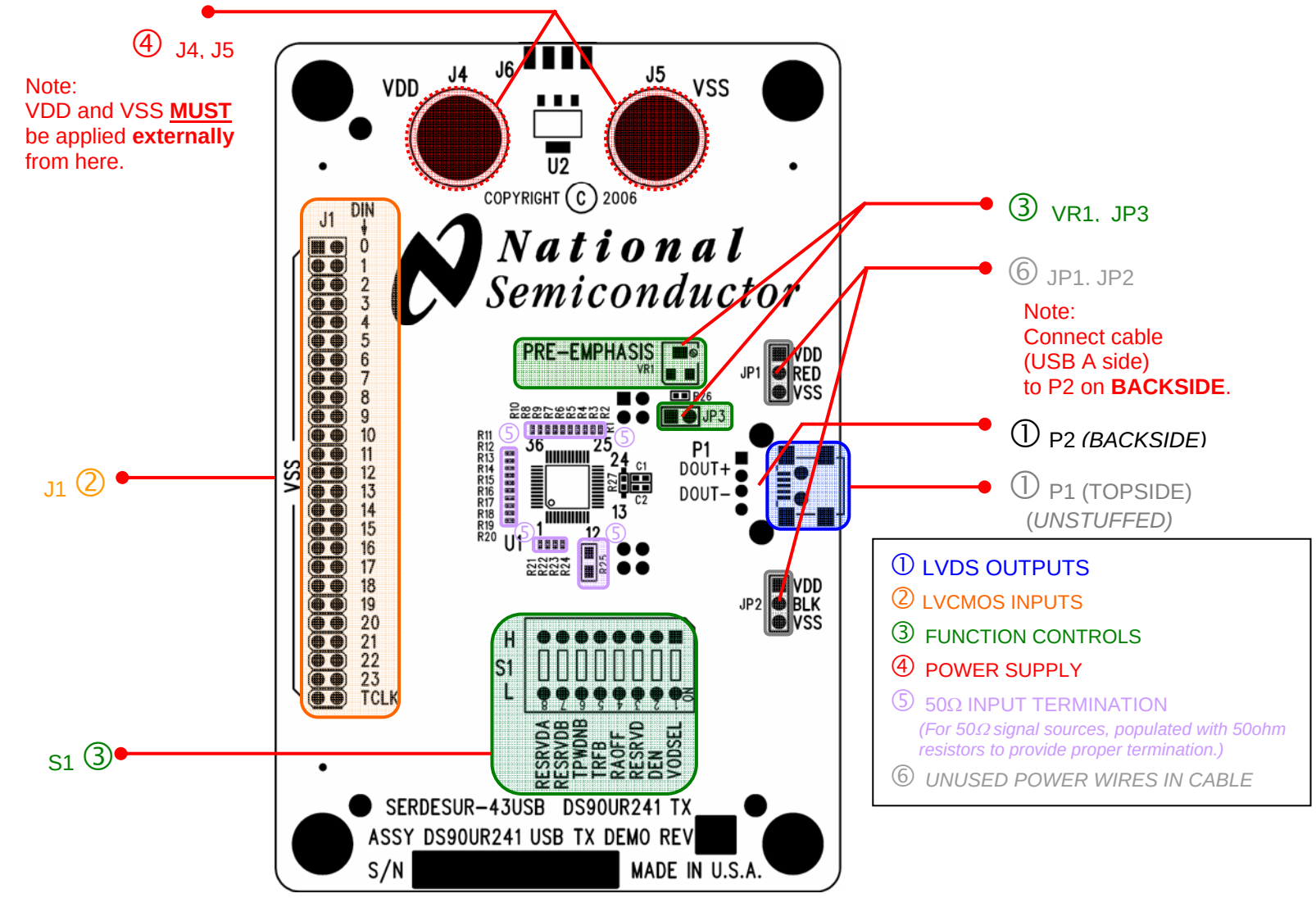
The serializer and de-serializer boards must be powered by supplying power externally through J4 (VDD) and J5 (VSS) on serializer Board and J4 (VDD) and J5 (VSS) on de-serializer board. Note +4V is the absolute MAXIMUM voltage (not operating voltage) that should ever be applied to the SERDES serializer (DS90UR241) or de-serializer (DS90UR124) VDD terminal. Damage to the device(s) can result if the voltage maximum is exceeded.

SERDES Serializer Board Description:

The 50-pin IDC connector J1 accepts 24 bits of LVCMOS RGB data (DIN0-DIN23) along with the clock input (TCLK).

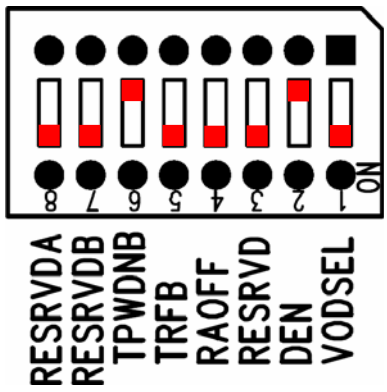
The SERDES serializer board is powered externally from the J4 (VDD) and J5 (VSS) connectors shown below. For the serializer to be operational, the Power Down (S1-TPWDNB) and Data Enable (S1-DEN) switches on S1 must be set HIGH. Rising or falling edge reference clock is also selected on S1-TRFB: HIGH (rising) or LOW (falling). FPD_LINKII is an AC coupled LVDS (series 0.1µF capacitors on each side of the LVDS serializer outputs and de-serializer inputs). JP1 and JP2 are configured from the factory to be shorted to VSS; these are the unused power wires in the cable harness.

The USB connector P2 (on the backside of the board) provides the interface connection to the LVDS signals to the de-serializer board.



Configuration Settings for the Serializer Board

S1: Serializer Input Features Selection

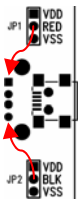
Reference	Description	Input = L	Input = H	S1
RESRVDA	**RES**e**RV**e**D A**	MUST be tied low for normal operation **(Default)**	Not allowed	
RESRVDB	**RES**e**RV**e**D B**	MUST be tied low for normal operation **(Default)**	Not allowed	
TPWDNB	**P**o**W**er**D**ow**N B**ar	Powers Down	Normal operation **(Default)**	
TRFB	Latch input data on **R**ising or **F**alling edge of TCLK	Falling Edge **(Default)**	Rising Edge	
RAOFF	**RA**ndomizer **OFF**	Randomizer ON. **(Default)** *Note: DS90**UR**124 RAOFF MUST also be set Low.*	Randomizer OFF. *Note: DS90**UR**124 RAOFF MUST also be set High.*	
RESRVD	**RES**e**RV**e**D**	MUST be tied low for normal operation **(Default)**	Not allowed	
DEN	Serializer Output **D**ata **EN**abled	Disabled	Enabled **(Default)**	
VODSEL	LVDS output **VOD SEL**ect	≈350mV **(Default)**	≈700mV	

JP3,VR1: Pre-Emphasis Feature Selection

Reference	Description	OPEN (floating)	CLOSED (Path to GND)	
JP3	Pre-Emphasis – helps to increase the eye pattern opening in the LVDS stream	Disabled – no jumper **(Default)** 	Enabled – With jumper 	
JP3 & VR1	Pre-Emphasis adjustment (via screw) JP1 **MUST** have a jumper to use VR1 potentiometer. VR1 = 0Ω to 20KΩ, JP1 + VR1 + 6KΩ *(R26)* = ~6KΩ (maximum pre-emphasis) to ~26KΩ (minimum pre-emphasis*). $I_{PRE} = [1.2/(R_{PRE})] \times 40$, R_{PRE} (minimum) $\geq$ 6KΩ **Note: maximum is based on resistor value. In this case ~26KΩ value is based on the ~6kΩ fixed resistor plus ~20KΩ maximum potentiometer value. User can use hundreds of Kohms to reduce the pre-emphasis value.*	Clockwise  increases R_{PRE} value which decreases pre-emphasis	Counter-Clockwise  decreases R_{PRE} value which increases pre-emphasis	

Pre-emphasis user note:
Pre-emphasis must be adjusted correctly based on application frequency, cable quality, cable length, and connector quality. Maximum pre-emphasis should only be used under extreme worse case conditions; for example at the upper frequency specification of the part and/or low grade cables at maximum cable lengths. Typically all that is needed is minimum pre-emphasis. Users should start with no pre-emphasis first and gradually apply pre-emphasis until there is clock lock and no data errors. The best way to monitor the pre-emphasis effect is to hook up a differential probe to the 100Ω termination resistor (R1) on the DS90UR124 Rx demo board (NOT to R27 on the DS90UR241 Tx demo board). The reason for monitoring R1 on the Rx side is because you want to see what the receiver will see the attenuation signal AFTER the cable/connector.

JP1, JP2: USB Cable Assembly - RED wire and BLK wire

Reference	Description	VDD	VSS	OPEN
JP1	RED wire in USB cable thru P1 connector. Jumper RED to VSS recommended. **CAUTION: Jumper settings should be set the same on the DS90UR124 board or a short can occur.**	RED wire tied to VDD 	RED wire tied to VSS **(Default)** 	RED wire floating (not recommended) 
JP2	BLACK wire in USB cable thru P1 connector. Jumper BLACK to VSS recommended. **CAUTION: Jumper settings should be set the same on the DS90UR124 board or a short can occur.**	BLACK wire tied to VDD 	BLACK wire tied to VSS **(Default)** 	BLACK wire floating (not recommended) 
JP1 and JP2 connections on connector P1  **P1**				

Serializer LVCMOS and LVDS Pinout by IDC Connector

The following two (2) tables illustrate how the serializer inputs are mapped to the IDC connector J1, the LVDS outputs on the USB connector P2 pinout. Note – labels are also printed on the demo boards for both the TTL input and LVDS outputs.

LVCMOS INPUT	
J1 pin no.	**name**
2	DIN0
4	DIN1
6	DIN2
8	DIN3
10	DIN4
12	DIN5
14	DIN6
16	DIN7
18	DIN8
20	DIN9
22	DIN10
24	DIN11
26	DIN12
28	DIN13
30	DIN14
32	DIN15
34	DIN16
36	DIN17
38	DIN18
40	DIN19
42	DIN20
44	DIN21
46	DIN22
48	DIN23
50	TCLK
all odd pins	gnd

LVDS OUTPUT	
P2 pin no.	**name**
1	RED
2	DOUT+
3	DOUT-
4	BLK

BOM (Bill of Materials) Serializer PCB:

DS90UR241 Tx USB Demo Board - Board Stackup Revised: Friday, September 15, 2006
DS90UR241 Tx USB Demo Board Revision: 1
Bill Of Materials September 15,2006 19:21:34

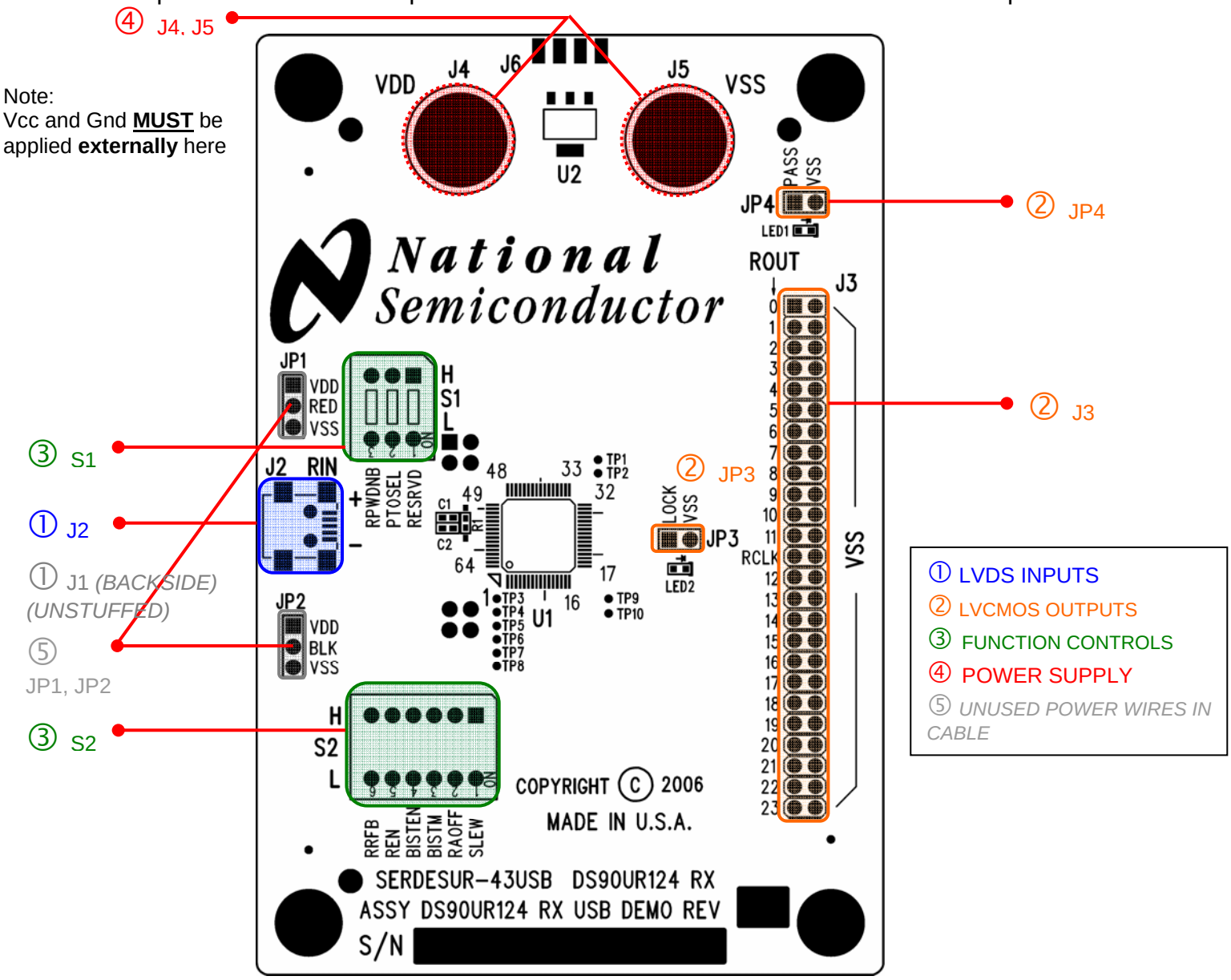
Item	Qty	Reference	Part	PCB Footprint
1	2	C1,C2	0.1uF	CAP/HDC-0402
2	1	C3	2.2uF	3528-21_EIA
3	1	C4	22uF	CAP/N
4	1	C5	0.1uF	CAP/HDC-1206
5	5	C6,C9,C10,C13,C20	22uF	CAP/EIA-B 3528-21
6	5	C7,C11,C15,C16,C19	0.01uF	CAP/HDC-0603
7	5	C8,C12,C14,C17,C18	0.1uF	CAP/HDC-0603
8	2	JP2,JP1	3-Pin Header	Header/3P
9	1	JP3	2-Pin Header	Header/2P
10	1	J1	IDC2X25_Unshrouded	IDC-50
11	2	J5,J4	BANANA	CON/BANANA-S
12	1	P1	mini USB 5pin_open	mini_B_USB_surface_mount
13	1	P2	USB A	USB_TYPE_A_4P
14	24	R1,R2,R3,R4,R5,R6,R7,R8, R9,R10,R11,R12,R13,R14, R15,R16,R17,R18,R19,R20, R21,R22,R23,R24	49.9ohm_open	RES/HDC-0201
15	1	R25	49.9ohm_open	RES/HDC-0805
16	1	R26	5.76K	RES/HDC-0402
17	1	R27	100 ohm,0402	RES/HDC-0402
18	1	R29	0_ohm	RES/HDC-0201
19	8	R38,R39,R40,R41,R42,R43, R44,R45	10K	RES/HDC-0805
20	1	S1	SW DIP-8	DIP-16
21	1	U1	DS90UR241	48 ld TQFP
22	1	VR1	SVR20K	Surface Mount 4mm Square
23	2	X2,X1	TP_0402	TP/0402

Rx SERDES De-serializer Board:

The USB connector J2 provides the interface connection for LVDS signals to the serializer board.

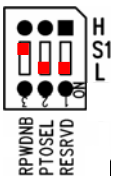
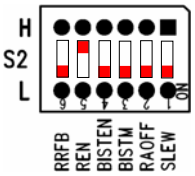
The SERDES de-serializer board is powered externally from the J4 (VDD) and J5 (VSS) connectors shown below. For the de-serializer to be operational, the Power Down (RPWDNB) and Receiver Enable (REN) switches on S1 and S2 must be set HIGH. Rising or falling edge reference clock is also selected by S1: HIGH (rising) or LOW (falling).

The 50 pin IDC Connector J3 provides access to the 24 bit LVCMOS and clock outputs.



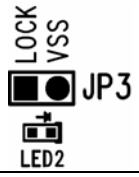
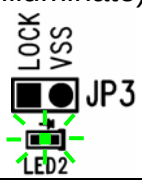
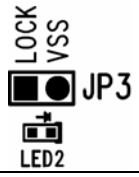
Configuration Settings for the De-serializer Board

S1, S2: De-serializer Input Features Selection

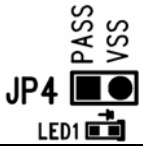
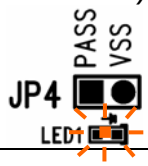
Reference	Description	Input = L	Input = H	S1
RPWDNB	**P**o**W**er**D**ow**N** **B**ar	Power Down (Disabled)	Normal Operational **(Default)**	
PTOSEL	**P**rogressive **T**urn **O**n **SEL**ect	Enabled **(Default)**	Disabled	
RESRVD	**RES**e**RV**e**D**	Don't care	Don't care	
Reference	**Description**	**Input = L**	**Input = H**	**S2**
RRFB	Latch input data on **R**ising or **F**alling edge of TCLK	Falling Edge **(Default)**	Rising Edge	
REN	**R**eceiver Output Data **EN**abled	Disabled	Enabled **(Default)**	
BISTEN	**BIST EN**able *Note: MUST set DS90UR241 ALL DIN[23:0] inputs Low or floating. Use in combination with BISTM pin.*	Normal Operating Mode, BIST Disabled **(Default)**	BIST Mode Enabled	
BISTM	**BIST M**ode Don't care if BISTEN=L. BISTEN MUST be High (enabled) for this pin to be functional.	Per Channel pass/fail; RxOUT[23:0] =H: pass; RxOUT[23:0] =H: fail	RxOUT[7:0]: binary error counting mode (up to 255 errors); RxOUT[23:8]: normal operation	
RAOFF	**RA**ndomizer **OFF**	Randomizer ON. **(Default)** *Note: DS90**UR**241 RAOFF MUST also be set Low.*	Randomizer OFF. *Note: DS90**UR**241 RAOFF MUST also be set High.*	
SLEW	**SLEW** rate control for ROUT[23:0] and RCLK	**(Default)**	~2X slew rate, ~2X drive strength	

Output Monitor Pins for the De-serializer Board

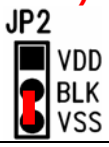
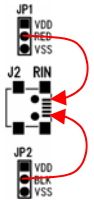
JP3: Output Lock Monitor

Reference	Description	Output = L	Output = H	JP3
LOCK	Receiver PLL **LOCK** **Note:** **DO NOT PUT A SHORTING JUMPER IN JP3.**	Unlocked 	PLL LOCKED (LED2 will illuminate) 	

JP4: PASS Monitor

Reference	Description	Output = L	Output = H	JP4
PASS	Receiver BIST monitor **PASS** flag **Note:** **DO NOT PUT A SHORTING JUMPER IN JP1.**	FAIL 	PASS (LED1 will illuminate) 	

JP1, JP2: USB Cable Assembly wire red and black

Reference	Description	VDD	VSS	OPEN
JP1	Red wire in USB cable thru JP1 connector. Jumper red wire to VSS recommended. **CAUTION:** **Jumper settings should be set the same on the DS90UR124 board or a short can occur.**	Red wire tied to VDD 	Red wire tied to VSS **(Default)** 	Red wire floating (not recommended) 
JP2	Black wire in USB cable thru JP2 connector. Jumper black wire to VSS recommended. **CAUTION:** **Jumper settings should be set the same on the DS90UR124 board or a short can occur.**	Black wire tied to VDD 	Black wire tied to VSS **(Default)** 	Black wire floating (not recommended) 
JP1 and JP2 connections on connector J2				

De-serializer LVDS Pinout and LVCMOS by IDC Connector

The following two tables illustrate how the LVDS inputs are mapped to the mini USB connector J2 and the Rx outputs are mapped to the IDC connector J3. Note – labels are also printed on the demo boards for both the LVDS inputs and TTL outputs.

LVDS INPUT	
J2 pin no.	**name**
1	RED
2	RIN+
3	RIN-
4	NC
5	BLK

LVCMOS OUTPUT	
J3 pin no.	**name**
1	ROUT0
3	ROUT1
5	ROUT2
7	ROUT3
9	ROUT4
11	ROUT5
13	ROUT6
15	ROUT7
17	ROUT8
19	ROUT9
21	ROUT10
23	ROUT11
25	RCLK
27	ROUT12
29	ROUT13
31	ROUT14
33	ROUT15
35	ROUT16
37	ROUT17
39	ROUT18
41	ROUT19
43	ROUT20
45	ROUT21
47	ROUT22
49	ROUT23
all even pins	gnd

BOM (Bill of Materials) De-serializer PCB:

DS90UR124 Rx USB Demo Board - Board Stackup Revised: Thursday, September 14, 2006
DS90UR124 Rx USB Demo Board Revision: 1
Bill Of Materials September 14,2006 18:28:58

Item	Qty	Reference	Part	PCB Footprint
1	2	C2,C1	0.1uF	CAP/HDC-0402
2	27	C3,C7,C8,C9,C10,C11,C12, C13,C14,C15,C16,C17,C18, C19,C20,C21,C22,C23,C24, C25,C26,C27,C28,C29,C30, C31,C42	open0402	CAP/HDC-0402
3	1	C4	2.2uF	3528-21_EIA
4	1	C5	22uF	CAP/N
5	1	C6	0.1uF	CAP/HDC-1206
6	8	C32,C33,C34,C41,C47,C50, C53,C54	22uF	CAP/EIA-B 3528-21
7	8	C35,C38,C40,C43,C46,C48, C52,C55	0.1uF	CAP/HDC-0603
8	8	C36,C37,C39,C44,C45,C49, C51,C56	0.01uF	CAP/HDC-0603
9	2	JP2,JP1	3-Pin Header	Header/3P
10	2	JP4,JP3	2-Pin Header_open	Header/2P
11	1	J1	mini USB 5pin_open	mini_USB_surface_mount
12	1	J2	mini USB 5pin	mini_USB_surface_mount
13	1	J3	IDC2X25_Unshrouded	IDC-50
14	2	J4,J5	BANANA	CON/BANANA-S
15	1	LED1	0402_orange_LED	0402
16	1	LED2	0603_green_LED	0603 (Super Thin)
17	1	R1	100 ohm,0402	RES/HDC-0402
18	9	R2,R3,R4,R34,R35,R36,R37, R38,R39	10K	RES/HDC-0805
19	1	S1	SW DIP-3	DIP-6
20	1	S2	SW DIP-6	DIP-12
21	1	U1	DS90UR124	64 pin TQFP

Typical Connection and Test Equipment

The following is a list of typical test equipment that may be used to generate signals for the TX inputs:

1) Digital Video Source – for generation of specific display timing such as Digital Video Processor or Graphics Controller with digital RGB (LVCMOS) output.
2) Astro Systems VG-835 - This video generator may be used for video signal sources for 6-bit Digital TTL/RGB.
3) Any other signal / video generator that generates the correct input levels as specified in the datasheet.
4) Optional – Logic Analyzer or Oscilloscope

The following is a list of typically test equipment that may be used to monitor the output signals from the RX:

1) LCD Display Panel which supports digital RGB (LVCMOS) inputs.
2) National Semiconductor DS90UR241 Serializer (Tx)
3) Optional – Logic Analyzer or Oscilloscope
4) Any SCOPE with a bandwidth of at least 43 MHz for TTL and/or 2 GHz for looking at the differential signal.

LVDS signals may be easily measured with high impedance / high bandwidth differential probes such as the TEK P6330 differential probes.

The picture below shows a typical test set up using a Graphics Controller and LCD Panel.

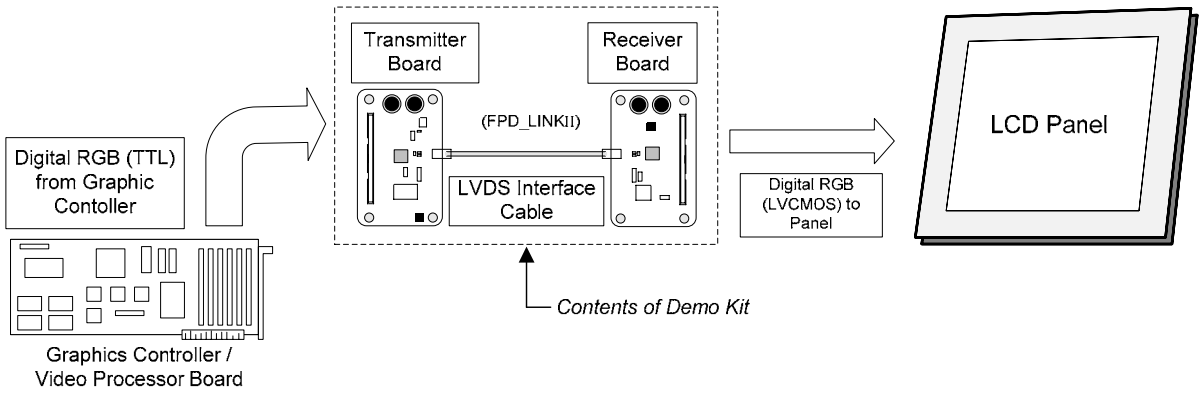


Figure 2. Typical SERDES Setup of LCD Panel Application

The picture below shows a typical test set up using a generator and scope.

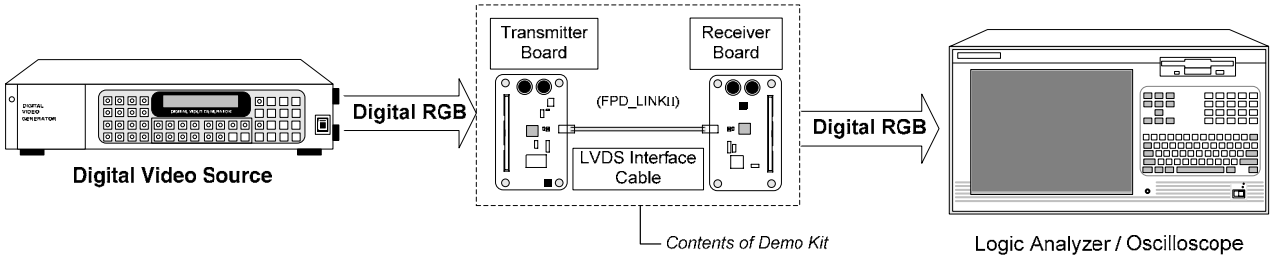


Figure 3. Typical SERDES Test Setup for Evaluation

Troubleshooting

If the demo boards are not performing properly, use the following as a guide for quick solutions to potential problems. If the problem persists, please contact the local Sales Representative for assistance.

QUICK CHECKS:

1. Check that Power and Ground are connected to both Tx AND Rx boards.
2. Check the supply voltage (typical 3.3V) and also current draw with both Tx and Rx boards. The Serializer board should draw about 55-65mA with clock and all data bits switching at 43MHz, (R_{PRE}=9KΩ). The De-serializer board should draw about 75-85mA with clock and all data bits switching at 43MHz, (minimum ROUT loading).
3. Verify input clock and input data signals meet requirements for VILmin, VILmax, VIHmin, VIHmax, tset, thold), also verify that data is strobed on the selected rising/falling (RFB pin) edge of the clock.
4. Check that the Jumpers and Switches are set correctly.
5. Check that the cable is properly connected.

TROUBLESHOOTING CHART

Problem…	**Solution…**
There is only the output clock. There is no output data.	Make sure the data is applied to the correct input pin. Make sure data is valid at the input.
No output data and clock.	Make sure Power is on. Input data and clock are active and connected correctly. Make sure that the cable is secured to both demo boards.
Power, ground, input data and input clock are connected correctly, but no outputs.	Check the Power Down pins of both Serializer and De-serializer boards to make sure that the devices are enabled (/PD=Vcc) for operation. Also check DEN on the Serializer board and REN on the Deserializer board is set HIGH.
The devices are pulling more than 1A of current.	Check for shorts in the cables connecting the TX and RX boards.
After powering up the demo boards, the power supply reads less than 3V when it is set to 3.3V.	Use a larger power supply that will provide enough current for the demo boards, a 500mA minimum power supply is recommended.

Note: Please note that the following references are supplied only as a courtesy to our valued customers. It is not intended to be an endorsement of any particular equipment or hardware supplier.

Connector References

Hirose Electric Europe B.V.
Beech Avenue 46
1119 PV Schiphol-Rijk
The Netherlands
Phone: +31 20 655 7467, Fax: +31 20 655 7469
www.HiroseEurope.com

Cable References

Nissei Electric Co., LTD
1509 Okubo-Cho, Hamamatsu-City
Shizuoka-Pref, 432-8006 Japan
Phone: +81 53 485 4114, Fax: +81 53 485 6908
www.nissei-el.co.jp

Cable Recommendations

- For optimal performance, we recommend Shielded Twisted Pair (STP) 100Ω differential impedance cable for high-speed data applications.

Equipment References

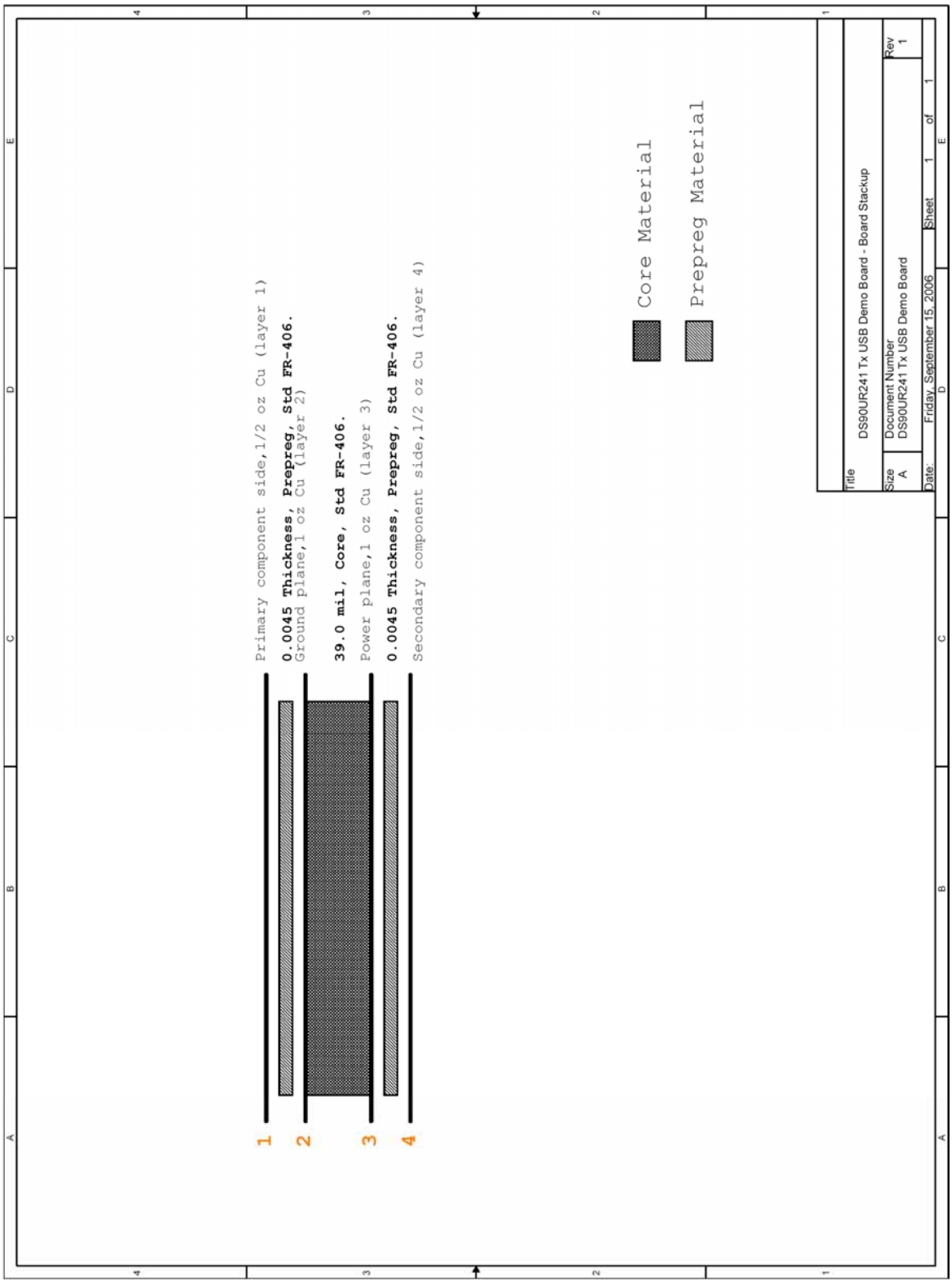
Astro Systems
425 S. Victory Blvd. Suite A
Burbank, CA 91502
Phone: (818) 848-7722 , Fax: (818) 848-7799
www.astro-systems.com
Digital Video Pattern Generator – Astro Systems VG-835 (or equivalent):

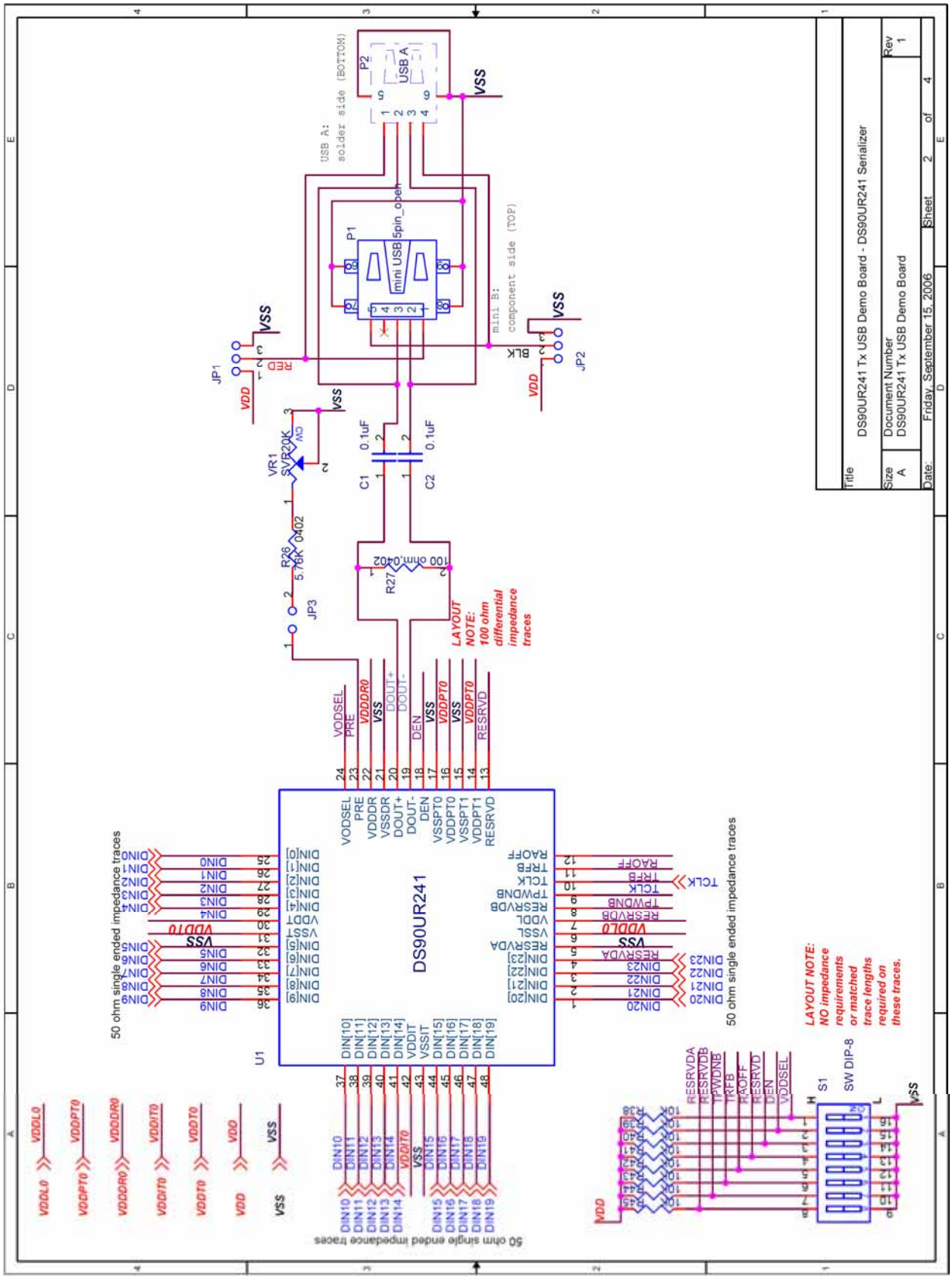
Extra Component References

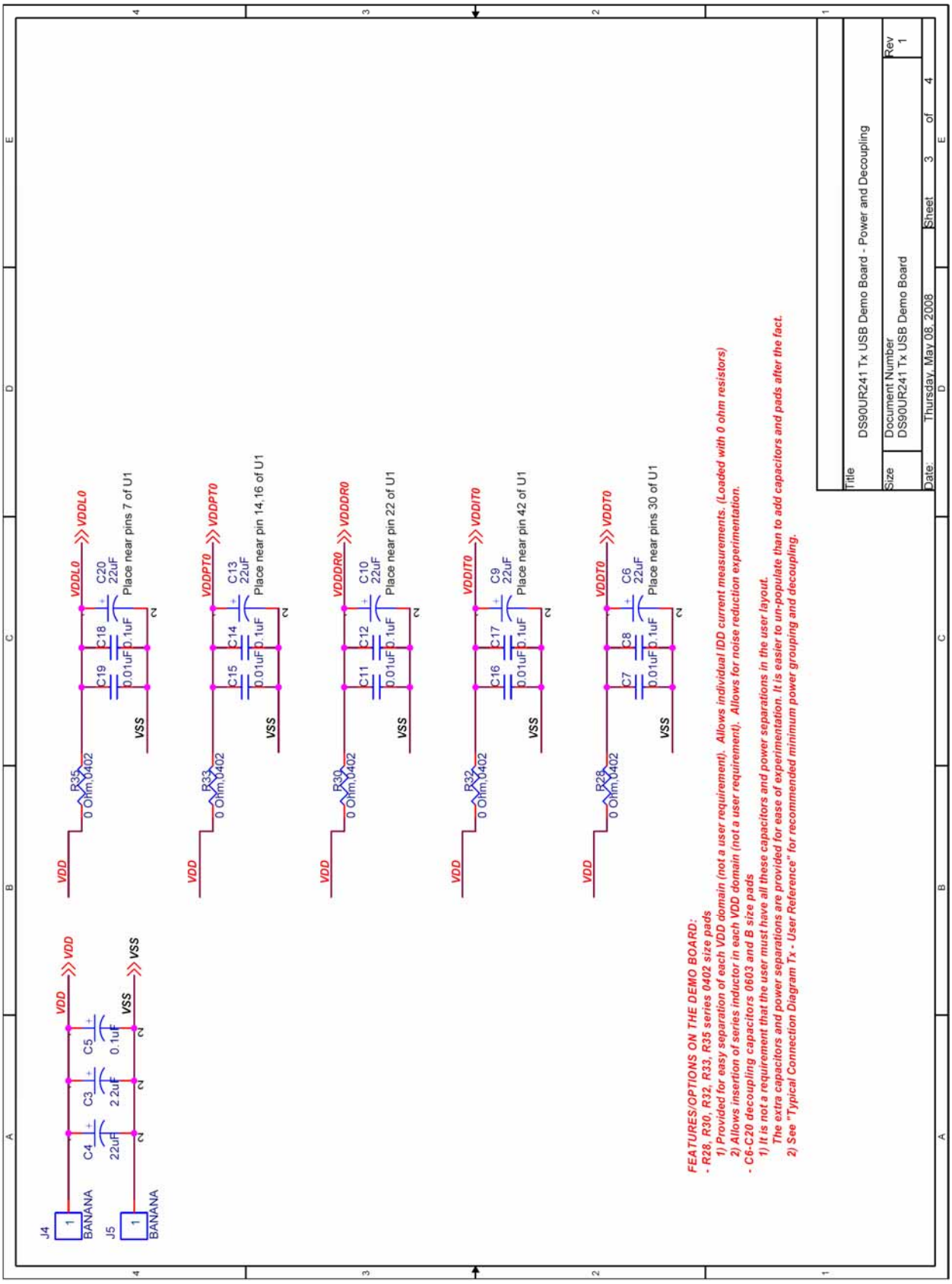
TDK Corporation of America
1740 Technology Drive, Suite 510
San Jose, CA 95110
Phone: (408) 437-9585, Fax: (408) 437-9591
www.component.tdk.com
Optional EMI Filters – TDK Chip Beads (or equivalent)

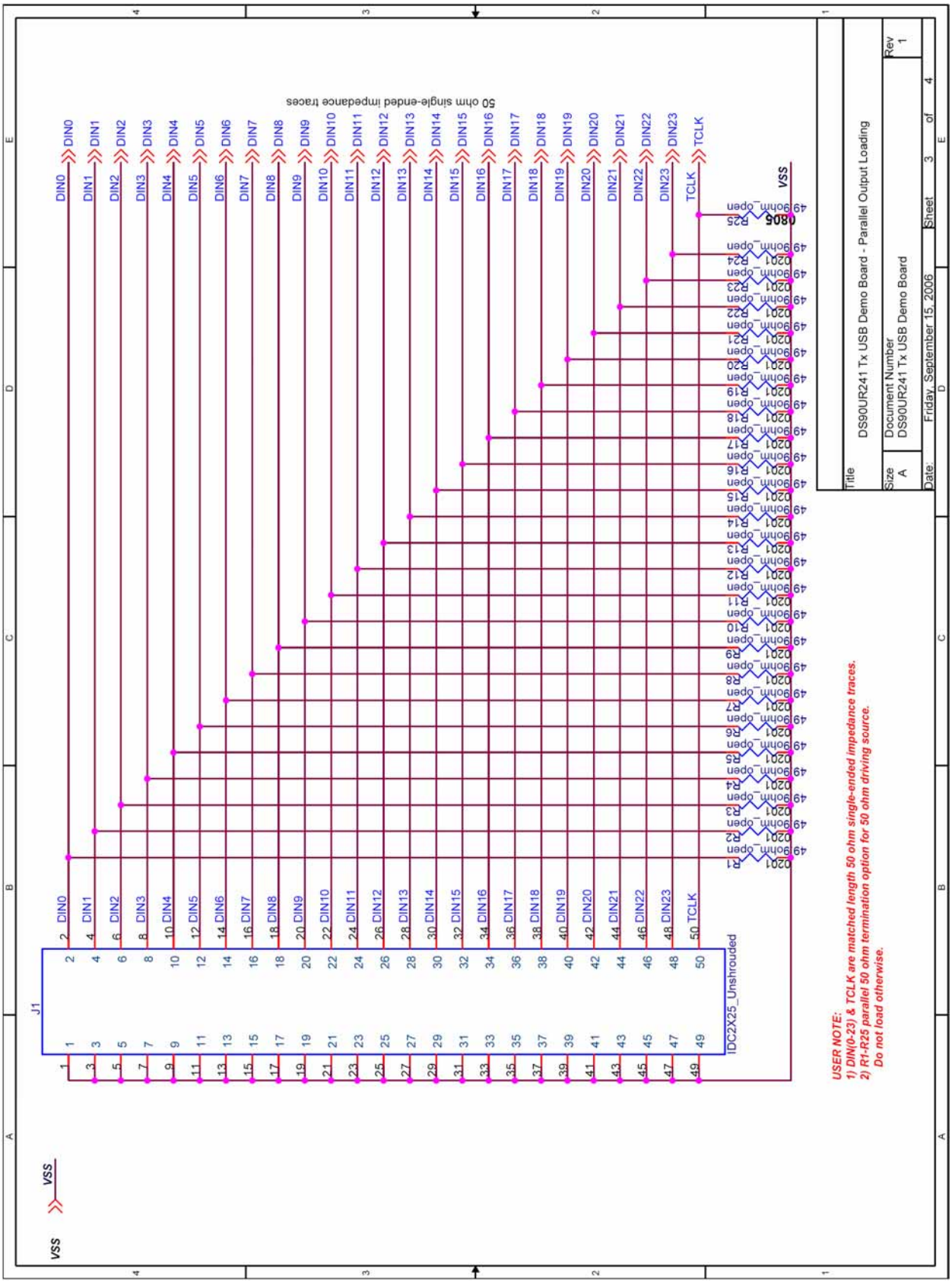
Appendix

Serializer (Tx) PCB Schematic:

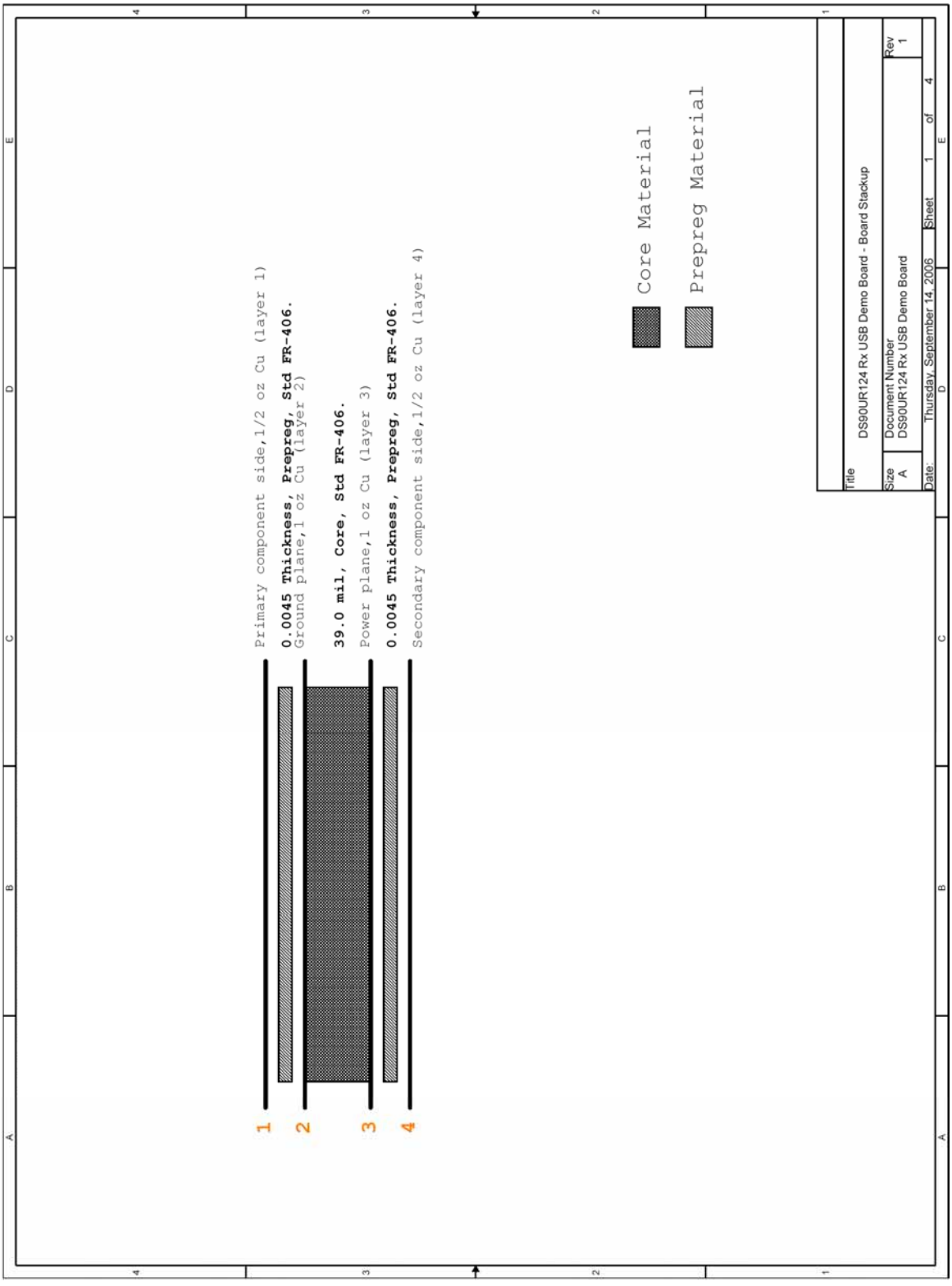


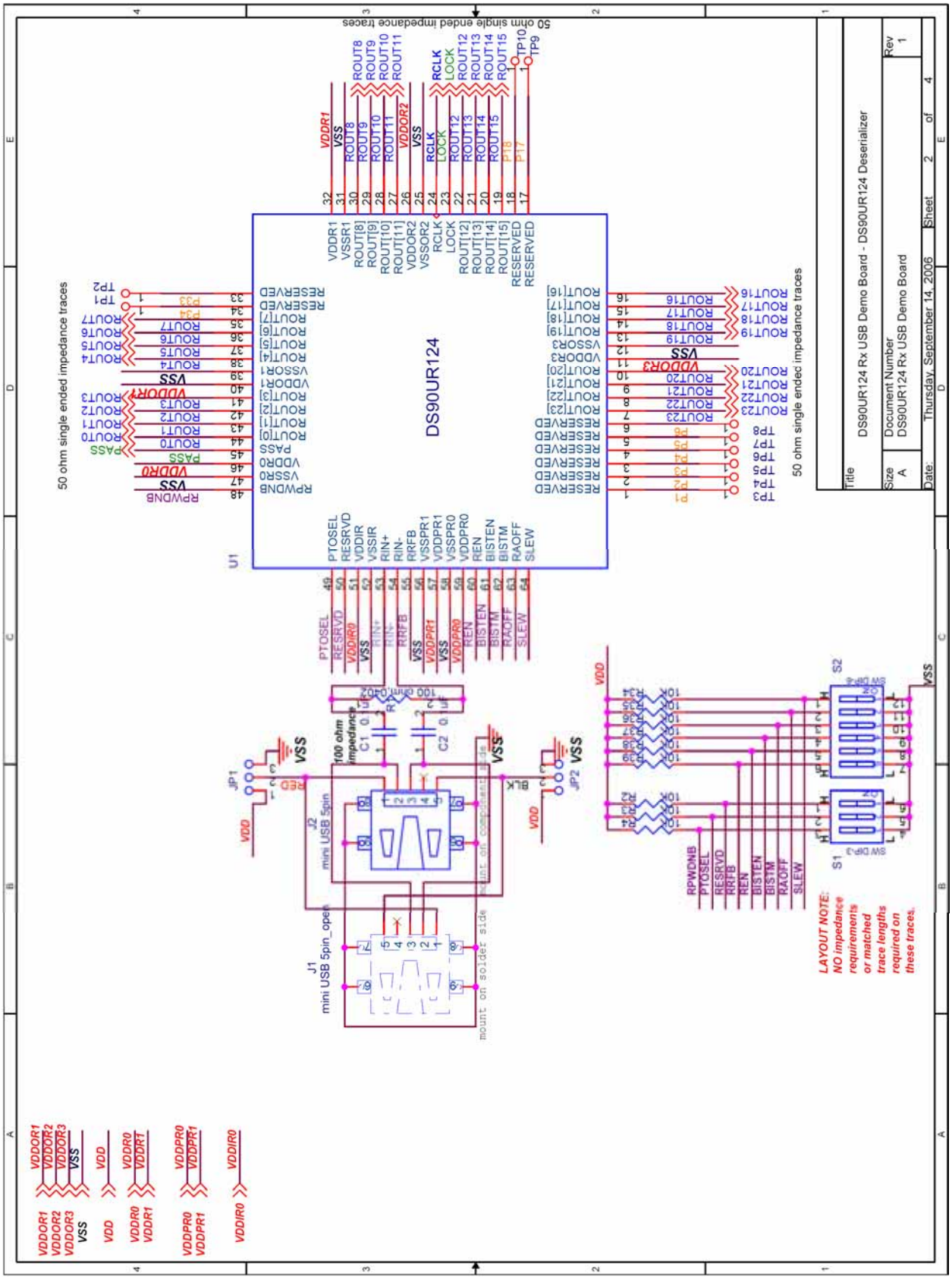

DS90UR241 Tx USB Demo Board - DS90UR241 Serializer
DS90UR241 Tx USB Demo Board
Friday, September 15, 2006
DS90UR241
LAYOUT NOTE: 100 ohm differential impedance traces
LAYOUT NOTE: NO impedance requirements or matched trace lengths required on these traces.
50 ohm single ended impedance traces
USB A
mini USB 5pin_oben
SW DIP-8

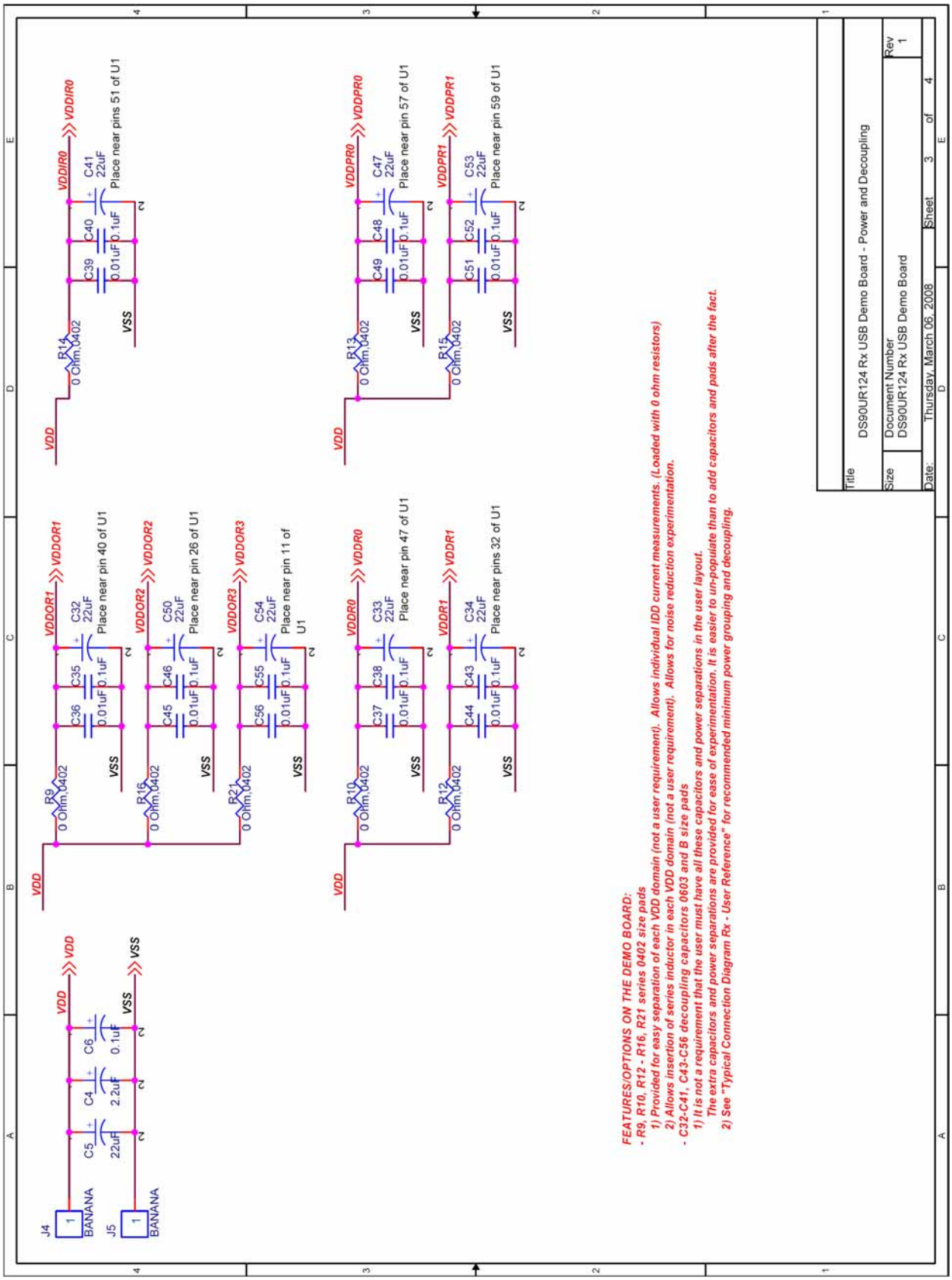

VDD
VSS
VDDL0
VDDPT0
VDDDR0
VDDIT0
VDDT0
R35 0 Ohm,0402
R33 0 Ohm,0402
R30 0 Ohm,0402
R32 0 Ohm,0402
R28 0 Ohm,0402
C20 22uF
C18 0.01uF
C19 0.1uF
C13 22uF
C14 0.01uF
C15 0.1uF
C10 22uF
C12 0.01uF
C11 0.1uF
C9 22uF
C17 0.01uF
C16 0.1uF
C6 22uF
C8 0.01uF
C7 0.1uF
Place near pins 7 of U1
Place near pin 14,16 of U1
Place near pin 22 of U1
Place near pin 42 of U1
Place near pins 30 of U1
J4 BANANA
J5 BANANA
C4 22uF
C3 2.2uF
C5 0.1uF
FEATURES/OPTIONS ON THE DEMO BOARD:
- R28, R30, R32, R33, R35 series 0402 size pads
1) Provided for easy separation of each VDD domain (not a user requirement). Allows individual IDD current measurements. (Loaded with 0 ohm resistors)
2) Allows insertion of series inductor in each VDD domain (not a user requirement). Allows for noise reduction experimentation.
- C6-C20 decoupling capacitors 0603 and B size pads
1) It is not a requirement that the user must have all these capacitors and power separations in the user layout.
The extra capacitors and power separations are provided for ease of experimentation. It is easier to un-populate than to add capacitors and pads after the fact.
2) See "Typical Connection Diagram Tx - User Reference" for recommended minimum power grouping and decoupling.
Title
DS90UR241 Tx USB Demo Board - Power and Decoupling
Size
Document Number
DS90UR241 Tx USB Demo Board
Rev
1
Date: Thursday, May 08, 2008
Sheet 3 of 4

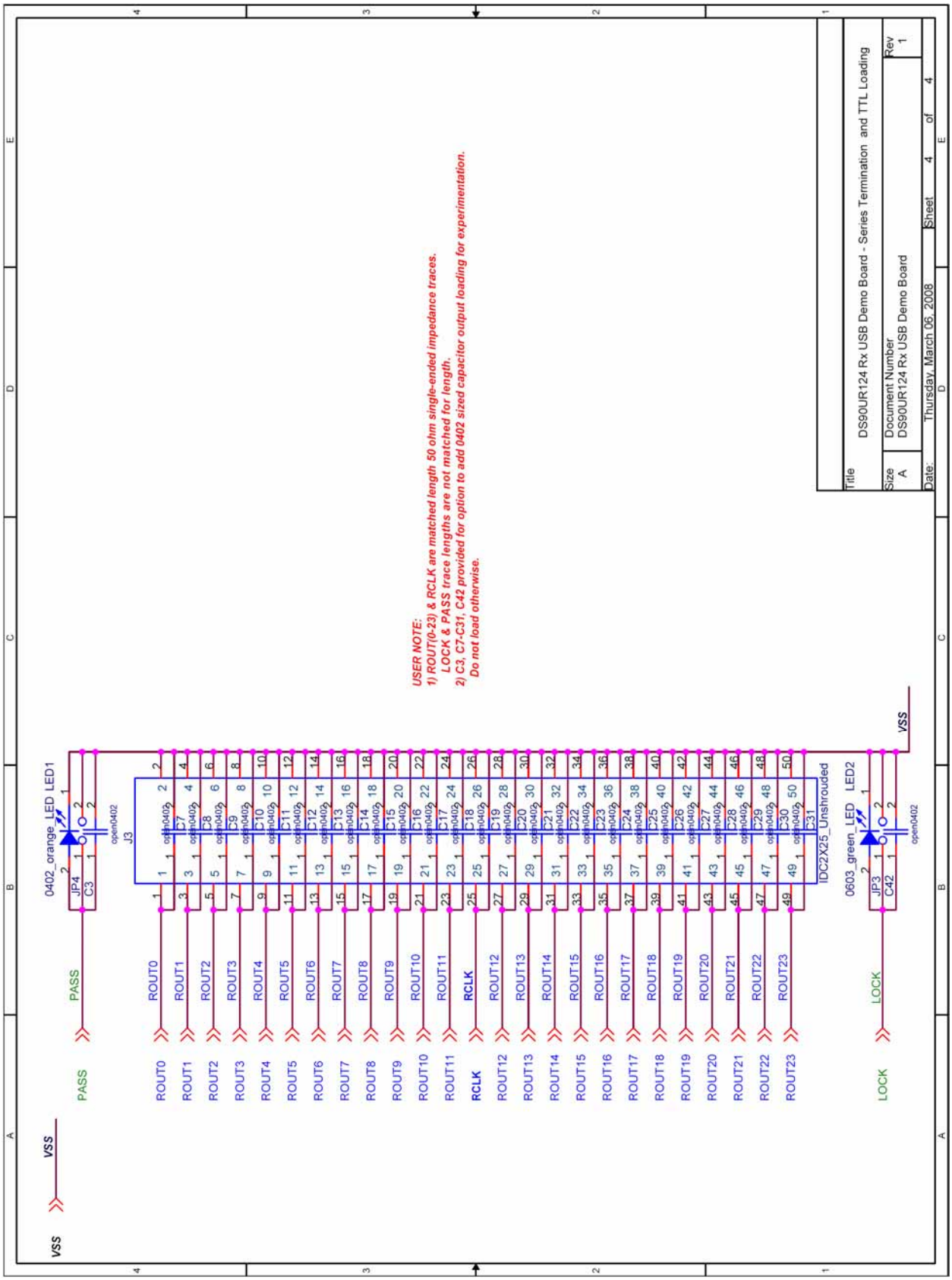

50 ohm single-ended impedance traces
J1
IDC2X25_Unshrouded
VSS
DIN0
DIN1
DIN2
DIN3
DIN4
DIN5
DIN6
DIN7
DIN8
DIN9
DIN10
DIN11
DIN12
DIN13
DIN14
DIN15
DIN16
DIN17
DIN18
DIN19
DIN20
DIN21
DIN22
DIN23
TCLK
0805
0201
49.9ohm_open
USER NOTE:
1) DIN(0-23) & TCLK are matched length 50 ohm single-ended impedance traces.
2) R1-R25 parallel 50 ohm termination option for 50 ohm driving source.
Do not load otherwise.
Title
DS90UR241 Tx USB Demo Board - Parallel Output Loading
Size
A
Document Number
DS90UR241 Tx USB Demo Board
Rev
1
Date:
Friday, September 15, 2006
Sheet
3
of
4

De-serializer (Rx) PCB Schematic:

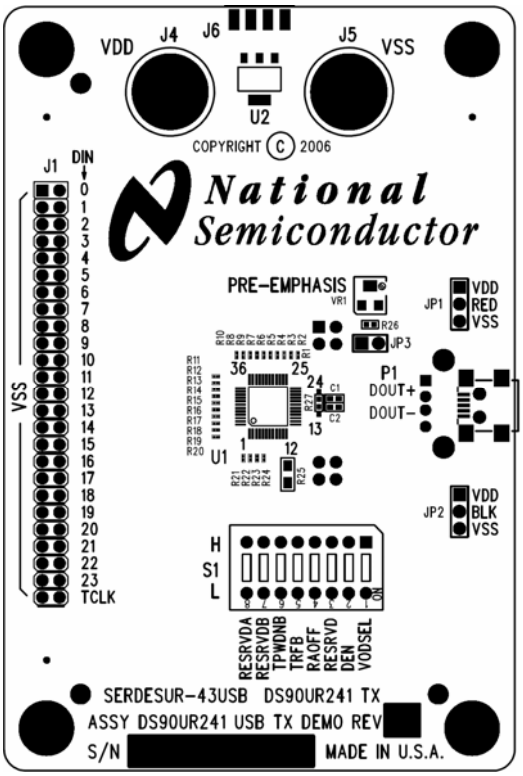



DS90UR124
U1
50 ohm single ended impedance traces
50 ohm single endec impedance traces
Title
DS90UR124 Rx USB Demo Board - DS90UR124 Deserializer
Size
A
Document Number
DS90UR124 Rx USB Demo Board
Rev
1
Date:
Thursday, September 14, 2006
Sheet
2
of
4
mini USB 5pin
J1
J2
S1
S2
LAYOUT NOTE:
NO impedance requirements or matched trace lengths required on these traces.

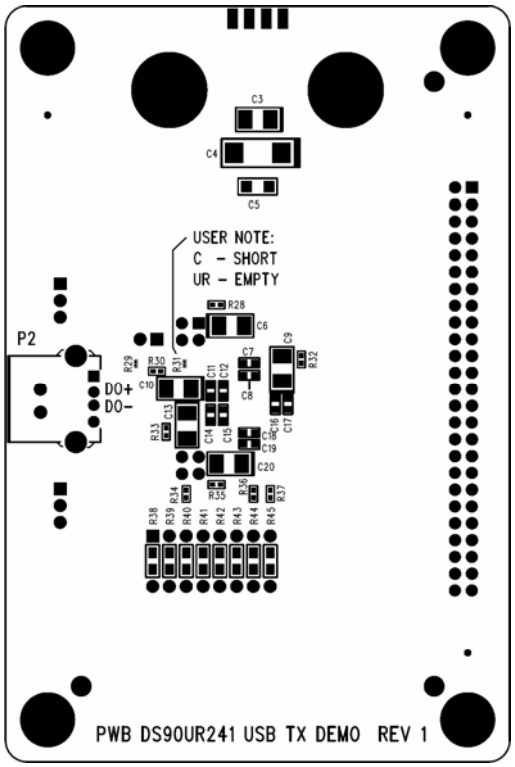

VDD
VSS
VDDIR0
VDDPR0
VDDPR1
VDDOR1
VDDOR2
VDDOR3
VDDR0
VDDR1
R9 0 Ohm,0402
R10 0 Ohm,0402
R12 0 Ohm,0402
R13 0 Ohm,0402
R14 0 Ohm,0402
R15 0 Ohm,0402
R16 0 Ohm,0402
R21 0 Ohm,0402
C4 2.2uF
C5 22uF
C6 0.1uF
C32 22uF
C33 22uF
C34 22uF
C35 0.01uF
C36 0.1uF
C37 0.01uF
C38 0.1uF
C39 0.01uF
C40 0.1uF
C41 22uF
C43 0.01uF
C44 0.1uF
C45 0.01uF
C46 0.1uF
C47 22uF
C48 0.01uF
C49 0.1uF
C50 22uF
C51 0.01uF
C52 0.1uF
C53 22uF
C54 22uF
C55 0.01uF
C56 0.1uF
Place near pin 40 of U1
Place near pin 47 of U1
Place near pins 32 of U1
Place near pin 26 of U1
Place near pin 11 of U1
Place near pins 51 of U1
Place near pin 57 of U1
Place near pin 59 of U1
J4 BANANA
J5 BANANA
FEATURES/OPTIONS ON THE DEMO BOARD:
- R9, R10, R12 - R16, R21 series 0402 size pads
1) Provided for easy separation of each VDD domain (not a user requirement). Allows individual IDD current measurements. (Loaded with 0 ohm resistors)
2) Allows insertion of series inductor in each VDD domain (not a user requirement). Allows for noise reduction experimentation.
- C32-C41, C43-C56 decoupling capacitors 0603 and B size pads
1) It is not a requirement that the user must have all these capacitors and power separations in the user layout.
The extra capacitors and power separations are provided for ease of experimentation. It is easier to un-populate than to add capacitors and pads after the fact.
2) See "Typical Connection Diagram Rx - User Reference" for recommended minimum power grouping and decoupling.
Title
DS90UR124 Rx USB Demo Board - Power and Decoupling
Size
Document Number
DS90UR124 Rx USB Demo Board
Rev
1
Date:
Thursday, March 06, 2008
Sheet
3
of
4


USER NOTE:
1) ROUT(0-23) & RCLK are matched length 50 ohm single-ended impedance traces.
LOCK & PASS trace lengths are not matched for length.
2) C3, C7-C31, C42 provided for option to add 0402 sized capacitor output loading for experimentation.
Do not load otherwise.
Title
DS90UR124 Rx USB Demo Board - Series Termination and TTL Loading
Size
A
Document Number
DS90UR124 Rx USB Demo Board
Rev
1
Date:
Thursday, March 06, 2008
Sheet
4
of
4
0402_orange_LED LED1
0603_green_LED LED2
JP4
JP3
C3
C42
J3
IDC2X25_Unshrouded
open0402
open0603
VSS
PASS
LOCK
ROUT0
ROUT1
ROUT2
ROUT3
ROUT4
ROUT5
ROUT6
ROUT7
ROUT8
ROUT9
ROUT10
ROUT11
RCLK
ROUT12
ROUT13
ROUT14
ROUT15
ROUT16
ROUT17
ROUT18
ROUT19
ROUT20
ROUT21
ROUT22
ROUT23

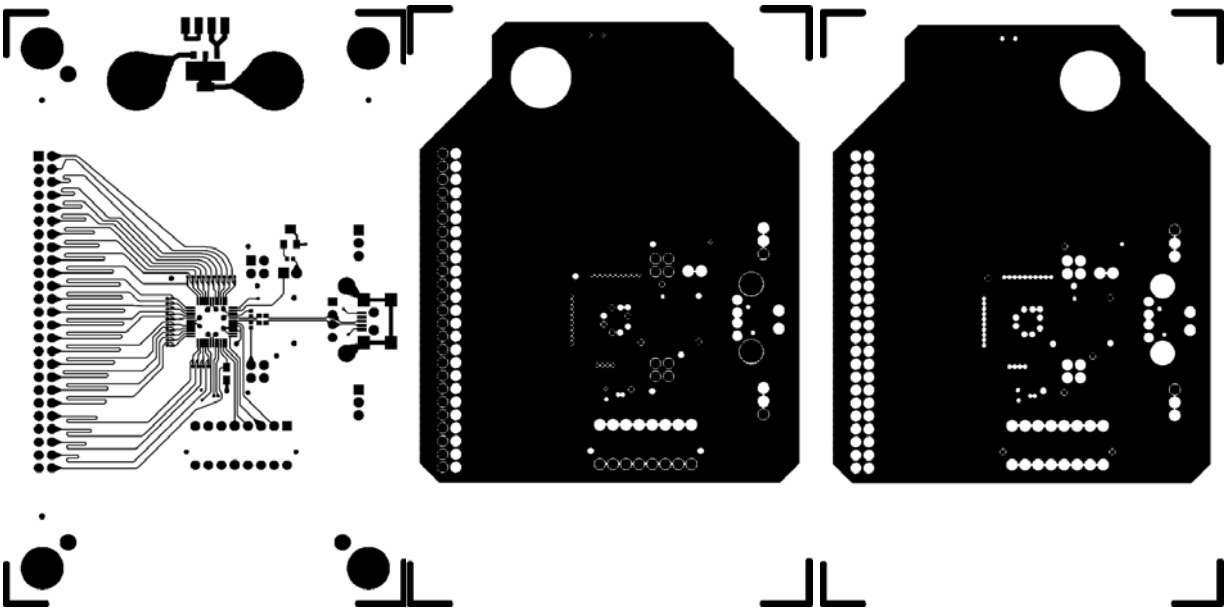
Serializer (Tx) PCB Layout:



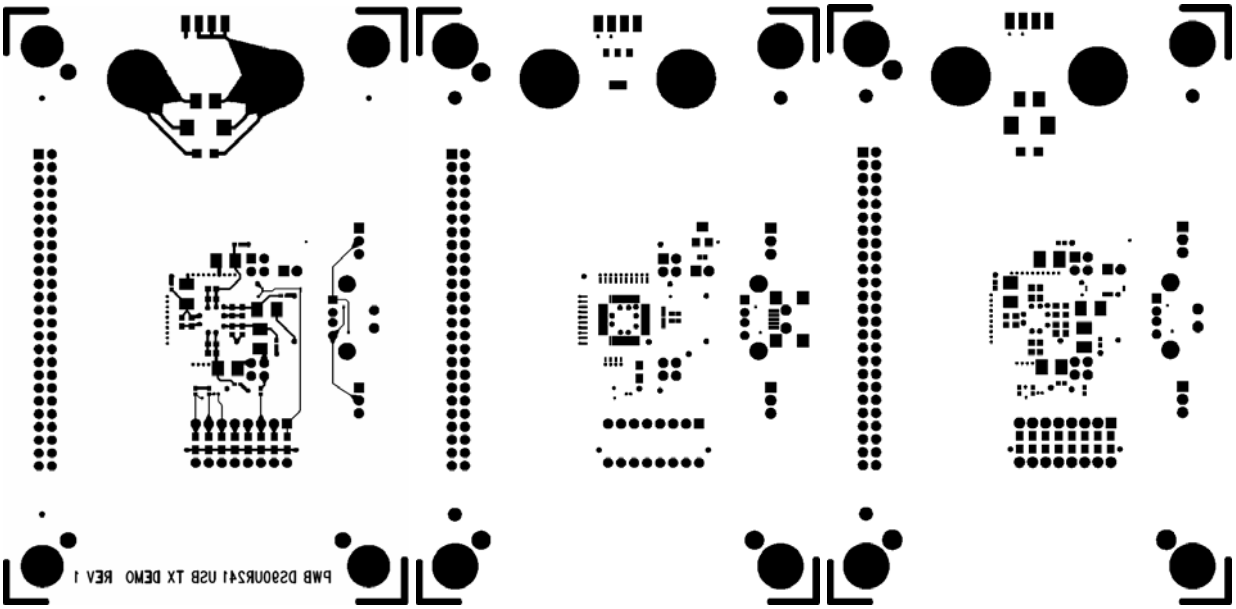
TOP VIEW



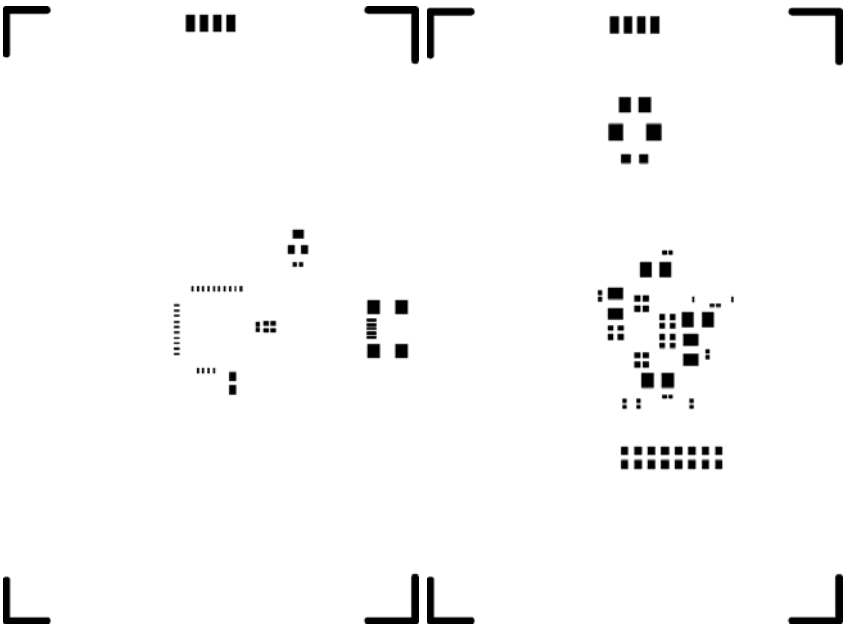
BOTTOMSIDE VIEW



PRIMARY COMPONENT SIDE – LAYER 1 GROUND PLANE (VSS) – LAYER 2 POWER PLANE (VDD) – LAYER 3

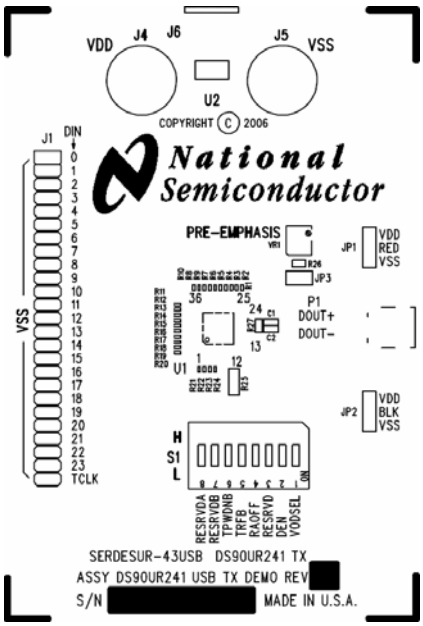


SECONDARY COMP SIDE – LAYER 4 PRIMARY COMP SIDE – SOLDER MASK (LAYER 1) SECONDARY COMP SIDE – SOLDER MASK (LAYER 4)

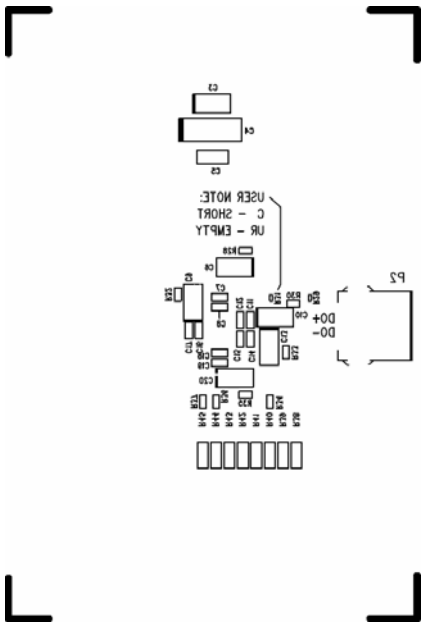


PRIMARY COMP SIDE – SOLDER PASTE (LAYER 1)

SECONDARY COMP SIDE – SOLDER PASTE (LAYER 4)

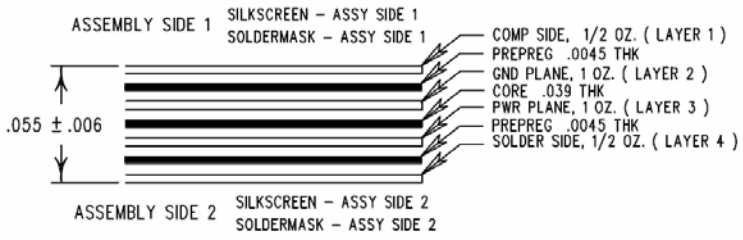


PRIMARY COMP SIDE – SILKSCREEN (LAYER 1)

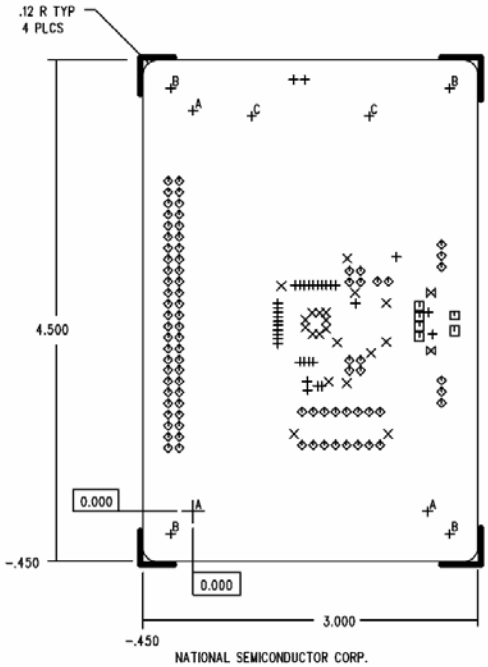


SILKSCREEN COMP SIDE – SILKSCREEN (LAYER 4)

Serializer (Tx) PCB Stackup:



HOLE CHART				
CODE	SIZE	QTY	PLATED	TOL
+	0.006	34	YES	± .003
×	0.014	20	YES	± .003
□	0.036	6	YES	± .003
◇	0.043	82	YES	± .003
⋈	0.091	2	YES	± .003
A	0.125	3	NO	+.003 −.000
B	0.156	4	YES	± .004
C	0.265	2	YES	± .005

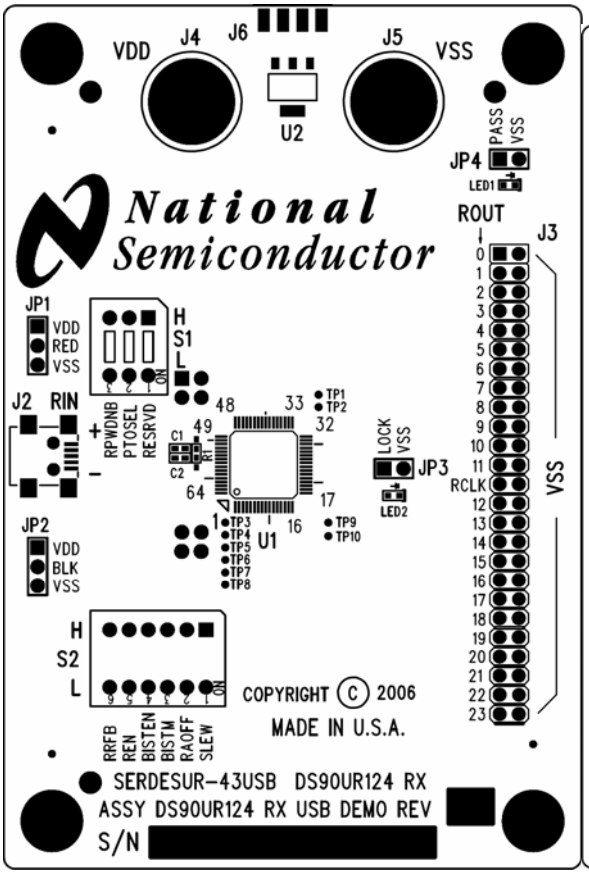


NATIONAL SEMICONDUCTOR CORP.
DS90UR241 USB TX DEMO BOARD
PWB DS90UR241 USB TX DEMO REV 1
DRILL DRAWING

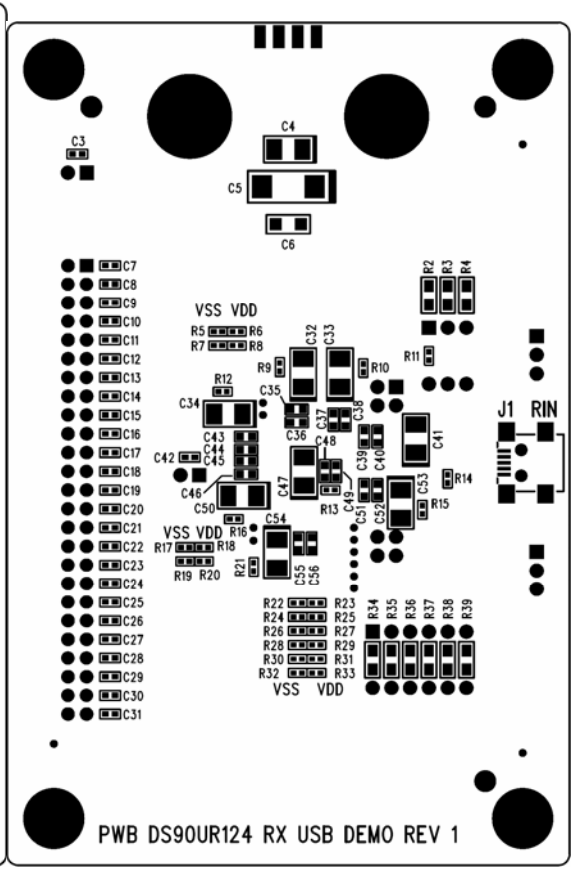
NOTES: UNLESS OTHERWISE SPECIFIED

1. PRIMARY COMPONENT SIDE IS SHOWN.
2. HOLES MARKED " A " ARE TOOLING HOLES, UNPLATED, AND SHALL BE "ONCE" DRILLED.
3. FABRICATE USING MASTER FILM DS90UR241 USB TX DEMO REV 1. USE GERBER FILE A467B0A.PHO FOR BOARD ROUTE.
4. ACCEPTABILITY SHALL BE BASED ON IPC-A-600, CLASS 2
5. MATERIAL: BASE MATERIAL IS NEMAL-1 GRADE FR-406, COLOR GREEN, 0.062 INCH NOM. THICKNESS. COPPER CLADDING SHALL BE 1/2 OZ FOR OUTSIDE LAYERS AND 1 OZ FOR INSIDE LAYERS.
6. PLATING: ALL HOLES AND CONDUCTIVE SURFACES SHALL BE PLATED WITH A MIN. OF .001 INCH COPPER.
   SURFACE FINISH: ELECTROLESS NICKEL IMMERSION GOLD.
7. FABRICATION TOLERANCES:
   END PRODUCT CONDUCTOR WIDTHS AND LAND DIAMETERS SHALL NOT VARY MORE THAN .002 INCH FROM THE 1:1 DIMENSIONS OF THE MASTER PATTERN. THE CONDUCTIVE PATTERN SHALL BE POSITIONED SO THAT THE LOCATION OF ANY LAND SHALL BE WITHIN .010 INCH DIAMETER TO THE TRUE POSITION OF THE HOLE IT CIRCUMSCRIBES THE MINIMUM ANNULAR RING SHALL BE .002 INCH. BOW AND TWIST SHALL NOT EXCEED .010 INCH PER INCH.
8. SOLDERMASK BOTH SIDES PER IPC-SM-840, TYPE A, CLASS B. COLOR-GREEN. THERE SHALL BE NO SOLDERMASK ON ANY LAND.
9. SILKSCREEN THE LEGEND ON BOTH SIDES USING NON CONDUCTIVE EPOXY INK, COLOR-WHITE. THERE SHALL BE NO INK ON ANY LAND.
10. THE .008 TRACES (LAYER 1) TO BE 50 OHM SINGLE ENDED IMPEDANCE THE .007 TRACES (LAYER 1) TO BE 100 OHM DIFFERENTIAL IMPEDANCE, AND THE DIELECTRIC REFERENCED IN BOARD STACK DETAIL IS SUGESTED. HOWEVER, TRACE WIDTHS AND OR DIELECTRIC THICKNESS MAY BE MICRO-MODIFIED IN ORDER TO FABRICATE BOARDS TO THE REQUIRED IMPEDANCE NOMINALS TO A TOLERANCE OF +/- 5%.
11. BOARD TO BE FABRICATED IN COMPLIANCY TO ROHS REQUIREMENTS.

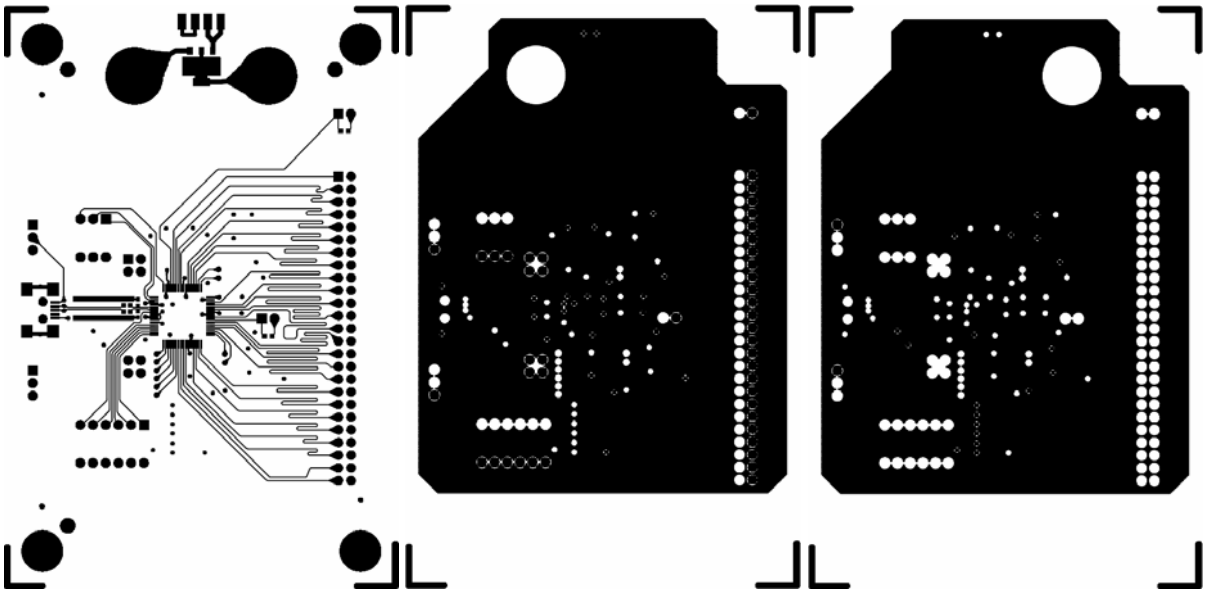
Deserializer (Rx) PCB Layout:



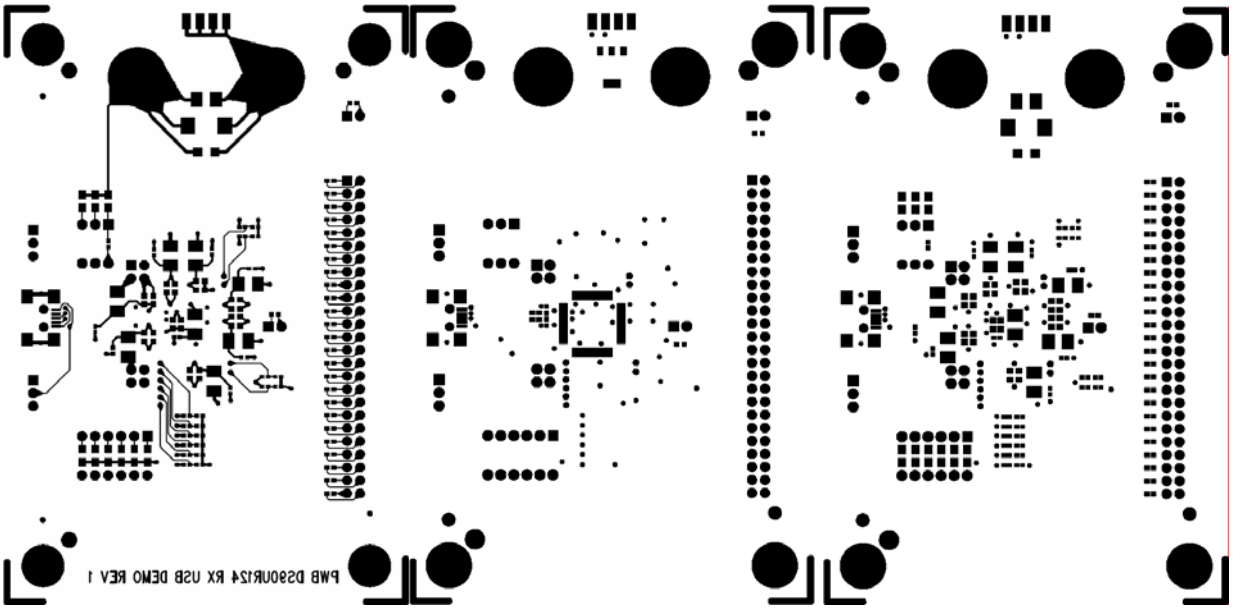
TOP VIEW



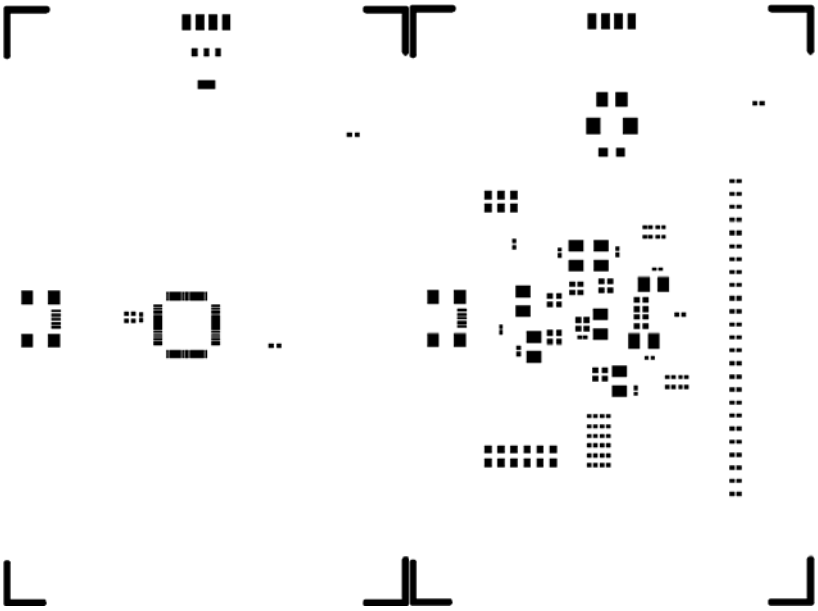
BOTTOMSIDE VIEW



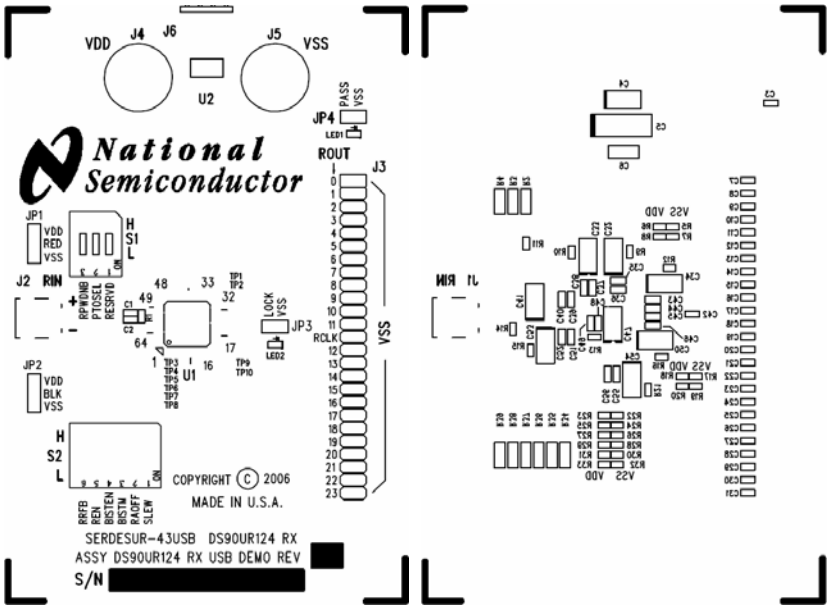
PRIMARY COMPONENT SIDE – LAYER 1 GROUND PLANE (VSS) – LAYER 2 POWER PLANE (VDD) – LAYER 3



SECONDARY COMP SIDE – LAYER 4 PRIMARY COMP SIDE – SOLDER MASK (LAYER 1) SECONDARY COMP SIDE – SOLDER MASK (LAYER 4)

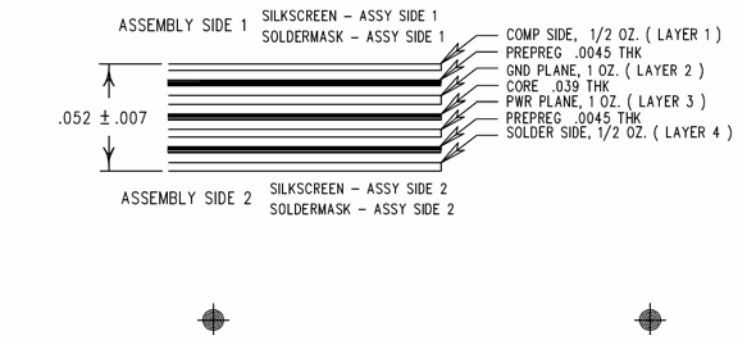


PRIMARY COMP SIDE – SOLDER PASTE (LAYER 1) SECONDARY COMP SIDE – SOLDER PASTE (LAYER 4)

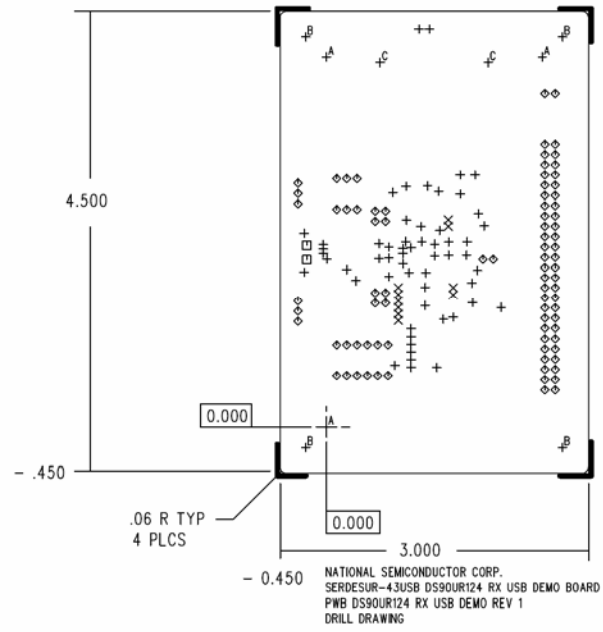


PRIMARY COMP SIDE – SILKSCREEN (LAYER 1) SILKSCREEN COMP SIDE – SILKSCREEN (LAYER 4)

Deserializer (Rx) PCB Stackup:



HOLE CHART				
CODE	SIZE	QTY	PLATED	TOL
+	0.011	57	YES	± .003
×	0.016	10	YES	± .003
□	0.035	2	YES	± .003
◇	0.043	86	YES	± .003
A	0.125	3	NO	+.003 –.000
B	0.156	4	YES	± .005
C	0.265	2	YES	± .005



NOTES: UNLESS OTHERWISE SPECIFIED

1. PRIMARY COMPONENT SIDE IS SHOWN.
2. HOLES MARKED " A " ARE TOOLING HOLES, UNPLATED, AND SHALL BE "ONCE" DRILLED.
3. FABRICATE USING MASTER FILM DS90UR124 RX USB DEMO REV 1. USE BOARD OUTLINE FILE A472B0A.PHO FOR BOARD ROUTE.
4. ACCEPTABILITY SHALL BE BASED ON IPC-A-600, CLASS 2
5. MATERIAL: BASE MATERIAL IS NEMAL-1 GRADE FR-406, COLOR GREEN, 0.052 INCH NOM. THICKNESS. COPPER CLADDING SHALL BE 1/2 OZ. OUTSIDE LAYERS AND 1 OZ INSIDE LAYERS.
6. PLATING: ALL HOLES AND CONDUCTIVE SURFACES SHALL BE PLATED WITH A MIN OF .001 INCH CU. SURFACE FINISH: GOLD FLASH, .000005 MIN.
7. FABRICATION TOLERANCES:
   END PRODUCT CONDUCTOR WIDTHS AND LAND DIAMETERS SHALL NOT VARY MORE THAN .003 INCH FROM THE 1:1 DIMENSIONS OF THE MASTER PATTERN. THE CONDUCTIVE PATTERN SHALL BE POSITIONED SO THAT THE LOCATION OF ANY LAND SHALL BE WITHIN .010 INCH DIAMETER TO THE TRUE POSITION OF THE HOLE IT CIRCUMSCRIBES THE MINIMUM ANNULAR RING SHALL BE .002 INCH. BOW AND TWIST SHALL NOT EXCEED .010 INCH PER INCH.
8. SOLDERMASK BOTH SIDES PER IPC-SM-840, TYPE A, CLASS B. COLOR-GREEN. THERE SHALL BE NO SOLDERMASK ON ANY LAND.
9. SILKSCREEN THE LEGEND ON BOTH SIDES USING NON CONDUCTIVE EPOXY INK, COLOR-WHITE. THERE SHALL BE NO INK ON ANY LAND.
10. THE .008 (LAYER 1) TRACES TO BE 50 OHM SINGLE ENDED IMPEDANCE AND THE .007 TRACES (LAYER 1) TO BE 100 OHM DIFFERENTIAL IMPEDANCE AND THE DIELECTRIC REFERENCED IN BOARD STACK DETAIL IS SUGGESTED. HOWEVER, TRACE WIDTHS AND OR DIELECTRIC THICKNESS MAY BE MICRO-MODIFIED IN ORDER TO FABRICATE BOARDS TO THE REQUIRED IMPEDANCE NOMINALS TO A TOLERANCE OF +/– 5%.
11. BOARD TO BE FABRICATED IN COMPLIANCY TO ROHS REQUIREMENTS.

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