LMK00105 User's Guide

LIST OF FIGURES

LIST OF TABLES

1. Introduction

This user guide describes how to set up and operate the LMK00105 evaluation board kit (EVK). The LMK00105 is a high performance, low noise, low voltage CMOS fanout buffer. The core voltage can be 2.5 or 3.3 volts, while the power supply for the outputs can be selected from: 1.5 V, 1.8 V, 2.5 V, or 3.3 V, provided that it does not exceed the core supply voltage.

Table 1: Part Description

BUFFER	IC	PACKAGE
U1	LMK00105	LLP-24

2. Quick Start

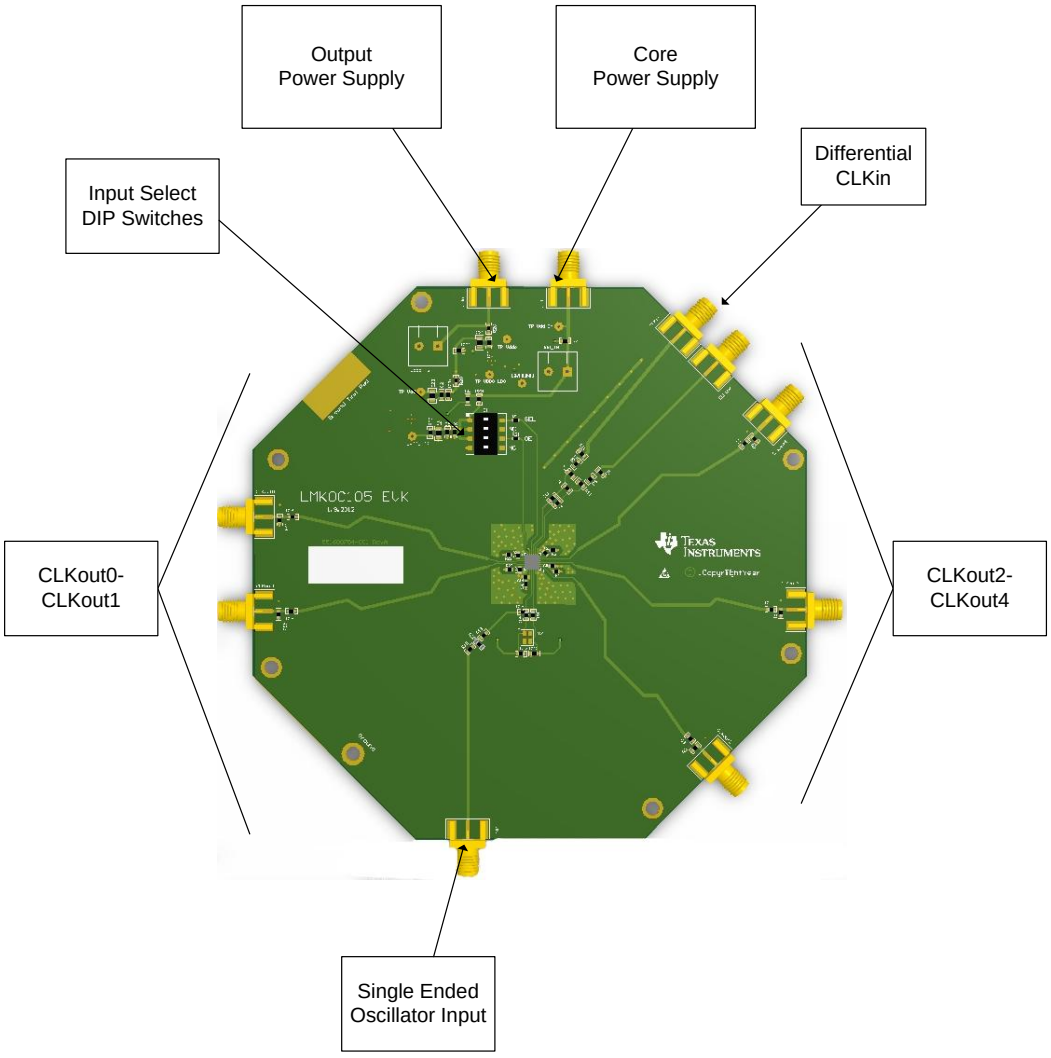

Figure 1: LMK00105 Quick Start Setup

2.1 Quick Start Description

The LMK00105 EVK allows full verification of the device functionality and performance specifications. To quickly set up and operate the board with basic equipment, refer to the quick start procedure below and test setup shown in Figure 1.

1. Verify the output mode control switches, S1[1:4], match the states shown in Table 2 to reflect the default output clock interfaces configured on the EVK.

Table 2: Default Clock Output Modes / Interfaces

SW Position/Name	SW State
S1[1] / SEL	0 (OFF)
S1[2] / NC	Unused
S1[3] / OE	1 (OFF)
S1[4] / NC	Unused

2. Connect the Vdd SMA from the board to a 3.3 V source. This powers the core portions of the LMK00105.
3. Connect the Vddo SMA from the board to a 3.3 V source. This powers the output drivers of the LMK00105
4. Set the desired clock input using the input selection control switches, S1[1], per Table 3. A differential clock source can be connected to SMAs **CLKin/CLKin***.

Table 3. Input Selection (0=SW OFF, 1=SW ON)

Selected Input	Default Input Mode	S1 CLKin_Sel State
CLKin/CLKin*	Differential clock	0
OSCin	Select OSCin	1

Note: CLKin path is configured by default to receive a differential clock as the input. The SMA input is AC coupled to the device inputs and terminated with 100 ohms differential. Refer to the Clock Inputs section to configure the EVK for a single-ended input.

5. Connect and measure any clock output SMA labeled **CLKoutX** to an oscilloscope or other test instrument using SMA cable(s). The output clock will be level-translated/buffered copy of the selected clock input or crystal oscillator. Note: All output clocks are AC-coupled to the SMA connectors to ensure safe use with RF instruments.

Note: Switching noise from one or more un-terminated outputs may impair the signal quality of the measured output(s). To minimize switching noise and EMI, properly terminate any unused output path using an SMA load or the component options near the SMA outputs, or alternatively, remove the 0-ohm series resistor nearest the unused output pin.

3. Signal Path and Control Switches

The LMK00105 supports single-ended or differential clocks on CLKin. A second input, OSCin, has an integrated crystal oscillator interface that supports a fundamental mode, AT-cut crystal or an external single-

ended clock. The two-input multiplexer is pin-controlled. To achieve the maximum operating frequency and lowest additive jitter, it is recommended to use a differential clock with high input slew rate (>1 V/ns) and DC-coupling to the CLKin port.

All control pins are configured with the control switch, S3. The output enable logic is shown in Table 4: Output Enable Selection (0=OFF, 1=ON).

Table 4: Output Enable Selection (0=OFF, 1=ON)

CLKout Enable Mode	S1[3] - OE
Disabled/Hi-Z	0
Enabled	1

4. Power Supplies

By default, Vdd and Vddo are supplied by two external power supplies. To modify the EVK with a different power supply configuration, populate the resistor options as shown in Table 5. Then, apply the appropriate voltage(s) to the EVK power input(s).

Decoupling capacitors and 0-ohm resistor footprints, which can accommodate ferrite beads, can be used to isolate the EVK power input(s) from the device power pins. Do not disconnect or ground any of the Vddo pins as they are all internally connected inside the device.

Table 5: Power Supply Configuration

	Dual Ext. Inputs (Default)	Single Ext. Input 3.3 V
Vdd input	Apply 3.3 V	Apply 3.3 V
Vddo input	Apply Voltage ≤ Vdd	Not used
R26	0 Ohm	DNP
R28	DNP	0 Ohm
R29	0 Ohm	0 Ohm

5. Clock Inputs

The SMA inputs labeled **CLKin** & **CLKin*** are configured to receive a differential clock or single-ended clock. Best performance is achieved with a DC-coupled differential input clock. To configure CLKin for a single-ended clock remove R8. Then either CLKin or CLKin* may be driven single ended.

5.1 Crystal Oscillator Interface

The LMK00105 has an integrated crystal oscillator interface (OSCin/OSCout) that supports a fundamental mode, AT-cut crystal. If the crystal input is selected, an optional onboard XTAL on either footprint Y1 or Y2 will start-up and the oscillator clock can be measured on any enabled output.

An XTAL with the HC49 footprint can be populated on the bottom side of the PCB. Alternatively, a 3.2 x 2.5 mm XTAL can be populated on Y2, located on the top side. Only one XTAL footprint should be used at a time.

The values of C12 and C10 (C_{EXT}) depend on the load capacitance (C_L) specified for the crystal. The OSC input capacitance (C_{IN}) of the device is 1 pF differential, and the trace capacitance (C_{TRACE}) of OSCin and OSCout is around 1 pF. If the selected crystal is specified for C_L of 18 pF, the C_{EXT} is calculated as follows:

$C_{EXT} = (C_L – C_{IN} – C_{TRACE}/2) * 2$
$C_{EXT} = (18\ pF – 1\ pF – 1\ pF/2) * 2$
$C_{EXT} = 33\ pF$

5.2 Configuring OSCin for a Crystal Mode

To configure the board to use crystal mode remove C15 to disconnect the OSCin Port. Install 0 Ohm resistors on R14 and R9. Install a crystal in either footprint (Y1 or Y2) and install the proper load capacitors in C10 and C12.

6. Clock Outputs

All clock outputs are LVCMOS. In the case that not all outputs are used, any unused outputs should be left floating.

7 Schematics

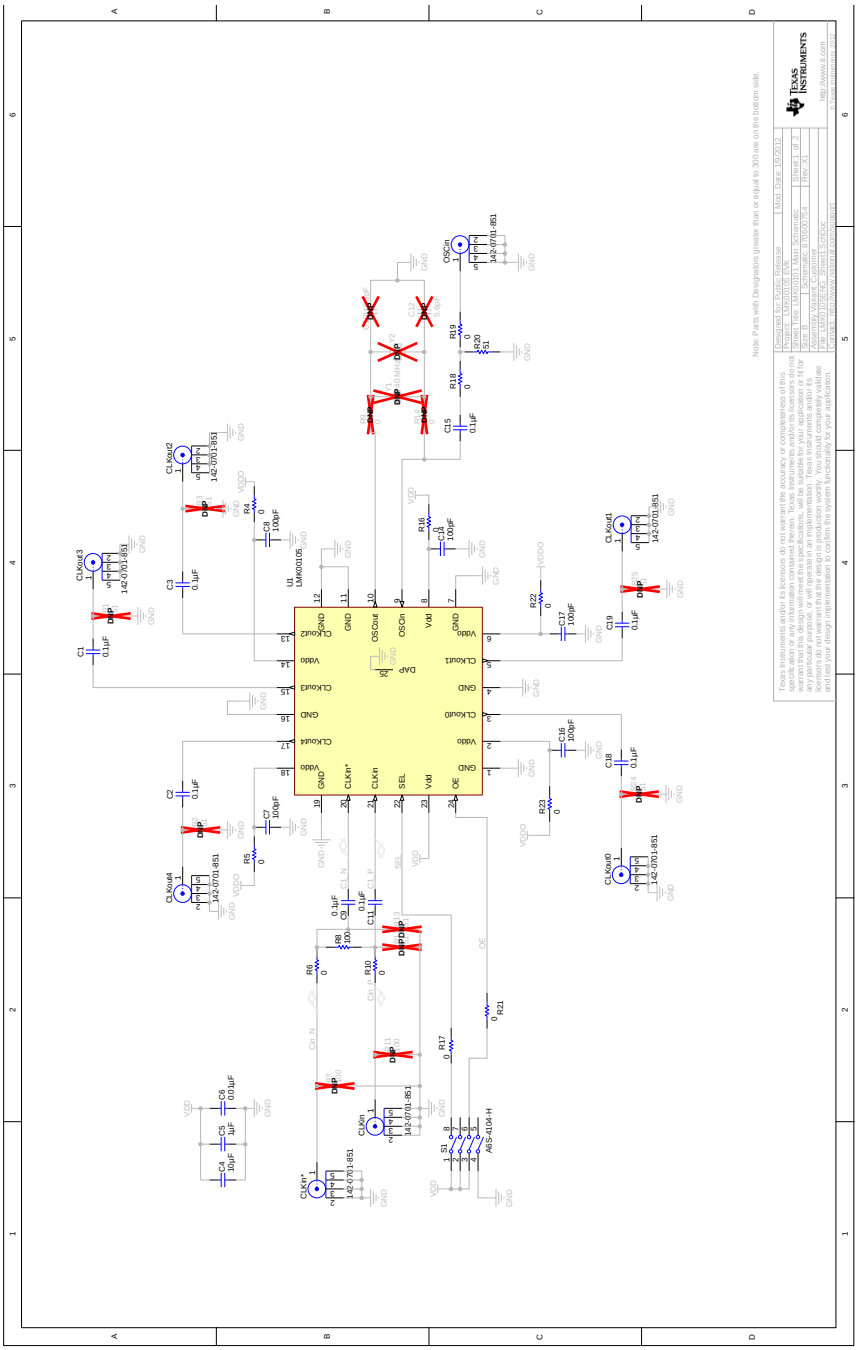

Figure 2: Schematic Sheet 1

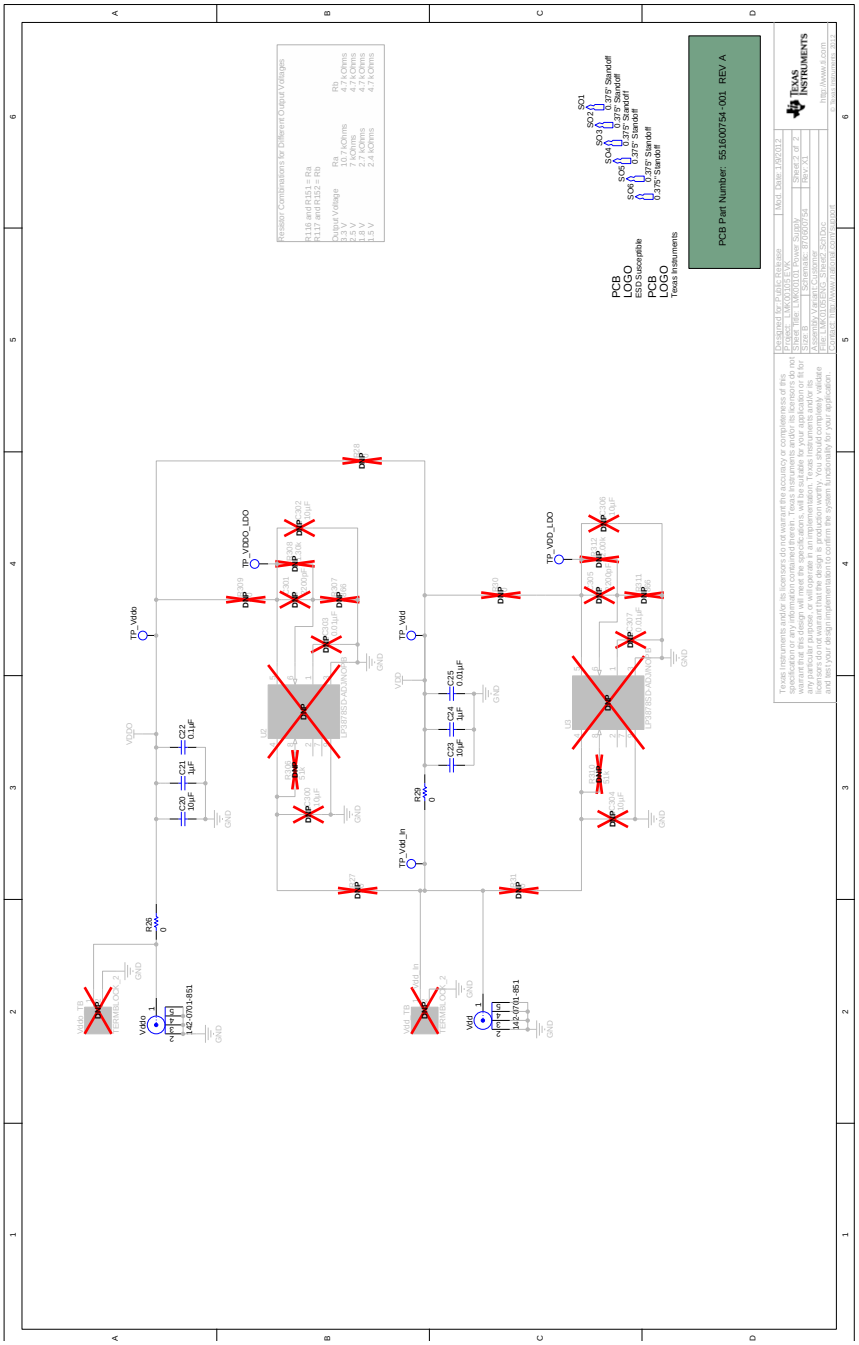

Figure 3: Schematic Sheet 2

7 PCB Layout

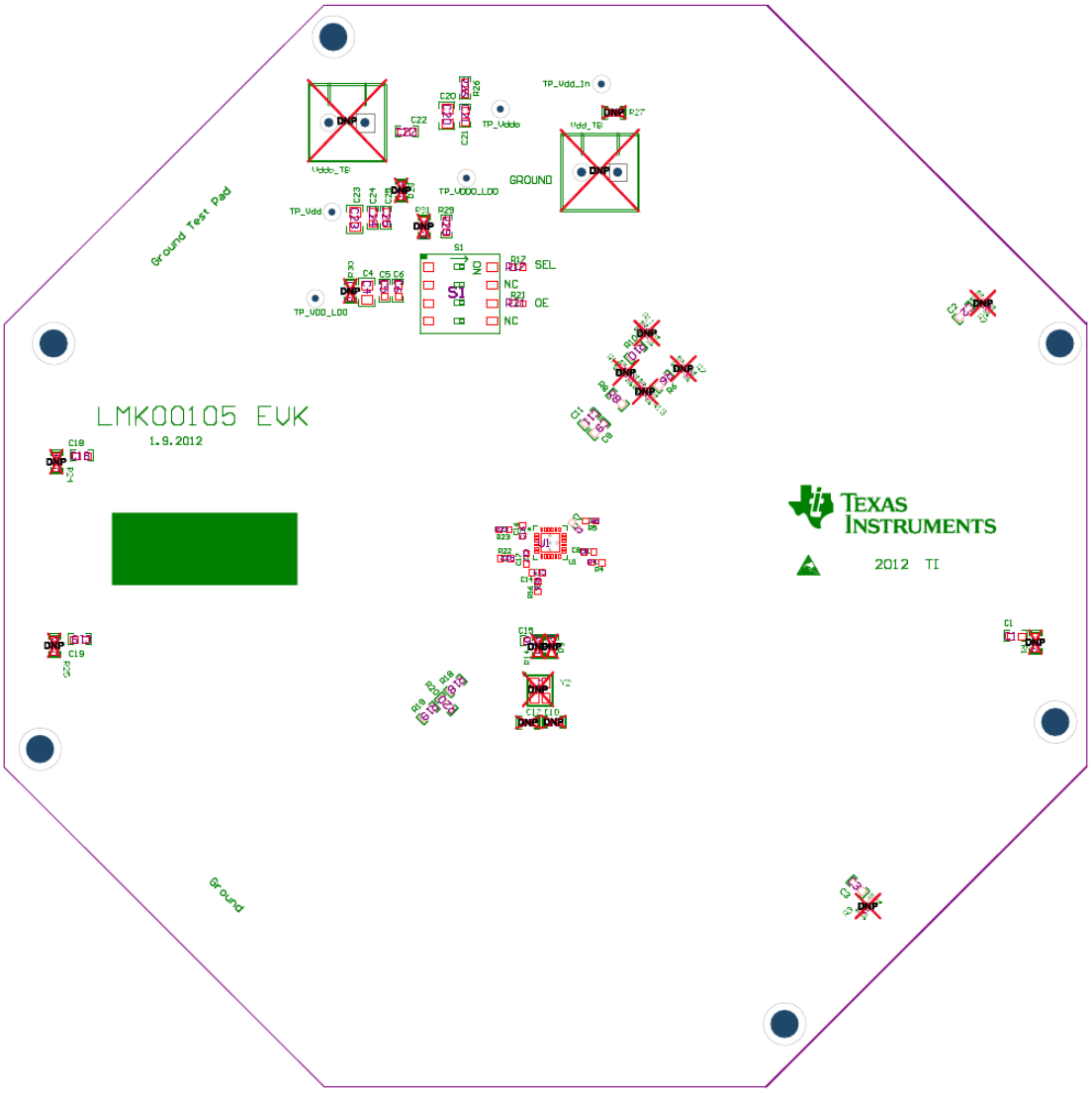

Figure 4: PCB Top

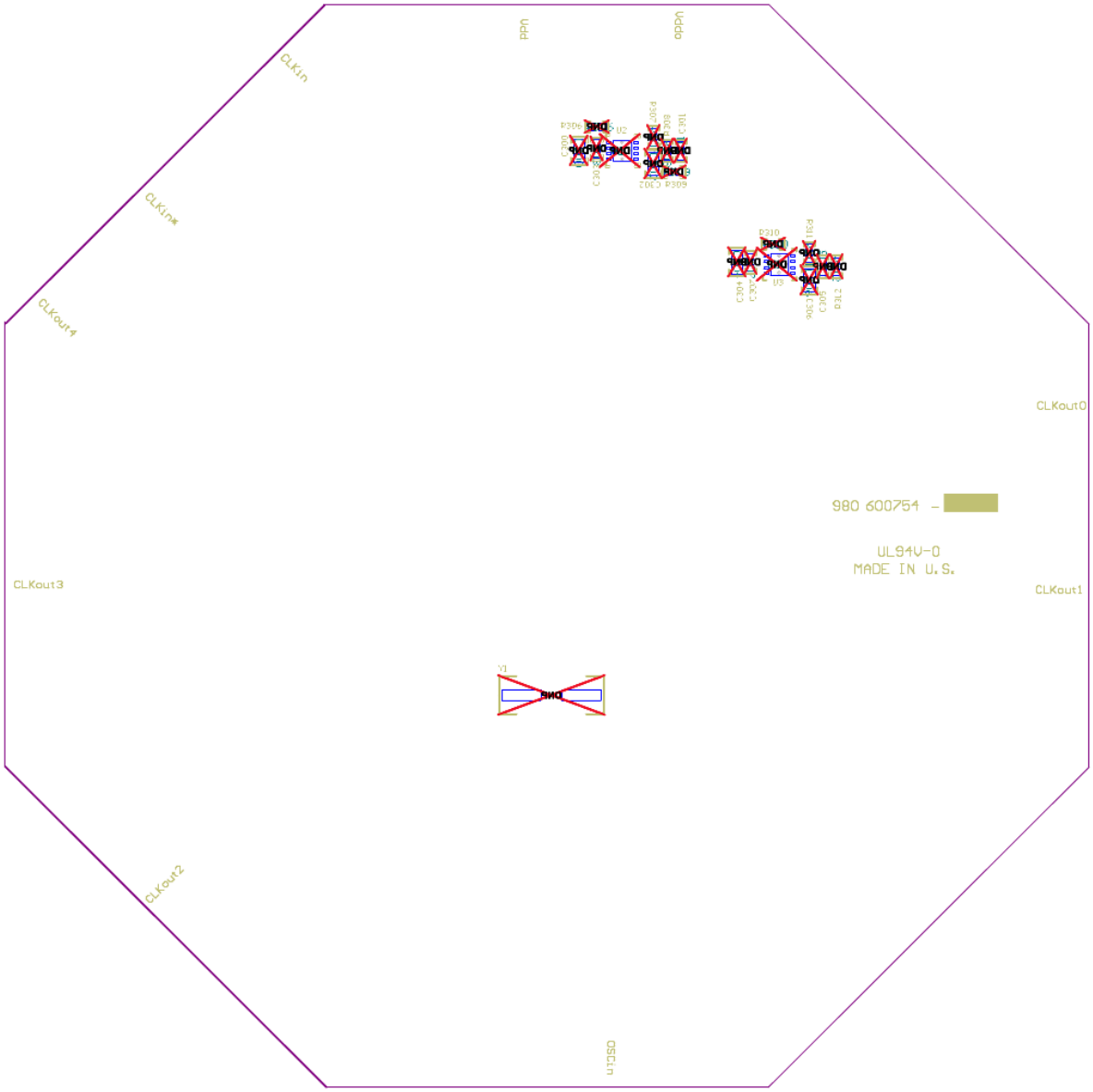

Figure 5: Bottom Side (Layer Inverted, Not to Scale)

8 Bill of Materials

Table 6: Bill of Materials

Item	Description	Qty	Designator	Manufacturer
1	Printed Circuit Board	1		
2	CAP, CERM, 0.1uF, 16V, +/-10%, X7R, 0603	8	C1, C2, C3, C9, C11, C15, C18, C19	TDK
3	CAP, CERM, 10uF, 10V, +/-10%, X5R, 0805	3	C4, C20, C23	MuRata
4	CAP, CERM, 1uF, 16V, +/-10%, X7R, 0603	3	C5, C21, C24	TDK
5	CAP, CERM, 0.01uF, 100V, +/-5%, X7R, 0603	2	C6, C25	Kemet
6	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603	5	C7, C8, C14, C16, C17	AVX
7	CAP, CERM, 0.1uF, 16V, +80/-20%, Y5V, 0603	1	C22	TDK
8	Connector, SMT, End launch SMA 50 ohm	10	CLKin, CLKin*, CLKout0, CLKout1, CLKout2, CLKout3, CLKout4, OSCin, Vdd, Vddo	Emerson Network Power Connectivity
9	RES, 0 ohm, 5%, 0.1W, 0603	13	R4, R5, R6, R10, R16, R17, R18, R19, R21, R22, R23, R26, R29	Vishay-Dale
10	RES, 100 ohm, 5%, 0.1W, 0603	1	R8	Vishay-Dale
11	RES, 51 ohm, 5%, 0.1W, 0603	1	R20	Vishay-Dale
12	DIP Switch, 4 position slide actuatoor, SPST, SMD	1	S1	Omron Electronic Components
13	0.375" Standoff	6	SO1, SO2, SO3, SO4, SO5, SO6	
14	Testpoint	NA	TP_Vdd, TP_Vdd_In, TP_VDD_LDO, TP_Vddo, TP_VDDO_LDO	NA
15	LMK00105	1	U1	Texas Instruments
16	CAP, CERM, 5.6pF, 50V, +/-5%, C0G/NP0, 0603	0	C10, C12	AVX
17	CAP, CERM, 10uF, 10V, +/-10%, X5R, 0805	0	C300, C302, C304, C306	MuRata
18	CAP, CERM, 2200pF, 100V, +/-5%, X7R, 0603	0	C301, C305	AVX
19	CAP, CERM, 0.01uF, 25V, +/-5%, C0G/NP0, 0603	0	C303, C307	TDK
20	RES, 51 ohm, 5%, 0.1W, 0603	0	R1, R2, R3, R12, R13, R24, R25	Vishay-Dale
21	RES, 100 ohm, 5%, 0.1W, 0603	0	R7, R11	Vishay-Dale
22	RES, 0 ohm, 5%, 0.1W, 0603	0	R9, R14, R27, R28, R30, R31, R309	Vishay-Dale

23	RES, 51k ohm, 5%, 0.1W, 0603	0	R306, R310	Vishay-Dale
24	RES, 866 ohm, 1%, 0.1W, 0603	0	R307, R311	Vishay-Dale
25	RES, 1.30k ohm, 1%, 0.1W, 0603	0	R308	Vishay-Dale
26	RES, 2.00k ohm, 1%, 0.1W, 0603	0	R312	Vishay-Dale
27	Micropower 800mA Low Noise "Ceramic Stable" Adjustable Voltage Regulator for 1V to 5V Applications, 8-pin LLP, Pb-Free	0	U2, U3	Texas Instruments
28	Crystal, xxxMHz, xxpF	0	Y1	
29	Crystal, Citizen CS325, 52 MHz	0	Y2	Citizen

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- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
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~

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Logic	logic.ti.com	Military	www.ti.com/military
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