DS90UR905 Serializer and DS90UR906 Deserializer Evaluation Kit

User's Manual

NSID: SERDESUR-65USB

Rev 0.4

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Introduction:

The demo boards are not intended for EMI testing. The demo boards were designed for easy accessibility to device pins with tap points for monitoring or applying signals, additional pads for termination, and multiple connector options.

National Semiconductor's Flat Panel Displays DS90UR905/906 FPD-LINKII evaluation kit contains one (1) DS90UR905 Serializer (Tx) board, one (1) DS90UR906 De-serializer (Rx) board, and one (1) two (2) meter* high speed USB 2.0 cable. **Note: the chipset can support up to ten (10) meters.*

The DS90UR905/906 chipset supports a variety of 8 bit color display applications on a two (2) wire serial stream. The single LVDS (FPD_LINKII) interface is well-suited for any display system interface. Typical applications include: navigation displays, automated teller machines (ATMs), POS, video cameras, global positioning systems (GPS), portable equipment/instruments, factory automation, etc.

The DS90UR905 and DS90UR906 can also be used as a 24-bit general purpose LVDS Serializer and De-serializer chipset designed to transmit data at clocks speeds ranging from 20 to 65 MHz at up to 10 meters cable lengths over -40 to +105 Deg C.

The Serializer board accepts 1.8V/3.3V input signals. FPD-LINKII Serializer converts the 1.8V/3.3V LVCMOS parallel lines into a single serialized LVDS data pair with an embedded LVDS clock. The serial data stream toggles at 28 times the base clock rate. With an input clock at 65 MHz, the transmission line rate for the FPD-LINKII is 1.56Gbps (24 data bits x 65MHz).

The De-serializer board accepts FPD-LINKII serialized data stream with embedded clock and converts the data back into parallel 1.8V/3.3V LVCMOS signals and clock. Note that NO external reference clock is needed to prevent harmonic lock as with other devices currently on the market. An added feature on this chipset is when the PCLK from the transmitter is lost; an internally generated 25MHz +/- 20% PCLK is outputted on the receiver clock output. This feature can be turned off if not needed.

Suggested equipment to evaluate the chipset, a 1.8V/3.3V LVCMOS signal source such as a video generator or word generator or pulse generator and oscilloscope with a bandwidth of at least 65 MHz will be needed.

The user needs to provide the proper 1.8V/3.3V LVCMOS/RGB inputs and 1.8V/3.3V LVCMOS clock to the Serializer and also provide a proper interface from the De-serializer output to an LCD panel or test equipment. The Serializer and De-serializer boards can also be used to evaluate device parameters. A cable conversion board or harness scramble may be necessary depending on type of cable/connector interface used on the input to the DS90UR905 and to the output of the DS90UR906.

Example of suggested display setup:

1) video generator with 1.8V/3.3V output
2) 24-bit LCD panel with a 1.8V/3.3V LVCMOS input interface.

Contents of the Demo Evaluation Kit:

1) One Serializer board with the DS90UR905
2) One De-serializer board with the DS90UR906
3) One 2-meter high speed USB 2.0 cable (4-pin USB A to 5-pin mini USB)
4) Evaluation Kit Documentation (this manual)
5) DS90UR905/906 Datasheet

DS90UR905/906 SERDES Typical Application:

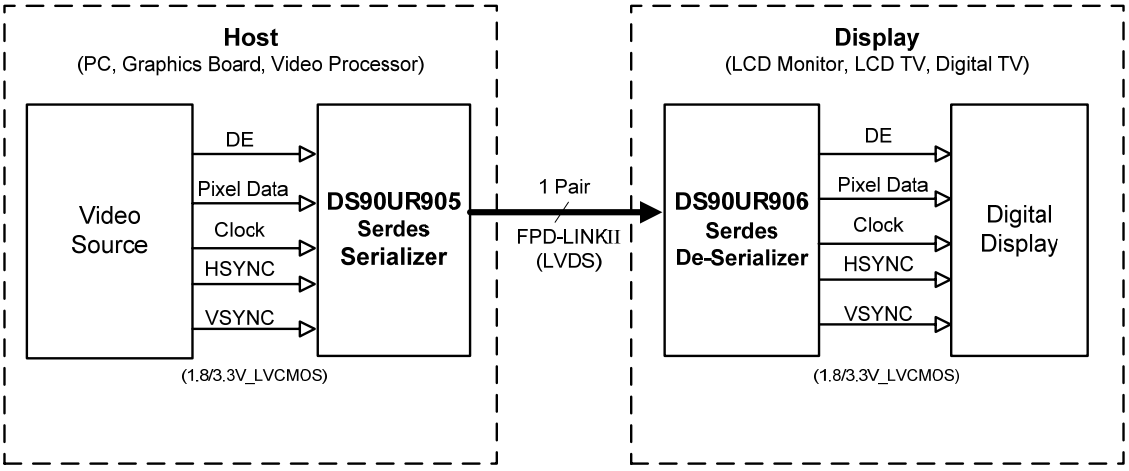


Figure 1a. Typical Application (24-bit RGB Color)

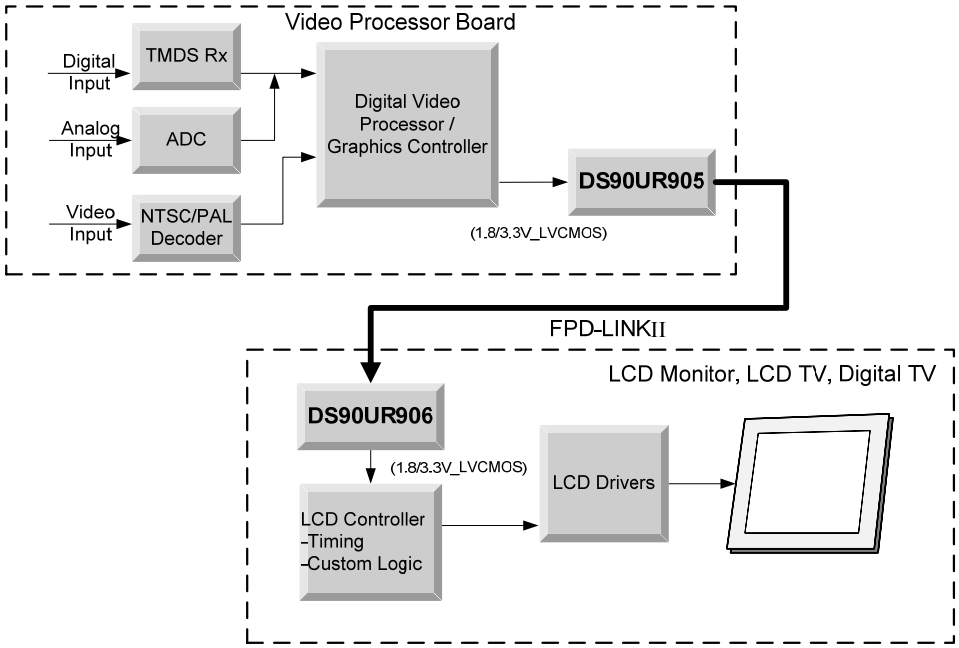


Figure 1b. Typical DS90UR905/906 SERDES System Diagram

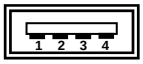
Figures 1a and 1b illustrate the use of the Chipset (Tx/Rx) in a Host to Flat Panel Interface.

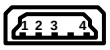
The chipsets support up to 24-bit color depth TFT LCD Panels.

Refer to the proper datasheet information on Chipsets (Tx/Rx) provided on each board for more detailed information.

How to set up the Demo Evaluation Kit:

The PCB routing for the Tx input pins (DIN) have been lay out to accept incoming 1.8V/3.3V LVCMOS signals from 2x25-pin IDC connector. The TxOUT/RxIN (DOUT/RIN) interface uses a single twisted pair cable (provided). The PCB routing for the Rx output pins (ROUT) are accessed through a 2x25-pin IDC connector. Please follow these steps to set up the evaluation kit for bench testing and performance measurements:

1) A two (2) meter high speed USB 2.0 cable has been included in the kit. Connect the 4-pin USB A 

A side of cable harness to the serializer board and the otherside of the harness, the 5-pin mini USB jack 

MINI to the de-serializer board. This completes the FPD-LINKII interface connection.
NOTE: The DS90UR905 and DS90UR906 are NOT USB compliant and should not be plugged into a USB device nor should a USB device be plugged into the demo boards.

2) Jumpers and switches have been configured at the factory; they should not require any changes for immediate operation of the chipset. See text on Configuration settings and datasheet for more details.

3) From the Video Decoder board, connect a flat cable (not supplied) to the Serializer board and connect another flat cable (not supplied) from the De-serializer board to the panel. *Note: For 50 ohm signal sources, provide 1.8V/3.3V LVCMOS input signal levels into DIN[23:0] and TCLK and add 50 ohm parallel termination resistors R1-R25 on the DS90UR905 Serializer board.*

4) Power for the Tx and Rx boards must be supplied externally through Power Jack (VDD). Grounds for both boards are connected through Power Jack (VSS) (see section below).

Demo Board Power Connections:

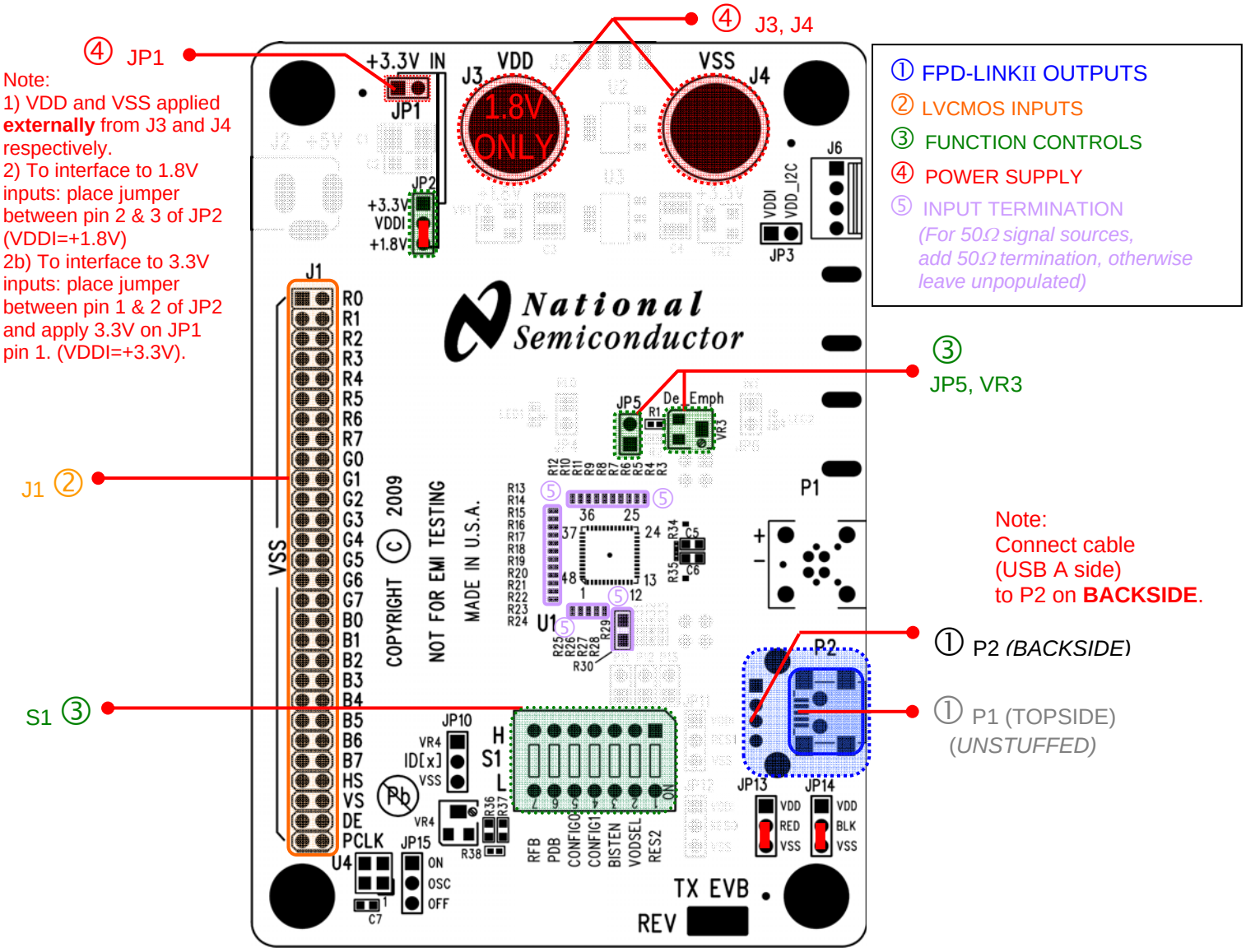
The Serializer and De-serializer boards must be powered by supplying power externally through J4 (VDD) and J5 (VSS) on Serializer Board and J4 (VDD) and J5 (VSS) on De-serializer board. Note +2.5V is the MAXIMUM voltage that should ever be applied to the Serializer (DS90UR905) or De-serializer (DS90UR906) VDD terminal (except on VDDI or VDDIO where the absolute maximum is +4.0V). Damage to the device(s) can result if the voltage maximum is exceeded.

DS90UR905 Tx Serializer Board Description:

The 2x25-pin IDC connector J1 accepts 24 bits of 1.8V or 3.3V RGB data along with the clock input. VDDI must be set externally for 1.8V or 3.3V LVCMOS inputs.

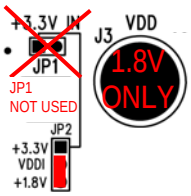
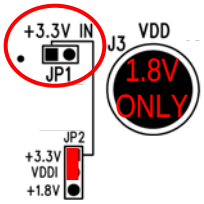
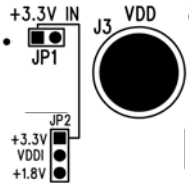
The Serializer board is powered externally from the J4 (VDD) and J5 (VSS) connectors shown below. For the Serializer to be operational, the S1-PDB switch on S1 must be set HIGH. S1- CONFIG0, CONFIG1, and BISTEN must be set LOW. Rising or falling edge reference clock is user selected on S1-RFB: HIGH (for rising edge data latching) or LOW (for falling edge data latching).

The USB connector P2 (USB-A side) on the bottom side of the board provides the interface connection to the LVDS signals to the De-serializer board. Note: P1 (mini USB) on the top side is un-stuffed and not to be used with the cable provided in the kit.

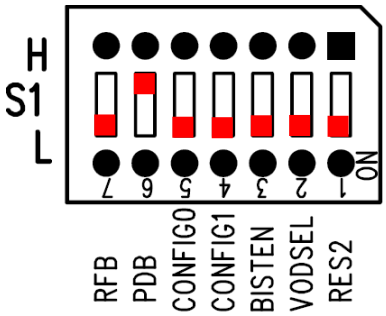


Configuration Settings for the Tx Demo Board

VDDI: 1.8V or 3.3V LVCMOS INPUT SELECTION

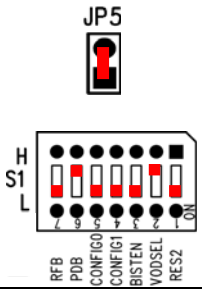
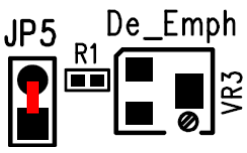
Reference	Description			
JP2	VDDI LVCMOS input configuration.	**VDDI = 1.8V (Default)**  1.8V LVCMOS inputs	**VDDI = 3.3V** apply external  3.3V LVCMOS inputs	

S1: Serializer Input Features Selection

Reference	Description	Input = L	Input = H	S1
RFB	Latch input data on **R**ising or **F**alling edge of TCLK	Falling Edge **(Default)**	Rising Edge	
PDB	**P**ower**D**own **B**ar	Powers Down	Operational **(Default)**	
CONFIG0 (* IMPORTANT See user note below)	See datasheet Table 2 for description of features	MUST be tied low for normal operation **(Default)**	-	
CONFIG1 (* IMPORTANT See user note below)	See datasheet Table 2 for description of features	MUST be tied low for normal operation **(Default)**	-	
BISTEN	**BIST EN**able See datasheet Table 2 for description	OFF **(Default)**	ON	
VODSEL	FPD-LINKII output **VOD SEL**ect	low **(Default)**	high	
RES 2 (* IMPORTANT See user note below)	**RES**erved	MUST be tied low for normal operation **(Default)**		

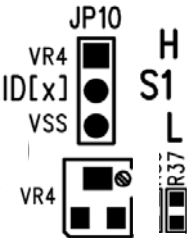
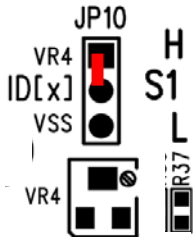
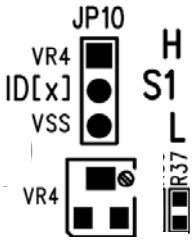
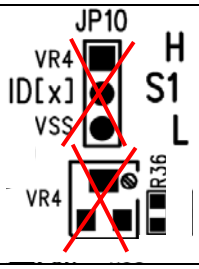
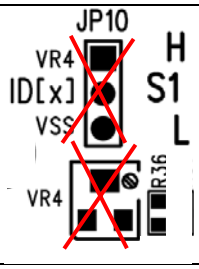
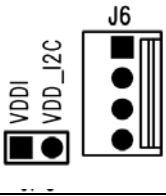
*Note:
In user layout CONFIG0 (pin 12), CONFIG1 (pin 13), RES 2 (pin 18) **MUST** be tied low for proper operation.

JP5,VR3: De-Emphasis Feature Selection

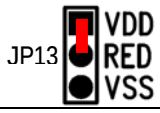
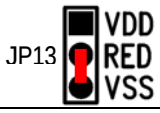
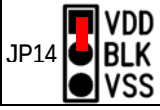
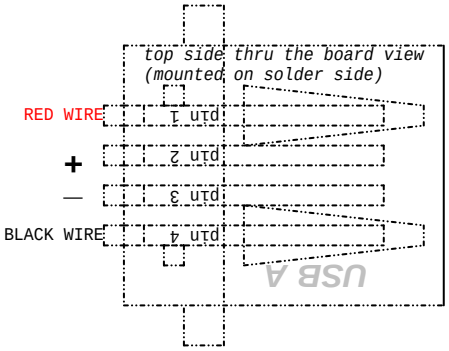
Reference	Description	OPEN (floating)	CLOSED (Path to GND)	
JP5	De-Emphasis Note, when using DeEmphasis, it is recommended that VODSEL = HIGH	Disabled – no jumper **(Default)** 	Enabled – With jumper 	
JP5 & VR3	De-Emphasis adjustment (via screw) JP3 **MUST** have a jumper to use VR3 potentiometer. VR3 = 0Ω to 20KΩ, R1 = 1.5KΩ, R1 + VR3 = 1.5KΩ (maximum DeEmph) to 21.5KΩ (minimum DeEmph). $I_{PRE} = [1.2/(R_{DeEmph})] \times 20$, $R_{DeEmph\ (minimum)} \geq 3K\Omega$ Note: There is no maximum R_{DeEmph} value limitation	Clockwise  increases R_{PRE} value which decreases De-emphasis	Counter-Clockwise  decreases R_{PRE} value which increases De-emphasis	

De-emphasis user note:
De-emphasis must be adjusted correctly based on application frequency, cable quality, cable length, and connector quality. Maximum De-emphasis should only be used under extreme worse case conditions; for example at the upper frequency specification of the part and/or low grade cables at maximum cable lengths. Typically all that is needed is minimum De-emphasis. Users should start with no De-emphasis first and gradually apply De-emphasis until there is clock lock and no data errors. The best way to monitor the De-emphasis effect is to hook up a differential probe to RIN+ and RIN- on the DS90UR906 Rx demo. The easiest tap point is pin2 of C1 and pin 2 of C2. The reason for monitoring RIN+/- on the Rx side is because you want to see what the receiver will see the attenuation signal AFTER the cable/connector.

ID[x]J6,JP3: I2C like register programmable interface

Reference	Description	ID[x]=OPEN (floating)	ID[x]	ID[x]
ID[x]	ID[x] I2C address	ID[x] = h'EC 	See RID 	
RID thru VR4	JP10 must have jumper between pin 1 and pin 2 to use VR4 RID value thru VR4 VR4 = 470Ω; ID[x]=h'E2 VR4 = 2.7KΩ; ID[x]=h'E4 VR4 = 8.2KΩ; ID[x]=h'E6		Counter clockwise decreases RID value:  Clockwise increases RID value 	
RID thru external resistor	No jumper on JP10 			
RID	RID value thru VR4 VR4 = 470Ω; ID[x]=h'E2 VR4 = 2.7KΩ; ID[x]=h'E4 VR4 = 8.2KΩ; ID[x]=h'E6	Clockwise  increases RID value	Counter-Clockwise  decreases RID value	
De-emphasis				

JP13, JP14: USB Red and Black wire

Reference	Description	VDD	VSS	OPEN
JP13	Power wire in USB cable thru P2 *(and P3, not mounted)* connector Jumper RED to VSS – recommended	Red wire tied to VDD 	Red wire tied to VSS **(Default)** 	Red wire floating (not recommended) 
JP14	Power wire in USB cable thru P2 *(and P3, not mounted)* connector Jumper BLACK to VSS – recommended	Black wire tied to VDD 	Black wire tied to VSS **(Default)** 	Black wire floating (not recommended) 
 **P2**				

Tx LVCMOS and LVDS Pinout by Connector

The following three tables illustrate how the Tx inputs are mapped to the IDC connector J1, the LVDS outputs on the USB-A connector P3, and the mini USB P2 (not mounted) pinouts. Note – labels are also printed on the demo boards for both the LVCMOS input and LVDS outputs.

J1
LVCMOS INPUT

pin no.	name	name	pin no.
1	GND	**R0**	2
3	GND	**R1**	4
5	GND	**R2**	6
7	GND	**R3**	8
9	GND	**R4**	10
11	GND	**R5**	12
13	GND	**R6**	14
15	GND	**R7**	16
17	GND	**G0**	18
19	GND	**G1**	20
21	GND	**G2**	22
23	GND	**G3**	24
25	GND	**G4**	26
27	GND	**G5**	28
29	GND	**G6**	30
31	GND	**G7**	32
33	GND	**B0**	34
35	GND	**B1**	36
37	GND	**B2**	38
39	GND	**B3**	40
41	GND	**B4**	42
43	GND	**B5**	44
45	GND	**B6**	46
47	GND	**B7**	48
49	GND	**HS**	50
51	GND	**VS**	52
53	GND	**DE**	54
55	GND	**PCLK**	56

P3
(bottom side)
FPD-LinkII
OUTPUT

pin no.	name
1	JP13
2	**DOUT+**
3	**DOUT-**
4	JP14

P2
(topside)

(not mounted)
FPD-LinkII
OUTPUT

pin no.	*name*
5	*JP14*
4	*NC*
3	***DOUT-***
2	***DOUT+***
1	*JP13*

BOM (Bill of Materials) Serializer Demo PCB:

DS90UR905 Tx Demo Board - Board Stackup Revised: Thursday, June 18, 2009

DS90UR905 Tx Demo Board Revision: 2

Bill Of Materials July 16,2009 19:47:16

Item	Qty	Reference	Part	PCB Footprint	Comments	MFR	MFR Part#
1	2	C1,C15	2.2uF	3528-21_EIA	CAPACITOR TANT 2.2UF 20V 10% SMD	KEMET	T491B225K020AT
2	2	C16,C2	0.1uF	CAP/HDC-1206	CAP .10UF 50V CERAMIC X7R 1206	KEMET	C1206C104K5RACTU
4	2	C5,C6	0.1uF	CAP/HDC-0603	CAP CERAMIC .1UF 50V X7R 0603	Panasonic	ECJ-1VB1H104K
5	7	C7,C14,C20,C23, C24,C28, C30	0.1uF	CAP/HDC-0603	CAP .1UF ±10% 25V CERAMIC X7R 0603	Panasonic	ECJ-1VB1E104K
6	2	C10,C13	22uF	CAP/N	CAP TANTALUM 22UF 25V 20% SMD	nichicon	F931E226MNC
7	2	C11,C12	5pF	CAP/HDC-0201	CAP CERAMIC 5.0PF 25V NP0 0201	Panasonic	ECJ-ZEC1E050C
8	6	C17,C18,C21,C31, C32,C33	22uF	CAP/EIA-B 3528-21	CAPACITOR TANT 22UF 16V 20% SMD	Kemet	T494B226M016AT
9	5	C19,C25,C26,C27, C29	0.01uF	CAP/HDC-0603	CAP CERAMIC .01UF 100V X7R 0603	KEMET	C0603C103K1RACTU
11	3	JP1,JP3,JP5	2-Pin Header	Header/2P	CONN HEADER VERT .100 2POS 30AU	AMP/Tyco	87220-2
12	5	JP2,JP10,JP13, JP14,JP15	3-Pin Header	Header/3P	CONN HEADER VERT .100 3POS 15AU	AMP/Tyco	87224-3
16	1	J1	HEADER 28x2	2x28 0.1"	CONN HEADER VERT 60POS .100 30AU. Cut to fit.	AMP/TYCO	3-87215-0
18	2	J3,J4	BANANA	CON/ BANANA-S	BANANA-female (non-insulated)	Johnson	108-0740-001
20	1	J6	IDC1X4	IDC-1x4	CONN HEADER 4POS .100 VERT GOLD	Molex/Waldom Electronics Corp	22-11-2042
26	1	P3	USB A	USB_TYPE _A_4P	CONN USB RECEPT R/A TYPE A 4POS.	AMP/Tyco	292303-1
27	1	R1	1.50K	RES/HDC-0402	RES 1.50K OHM 1/16W 1% 0402 SMD	Panasonic	ERJ-2RKF1501X
31	10	R31,R32,R33,R45, R46,R47,R48,R53, R56,R57	0 Ohm, 0402	RES/HDC-0402	RES ZERO OHM 1/16W 5% 0402 SMD	Panasonic	ERJ-2GEJ0R00X
33	8	R37,R58,R59,R60, R61,R62, R63,R64	10K	RES/HDC-0603	RES 10.0K OHM 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF1002V
34	2	R40,R39	4.7K	RES/HDC-0603	RES 4.7K OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ472V
38	2	R52,R51	0 ohm	RES/HDC-0201	RES 0.0 OHM 1/20W 5% 0201 SMD	Panasonic	ERJ-1GE0R00C
39	1	S1	SW DIP-7	DIP-14	SWITCH DIP EXTENDED SEALED 7POS	Grayhill	78B07ST
40	1	U1	DS90UR905	48ld LLP	DS90UR905Q	National	DS90UR905Q
44	1	VR3	SVR20K	Surface Mount 4mm Square	11-Turn Trimming Potentiometer; Top Adjust	Bourns	3224W-1-203E
45	1	VR4	SVR100K	Surface Mount 4mm Square	11-Turn Trimming Potentiometer; Top Adjust	Bourns	3224W-1-104E

DS90UR906 Rx De-serializer Board Description:

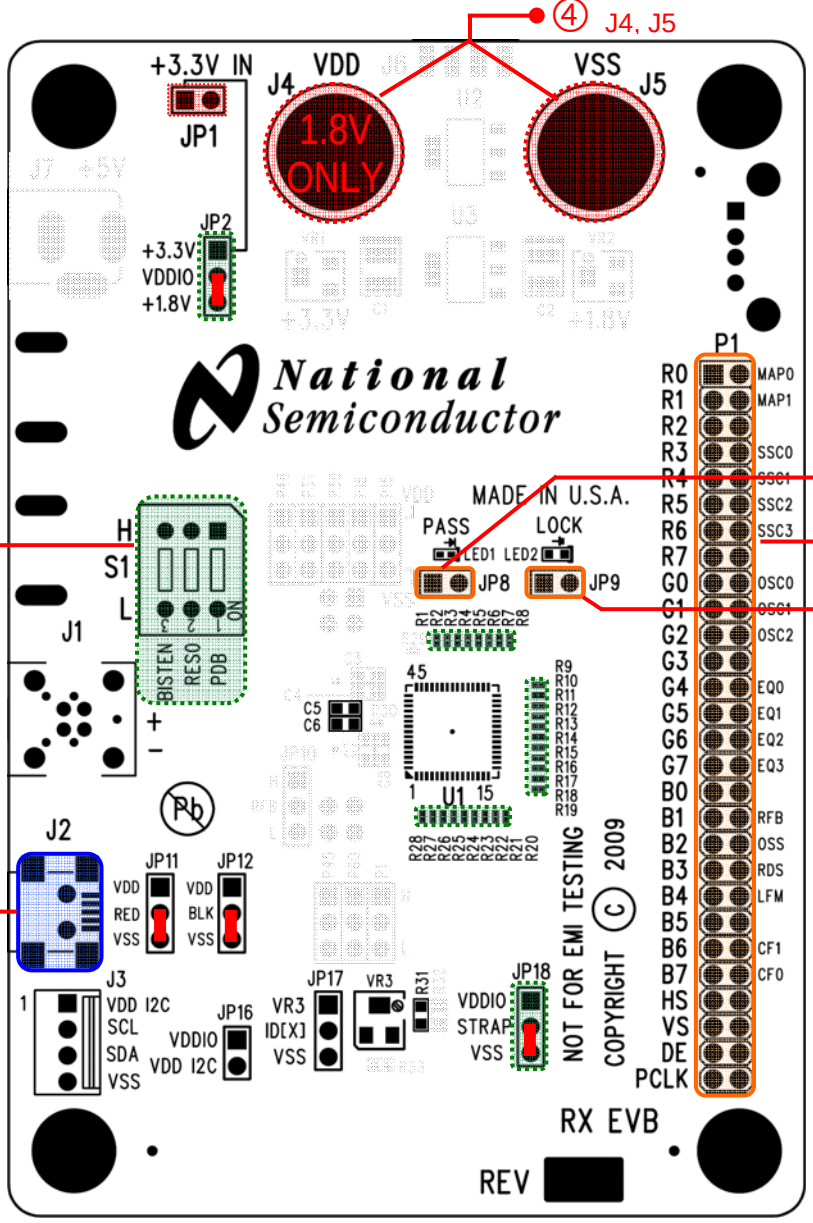
The USB connector J2 (mini USB) on the topside of the board provides the interface connection for FPD-LINKII signals to the Serializer board. Note: J3 (mini USB) on the bottom side is un-stuffed and not used with the cable provided in the kit.

The De-serializer board is powered externally from the J9 (VDD) and J7 (VSS) connectors shown below. For the De-serializer to be operational, the S1 – SLEEPB and switche on S1 must be set HIGH. Rising or falling edge reference clock is user selected by S1-RRFB: HIGH (for rising edge strobing) or LOW (for falling edge strobing).

The 2x25 pin IDC Connector P1 provides access to the 24 bit 1.8V or 3.3V LVCMOS and clock outputs.

④ J4, J5, JP1

Note:
1) VDD and VSS applied **externally** from J4 and J5 respectively.
2) To interface to 1.8V inputs: place jumper between pin 2 & 3 of JP2 (VDDIO=+1.8V)
2b) To interface to 3.3V inputs: place jumper between pin 1 & 2 of JP2 and apply 3.3V on JP1 pin 1. (VDDIO=+3.3V).

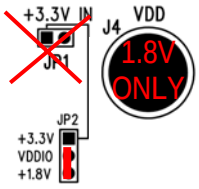
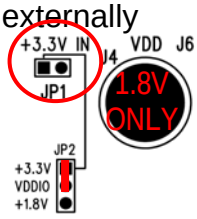
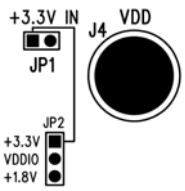


Note:
Connect cable (mini USB side) to J2 on **(TOPSIDE)**.

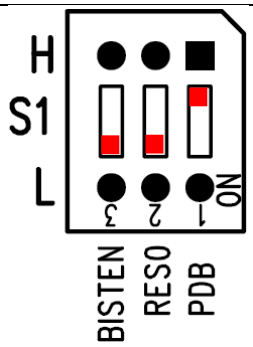
① J2 (TOPSIDE)
① J3 (BACKSIDE) *(UNSTUFFED)*

Configuration Settings for the Rx Demo Board

VDDIO: 1.8V or 3.3V LVCMOS INPUT/OUTPUT SELECTION

Reference	Description			
JP1	VDDIO LVCMOS input/output configuration.	**VDDIO = 1.8V (Default)**  1.8V LVCMOS	**VDDIO = 3.3V** apply externally  3.3V LVCMOS	

S1, STRAPS: De-serializer Input Features Selection

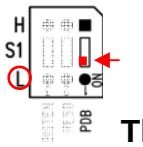
Reference	Description	Input = L	Input = H	S1
PDB	**P**ower**D**own **B**ar	Power Down (Disabled)	Operational **(Default)**	
BISTEN	**BIST EN**able See datasheet Table 2 for description Note: Set BISTEN on the DS90UR905 before the DS90UR906	OFF **(Default)**	ON	
RES0 (* IMPORTANT See user note below)	**RES**erved	MUST be tied low for normal operation **(Default)**		

*Note: In user layout RES0 (pin 47) **MUST** be tied low for proper operation.

STRAPs: De-serializer Input Features Selection

There are two options for setting strap(s):

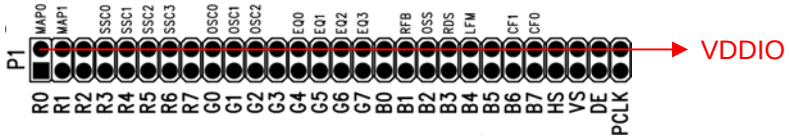
1) On-the-fly strap selection on the demo board is a six (6) step process:



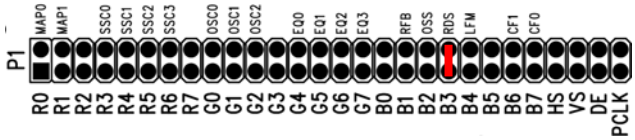
Step 1: Set PDB to LOW on SW1. **This will place the part in power down mode.**

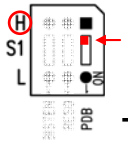
Step 2: Place jumper between pin 1 and 2 of JP18.

This ties the even numbered pins on P1 to VDDIO which will provide the pullup for the strap option.



Step 3: Place jumper(s) on strap pins option(s) desired.
E.g. if you wanted to change RDS from default RDS=L (low drive strength) to RDS=H (high drive strength), place a jumper on RDS of P1.



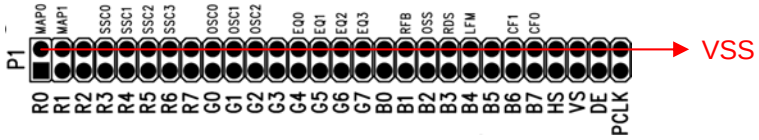


Step 4: Switch PDB on SW1 from LOW to HIGH. **This overrides the default register(s) and will place the part in normal operating mode.**

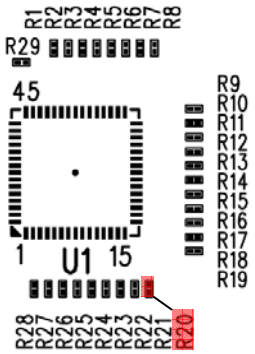
Step 5: Remove ALL jumper(s) on strap pin placed in Step 3.

Step 6: Remove jumper between pin 1 and 2 of JP18 and place the jumper between pin 2 and 3 of JP18.

This ties the even numbered pins on P1 to VSS and is used as the ground reference for R[7:0], G[7:0], B[7:0], HS, VS, DE, PCLK under normal operating conditions.

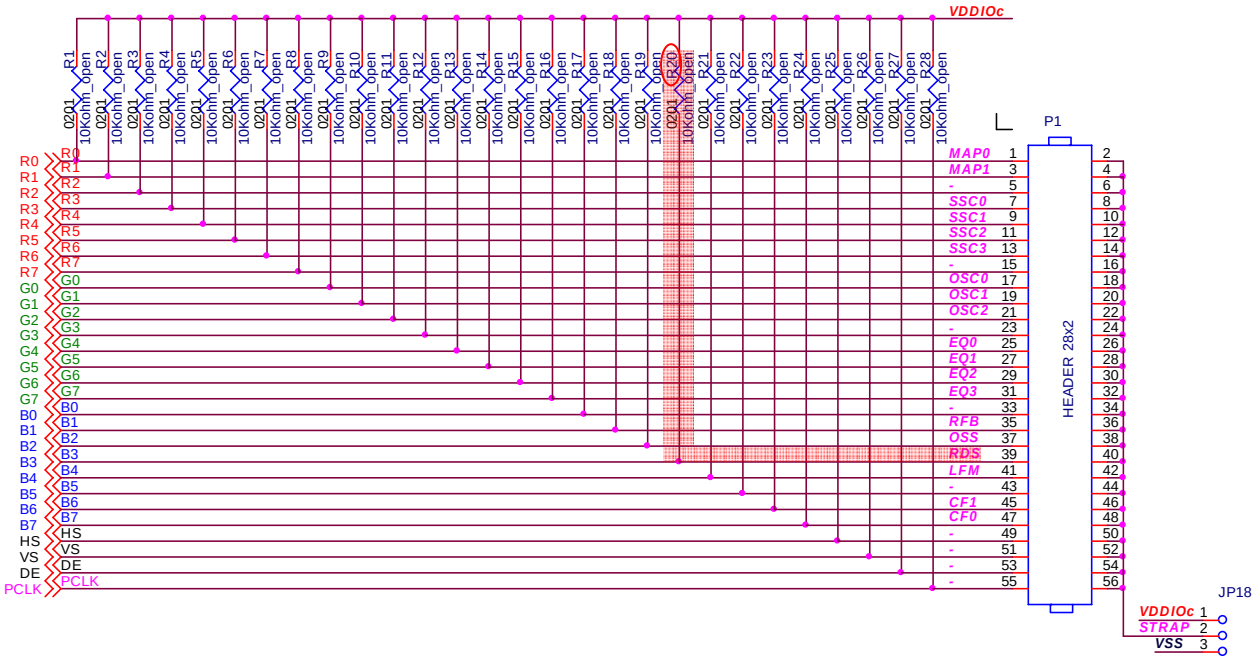


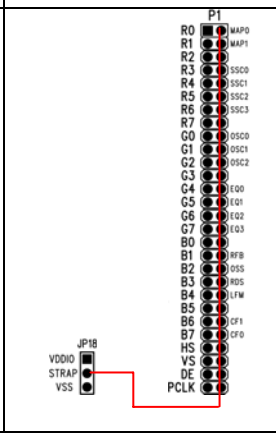
2) For straps options to be loaded permanently without using the on-the-fly option: Place a 10K ohm 0201 size resistor on corresponding resistor pads.

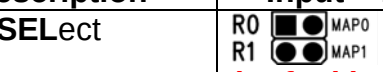
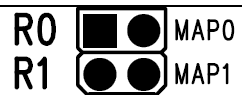
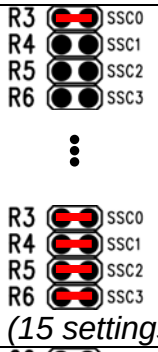
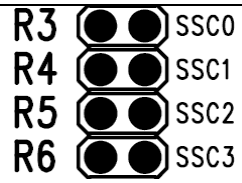
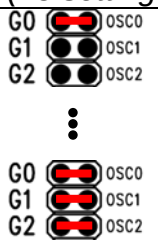
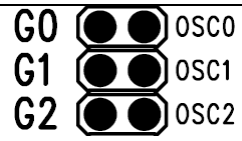
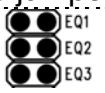
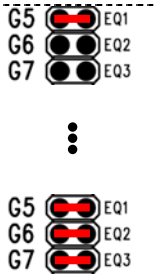
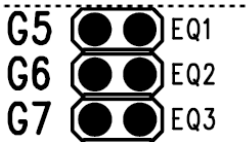


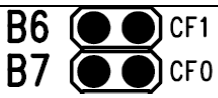
E.g.

Note: ***This is the same configuration setting as previous example using 10K ohm resistor instead of jumpers***

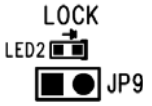
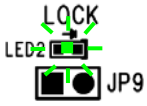
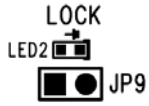


		Normal operation	For strap pullup	
	Ties all even pins on P1 to HIGH or LOW.	JP18 VDDIO STRAP VSS **All strap inputs = L**	JP18 VDDIO STRAP VSS **Strap pullup to VDDIO**	

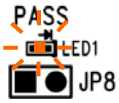
Reference	Description	Input = L	Input = H	P1
MAPSEL[1:0]	**MAP SEL**ect	 **(Default)** No jumpers		
SSC[3:0]	**S**pread **S**pectrum **C**lock Generation control See datasheet for settings	Disabled **(Default)**  No jumpers	 *(15 settings)*	
OSC[2:0]	**OSC**illator Frequency select See datasheet for settings	Disabled  **(Default)** No jumpers	 *(7 settings)*	
EQ[0]	**Eq**ualizer Disable/Enable	Disabled  **(Default)** No jumper	Enabled 	
EQ[3:1]	**EQ**ualizer control See datasheet for settings	 **(Default)** No jumpers		
RFB	Latch output data on **R**ising or **F**alling Data Strobe of RCLK	Falling  **(Default)** No jumper	Rising  **Must also set JP18**	
OSS SEL	**O**utput **S**elect **S**leep **SEL**ect	Disabled  **(Default)** No jumper	Enabled 	
RDS	**R**eciever Output **D**rive **S**trength	Low drive strength  **(Default)**	High drive strength 	

		No jumper		
LF_MODE	**L**ow **F**requency **MODE** Used only when SSCG is enabled otherwise this pin is a don't care	PCLK≥20MHz  **(Default)** No jumper	PCLK<20MHz 	
CONFIG[1:0]	**CONFIG**uration control See datasheet for settings	 **(Default)** No jumper		

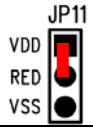
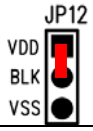
JP4: Output Lock Monitor

Reference	Description	Output = L	Output = H	JP4
LOCK (JP9)	Receiver PLL **LOCK** **Note:** **DO NOT PUT A SHORTING JUMPER IN JP4.**	Unlocked 	Locked 	

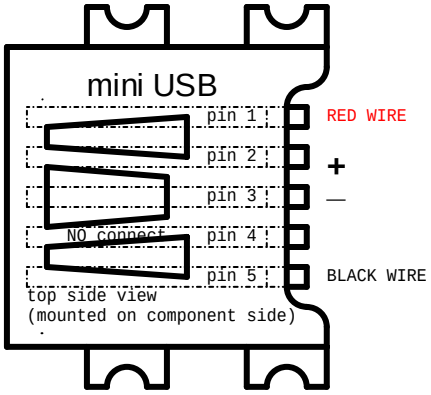
JP3: Output Pass Monitor

Reference	Description	Output = L	Output = H	JP3
PASS (JP8)	BIST **PASS** **Note:** **DO NOT PUT A SHORTING JUMPER IN JP3.**	Unlocked 	PASS 	

JP1, JP2: USB Red and Black wire

Reference	Description	VDD	VSS	OPEN
JP11	Power wire in USB cable thru J2 *(and J3 not mounted)* connector Jumper RED to VSS – recommended *Note: Normally VDD in USB application*	Red wire tied to VDD 	Red wire tied to VSS **(Default)** 	Red wire floating (not recommended) 
JP12	Power wire in USB cable thru J2 *(and J3 not mounted)* connector Jumper BLACK to VSS – recommended *Note: Normally VSS in USB application*	Black wire tied to VDD 	Black wire tied to VSS **(Default)** 	Black wire floating (not recommended) 

J2



Rx LVDS Pinout and LVCMOS by Connector

The following three tables illustrate how the Rx outputs are mapped to the IDC connector P1, the mini USB LVDS connector J2, and the mini USB LVDS connector J5 pinouts. Note – labels are also printed on the demo boards for both the LVDS inputs and LVCMOS outputs.

P1 LVCMOS OUTPUT			
pin no.	**name**	**name**	**pin no.**
1	**R0**	GND	2
3	**R1**	GND	4
5	**R2**	GND	6
7	**R3**	GND	8
9	**R4**	GND	10
11	**R5**	GND	12
13	**R6**	GND	14
15	**R7**	GND	16
17	**G0**	GND	18
19	**G1**	GND	20
21	**G2**	GND	22
23	**G3**	GND	24
25	**G4**	GND	26
27	**G5**	GND	28
29	**G6**	GND	30
31	**G7**	GND	32
33	**B0**	GND	34
35	**B1**	GND	36
37	**B2**	GND	38
39	**B3**	GND	40
41	**B4**	GND	42
43	**B5**	GND	44
45	**B6**	GND	46
47	**B7**	GND	48
49	**HS**	GND	50
51	**VS**	GND	52
53	**DE**	GND	54
55	**PCLK**	GND	56

J2 (topside) LVDS OUTPUT	
pin no.	**name**
1	JP5
2	**RIN+**
3	**RIN-**
4	NC
5	JP6

J5 (bottom side) (not mounted) LVDS OUTPUT	
pin no.	***name***
5	*JP6*
4	*NC*
3	***RIN-***
2	***RIN+***
1	*JP5*

BOM (Bill of Materials) De-serializer Demo PCB:

DS90UR906 Rx Demo Board - Board Stackup Revised: Friday, September 18, 2009

DS90UR906 Rx Demo Board Revision: 2

Bill Of Materials September 18,2009 18:25:53

Item	Qty	Reference	Part	PCB Footprint	Comments	MFR	MFR Part#
2	6	C3,C7,C21, C29,C30,C34	0.1uF	CAP/HDC-0603	CAP .1UF ±10% 25V CERAMIC X7R 0603	Panasonic	ECJ-1VB1E104K
3	5	C4,C8,C22, C25,C31	0.01uF	CAP/HDC-0603	CAP CERAMIC .01UF 100V X7R 0603	KEMET	C0603C103K1RACTU
4	4	C5,C6,C15,C16	0.1uF	CAP/HDC-0603	CAP CERAMIC .1UF 50V X7R 0603	Panasonic	ECJ-1VB1H104K
5	2	C11,C14	22uF	CAP/N	CAP TANTALUM 22UF 25V 20% SMD	nichicon	F931E226MNC
6	2	C12,C17	2.2uF	3528-21_EIA	CAPACITOR TANT 2.2UF 20V 10% SMD	KEMET	T491B225K020AT
7	2	C18,C13	0.1uF	CAP/HDC-1206	CAP .10UF 50V CERAMIC X7R 1206	KEMET	C1206C104K5RACTU
8	6	C19,C20,C24, C28,C32,C33	22uF	CAP/EIA-B 3528-21	CAPACITOR TANT 22UF 16V 20% SMD	Kemet	T494B226M016AT
10	1	C26	4.7µF	CAP/HDC-0402	CAP CERAMIC 4.7UF 6.3V X5R 0402	Panasonic	ECJ-0EB0J475M
11	2	C35,C36	5pF	CAP/HDC-0201	CAP CERAMIC 5.0PF 25V NP0 0201	Panasonic	ECJ-ZEC1E050C
12	2	JP1,JP16	2-Pin Header	Header/2P	CONN HEADER VERT .100 2POS 30AU	AMP/Tyco	87220-2
13	3	JP2,JP17,JP18	3-Pin Header	Header/3P	CONN HEADER VERT .100 3POS 15AU	AMP/Tyco	87224-3
16	2	JP11,JP12	3-Pin Header	Header/3P	CONN HEADER VERT .100 3POS 15AU.	AMP/Tyco	87224-3
19	1	J2	mini USB 5pin	mini_B USB surface mount	CONN RECEPT MINI USB2.0 5POS.	Hirose	UX60-MB-5ST
20	1	J3	IDC1X4	IDC-1x4	CONN HEADER 4POS .100 VERT GOLD	Molex/ Waldom Electronics Corp	22-11-2042
21	2	J4,J5	BANANA	CON/ BANANA-S	BANANA-female (non-insulated)	Johnson	108-0740-001
26	1	LED1	0402 Orange LED	0402 SMT	LED ORN/CLEAR 610NM 0402 SMD	Lumex Opto/ Components Inc	SML-LX0402SOC-TR
27	1	LED2	0603 Green LED	0603 (Super Thin)	LED GREEN CLEAR THIN 0603 SMD	LITE-ON INC	LTST-C191KGKT
28	1	P1	HEADER 28x2	2x28 0.1"	CONN HEADER VERT 56POS .100 30AU. Cut 60 POS or use AMP part #2-87215-9.	AMP/TYCO	3-87215-0
32	4	R31,R37, R38,R39	10K	RES/HDC-0603	RES 10.0K OHM 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF1002V
37	8	R40,R43,R44,R45, R46,R47,R59,R60	0 Ohm, 0402	RES/HDC-0402	RES ZERO OHM 1/16W 5% 0402 SMD	Panasonic	ERJ-2GEJ0R00X
40	3	R56,R57,R58	0 ohm	RES/HDC-0201	RES 0.0 OHM 1/20W 5% 0201 SMD.	Panasonic	ERJ-1GE0R00C
41	2	R62,R61	4.7K	RES/HDC-0603	RES 4.7K OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ472V
42	1	S1	SW DIP-3	DIP-6	SWITCH DIP EXTENDED SEALED 3POS	Grayhill	78B03ST
43	1	U1	DS90UR906	60ld LLP Surface Mount	DO NOT PURCHASE, National will supply.	National	DS90UR906
46	1	VR3	SVR50K	4mm Square	TRIMPOT 50K OHM 4MM CERMET SMD	Bourns	3224W-1-503E

Typical Connection and Test Equipment

The following is a list of typical test equipment that may be used to generate signals for the TX inputs:

1) Digital Video Source – for generation of specific display timing such as Digital Video Processor or Graphics Controller with digital RGB (1.8V/3.3V LVCMOS) output.
2) Astro Systems VG-835 - This video generator may be used for video signal sources for 6/8-bit Digital 1.8V/3.3V LVCMOS/RGB.
3) Any other signal / video generator that generates the correct input levels as specified in the datasheet.
4) Optional – Logic Analyzer or Oscilloscope

The following is a list of typical test equipment that may be used to monitor the output signals from the RX:

1) LCD Display Panel which supports digital RGB (1.8V/3.3V LVCMOS) inputs.
2) National Semiconductor DS90UR905 Serializer (Tx)
3) Optional – Logic Analyzer or Oscilloscope
4) Any SCOPE with a bandwidth of at least 65MHz for 1.8V/3.3V LVCMOS and/or 1GHz for looking at the differential signal.

LVDS signals may be easily measured with high impedance / high bandwidth differential probes such as the TEK P6247 or P6248 differential probes.

The picture below shows a typical test set up using a Graphics Controller and LCD Panel.

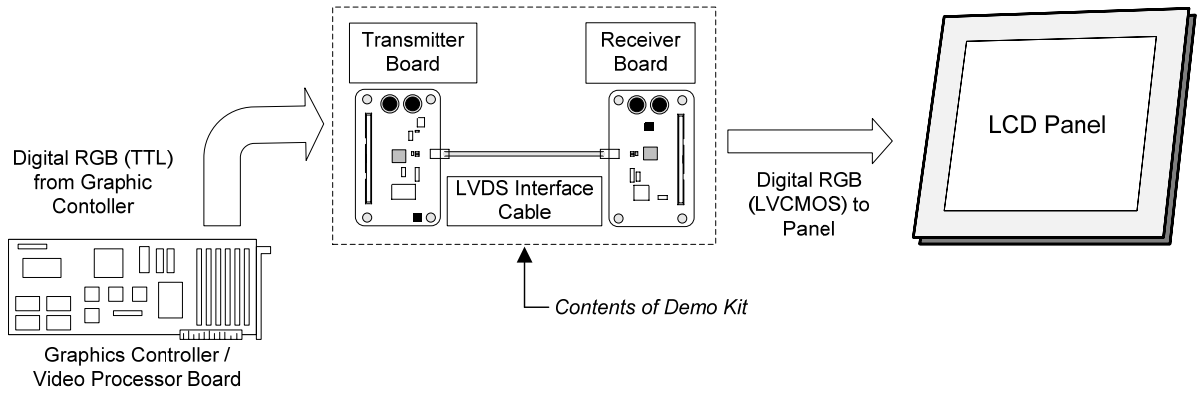


Figure 2. Typical SERDES Setup of LCD Panel Application

The picture below shows a typical test set up using a generator and scope.

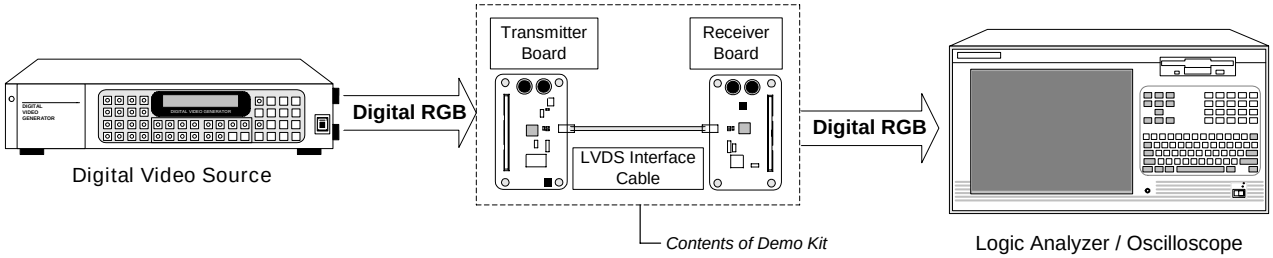


Figure 3. Typical SERDES Test Setup for Evaluation

Troubleshooting Demo Setup

NOTE: The DS90UR905 and DS90UR906 are NOT USB compliant and should not be plugged into a USB device nor should a USB device be plugged into the demo boards.

If the demo boards are not performing properly, use the following as a guide for quick solutions to potential problems. If the problem persists, please contact the local Sales Representative for assistance.

QUICK CHECKS:

1. Check that Powers and Grounds are connected to both Tx AND Rx boards.
2. Check the supply voltage (typical 1.8V) and also current draw with both Tx and Rx boards. The Serializer board should draw about 100mA with clock and all data bits switching at 65MHz. The De-serializer board should draw about 120mA with clock and all data bits switching at 65MHz.
3. Verify input clock and input data signals meet requirements (VIL, VIH, tset, thold), Also verify that data is strobed on the selected rising/falling (RFB pin) edge of the clock.
4. Check that the Jumpers and Switches are set correctly.
5. Check that the cable is properly connected.

TROUBLESHOOTING CHART

Problem…	**Solution…**
There is only the output clock. There is no output data.	Make sure the data is applied to the correct input pin. Make sure data is valid at the input.
No output data and clock.	Make sure Power is on. Input data and clock are active and connected correctly. Make sure that the cable is secured to both demo boards.
Power, ground, input data and input clock are connected correctly, but no outputs.	Check the Power Down pins of both Serializer and De-serializer boards to make sure that the devices are enabled (/PD=Vcc) for operation. Also check DEN on the Serializer board and REN on the Deserializer board is set HIGH.
The devices are pulling more than 1A of current.	Check for shorts in the cables connecting the TX and RX boards.
After powering up the demo boards, the power supply reads less than 1.8V when it is set to 1.8V.	Use a larger power supply that will provide enough current for the demo boards, a 500mA minimum power supply is recommended.

Note: Please note that the following references are supplied only as a courtesy to our valued customers. It is not intended to be an endorsement of any particular equipment or hardware supplier.

Equipment References

Digital Video Pattern Generator – Astro Systems VG-835 (or equivalent):

Astro Systems
425 S. Victory Blvd. Suite A
Burbank, CA 91502
Phone: (818) 848-7722
Fax: (818) 848-7799
www.astro-systems.com

Extra Component References

TDK Corporation of America
1740 Technology Drive, Suite 510
San Jose, CA 95110
Phone: (408) 437-9585
Fax: (408) 437-9591
www.component.tdk.com
Optional EMI Filters – TDK Chip Beads (or equivalent)

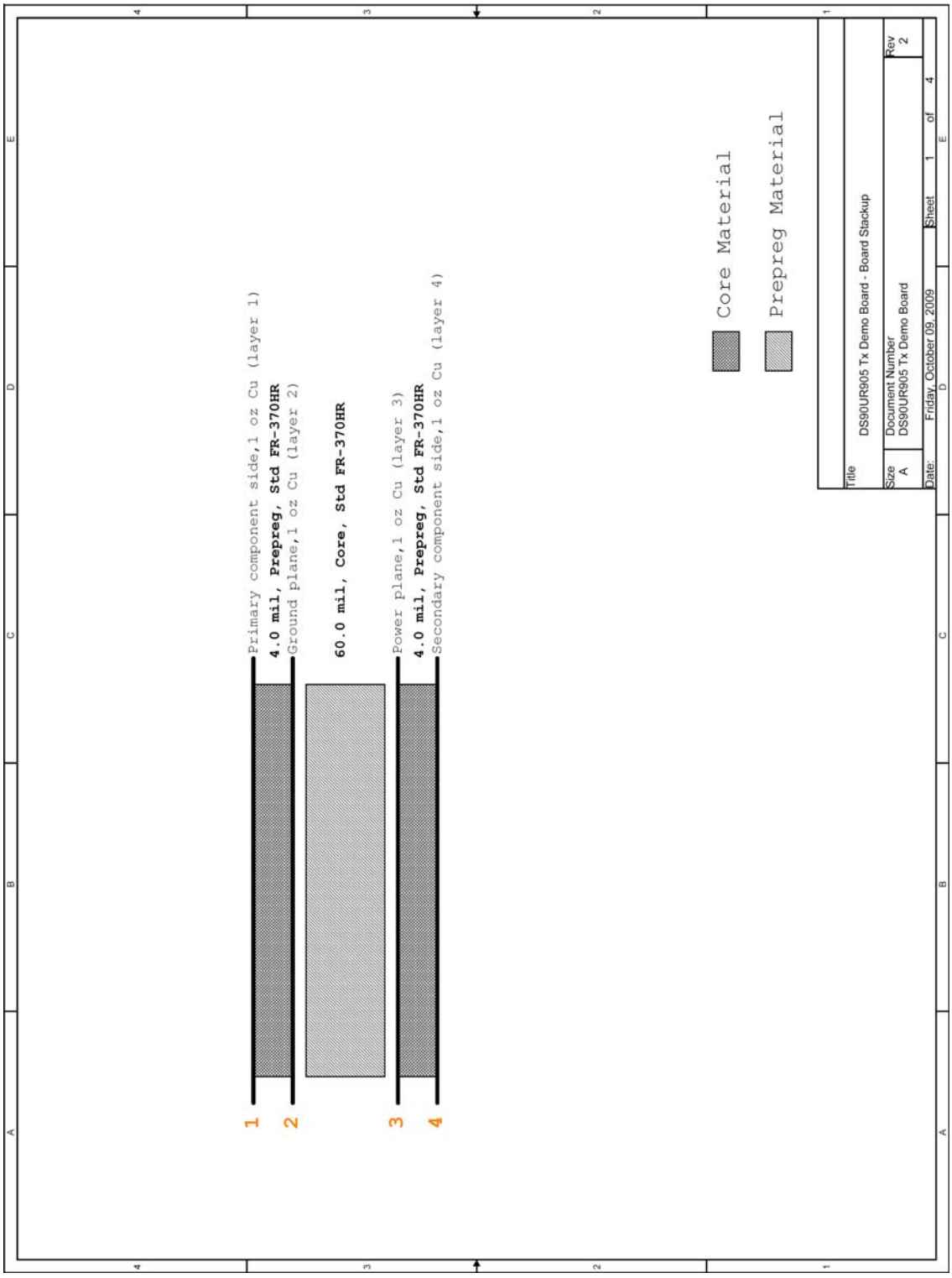
Cable References

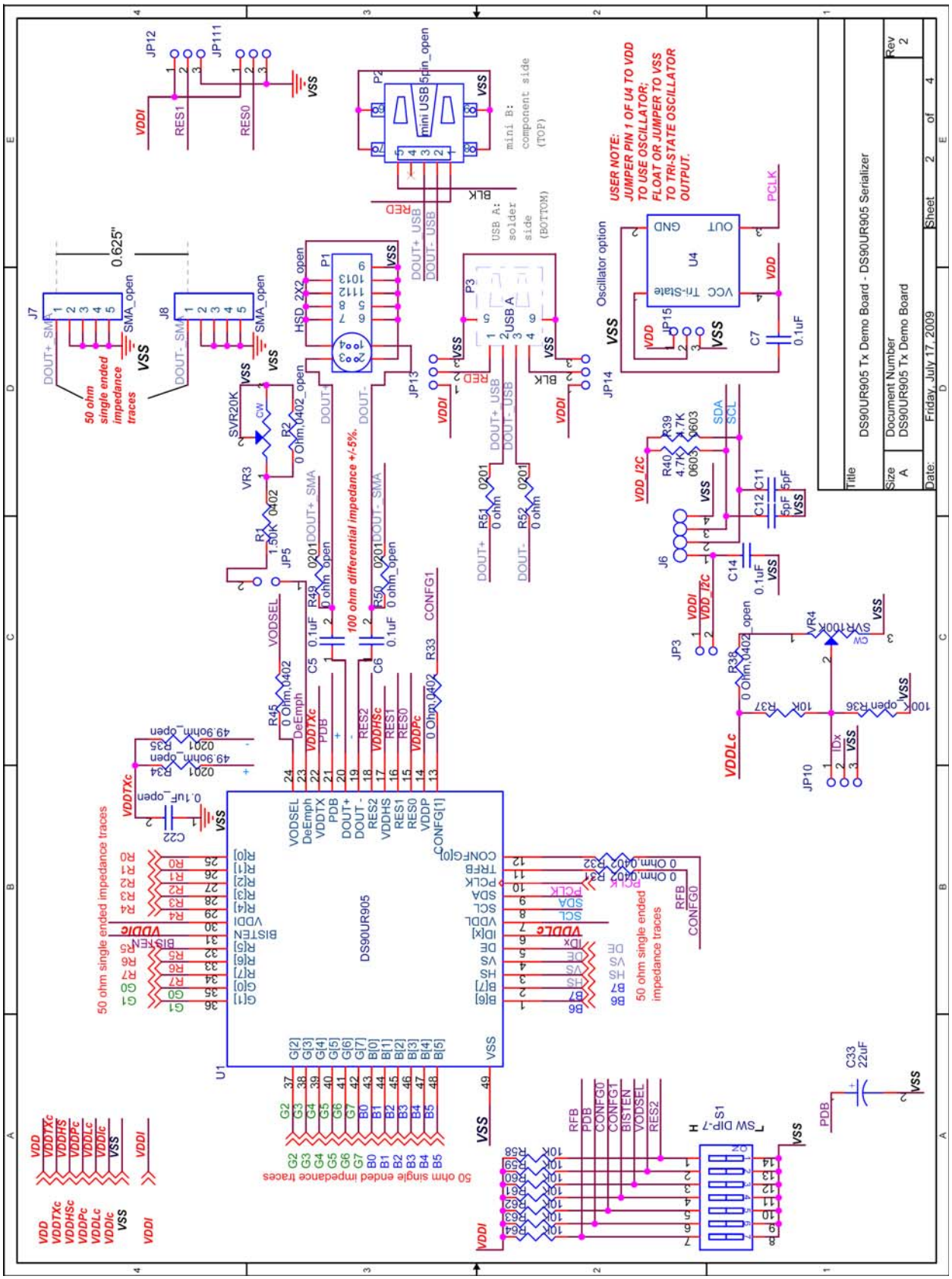
The FPD-LINKII interface cable included in the kit is a standard off-the-shelf high-speed USB 2.0 with a 4-pin USB A type on one end and a 5-pin mini USB on the other end and is included for demonstration purposes only.
NOTE: The DS90UR905 and DS90UR906 are NOT USB compliant and should not be plugged into a USB device nor should a USB device be plugged into the demo boards.
The inclusion of the USB cable in the kit is for:
1) Demonstrating the robustness of the FPD-LINKII link over ordinary twisted pair data cables.
2) Readily available and in different lengths without having custom cables made.

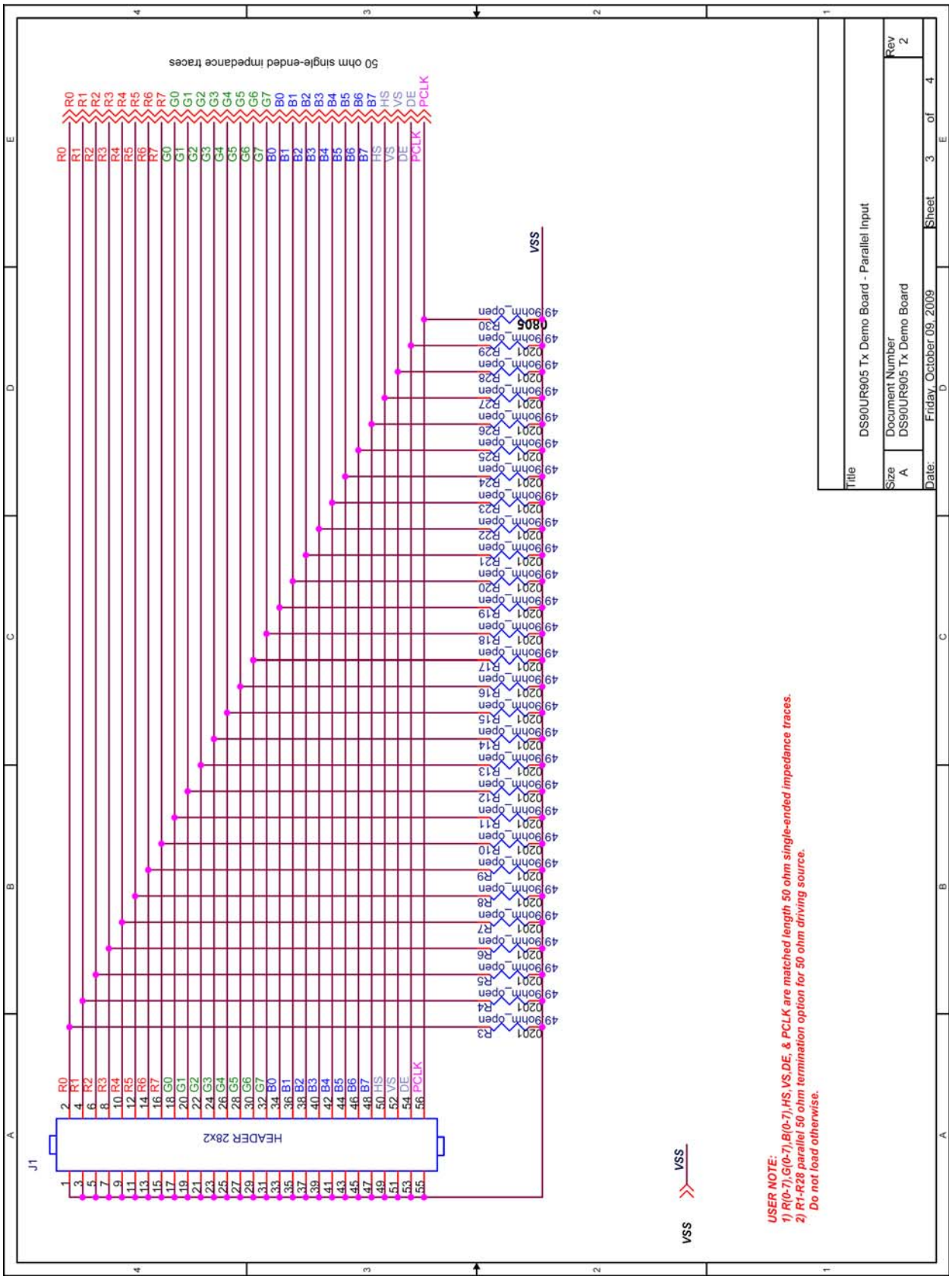
- For optimal performance, we recommend Shielded Twisted Pair (STP) 100Ω differential impedance cable for high-speed data applications.

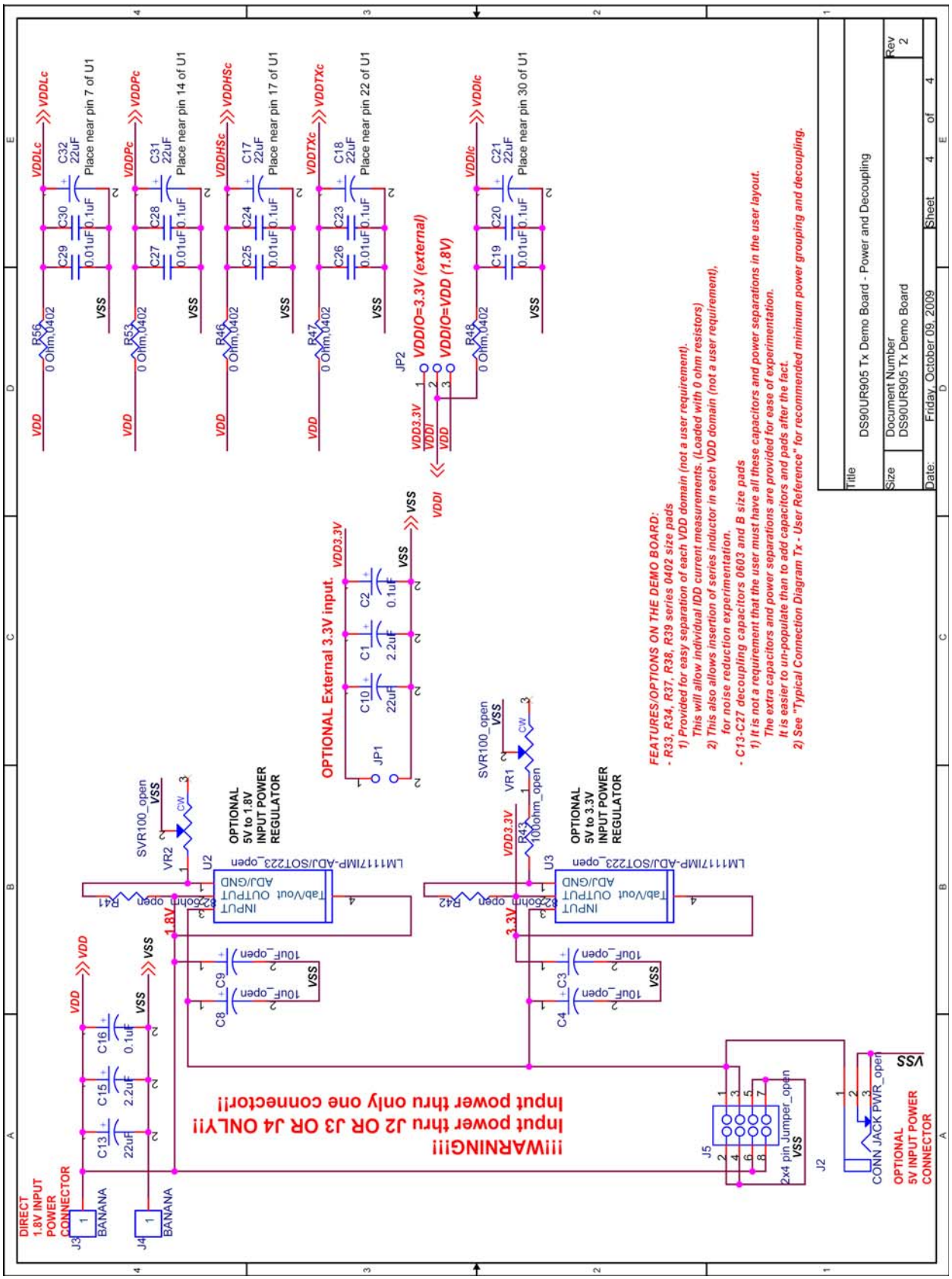
Appendix

Serializer (Tx) Demo PCB Schematic:

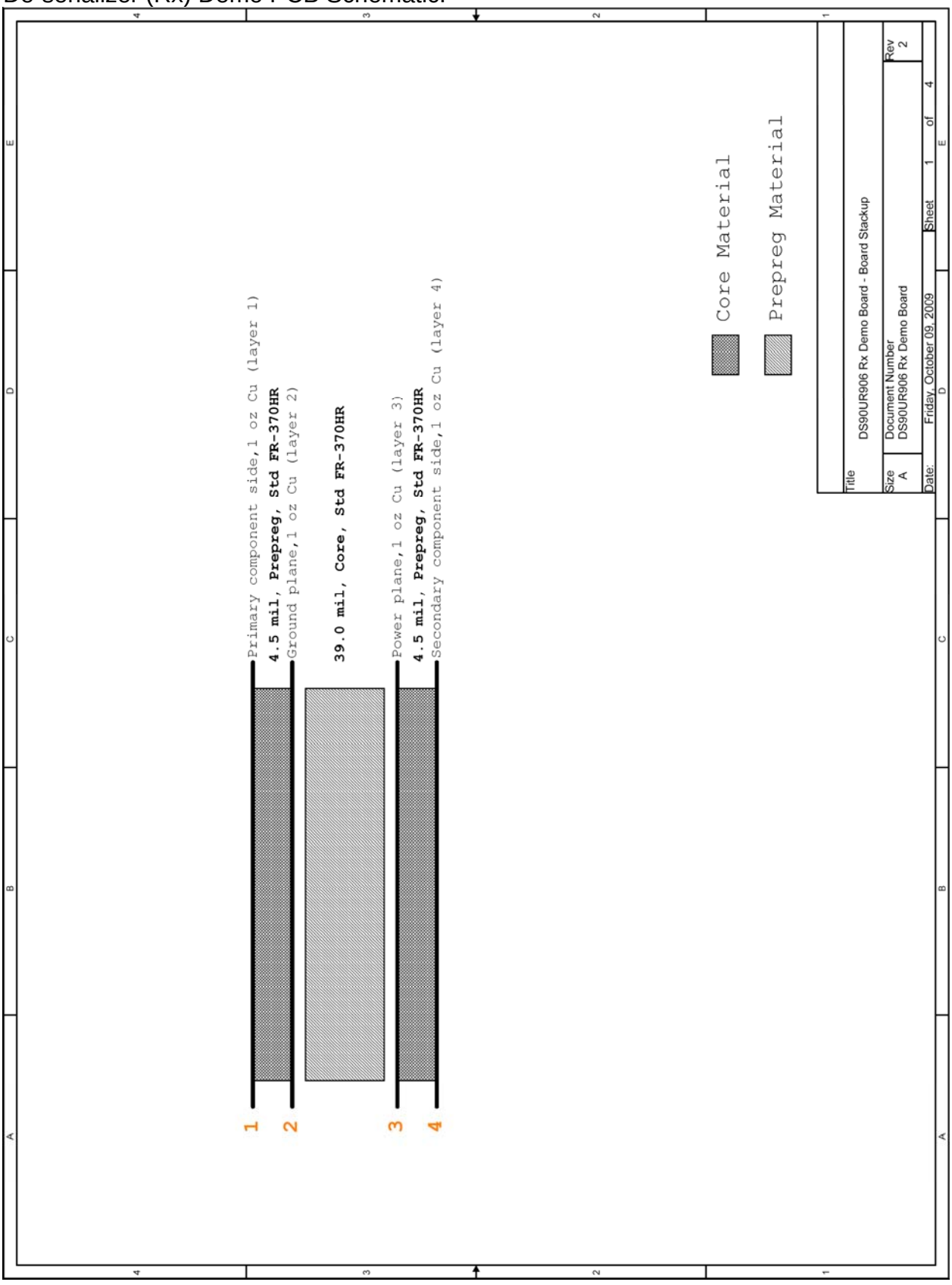


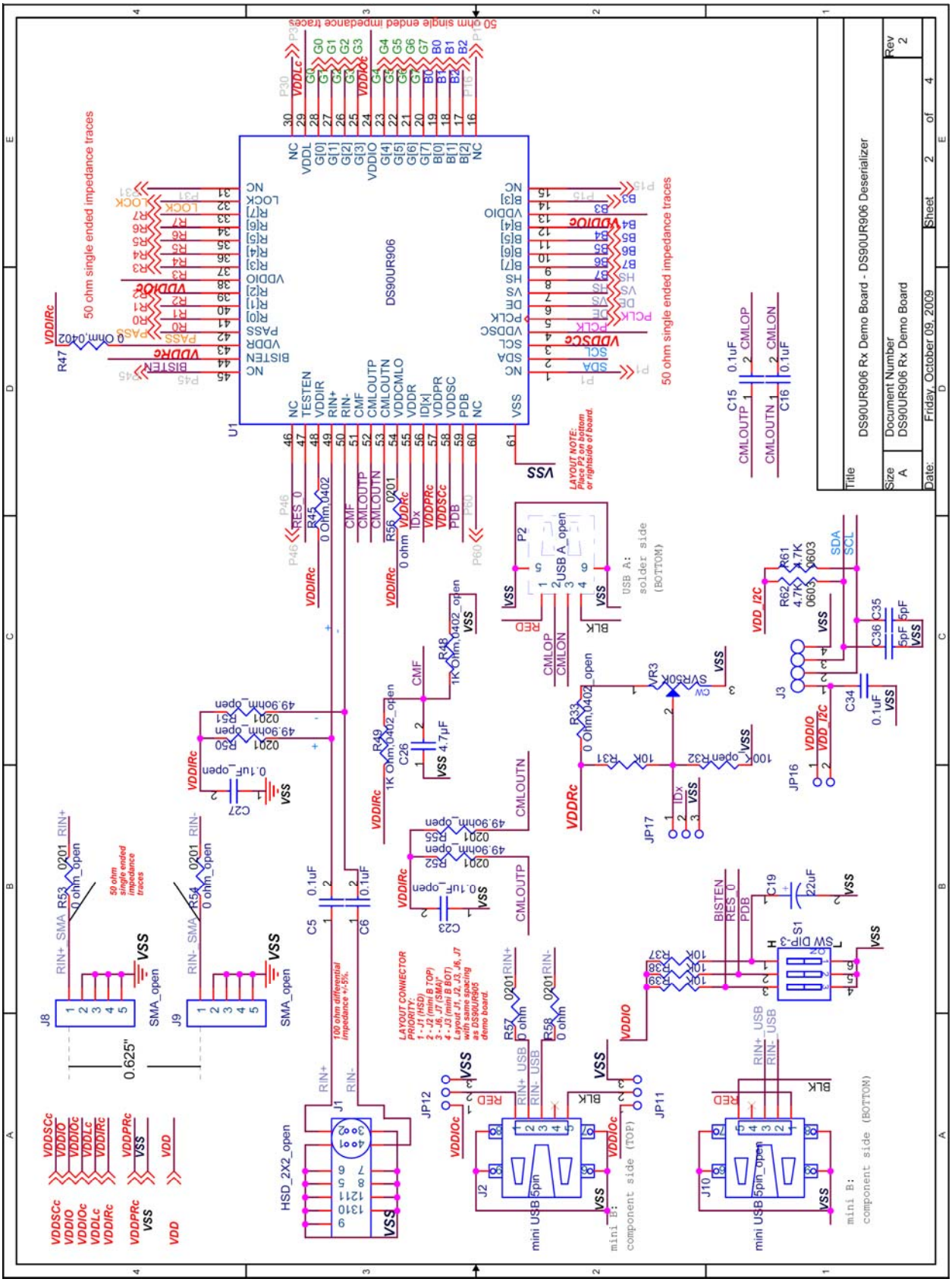

DS90UR905 Tx Demo Board - DS90UR905 Serializer
Document Number
DS90UR905 Tx Demo Board
Rev 2
Friday, July 17, 2009
Sheet 2 of 4
USER NOTE:
JUMPER PIN 1 OF U4 TO VDD TO USE OSCILLATOR;
FLOAT OR JUMPER TO VSS TO TRI-STATE OSCILLATOR OUTPUT.
100 ohm differential impedance +/-5%.
50 ohm single ended impedance traces
DS90UR905
SW DIP-7

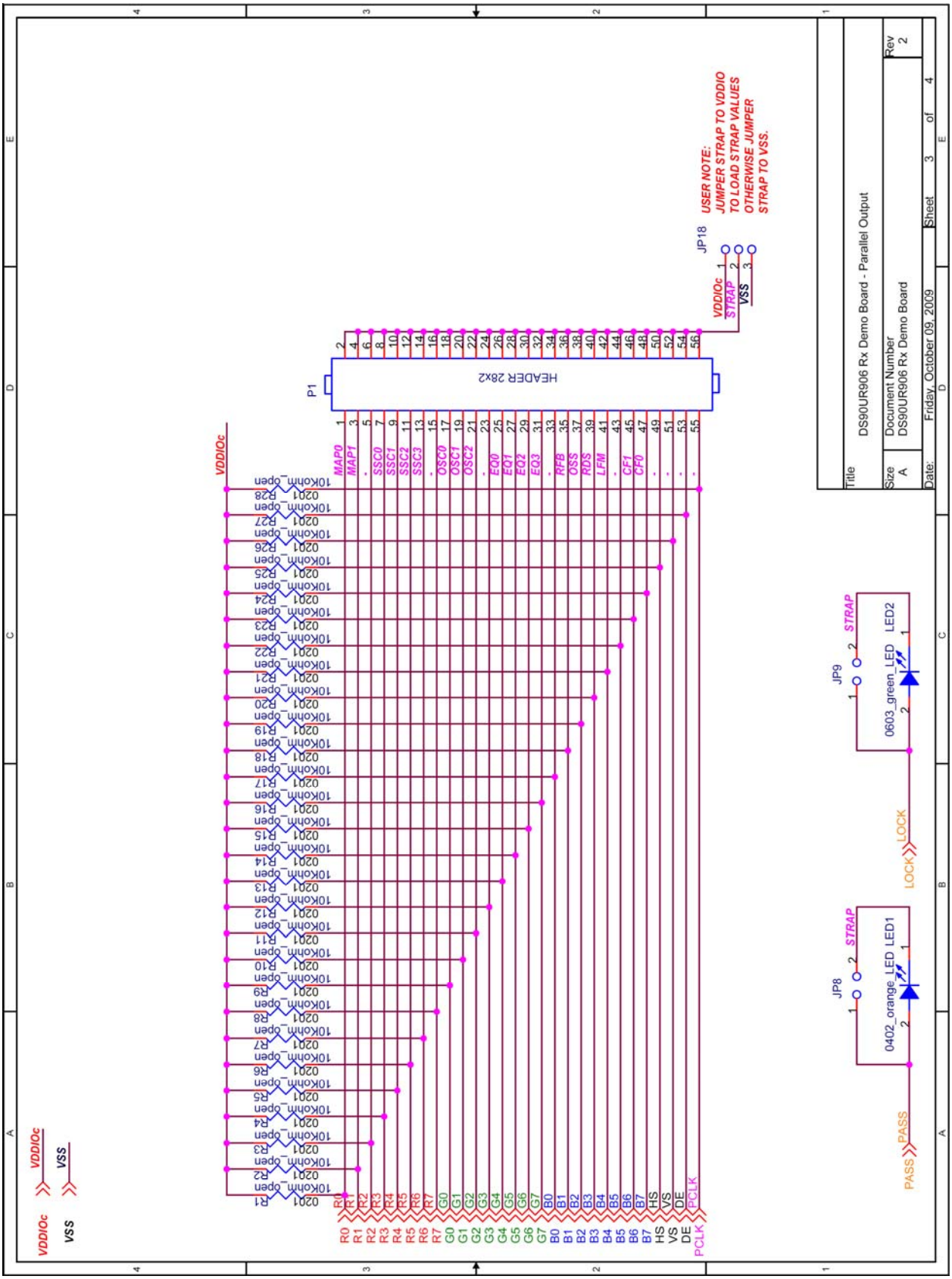

50 ohm single-ended impedance traces
HEADER 28x2
J1
VSS
USER NOTE:
1) R(0-7),G(0-7),B(0-7),HS,VS,DE, & PCLK are matched length 50 ohm single-ended impedance traces.
2) R1-R28 parallel 50 ohm termination option for 50 ohm driving source.
Do not load otherwise.
Title
DS90UR905 Tx Demo Board - Parallel Input
Size
A
Document Number
DS90UR905 Tx Demo Board
Rev
2
Date:
Friday, October 09, 2009
Sheet
3
of
4

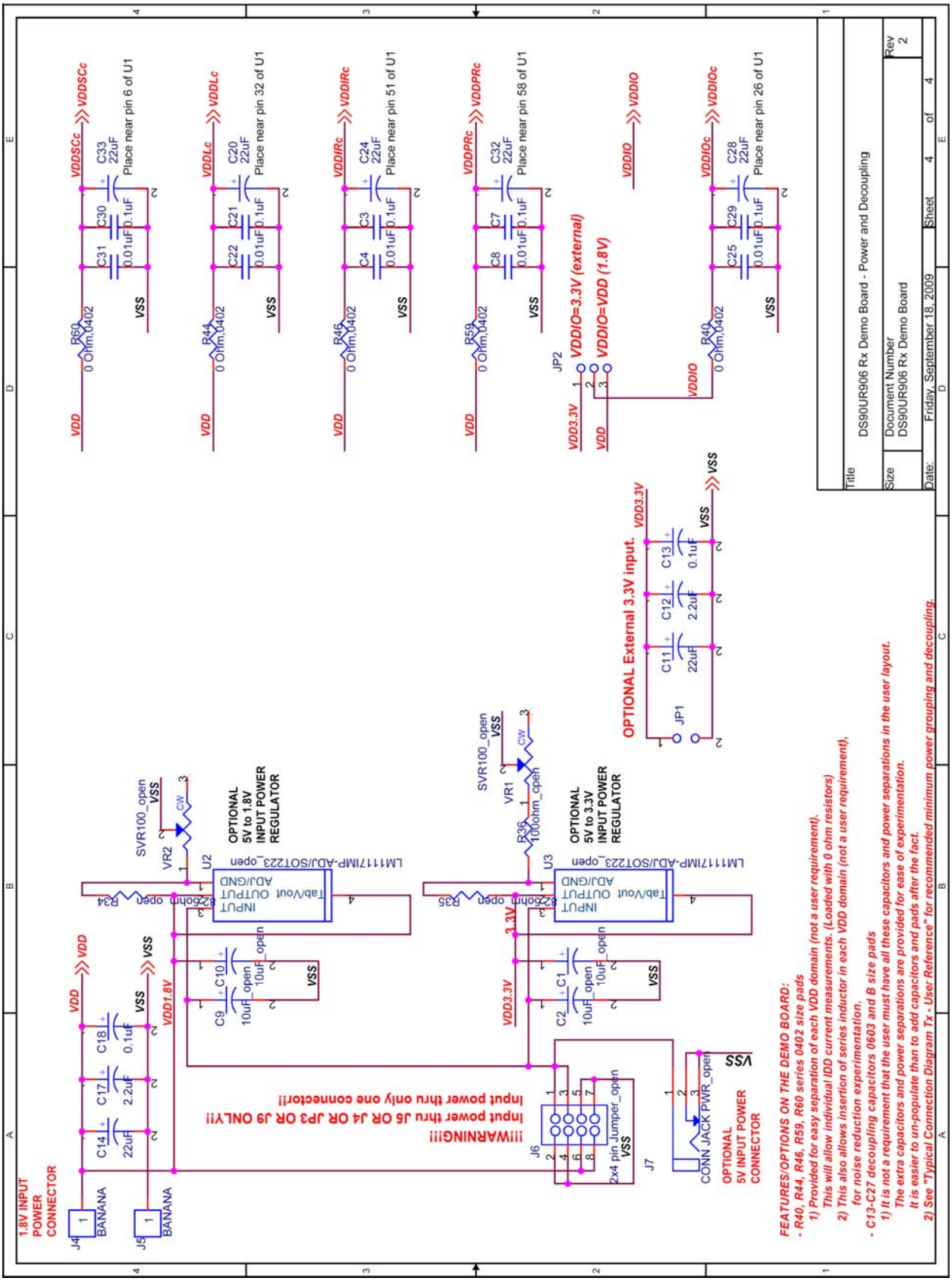

DS90UR905 Tx Demo Board - Power and Decoupling
Document Number
DS90UR905 Tx Demo Board
Rev 2
Friday, October 09, 2009
Sheet 4 of 4
FEATURES/OPTIONS ON THE DEMO BOARD:
- R33, R34, R37, R38, R39 series 0402 size pads
1) Provided for easy separation of each VDD domain (not a user requirement).
This will allow individual IDD current measurements. (Loaded with 0 ohm resistors)
2) This also allows insertion of series inductor in each VDD domain (not a user requirement), for noise reduction experimentation.
- C13-C27 decoupling capacitors 0603 and B size pads
1) It is not a requirement that the user must have all these capacitors and power separations in the user layout.
The extra capacitors and power separations are provided for ease of experimentation.
It is easier to un-populate than to add capacitors and pads after the fact.
2) See "Typical Connection Diagram Tx - User Reference" for recommended minimum power grouping and decoupling.
OPTIONAL External 3.3V input.
VDD/IO=3.3V (external)
VDD/IO=VDD (1.8V)
OPTIONAL 5V to 1.8V INPUT POWER REGULATOR
OPTIONAL 5V to 3.3V INPUT POWER REGULATOR
LM1117IMP-ADJ/SOT223_open
DIRECT 1.8V INPUT POWER CONNECTOR
OPTIONAL 5V INPUT POWER CONNECTOR
!!!WARNING!!!
Input power thru J2 OR J3 OR J4 ONLY!!
Input power thru only one connector!!
2x4 pin Jumper_open
CONN JACK PWR_open
Place near pin 7 of U1
Place near pin 14 of U1
Place near pin 17 of U1
Place near pin 22 of U1
Place near pin 30 of U1

De-serializer (Rx) Demo PCB Schematic:

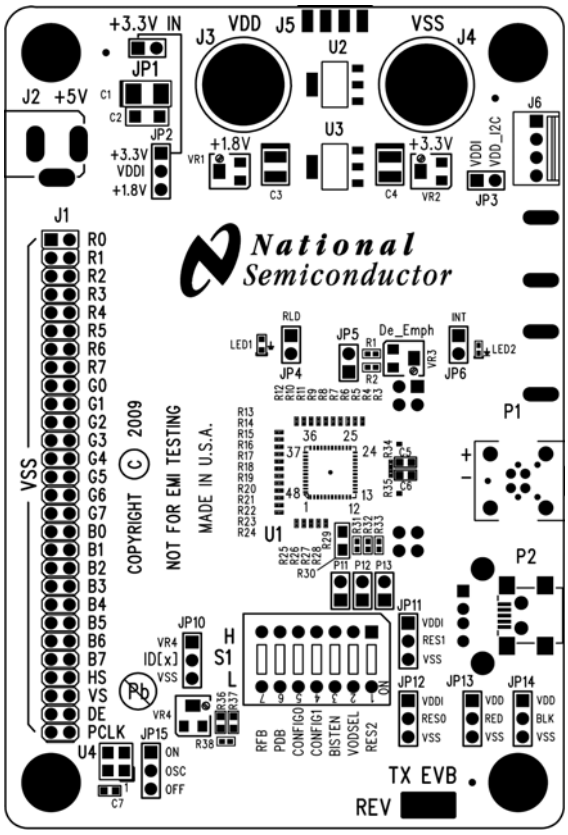



DS90UR906 Rx Demo Board - DS90UR906 Deserializer
Document Number
DS90UR906 Rx Demo Board
Rev 2
Friday, October 09, 2009
Sheet 2 of 4
DS90UR906
U1
50 ohm single ended impedance traces
50 ohm single ended impedance traces
LAYOUT NOTE: Place P2 on bottom or right side of board.
USB A: solder side (BOTTOM)
mini B: component side (TOP)
mini B: component side (BOTTOM)
LAYOUT CONNECTOR PRIORITY: 1 - J1 (HSD) 2 - J2 (mini B TOP) 3 - J6, J7 (SMA)* 4 - J3 (mini B BOT) Layout J1, J2, J3, J6, J7 with same spacing as DS90UR905 demo board.
100 ohm differential impedance +/-5%.
50 ohm single ended impedance traces
0.625"
HSD_2X2_open
mini USB 5pin
SMA_open
5pin_open
SW DIP-3
VDD_I2C
VDD_T2C
VDDIO
VSS

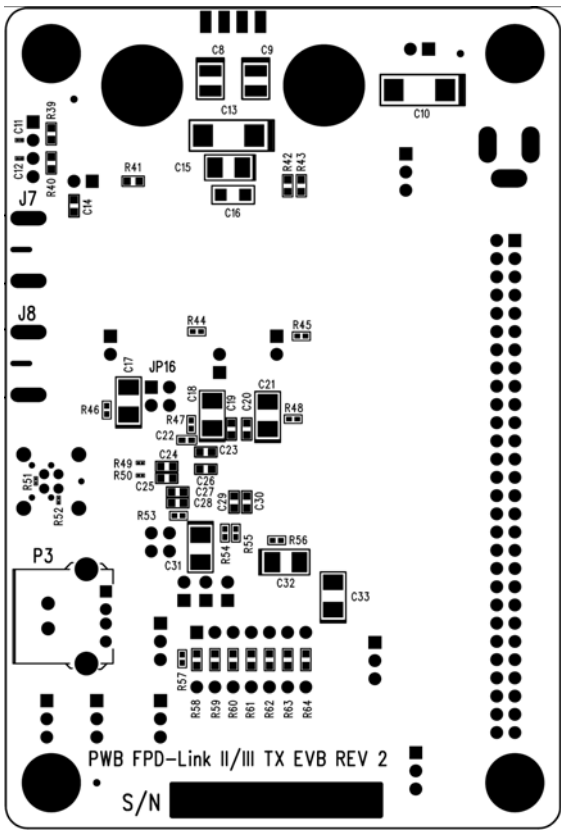

Title
DS90UR906 Rx Demo Board - Parallel Output
Size
A
Document Number
DS90UR906 Rx Demo Board
Rev
2
Date:
Friday, October 09, 2009
Sheet
3
of
4
USER NOTE:
JUMPER STRAP TO VDDIO
TO LOAD STRAP VALUES
OTHERWISE JUMPER
STRAP TO VSS.
JP18
VDDIOc
STRAP
VSS
P1
HEADER 28X2
JP8
JP9
0402_orange_LED
LED1
0603_green_LED
LED2
STRAP
LOCK
PASS
PCLK
VDDIOc
VSS


1.8V INPUT POWER CONNECTOR
OPTIONAL 5V INPUT POWER CONNECTOR
OPTIONAL 5V to 1.8V INPUT POWER REGULATOR
OPTIONAL 5V to 3.3V INPUT POWER REGULATOR
OPTIONAL External 3.3V input.
VDDIO=3.3V (external)
VDDIO=VDD (1.8V)
!!!WARNING!!! Input power thru only one connector!! Input power thru J5 OR J4 OR J3 OR J9 ONLY!!
FEATURES/OPTIONS ON THE DEMO BOARD:
- R40, R44, R46, R59, R60 series 0402 size pads
1) Provided for easy separation of each VDD domain (not a user requirement).
This will allow individual IDD current measurements. (Loaded with 0 ohm resistors)
2) This also allows insertion of series inductor in each VDD domain (not a user requirement), for noise reduction experimentation.
- C13-C27 decoupling capacitors 0603 and B size pads
1) It is not a requirement that the user must have all these capacitors and power separations in the user layout. The extra capacitors and power separations are provided for ease of experimentation. It is easier to un-populate than to add capacitors and pads after the fact.
2) See "Typical Connection Diagram Tx - User Reference" for recommended minimum power grouping and decoupling.
Title
DS90UR906 Rx Demo Board - Power and Decoupling
Size
Document Number
DS90UR906 Rx Demo Board
Rev
2
Date: Friday, September 18, 2009
Sheet 4 of 4

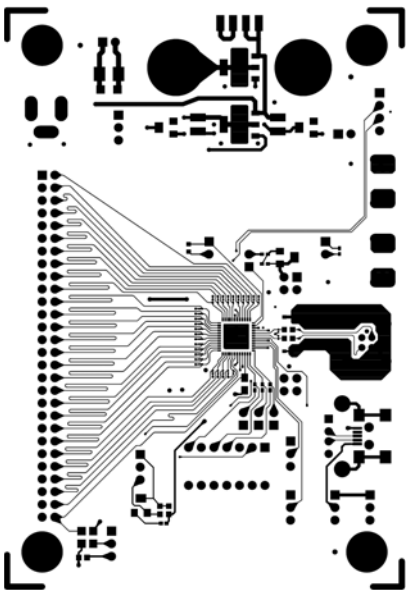
Serializer (Tx) Demo PCB Layout:



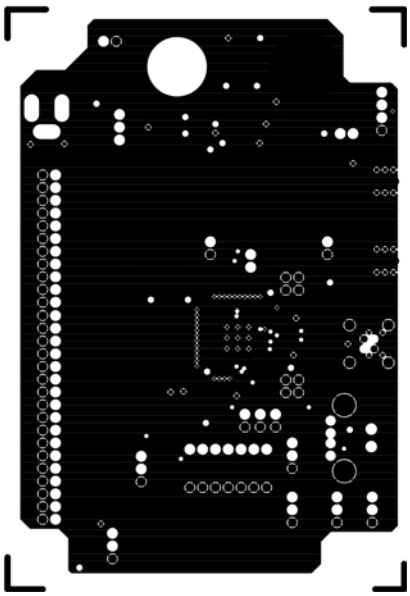
TOP VIEW



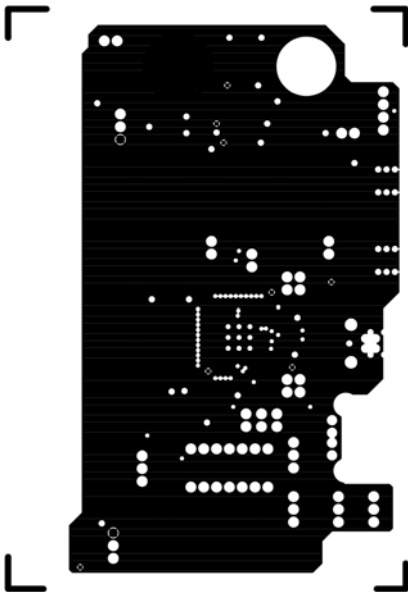
BOTTOMSIDE VIEW



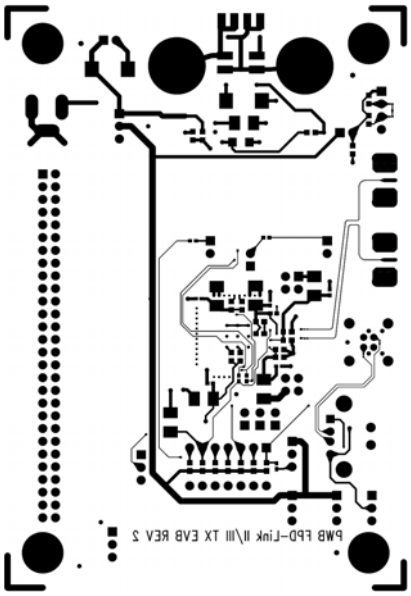
PRIMARY COMPONENT SIDE – LAYER 1



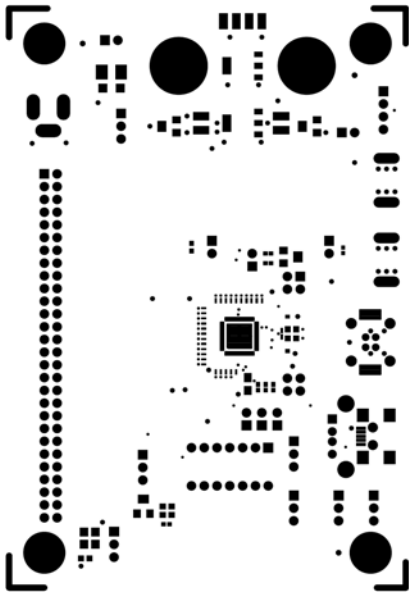
GROUND PLANE (VSS) – LAYER 2



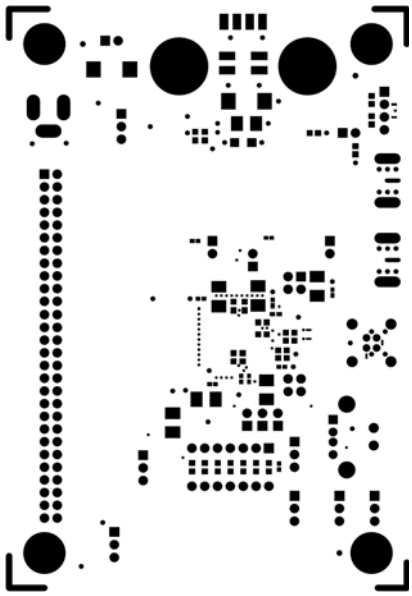
POWER PLANE (VDD) – LAYER 3



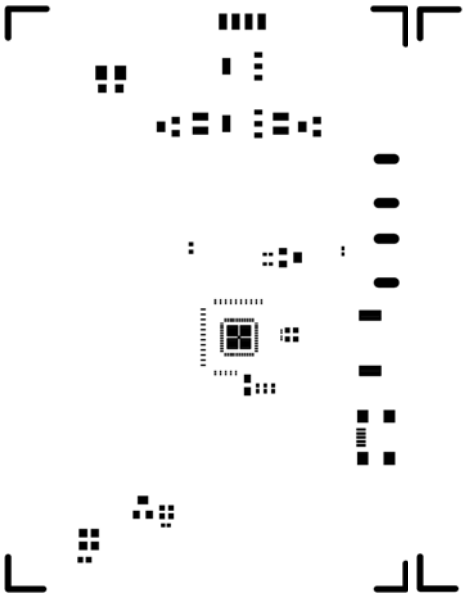
SECONDARY COMP SIDE – LAYER 4



PRIMARY COMP SIDE – SOLDER MASK (LAYER 1)

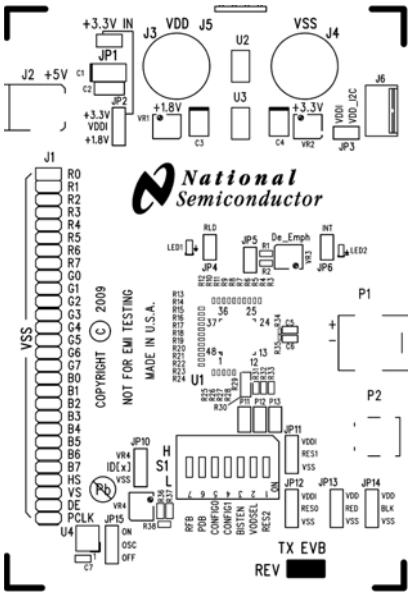


SECONDARY COMP SIDE – SOLDER MASK (LAYER 4)

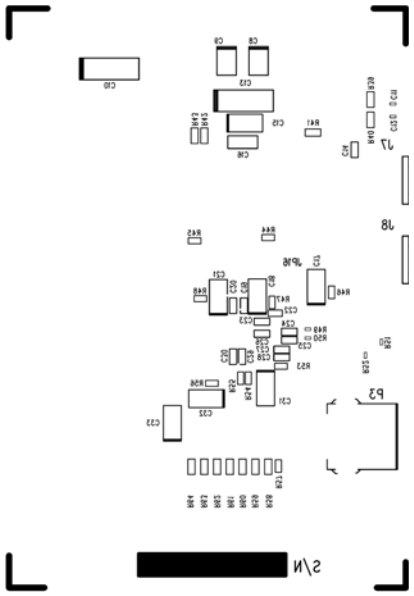


PRIMARY COMP SIDE – SOLDER PASTE (LAYER 1)

SECONDARY COMP SIDE – SOLDER PASTE (LAYER 4)

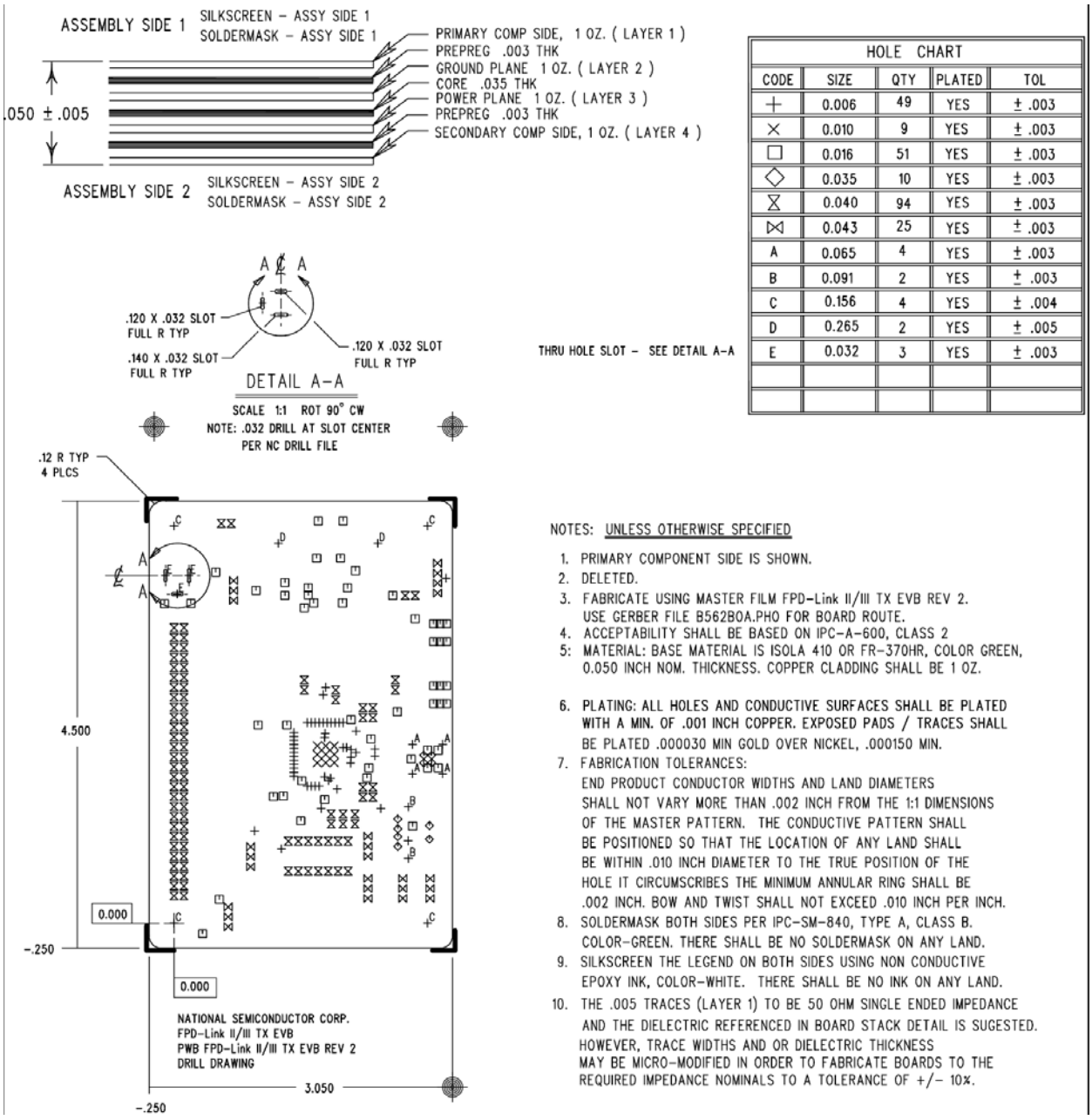


PRIMARY COMP SIDE – SILKSCREEN (LAYER 1)



SILKSCREEN COMP SIDE – SILKSCREEN (LAYER 4)

Serializer (Tx) Demo PCB Stackup:

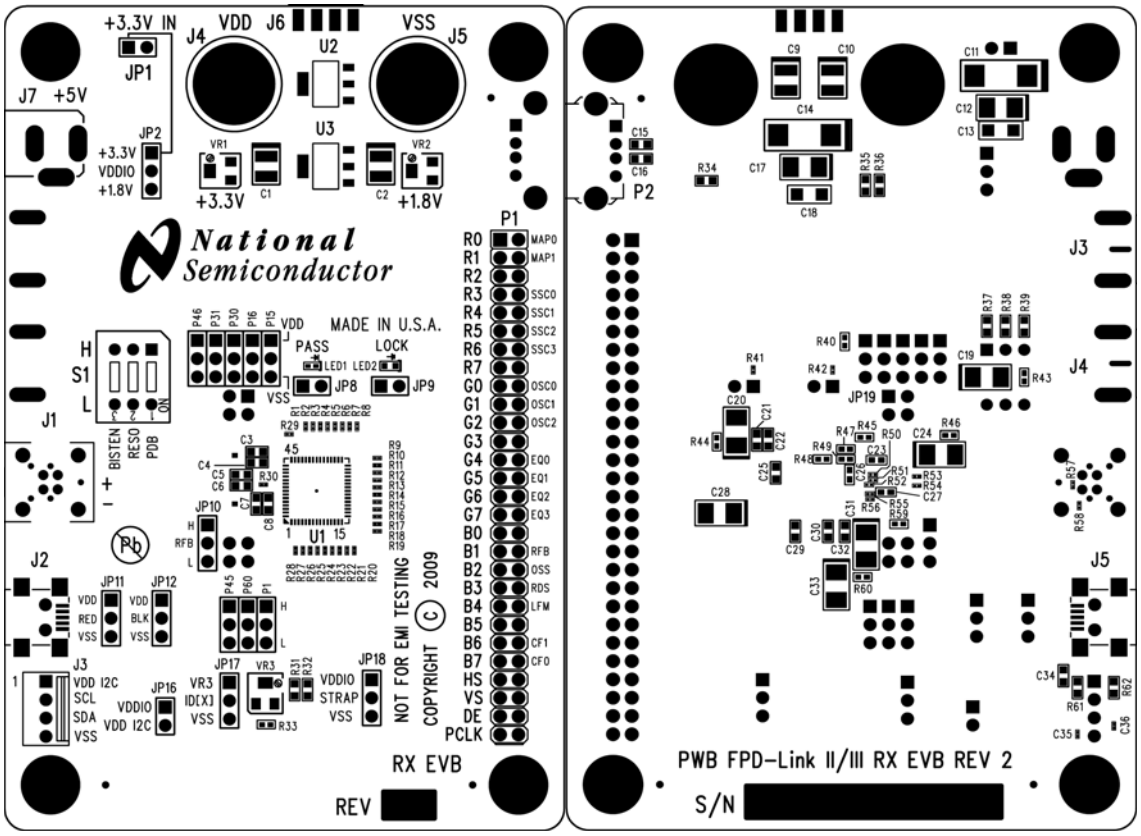


HOLE CHART				
CODE	SIZE	QTY	PLATED	TOL
+	0.006	49	YES	± .003
×	0.010	9	YES	± .003
□	0.016	51	YES	± .003
◇	0.035	10	YES	± .003
⧖	0.040	94	YES	± .003
⋈	0.043	25	YES	± .003
A	0.065	4	YES	± .003
B	0.091	2	YES	± .003
C	0.156	4	YES	± .004
D	0.265	2	YES	± .005
E	0.032	3	YES	± .003

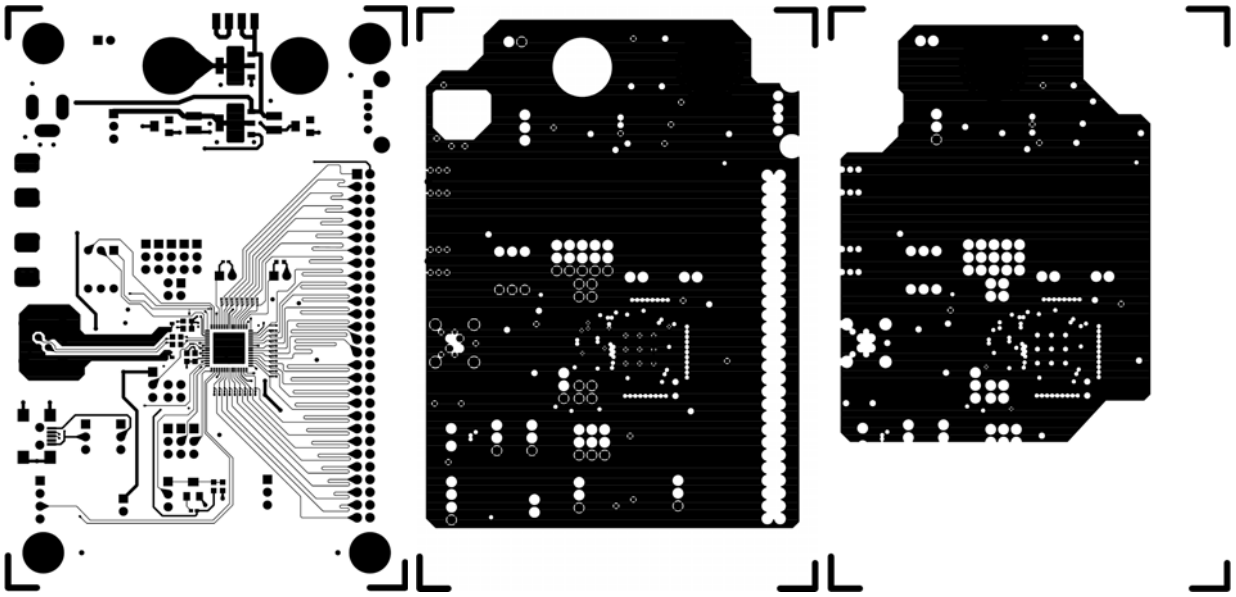
NOTES: UNLESS OTHERWISE SPECIFIED

1. PRIMARY COMPONENT SIDE IS SHOWN.
2. DELETED.
3. FABRICATE USING MASTER FILM FPD–Link II/III TX EVB REV 2. USE GERBER FILE B562BOA.PHO FOR BOARD ROUTE.
4. ACCEPTABILITY SHALL BE BASED ON IPC–A–600, CLASS 2
5. MATERIAL: BASE MATERIAL IS ISOLA 410 OR FR–370HR, COLOR GREEN, 0.050 INCH NOM. THICKNESS. COPPER CLADDING SHALL BE 1 OZ.
6. PLATING: ALL HOLES AND CONDUCTIVE SURFACES SHALL BE PLATED WITH A MIN. OF .001 INCH COPPER. EXPOSED PADS / TRACES SHALL BE PLATED .000030 MIN GOLD OVER NICKEL, .000150 MIN.
7. FABRICATION TOLERANCES: END PRODUCT CONDUCTOR WIDTHS AND LAND DIAMETERS SHALL NOT VARY MORE THAN .002 INCH FROM THE 1:1 DIMENSIONS OF THE MASTER PATTERN. THE CONDUCTIVE PATTERN SHALL BE POSITIONED SO THAT THE LOCATION OF ANY LAND SHALL BE WITHIN .010 INCH DIAMETER TO THE TRUE POSITION OF THE HOLE IT CIRCUMSCRIBES THE MINIMUM ANNULAR RING SHALL BE .002 INCH. BOW AND TWIST SHALL NOT EXCEED .010 INCH PER INCH.
8. SOLDERMASK BOTH SIDES PER IPC–SM–840, TYPE A, CLASS B. COLOR–GREEN. THERE SHALL BE NO SOLDERMASK ON ANY LAND.
9. SILKSCREEN THE LEGEND ON BOTH SIDES USING NON CONDUCTIVE EPOXY INK, COLOR–WHITE. THERE SHALL BE NO INK ON ANY LAND.
10. THE .005 TRACES (LAYER 1) TO BE 50 OHM SINGLE ENDED IMPEDANCE AND THE DIELECTRIC REFERENCED IN BOARD STACK DETAIL IS SUGESTED. HOWEVER, TRACE WIDTHS AND OR DIELECTRIC THICKNESS MAY BE MICRO–MODIFIED IN ORDER TO FABRICATE BOARDS TO THE REQUIRED IMPEDANCE NOMINALS TO A TOLERANCE OF +/– 10%.

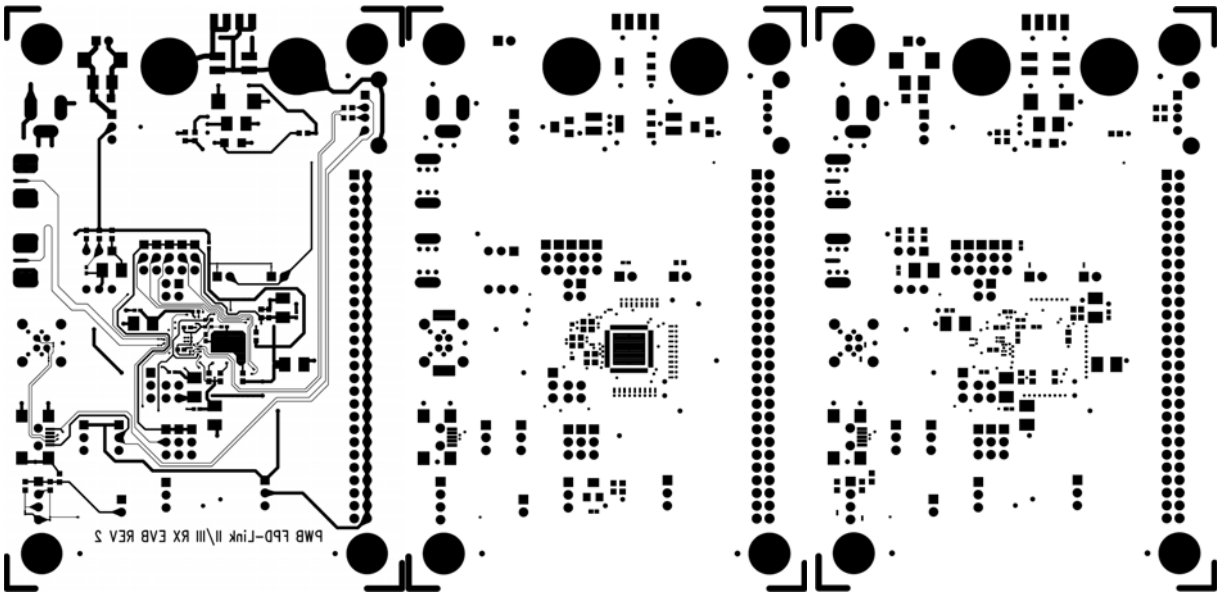
Deserializer (Rx) Demo PCB Layout:



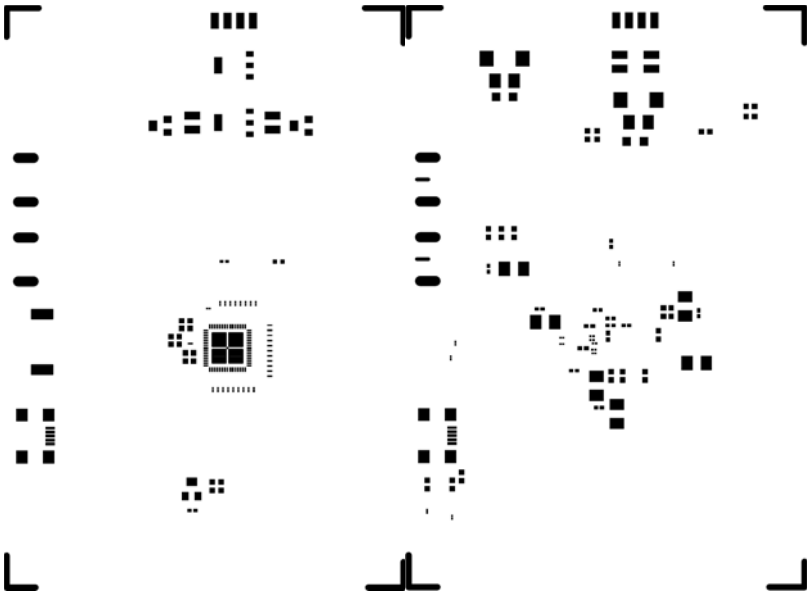
TOP VIEW BOTTOMSIDE VIEW



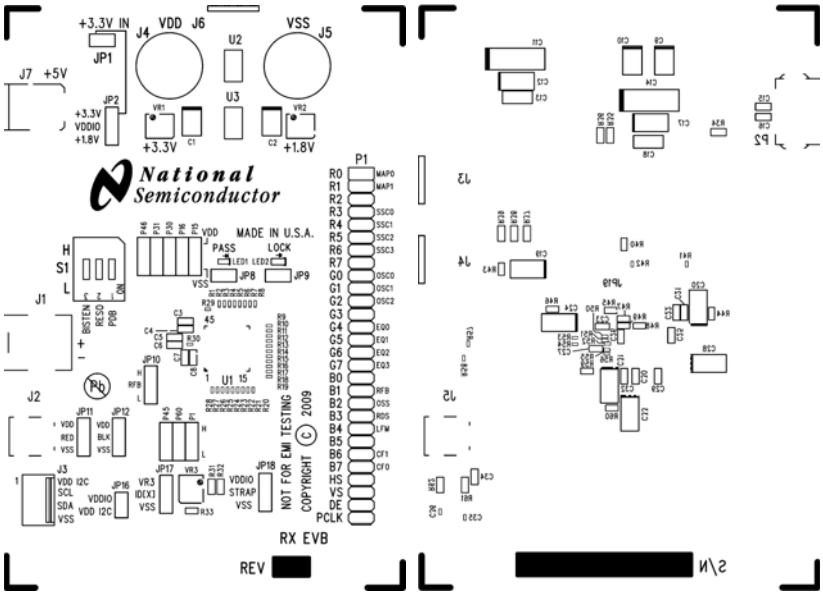
PRIMARY COMPONENT SIDE – LAYER 1 GROUND PLANE (VSS) – LAYER 2 POWER PLANE (VDD) – LAYER 3



SECONDARY COMP SIDE – LAYER 4 PRIMARY COMP SIDE – SOLDER MASK (LAYER 1) SECONDARY COMP SIDE – SOLDER MASK (LAYER 4)

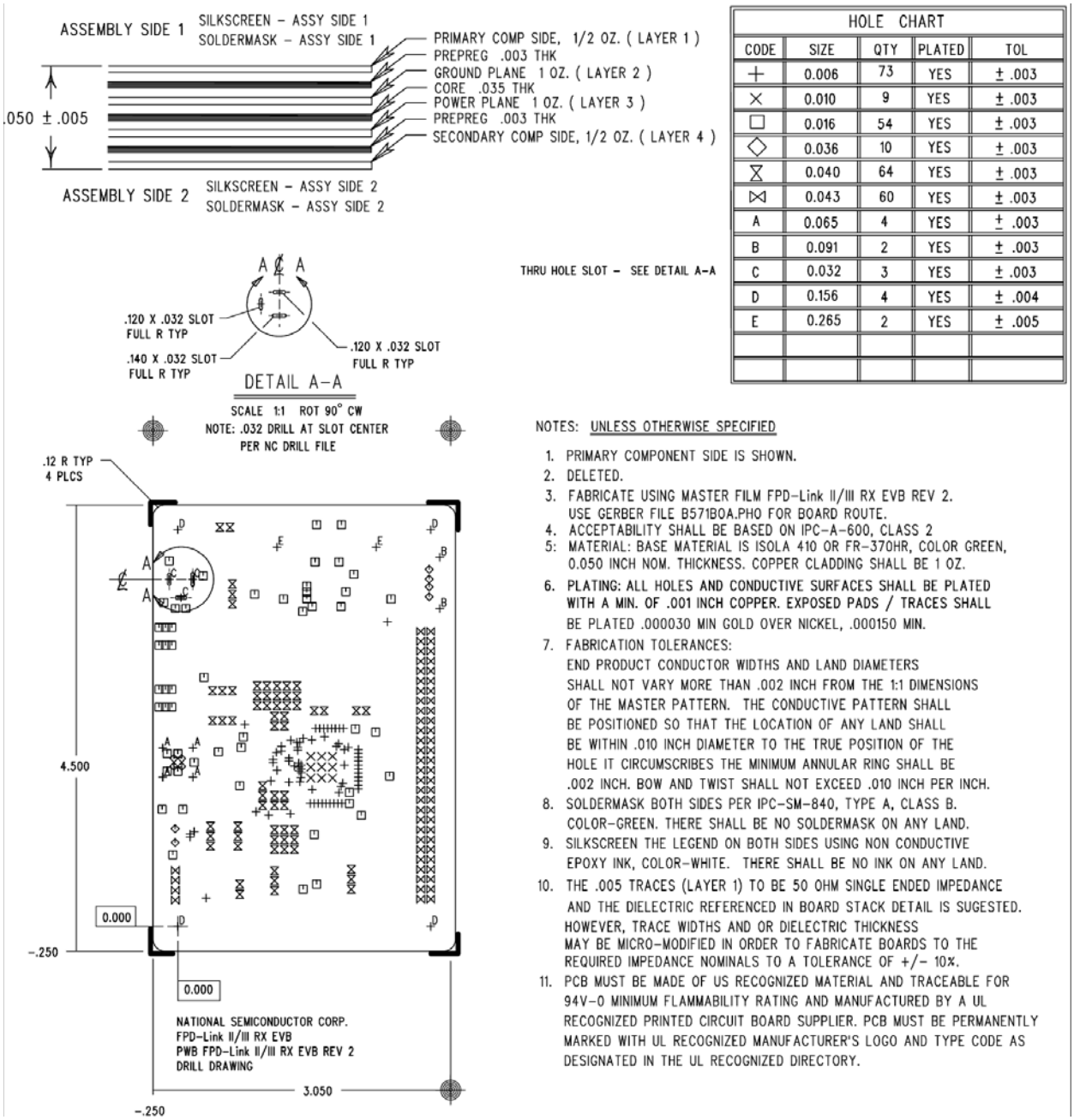


PRIMARY COMP SIDE – SOLDER PASTE (LAYER 1) SECONDARY COMP SIDE – SOLDER PASTE (LAYER 4)



PRIMARY COMP SIDE – SILKSCREEN (LAYER 1) SILKSCREEN COMP SIDE – SILKSCREEN (LAYER 4)

Deserializer (Rx) Demo PCB Stackup:



HOLE CHART				
CODE	SIZE	QTY	PLATED	TOL
+	0.006	73	YES	± .003
×	0.010	9	YES	± .003
□	0.016	54	YES	± .003
◇	0.036	10	YES	± .003
⧖	0.040	64	YES	± .003
⋈	0.043	60	YES	± .003
A	0.065	4	YES	± .003
B	0.091	2	YES	± .003
C	0.032	3	YES	± .003
D	0.156	4	YES	± .004
E	0.265	2	YES	± .005

NOTES: UNLESS OTHERWISE SPECIFIED

1. PRIMARY COMPONENT SIDE IS SHOWN.
2. DELETED.
3. FABRICATE USING MASTER FILM FPD–Link II/III RX EVB REV 2. USE GERBER FILE B571BOA.PHO FOR BOARD ROUTE.
4. ACCEPTABILITY SHALL BE BASED ON IPC–A–600, CLASS 2
5. MATERIAL: BASE MATERIAL IS ISOLA 410 OR FR–370HR, COLOR GREEN, 0.050 INCH NOM. THICKNESS. COPPER CLADDING SHALL BE 1 OZ.
6. PLATING: ALL HOLES AND CONDUCTIVE SURFACES SHALL BE PLATED WITH A MIN. OF .001 INCH COPPER. EXPOSED PADS / TRACES SHALL BE PLATED .000030 MIN GOLD OVER NICKEL, .000150 MIN.
7. FABRICATION TOLERANCES: END PRODUCT CONDUCTOR WIDTHS AND LAND DIAMETERS SHALL NOT VARY MORE THAN .002 INCH FROM THE 1:1 DIMENSIONS OF THE MASTER PATTERN. THE CONDUCTIVE PATTERN SHALL BE POSITIONED SO THAT THE LOCATION OF ANY LAND SHALL BE WITHIN .010 INCH DIAMETER TO THE TRUE POSITION OF THE HOLE IT CIRCUMSCRIBES THE MINIMUM ANNULAR RING SHALL BE .002 INCH. BOW AND TWIST SHALL NOT EXCEED .010 INCH PER INCH.
8. SOLDERMASK BOTH SIDES PER IPC–SM–840, TYPE A, CLASS B. COLOR–GREEN. THERE SHALL BE NO SOLDERMASK ON ANY LAND.
9. SILKSCREEN THE LEGEND ON BOTH SIDES USING NON CONDUCTIVE EPOXY INK, COLOR–WHITE. THERE SHALL BE NO INK ON ANY LAND.
10. THE .005 TRACES (LAYER 1) TO BE 50 OHM SINGLE ENDED IMPEDANCE AND THE DIELECTRIC REFERENCED IN BOARD STACK DETAIL IS SUGESTED. HOWEVER, TRACE WIDTHS AND OR DIELECTRIC THICKNESS MAY BE MICRO–MODIFIED IN ORDER TO FABRICATE BOARDS TO THE REQUIRED IMPEDANCE NOMINALS TO A TOLERANCE OF +/– 10%.
11. PCB MUST BE MADE OF US RECOGNIZED MATERIAL AND TRACEABLE FOR 94V–0 MINIMUM FLAMMABILITY RATING AND MANUFACTURED BY A UL RECOGNIZED PRINTED CIRCUIT BOARD SUPPLIER. PCB MUST BE PERMANENTLY MARKED WITH UL RECOGNIZED MANUFACTURER'S LOGO AND TYPE CODE AS DESIGNATED IN THE UL RECOGNIZED DIRECTORY.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

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