# AN–1357 LM2744 Evaluation Board

## 1 Introduction

This application note describes the LM2743 printed circuit board (PCB) design and provides an example typical application circuit. The demo board allows component design flexibility in order to demonstrate the versatility of the LM2744 IC.

The demo board contains a voltage-mode, high-speed synchronous buck regulator controller with an external adjustable reference voltage between 0.5V and 1.5V. The demo board design incorporates the LM4140 high precision low noise reference IC providing 1.0V to the reference pin ($V_{REF}$). Though the control sections of the IC are rated for 3 to 6V ($V_{CC}$), the driver sections are designed to accept input supply rails ($V_{IN}$) as high as 14V. It operates at a fixed-frequency, adjustable from 50 kHz to 1 MHz with one external resistor.

The demo board design regulates to an output voltage of 1.2V at 3.5A with a switching frequency of 1MHz. Note, the demo board is optimized for a 1MHz, 14V input voltage compensation design; if another switching frequency and input voltage is desired, please consult the LM2744 data sheet for control loop compensation procedures. For additional design modifications refer to the Design Consideration section of the *LM2744 Low Voltage N-Channel MOSFET Synchronous Buck Regulator Controller with External Reference* SNVS292 data sheet.

## 2 Additional Footprints

A Schottky diode footprint (D1) is available in parallel to the low side MOSFET. This component can improve efficiency, due to the lower forward drop than the low side MOSFET body diode conducting during the anti-shoot through period. Select a Schottky diode that maintains a forward drop around 0.4 to 0.6V at the maximum load current (consult the I-V curve). In addition select the reverse breakdown voltage to have sufficient margin above the maximum input voltage.

Footprint C13 is available for a multilayer ceramic capacitor (MLCC) connected as close as possible to the source of the low side MOSFET and drain of the high side MOSFET. This will provide low supply impedance to the high speed switch currents, thus minimizing the input supply noise. For example; a MLCC is used (C13) in combination with aluminum electrolytic input filter capacitors, placed in designators C12 and C14, because MLCC have lower impedance than electrolytics. If MLCCs are used in designators C12 and C14 component C13 is not necessary.

The PCB is designed on two layers with 1oz. copper on a 62mil FR4 laminate.

## 3 Guidelines for Additional Options

When using a DC power supply to set a reference voltage ($V_{REF}$), connect a capacitor (C20) from $V_{DCS}$ to GND to filter the DC power supply. A good starting point is 10µF, but may need to be varied depending on the magnitude of the DC power supply noise (any make of capacitor will do as long as the capacitance is maintained within the operating temperature range). Remove R10 and place a zero ohm jumper in designator R12 .

Designators R12 and R13 are provided for DDR SDRAM (double data rate synchronous dynamic random access memory) active termination design. Set $V_{REF}$ to half the DDR supply voltage by using designators R12 and R13 as a voltage divider. Remove resistors R7, R10 and capacitor C21, and connect the DDR supply voltage rail to terminal $V_{DCS}$, refer to Figure 2. The modified circuit in Figure 1 can sink or source current in excess of 3A – a load transient response applied to the output of Figure 2 is provided in Figure 3.

Do not exceed 5.6V on the VCC pin of the demo board. The board layout connects together both the input voltage of the LM4140-1.0 (pin 2) and the control section of the LM2744 (VCC). The maximum DC supply voltage for the control section of the LM2744 is 6V, while 5.6V is the maximum rating for any input pin of the LM4140. If the design requires the control section of the LM2744 to be 6V, a shunt zener reference may be placed at designator location (D3) to maintain the input voltage of the LM4140 between 1.8V and 5.5V. The cathode of the zener is connected to the input of the LM4140 and the anode to GND. The resistance of R10 must be selected to supply the appropriate amount of biasing current into the zener and the LM4140 (refer to the Electrical Characteristic table of the *LM4140 High Precision Low Noise Low Dropout Voltage Reference* LM4140 data sheet).

## 4 Typical Application Circuit

The typical application circuit in Figure 1 provides the component designators used on the demo board.

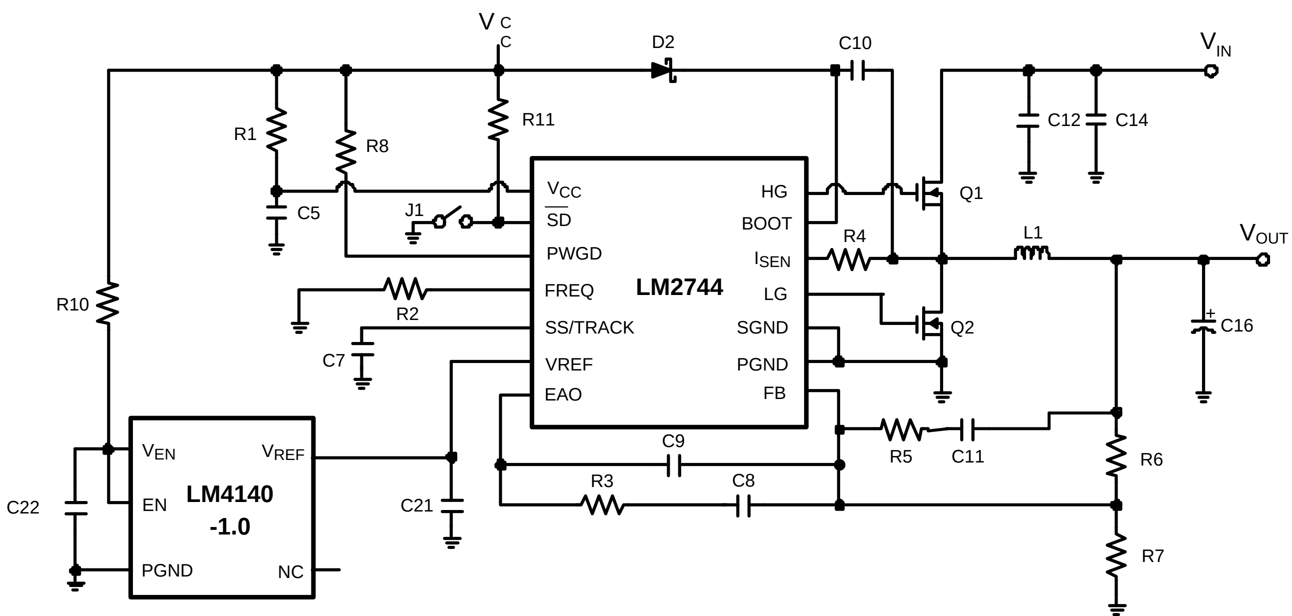


**Figure 1. Typical Application**

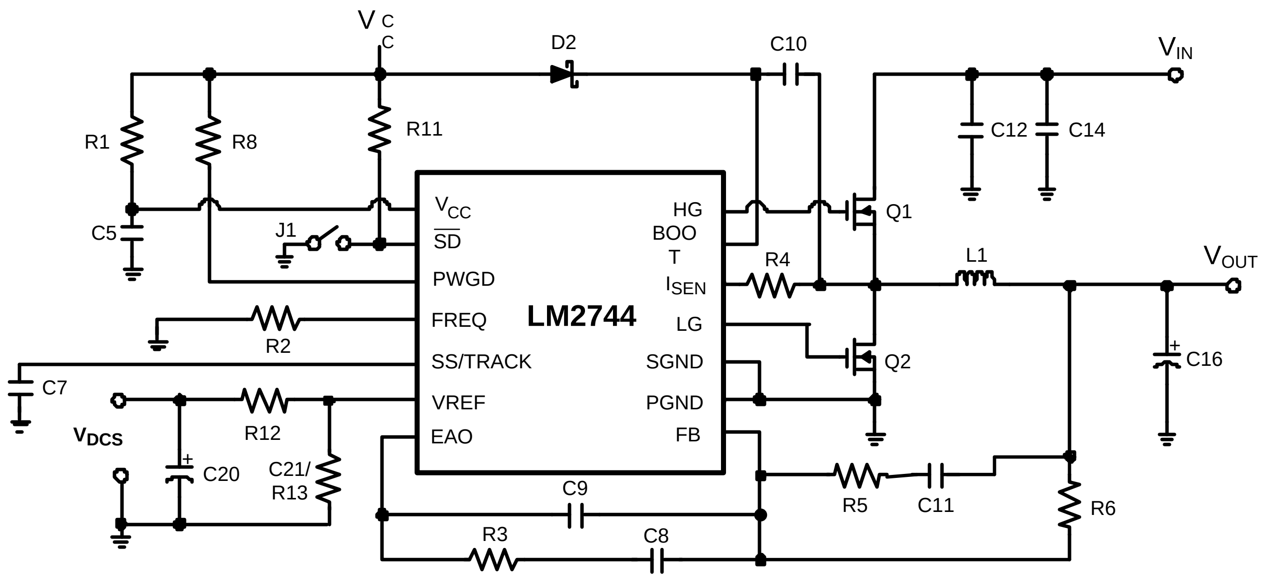


**Figure 2. DDR SDRAM Termination Supply**

# 5 Performance Characteristics

## *5.1 Load Transient Response*

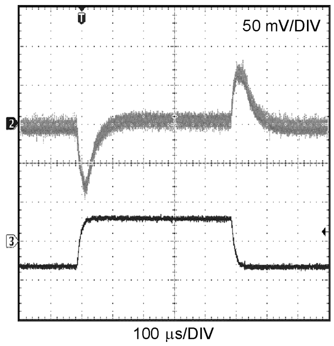


**Figure 3. ± 3A Load Transient Response Applied to circuit in Figure 2 ($V_{IN}$ = $V_{CC}$ = 3.3V and $V_{OUT}$ = 1.2V). CH 2 - $V_{OUT}$ AC coupled and CH 3 - 5A/ DIV**

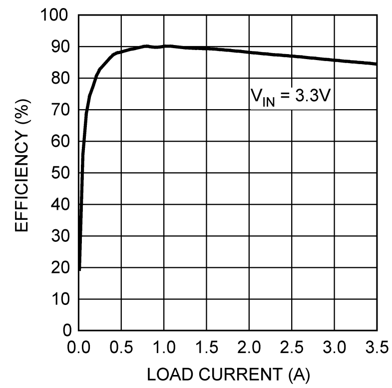


**Figure 4. Efficiency vs. Load Current $V_{OUT}$ = 1.2V, $f_{SW}$ = 1MHz**

## *5.2 Switch Node Voltage and Output Ripple Voltage*

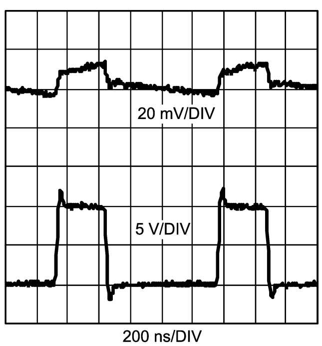


**Figure 5. $V_{IN}$ = $V_{CC}$ = 3.3V, $V_{OUT}$ = 1.2V, $I_{LOAD}$ = 0A, $f_{SW}$ = 1MHz. 20 MHz Bandwidth Limit**

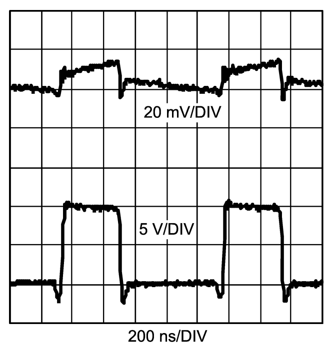


**Figure 6. $V_{IN}$ = $V_{CC}$ = 3.3V, $V_{OUT}$ = 1.2V, $I_{LOAD}$ = 3.5A, $f_{SW}$ = 1MHz. 20 MHz Bandwidth Limit**

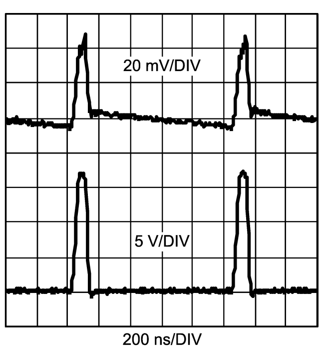


**Figure 7. $V_{IN}$ = 14V, $V_{CC}$ = 5V, $V_{OUT}$ = 1.2V, $I_{LOAD}$ = 0A, $f_{SW}$ = 1MHz. 20 MHz Bandwidth Limit**

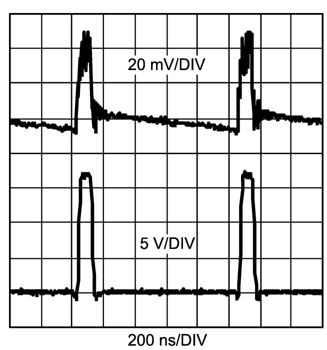


**Figure 8. $V_{IN}$ = 14V, $V_{CC}$ = 5V, $V_{OUT}$ = 1.2V, $I_{LOAD}$ = 3.5A, $f_{SW}$ = 1MHz. 20 MHz Bandwidth Limit**

### Table 1. Bill of Materials

| Designator | Function | Part Description | Part Number |
|---|---|---|---|
| U1 | Controller | IC LM2744 TSSOP14 | Texas Instruments |
| U2 | Low Dropout Reg | IC LM4140BCM-1.0 SOIC-8 | Texas Instruments |
| C5 | VCC Decoupling | Cer Cap 1µF 25V 10% 0805 | Murata GRM216R61E105KA12B |
| C7 | Soft Start Cap | Cer Cap 12nF 25V 10% 0805 | Vishay VJ0805Y123KXX |
| C8 | Comp Cap | Cer Cap 1.2nF 25V 10% 0805 | Vishay VJ0805Y122KXX |
| C9 | Comp Cap | Cer Cap 15pF 50V 10% 0805 | Vishay VJ0805A150KAA |
| C10 | Cboot | Cer Cap 0.1µF 25V 10% 0805 | Vishay VJ0805Y104KXX |
| C11 | Comp Cap | Cer Cap 1.8nF 25V 10% 0805 | Vishay VJ0805Y182KXX |
| C12 | Input Filter Cap | Cer Cap 10uF 25V 10% 1210 | AVX 12103D106MAT |
| C14 | Input Filter Cap | Cer Cap 10uF 25V 10% 1210 | AVX 12103D106MAT |
| C16 | Output Filter Cap | 470uF, 6.3V, 10m ohm ESR POScap | Sanyo 6TPD470 |
| C21 | Reference Output Cap | Niobium Oxide Cap 4.7µF 6V | AVX NOJA475M0006R |
| C22 | Reference Input Cap | Cer Cap 0.47µF 25V 10% 1206 | Vishay VJ1206Y474KXX |
| R1 | VCC Filter Res | Res 10Ω .25W 0805 | Vishay CRCW08051000F |
| R2 | Frequency Adjust Res | Res 24.9KΩ .25W 0805 | Vishay CRCW08052492F |
| R3 | Comp Res | Res 21KΩ .25W 0805 | Vishay CRCW08052102F |
| R4 | Current Limit Res | Res 3.16KΩ .25W 0805 | Vishay CRCW08053161F |
| R5 | Comp Res | Res 2.94KΩ .25W 0805 | Vishay CRCW08052941F |
| R6 | Res Divider, upper | Res 10.0KΩ .25W 0805 | Vishay CRCW08051002F |
| R7 | Res Divider, lower | Res 59KΩ .25W 0805 | Vishay CRCW08055902F |
| R8 | PWGD Pull-Up | Res 100KΩ .25W 0805 | Vishay CRCW08051003F |
| R10 | Zero Ohm | Res 0Ω 0805 | Vishay CRCW08050000 |
| R11 | Shut Down Pull-Up | Res 100KΩ .25W 0805 | Vishay CRCW12061003F |
| D2 | Bootstrap Diode | Schottky Diode, SOD-123 | MBR0530LTI |
| L1 | Output Filter Inductor | Inductor 1µH, 5.3Arms, 10.2mΩ | Cooper DR73-1R0 |
| Q1-Q2 | Top and Bottom FETs | Dual N-MOSFET, $V_{DS}$ = 20V, 24mΩ at 2.5V | Vishay 9926BDY |

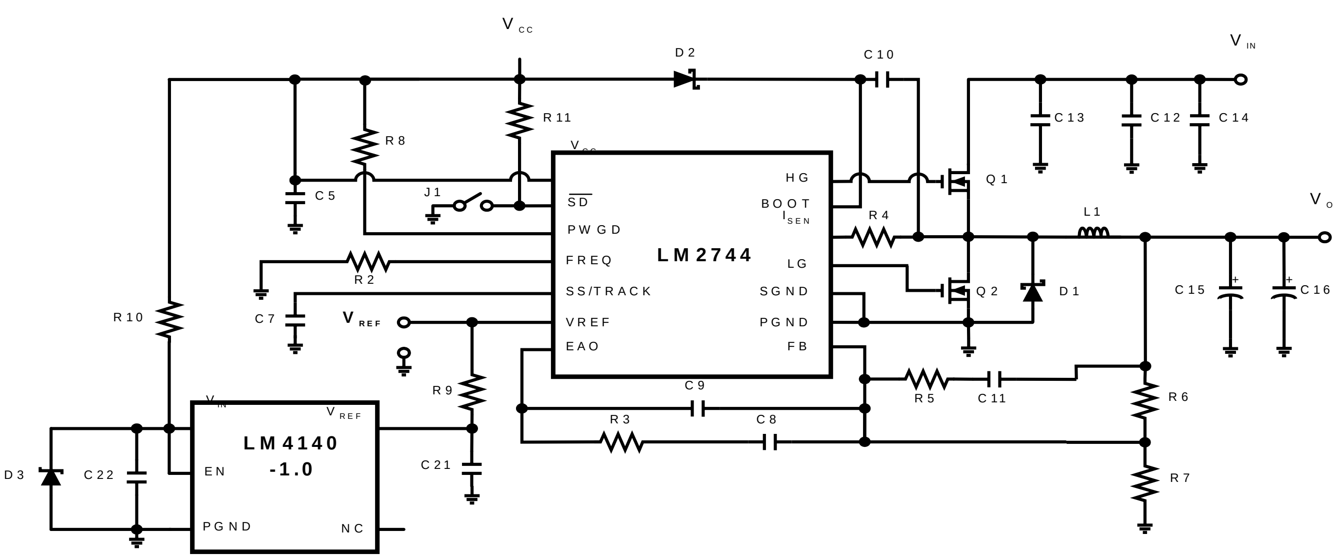


**Figure 9. Complete Demo Board Schematic**

# 6 PCB Layout Diagram(s)

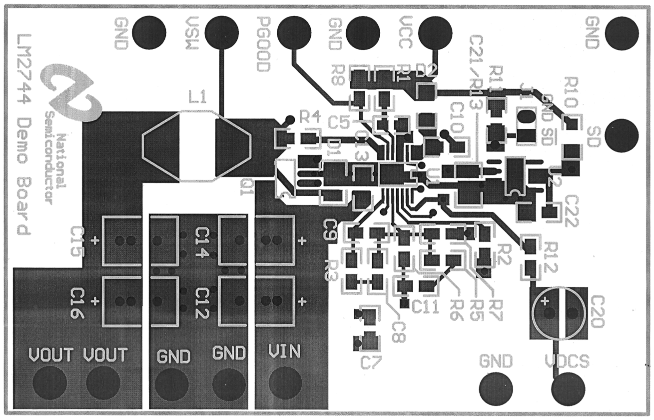


**Figure 10. Top Layer and Top Overlay**

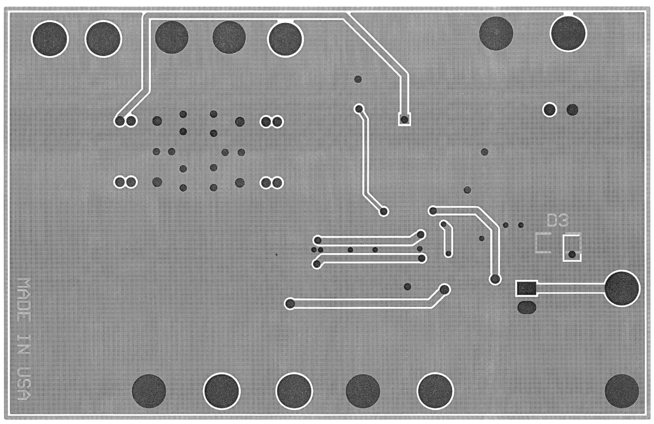

**Figure 11. Bottom Layer**

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