Tiva™ TM4C129DNCPDT Microcontroller

TECHNICAL BRIEF

TB-TM4C129DNCPDT-15443.2698
SPMT299

Copyright

ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Texas Instruments Incorporated
108 Wild Basin, Suite 350
Austin, TX 78746
http://www.ti.com/tm4c
http://www-k.ext.ti.com/sc/technical-support/product-information-centers.htm

WARNING – EXPORT NOTICE: Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from Disclosing party under this Agreement, or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

According to our best knowledge of the state and end-use of this product or technology, and in compliance with the export control regulations of dual-use goods in force in the origin and exporting countries, this technology is classified as follows:

- **US ECCN: EAR99**
- **EU ECCN: EAR99**

And may require export or re-export license for shipping it in compliance with the applicable regulations of certain countries.

Table of Contents

List of Figures

List of Tables

1 Architectural Overview

Texas Instrument's Tiva™ C Series microcontrollers provide designers a high-performance ARM® Cortex™-M-based architecture with a broad set of integration capabilities and a strong ecosystem of software and development tools. Targeting performance and flexibility, the Tiva™ C Series architecture offers a 120 MHz Cortex-M with FPU, a variety of integrated memories and multiple programmable GPIO. Tiva™ C Series devices offer consumers compelling cost-effective solutions by integrating application-specific peripherals and providing a comprehensive library of software tools which minimize board costs and design-cycle time. Offering quicker time-to-market and cost savings, the Tiva™ C Series microcontrollers are the leading choice in high-performance 32-bit applications.

This chapter contains an overview of the Tiva™ C Series microcontrollers as well as details on the TM4C129DNCPDT microcontroller:

1.1 Tiva™ C Series Overview

The Tiva™ C Series ARM Cortex-M4 microcontrollers provide top performance and advanced integration. The product family is positioned for cost-effective applications requiring significant control processing and connectivity capabilities such as:

- Industrial communication equipment
- Network appliances, gateways & adapters
- Residential & commercial site monitoring & control
- Remote connectivity & monitoring
- Security/access systems
- HMI control panels
- Factory automation control
- Test and measurement equipment
- Fire & security systems
- Motion control & power inversion
- Medical instrumentation
- Gaming equipment
- Electronic point-of-sale (POS) displays
- Smart Energy/Smart Grid solutions
- Intelligent lighting control
- Vehicle tracking

Tiva™ C Series microcontrollers integrate a large variety of rich communication features to enable a new class of highly connected designs with the ability to allow critical, real-time control between performance and power. The microcontrollers feature integrated communication peripherals along with other high-performance analog and digital functions to offer a strong foundation for many

different target uses, spanning from human machine interface to networked system management controllers.

In addition, Tiva™ C Series microcontrollers offer the advantages of ARM's widely available development tools, System-on-Chip (SoC) infrastructure, and a large user community. Additionally, these microcontrollers use ARM's Thumb®-compatible Thumb-2 instruction set to reduce memory requirements and, thereby, cost. Finally, the TM4C129DNCPDT microcontroller is code-compatible to all members of the extensive Tiva™ C Series, providing flexibility to fit precise needs.

Texas Instruments offers a complete solution to get to market quickly, with evaluation and development boards, white papers and application notes, an easy-to-use peripheral driver library, and a strong support, sales, and distributor network.

1.2 TM4C129DNCPDT Microcontroller Overview

The TM4C129DNCPDT microcontroller combines complex integration and high performance with the features shown in Table 1-1.

Table 1-1. TM4C129DNCPDT Microcontroller Features

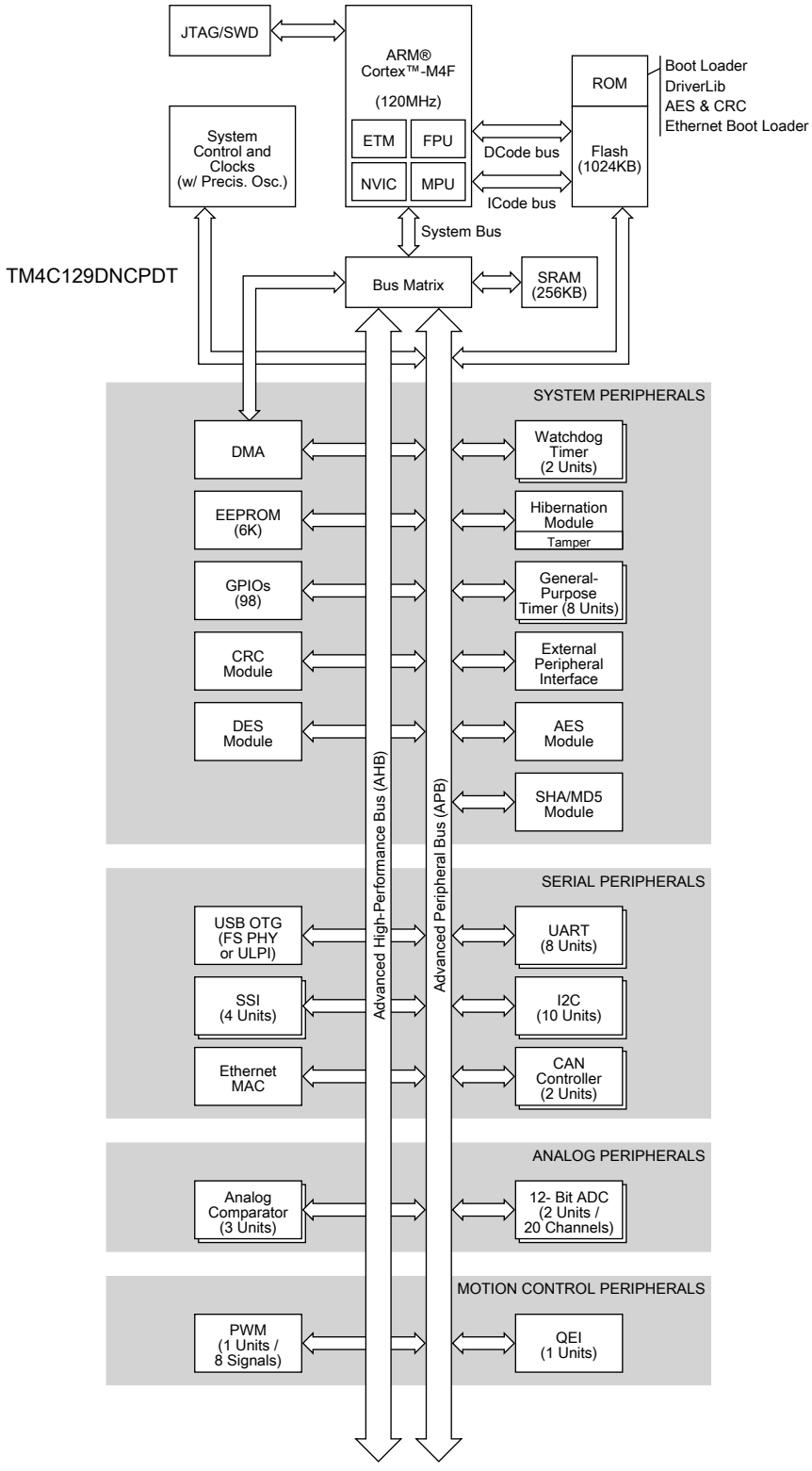
Feature	Description
Performance	
Core	ARM Cortex-M4F processor core
Performance	120-MHz operation; 150 DMIPS performance
Flash	1024 KB Flash memory
System SRAM	256 KB single-cycle System SRAM
EEPROM	6KB of EEPROM
Internal ROM	Internal ROM loaded with TivaWare™ for C Series software
External Peripheral Interface (EPI)	8-/16-/32- bit dedicated interface for peripherals and memory
Security	
Cyclical Redundancy Check (CRC) Hardware	16-/32-bit Hash function that supports four CRC forms
Advanced Encryption Standard (AES)	Hardware accelerated data encryption and decryption based on 128-, 192-, and 256-bit keys
Data Encryption Standard (DES)	Block cipher implementation with 168-bit effective key length
Hardware Accelerated Hash (SHA/MD5)	Advanced hash engine that supports SHA-1, SHA-2 or MD5 Hash computation
Tamper	Support for four tamper inputs and configurable tamper event response
Communication Interfaces	
Universal Asynchronous Receivers/Transmitter (UART)	Eight UARTs
Quad Synchronous Serial Interface (QSSI)	Four SSI modules with Bi-, Quad- and advanced SSI support
Inter-Integrated Circuit (I^2C)	Ten I^2C modules with four transmission speeds including high-speed mode
Controller Area Network (CAN)	Two CAN 2.0 A/B controllers
Ethernet MAC	10/100 Ethernet MAC with Media Independent Interface (MII) and Reduced MII (RMII)
Universal Serial Bus (USB)	USB 2.0 OTG/Host/Device with ULPI interface option and Link Power Management (LPM) support
System Integration	
Micro Direct Memory Access (µDMA)	ARM® PrimeCell® 32-channel configurable µDMA controller

Table 1-1. TM4C129DNCPDT Microcontroller Features *(continued)*

Feature	Description
General-Purpose Timer (GPTM)	Eight 16/32-bit GPTM blocks
Watchdog Timer (WDT)	Two watchdog timers
Hibernation Module (HIB)	Low-power battery-backed Hibernation module
General-Purpose Input/Output (GPIO)	15 physical GPIO blocks
Advanced Motion Control	
Pulse Width Modulator (PWM)	One PWM module, with four PWM generator blocks and a control block, for a total of 8 PWM outputs.
Quadrature Encoder Interface (QEI)	One QEI module
Analog Support	
Analog-to-Digital Converter (ADC)	Two 12-bit ADC modules, each with a maximum sample rate of one million samples/second
Analog Comparator Controller	Three independent integrated analog comparators
Digital Comparator	16 digital comparators
JTAG and Serial Wire Debug (SWD)	One JTAG module with integrated ARM SWD
Package Information	
Package	128-pin TQFP
Operating Range (Ambient)	Industrial (-40°C to 85°C) temperature range Extended (-40°C to 105°C) temperature range

Figure 1-1 on page 9 shows the features on the TM4C129DNCPDT microcontroller. Note that there are two on-chip buses that connect the core to the peripherals. The Advanced Peripheral Bus (APB) bus is the legacy bus. The Advanced High-Performance Bus (AHB) bus provides better back-to-back access performance than the APB bus.

Figure 1-1. Tiva™ TM4C129DNCPDT Microcontroller High-Level Block Diagram



1.3 TM4C129DNCPDT Microcontroller Features

The TM4C129DNCPDT microcontroller component features and general function are discussed in more detail in the following section.

1.3.1 ARM Cortex-M4F Processor Core

All members of the Tiva™ C Series, including the TM4C129DNCPDT microcontroller, are designed around an ARM Cortex-M processor core. The ARM Cortex-M processor provides the core for a high-performance, low-cost platform that meets the needs of minimal memory implementation, reduced pin count, and low power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

1.3.1.1 Processor Core

- 32-bit ARM Cortex-M4F architecture optimized for small-footprint embedded applications
- 120-MHz operation; 150 DMIPS performance
- Outstanding processing performance combined with fast interrupt handling
- Thumb-2 mixed 16-/32-bit instruction set delivers the high performance expected of a 32-bit ARM core in a compact memory size usually associated with 8- and 16-bit devices, typically in the range of a few kilobytes of memory for microcontroller-class applications
  - Single-cycle multiply instruction and hardware divide
  - Atomic bit manipulation (bit-banding), delivering maximum memory utilization and streamlined peripheral control
  - Unaligned data access, enabling data to be efficiently packed into memory
- IEEE754-compliant single-precision Floating-Point Unit (FPU)
- 16-bit SIMD vector processing unit
- Fast code execution permits slower processor clock or increases sleep mode time
- Harvard architecture characterized by separate buses for instruction and data
- Efficient processor core, system and memories
- Hardware division and fast digital-signal-processing orientated multiply accumulate
- Saturating arithmetic for signal processing
- Deterministic, high-performance interrupt handling for time-critical applications
- Memory protection unit (MPU) to provide a privileged mode for protected operating system functionality
- Enhanced system debug with extensive breakpoint and trace capabilities
- Serial Wire Debug and Serial Wire Trace reduce the number of pins required for debugging and tracing

- Migration from the ARM7™ processor family for better performance and power efficiency
- Optimized for single-cycle Flash memory usage up to specific frequencies; see the data sheet for more information.
- Ultra-low power consumption with integrated sleep modes

1.3.1.2 System Timer (SysTick)

ARM Cortex-M4F includes an integrated system timer, SysTick. SysTick provides a simple, 24-bit, clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used in several different ways, for example:

- An RTOS tick timer that fires at a programmable rate (for example, 100 Hz) and invokes a SysTick routine
- A high-speed alarm timer using the system clock
- A variable rate alarm or signal timer—the duration is range-dependent on the reference clock used and the dynamic range of the counter
- A simple counter used to measure time to completion and time used
- An internal clock-source control based on missing/meeting durations

1.3.1.3 Nested Vectored Interrupt Controller (NVIC)

The TM4C129DNCPDT controller includes the ARM Nested Vectored Interrupt Controller (NVIC). The NVIC and Cortex-M4F prioritize and handle all exceptions in Handler Mode. The processor state is automatically stored to the stack on an exception and automatically restored from the stack at the end of the Interrupt Service Routine (ISR). The interrupt vector is fetched in parallel to the state saving, enabling efficient interrupt entry. The processor supports tail-chaining, meaning that back-to-back interrupts can be performed without the overhead of state saving and restoration. Software can set eight priority levels on 7 exceptions (system handlers) and 106 interrupts.

- Deterministic, fast interrupt processing: always 12 cycles, or just 6 cycles with tail-chaining (these values reflect no FPU stacking)
- External non-maskable interrupt signal (NMI) available for immediate execution of NMI handler for safety critical applications
- Dynamically reprioritizable interrupts
- Exceptional interrupt handling via hardware implementation of required register manipulations

1.3.1.4 System Control Block (SCB)

The SCB provides system implementation information and system control, including configuration, control, and reporting of system exceptions.

1.3.1.5 Memory Protection Unit (MPU)

The MPU supports the standard ARM7 Protected Memory System Architecture (PMSA) model. The MPU provides full support for protection regions, overlapping protection regions, access permissions, and exporting memory attributes to the system.

1.3.1.6 Floating-Point Unit (FPU)

The FPU fully supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions.

- 32-bit instructions for single-precision (C float) data-processing operations
- Combined multiply and accumulate instructions for increased precision (Fused MAC)
- Hardware support for conversion, addition, subtraction, multiplication with optional accumulate, division, and square-root
- Hardware support for denormals and all IEEE rounding modes
- 32 dedicated 32-bit single-precision registers, also addressable as 16 double-word registers
- Decoupled three stage pipeline

1.3.2 On-Chip Memory

The TM4C129DNCPDT microcontroller is integrated with the following set of on-chip memory and features:

- 256 KB single-cycle SRAM
- 1024 KB Flash memory
- 6KB EEPROM
- Internal ROM loaded with TivaWare™ for C Series software:
  - TivaWare™ Peripheral Driver Library
  - TivaWare Boot Loader
  - Advanced Encryption Standard (AES) cryptography tables
  - Cyclic Redundancy Check (CRC) error detection functionality

1.3.2.1 SRAM

The TM4C129DNCPDT microcontroller provides 256 KB of single-cycle on-chip SRAM. The internal SRAM of the device is located at offset 0x2000.0000 of the device memory map.

The SRAM is implemented using four 32-bit wide interleaving SRAM banks (separate SRAM arrays) which allow for increased speed between memory accesses. The SRAM memory provides nearly 2 GB/s memory bandwidth at a 120 MHz clock frequency.

Because read-modify-write (RMW) operations are very time consuming, ARM has introduced *bit-banding* technology in the Cortex-M4F processor. With a bit-band-enabled processor, certain regions in the memory map (SRAM and peripheral space) can use address aliases to access individual bits in a single, atomic operation.

Data can be transferred to and from SRAM by the following masters:

- µDMA
- USB
- Ethernet Controller

1.3.2.2 Flash Memory

The TM4C129DNCPDT microcontroller provides 1024 KB of on-chip Flash memory. The Flash memory is configured as four banks of 16K x 128 bits (4 * 256 KB total) which are two-way interleaved. Memory blocks can be marked as read-only or execute-only, providing different levels of code protection. Read-only blocks cannot be erased or programmed, protecting the contents of those blocks from being modified. Execute-only blocks cannot be erased or programmed, and can only be read by the controller instruction fetch mechanism, protecting the contents of those blocks from being read by either the controller or by a debugger.

The TM4C129DNCPDT microcontroller provides enhanced performance and power savings by implementation of two sets of instruction prefetch buffers. Each prefetch buffer is 2 x 256 bits and can be combined as a 4 x 256-bit prefetch buffer.

1.3.2.3 ROM

The TM4C129DNCPDT ROM is preprogrammed with the following software and programs:

- TivaWare Peripheral Driver Library
- TivaWare Boot Loader
- Advanced Encryption Standard (AES) cryptography tables
- Cyclic Redundancy Check (CRC) error-detection functionality

The TivaWare Peripheral Driver Library is a royalty-free software library for controlling on-chip peripherals with a boot-loader capability. The library performs both peripheral initialization and control functions, with a choice of polled or interrupt-driven peripheral support. In addition, the library is designed to take full advantage of the stellar interrupt performance of the ARM Cortex-M4F core. No special pragmas or custom assembly code prologue/epilogue functions are required. For applications that require in-field programmability, the royalty-free TivaWare Boot Loader can act as an application loader and support in-field firmware updates.

The Advanced Encryption Standard (AES) is a publicly defined encryption standard used by the U.S. Government. AES is a strong encryption method with reasonable performance and size. In addition, it is fast in both hardware and software, is fairly easy to implement, and requires little memory. The Texas Instruments encryption package is available with full source code, and is based on Lesser General Public License (LGPL) source. An LGPL means that the code can be used within an application without any copyleft implications for the application (the code does not automatically become open source). Modifications to the package source, however, must be open source.

CRC (Cyclic Redundancy Check) is a technique to validate a span of data has the same contents as when previously checked. This technique can be used to validate correct receipt of messages (nothing lost or modified in transit), to validate data after decompression, to validate that Flash memory contents have not been changed, and for other cases where the data needs to be validated. A CRC is preferred over a simple checksum (e.g. XOR all bits) because it catches changes more readily.

Note: CRC and AES software programs are available in the TivaWare™ for C Series software for backward-compatibility. A device that has enhanced CRC and AES integrated modules should utilize this hardware for best performance.

1.3.2.4 EEPROM

The TM4C129DNCPDT microcontroller includes an EEPROM with the following features:

- 6Kbytes of memory accessible as 1536 32-bit words
- 96 blocks of 16 words (64 bytes) each
- Built-in wear leveling
- Access protection per block
- Lock protection option for the whole peripheral as well as per block using 32-bit to 96-bit unlock codes (application selectable)
- Interrupt support for write completion to avoid polling
- Endurance of 500K writes (when writing at fixed offset in every alternate page in circular fashion) to 15M operations (when cycling through two pages) per each 2-page block.

1.3.3 External Peripheral Interface

The External Peripheral Interface (EPI) provides access to external devices using a parallel path. Unlike communications peripherals such as SSI, UART, and I^2C, the EPI is designed to act like a bus to external peripherals and memory.

The EPI has the following features:

- 8/16/32-bit dedicated parallel bus for external peripherals and memory
- Memory interface supports contiguous memory access independent of data bus width, thus enabling code execution directly from SDRAM, SRAM and Flash memory
- Blocking and non-blocking reads
- Separates processor from timing details through use of an internal write FIFO
- Efficient transfers using Micro Direct Memory Access Controller (µDMA)
  - Separate channels for read and write
  - Read channel request asserted by programmable levels on the internal Non-Blocking Read FIFO (NBRFIFO)
  - Write channel request asserted by empty on the internal Write FIFO (WFIFO)

The EPI supports three primary functional modes: Synchronous Dynamic Random Access Memory (SDRAM) mode, Traditional Host-Bus mode, and General-Purpose mode. The EPI module also provides custom GPIOs; however, unlike regular GPIOs, the EPI module uses a FIFO in the same way as a communication mechanism and is speed-controlled using clocking.

- Synchronous Dynamic Random Access Memory (SDRAM) mode
  - Supports x16 (single data rate) SDRAM at up to 60 MHz
  - Supports low-cost SDRAMs up to 64 MB (512 megabits)
  - Includes automatic refresh and access to all banks/rows
  - Includes a Sleep/Standby mode to keep contents active with minimal power draw

  - Multiplexed address/data interface for reduced pin count

- Host-Bus mode
  - Traditional x8 and x16 MCU bus interface capabilities
  - Similar device compatibility options as PIC, ATmega, 8051, and others
  - Access to SRAM, NOR Flash memory, and other devices, with up to 1 MB of addressing in unmultiplexed mode and 256 MB in multiplexed mode (512 MB in Host-Bus 16 mode with no byte selects)
  - Support for up to 512 Mb PSRAM in quad chip select mode, with dedicated configuration register read and write enable.
  - Support of both muxed and de-muxed address and data
  - Access to a range of devices supporting the non-address FIFO x8 and x16 interface variant, with support for external FIFO (XFIFO) EMPTY and FULL signals
  - Speed controlled, with read and write data wait-state counters
  - Support for read/write burst mode to Host Bus
  - Multiple chip select modes including single, dual, and quad chip selects, with and without ALE
  - External iRDY signal provided for stall capability of reads and writes
  - Manual chip-enable (or use extra address pins)
- General-Purpose mode
  - Wide parallel interfaces for fast communications with CPLDs and FPGAs
  - Data widths up to 32 bits
  - Data rates up to 150 MB/second
  - Optional "address" sizes from 4 bits to 20 bits
  - Optional clock output, read/write strobes, framing (with counter-based size), and clock-enable input
- General parallel GPIO
  - 1 to 32 bits, FIFOed with speed control
  - Useful for custom peripherals or for digital data acquisition and actuator controls

1.3.4 Cyclical Redundancy Check (CRC)

The TM4C129DNCPDT microcontroller includes a CRC computation module for uses such as message transfer and safety system checks. This module can be used in conjunction with the AES and DES modules. The CRC has the following features:

- Support four major CRC forms:
  - CRC16-CCITT as used by CCITT/ITU X.25
  - CRC16-IBM as used by USB and ANSI
  - CRC32-IEEE as used by IEEE802.3 and MPEG2
  - CRC32C as used by G.Hn
- Allows word and byte feed
- Supports auto-initialization and manual initialization
- Supports MSb and LSb
- Supports CCITT post-processing
- Can be fed by µDMA, Flash memory and code

1.3.5 Advanced Encryption Standard (AES) Accelerator

The advanced encryption standard (AES) accelerator module provides hardware-accelerated data encryption and decryption operations based on a binary key. The AES module is a symmetrical cipher modules that supports a 128-bit, 192-bit, or 256-bit key in hardware for both encryption and decryption.

The AES has following features:

- Support for basic AES encrypt and decrypt operations:
  - Galois/Counter Mode (GCM), with basic GHASH operation
  - Counter Mode with CBC-MAC (CCM)
  - XTS Mode
- Availability of the following feedback operating modes:
  - Electronic Code Book Mode (ECB)
  - Cipher Block Chaining Mode (CBC)
  - Counter Mode (CTR)
  - Cipher Feedback Mode (CFB), 128-bit
  - F8 Mode
- Key sizes 128-, 192- and 256-bits
- Support for CBC_MAC and Fedora 9 (F9) authentication modes
- Basic GHASH operation (when selecting no encryption)
- Key scheduling in hardware

- Support for µDMA transfers
- Fully synchronous design

1.3.6 Data Encryption Standard (DES) Accelerator

The DES module provides hardware accelerated data encryption and decryption functions. The module runs either the single DES or the triple DES (3DES) algorithm and supports electronic codebook (ECB), cipher block chaining (CBC), and cipher feedback (CFB) modes of operation.

The DES accelerator includes the following main features:

- DES/3DES encryption and decryption.
- Feedback modes: ECB, CBC, CFB
- Host interrupt or µDMA driven modes of operation. µDMA support for data and context in/result out
- Fully synchronous design
- Internal wide-bus interface

1.3.7 Secure Hash Algorithm / Message Digest Algorithm (SHA/MD5)

The SHA/MD5 module provides hardware-accelerated hash functions and can run:

- MD5 message digest algorithm developed by Ron Rivest in 1991
- SHA-1 algorithm compliant with the FIPS 180-3 standard
- SHA-2 (SHA-224 and SHA-256) algorithm compliant with the FIPS 180-3 standard
- Hash message authentication code (HMAC) operation

The algorithms produce a condensed representation of a message or a data file which can then be used to verify the message integrity.

The SHA/MD5 accelerator module includes the following main features:

- Hashing of 0 to 2^{33} - 2 bytes of data (of which 2^{32} - 1 bytes are in one pass) using the MD5, SHA-1, SHA-224, or SHA-256 hash algorithm (byte granularity only, no support for bit granularity)
- Automatic HMAC key pre-processing for HMAC keys up to 64 bytes
- Host-assisted HMAC key pre-processing for HMAC keys larger than 64 bytes
- HMAC from pre-computes (inner/outer digest) for improved performance on small blocks
- Supports µDMA operation for data and context in/result out transfers
- Supports interrupt to read the digest (signature)

1.3.8 Serial Communications Peripherals

The TM4C129DNCPDT controller supports both asynchronous and synchronous serial communications with:

- 10/100 Ethernet MAC with Advanced IEEE 1588 PTP hardware and both Media Independent Interface (MII) and Reduced MII (RMII) support
- Two CAN 2.0 A/B controllers
- USB 2.0 Controller OTG/Host/Device with optional high speed using external PHY through ULPI interface
- Eight UARTs with IrDA, 9-bit and ISO 7816 support.
- Ten I^2C modules with four transmission speeds including high-speed mode
- Four Quad Synchronous Serial Interface modules (QSSI) with bi- and quad-SSI support

The following sections provide more detail on each of these communications functions.

1.3.8.1 Ethernet MAC

The TM4C129DNCPDT Ethernet Controller consists of a fully integrated media access controller (MAC) with the following features:

- Conforms to the IEEE 802.3 specification
  - 10BASE-T/100BASE-TX IEEE-802.3 compliant
  - Supports 10/100 Mbps data transmission rates
  - Supports full-duplex and half-duplex (CSMA/CD) operation
  - Supports flow control and back pressure
  - Full-featured and enhanced auto-negotiation
  - Supports IEEE 802.1Q VLAN tag detection
- Conforms to IEEE 1588-2002 Timestamp Precision Time Protocol (PTP) protocol and the IEEE 1588-2008 Advanced Timestamp specification
  - Transmit and Receive frame time stamping
  - Precision Time Protocol
  - Flexible pulse per second output
  - Supports coarse and fine correction methods
- Multiple addressing modes
  - Four MAC address filters
  - Programmable 64-bit Hash Filter for multicast address filtering
  - Promiscuous mode support
- Processor offloading
  - Programmable insertion (TX) or deletion (RX) of preamble and start-of-frame data

  - Programmable generation (TX) or deletion (RX) of CRC and pad data
  - IP header and hardware checksum checking (IPv4, IPv6, TCP/UDP/ICMP)
- Highly configurable
  - Supports network statistics with RMON/MIB counters
  - Supports Magic Packet and wakeup frames
- Efficient transfers using integrated Direct Memory Access (DMA)
  - Dual-buffer (ring) or linked-list (chained) descriptors
  - Round-robin or fixed priority arbitration between TX/RX
  - Descriptors support up to 8 kB transfer blocks size
  - Programmable interrupts for flexible system implementation
- MII and RMII interface support

1.3.8.2 Controller Area Network (CAN)

Controller Area Network (CAN) is a multicast shared serial-bus standard for connecting electronic control units (ECUs). CAN was specifically designed to be robust in electromagnetically noisy environments and can utilize a differential balanced line like RS-485 or twisted-pair wire. Originally created for automotive purposes, it is now used in many embedded control applications (for example, industrial or medical). Bit rates up to 1 Mbps are possible at network lengths below 40 meters. Decreased bit rates allow longer network distances (for example, 125 Kbps at 500m).

A transmitter sends a message to all CAN nodes (broadcasting). Each node decides on the basis of the identifier received whether it should process the message. The identifier also determines the priority that the message enjoys in competition for bus access. Each CAN message can transmit from 0 to 8 bytes of user information.

The TM4C129DNCPDT microcontroller includes two CAN units with the following features:

- CAN protocol version 2.0 part A/B
- Bit rates up to 1 Mbps
- 32 message objects with individual identifier masks
- Maskable interrupt
- Disable Automatic Retransmission mode for Time-Triggered CAN (TTCAN) applications
- Programmable loopback mode for self-test operation
- Programmable FIFO mode enables storage of multiple message objects
- Gluelessly attaches to an external CAN transceiver through the CANnTX and CANnRX signals

1.3.8.3 Universal Serial Bus (USB)

Universal Serial Bus (USB) is a serial bus standard designed to allow peripherals to be connected and disconnected using a standardized interface without rebooting the system.

The TM4C129DNCPDT microcontroller has one USB controller that supports high and full speed multi-point communications and complies with the USB 2.0 standard for high-speed function. The USB controller can have three configurations: USB Device, USB Host, and USB On-The-Go (negotiated on-the-go as host or device when connected to other USB-enabled systems). Support for full-speed communication is provided by using the integrated USB PHY or optionally, a high-speed ULPI interface can communicate to an external PHY.

The USB module has the following features:

- Complies with USB-IF (Implementer's Forum) certification standards
- USB 2.0 high-speed (480 Mbps) operation with the integrated ULPI interface communicating with an external PHY
- Link Power Management support which uses link-state awareness to reduce power usage
- 4 transfer types: Control, Interrupt, Bulk, and Isochronous
- 16 endpoints
  - 1 dedicated control IN endpoint and 1 dedicated control OUT endpoint
  - 7 configurable IN endpoints and 7 configurable OUT endpoints
- 4 KB dedicated endpoint memory: one endpoint may be defined for double-buffered 1023-byte isochronous packet size
- VBUS droop detection and interrupt
- Integrated USB DMA with bus master capability
  - Up to eight RX Endpoint channels and up to eight TX Endpoint channels are available.
  - Each channel can be separately programmed to operate in different modes
  - Incremental burst transfers of 4-, 8-, 16- or unspecified length supported

1.3.8.4 UART

A Universal Asynchronous Receiver/Transmitter (UART) is an integrated circuit used for RS-232C serial communications, containing a transmitter (parallel-to-serial converter) and a receiver (serial-to-parallel converter), each clocked separately.

The TM4C129DNCPDT microcontroller includes eight fully programmable 16C550-type UARTs. Although the functionality is similar to a 16C550 UART, this UART design is not register compatible. The UART can generate individually masked interrupts from the Rx, Tx, modem flow control, modem status, and error conditions. The module generates a single combined interrupt when any of the interrupts are asserted and are unmasked.

The eight UARTs have the following features:

- Programmable baud-rate generator allowing speeds up to 7.5 Mbps for regular speed (divide by 16) and 15 Mbps for high speed (divide by 8)

- Separate 16x8 transmit (TX) and receive (RX) FIFOs to reduce CPU interrupt service loading
- Programmable FIFO length, including 1-byte deep operation providing conventional double-buffered interface
- FIFO trigger levels of 1/8, 1/4, 1/2, 3/4, and 7/8
- Standard asynchronous communication bits for start, stop, and parity
- Line-break generation and detection
- Fully programmable serial interface characteristics
  - 5, 6, 7, or 8 data bits
  - Even, odd, stick, or no-parity bit generation/detection
  - 1 or 2 stop bit generation
- IrDA serial-IR (SIR) encoder/decoder providing
  - Programmable use of IrDA Serial Infrared (SIR) or UART input/output
  - Support of IrDA SIR encoder/decoder functions for data rates up to 115.2 Kbps half-duplex
  - Support of normal 3/16 and low-power (1.41-2.23 µs) bit durations
  - Programmable internal clock generator enabling division of reference clock by 1 to 256 for low-power mode bit duration
- Support for communication with ISO 7816 smart cards
- Modem functionality available on the following UARTs:
  - UART0 (modem flow control and modem status)
  - UART1 (modem flow control and modem status)
  - UART2 (modem flow control)
  - UART3 (modem flow control)
  - UART4 (modem flow control)
- EIA-485 9-bit support
- Standard FIFO-level and End-of-Transmission interrupts
- Efficient transfers using Micro Direct Memory Access Controller (µDMA)
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted at programmed FIFO level
  - Transmit single request asserted when there is space in the FIFO; burst request asserted at programmed FIFO level

- Global Alternate Clock (ALTCLK) resource or System Clock (SYSCLK) can be used to generate baud clock

1.3.8.5 I²C

The Inter-Integrated Circuit (I^2C) bus provides bi-directional data transfer through a two-wire design (a serial data line SDA and a serial clock line SCL). The I^2C bus interfaces to external I^2C devices such as serial memory (RAMs and ROMs), networking devices, LCDs, tone generators, and so on. The I^2C bus may also be used for system testing and diagnostic purposes in product development and manufacture.

Each device on the I^2C bus can be designated as either a master or a slave. I^2C module supports both sending and receiving data as either a master or a slave and can operate simultaneously as both a master and a slave. Both the I^2C master and slave can generate interrupts.

The TM4C129DNCPDT microcontroller includes I^2C modules with the following features:

- Devices on the I^2C bus can be designated as either a master or a slave
  - Supports both transmitting and receiving data as either a master or a slave
  - Supports simultaneous master and slave operation
- Four I^2C modes
  - Master transmit
  - Master receive
  - Slave transmit
  - Slave receive
- Two 8-entry FIFOs for receive and transmit data
  - FIFOs can be independently assigned to master or slave
- Four transmission speeds:
  - Standard (100 Kbps)
  - Fast-mode (400 Kbps)
  - Fast-mode plus (1 Mbps)
  - High-speed mode (3.33 Mbps)
- Glitch suppression
- SMBus support through software
  - Clock low timeout interrupt
  - Dual slave address capability
  - Quick command capability

- Master and slave interrupt generation
  - Master generates interrupts when a transmit or receive operation completes (or aborts due to an error)
  - Slave generates interrupts when data has been transferred or requested by a master or when a START or STOP condition is detected
- Master with arbitration and clock synchronization, multimaster support, and 7-bit addressing mode
- Efficient transfers using Micro Direct Memory Access Controller (µDMA)
  - Separate channels for transmit and receive
  - Ability to execute single data transfers or burst data transfers using the RX and TX FIFOs in the I^2C

1.3.8.6 QSSI

Quad Synchronous Serial Interface (QSSI) is a bi-directional communications interface that converts data between parallel and serial. The QSSI module performs serial-to-parallel conversion on data received from a peripheral device, and parallel-to-serial conversion on data transmitted to a peripheral device. The QSSI module can be configured as either a master or slave device. As a slave device, the QSSI module can also be configured to disable its output, which allows a master device to be coupled with multiple slave devices. The TX and RX paths are buffered with separate internal FIFOs.

The QSSI module also includes a programmable bit rate clock divider and prescaler to generate the output serial clock derived from the QSSI module's input clock. Bit rates are generated based on the input clock and the maximum bit rate is determined by the connected peripheral.

The TM4C129DNCPDT microcontroller includes four QSSI modules with the following features:

- Four QSSI channels with Advanced, Bi- and Quad-SSI functionality
- Programmable interface operation for Freescale SPI or Texas Instruments synchronous serial interfaces in Legacy Mode. Support for Freescale interface in Bi- and Quad-SSI mode.
- Master or slave operation
- Programmable clock bit rate and prescaler
- Separate transmit and receive FIFOs, each 16 bits wide and 8 locations deep
- Programmable data frame size from 4 to 16 bits
- Internal loopback test mode for diagnostic/debug testing
- Standard FIFO-based interrupts and End-of-Transmission interrupt
- Efficient transfers using Micro Direct Memory Access Controller (µDMA)
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted when FIFO contains 4 entries

  - Transmit single request asserted when there is space in the FIFO; burst request asserted when four or more entries are available to be written in the FIFO
  - Maskable µDMA interrupts for receive and transmit complete
- Global Alternate Clock (ALTCLK) resource or System Clock (SYSCLK) can be used to generate baud clock.

1.3.9 System Integration

The TM4C129DNCPDT microcontroller provides a variety of standard system functions integrated into the device, including:

- Direct Memory Access Controller (DMA)
- System control and clocks including on-chip precision 16-MHz oscillator
- Eight 32-bit timers (each of which can be configured as two 16-bit timers)
- Lower-power battery-backed Hibernation module
- Real-Time Clock in Hibernation module
- Two Watchdog Timers
  - One timer runs off the main oscillator
  - One timer runs off the precision internal oscillator
- Up to 98 GPIOs, depending on configuration
  - Highly flexible pin muxing allows use as GPIO or one of several peripheral functions
  - Independently configurable to 2-, 4-, 8-, 10-, or 12-mA drive capability
  - Up to 4 GPIOs can have 18-mA drive capability

The following sections provide more detail on each of these functions.

1.3.9.1 Direct Memory Access

The TM4C129DNCPDT microcontroller includes a Direct Memory Access (DMA) controller, known as micro-DMA (µDMA). The µDMA controller provides a way to offload data transfer tasks from the Cortex-M4F processor, allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform transfers between memory and peripherals. It has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory as the peripheral is ready to transfer more data. The µDMA controller provides the following features:

- ARM PrimeCell® 32-channel configurable µDMA controller
- Support for memory-to-memory, memory-to-peripheral, and peripheral-to-memory in multiple transfer modes
  - Basic for simple transfer scenarios
  - Ping-pong for continuous data flow
  - Scatter-gather for a programmable list of up to 256 arbitrary transfers initiated from a single request

- Highly flexible and configurable channel operation
  - Independently configured and operated channels
  - Dedicated channels for supported on-chip modules
  - Flexible channel assignments
  - One channel each for receive and transmit path for bidirectional modules
  - Dedicated channel for software-initiated transfers
  - Per-channel configurable priority scheme
  - Optional software-initiated requests for any channel
- Two levels of priority
- Design optimizations for improved bus access performance between µDMA controller and the processor core
  - µDMA controller access is subordinate to core access
  - RAM striping
  - Peripheral bus segmentation
- Data sizes of 8, 16, and 32 bits
- Transfer size is programmable in binary steps from 1 to 1024
- Source and destination address increment size of byte, half-word, word, or no increment
- Maskable peripheral requests
- Interrupt on transfer completion, with a separate interrupt per channel

1.3.9.2 System Control and Clocks

System control determines the overall operation of the device. It provides information about the device, controls power-saving features, controls the clocking of the device and individual peripherals, and handles reset detection and reporting.

- Device identification information: version, part number, SRAM size, Flash memory size, and so on
- Power control
  - On-chip fixed Low Drop-Out (LDO) voltage regulator
  - Hibernation module handles the power-up/down 3.3 V sequencing and control for the core digital logic and analog circuits
  - Low-power options for microcontroller: Sleep and Deep-sleep modes with clock gating
  - Low-power options for on-chip modules: software controls shutdown of individual peripherals and memory

  - 3.3-V supply brown-out detection and reporting via interrupt or reset

- Multiple clock sources for microcontroller system clock. The TM4C129DNCPDT microcontroller is clocked by the system clock (SYSCLK) that is distributed to the processor and integrated peripherals after clock gating. The SYSCLK frequency is based on the frequency of the clock source and a divisor factor. A PLL is provided for the generation of system clock frequencies in excess of the reference clock provided. The reference clocks for the PLL are the PIOSC and the main crystal oscillator. The following clock sources are provided to the TM4C129DNCPDT microcontroller:

  - 16-MHz Precision Oscillator (PIOSC)

  - Main Oscillator (MOSC): A frequency-accurate clock source by one of two means: an external single-ended clock source is connected to the OSC0 input pin, or an external crystal is connected across the OSC0 input and OSC1 output pins.

  - Low Frequency Internal Oscillator (LFIOSC): On-chip resource used during power-saving modes

  - Hibernate RTC oscillator (RTCOSC) clock that can be configured to be the 32.768-kHz external oscillator source from the Hibernation (HIB) module or the HIB Low Frequency clock source (HIB LFIOSC), which is located within the Hibernation Module.

- Flexible reset sources

  - Power-on reset (POR)

  - Reset pin assertion

  - Brown-out reset (BOR) detector alerts to system power drops

  - Software reset

  - Watchdog timer reset

  - Hibernation module event

  - MOSC failure

1.3.9.3 Programmable Timers

Programmable timers can be used to count or time external events that drive the Timer input pins. Each 16/32-bit GPTM block provides two 16-bit timers/counters that can be configured to operate independently as timers or event counters, or configured to operate as one 32-bit timer or one 32-bit Real-Time Clock (RTC). Timers can also be used to trigger analog-to-digital (ADC) conversions and DMA transfers.

The General-Purpose Timer Module (GPTM) contains eight 16/32-bit GPTM blocks with the following functional options:

- Operating modes:

  - 16- or 32-bit programmable one-shot timer

  - 16- or 32-bit programmable periodic timer

  - 16-bit general-purpose timer with an 8-bit prescaler
  - 32-bit Real-Time Clock (RTC) when using an external 32.768-KHz clock as the input
  - 16-bit input-edge count- or time-capture modes with an 8-bit prescaler
  - 16-bit PWM mode with an 8-bit prescaler and software-programmable output inversion of the PWM signal
  - The System Clock or a global Alternate Clock (ALTCLK) resource can be used as timer clock source. The global ALTCLK can be:
    - PIOSC
    - Hibernation Module Real-time clock output (RTCOSC)
    - Low-frequency internal oscillator (LFIOSC)
- Count up or down
- Twelve 16/32-bit Capture Compare PWM pins (CCP)
- Daisy chaining of timer modules to allow a single timer to initiate multiple timing events
- Timer synchronization allows selected timers to start counting on the same clock cycle
- ADC event trigger
- User-enabled stalling when the microcontroller asserts CPU Halt flag during debug (excluding RTC mode)
- Ability to determine the elapsed time between the assertion of the timer interrupt and entry into the interrupt service routine
- Efficient transfers using Micro Direct Memory Access Controller (µDMA)
  - Dedicated channel for each timer
  - Burst request generated on timer interrupt

1.3.9.4 CCP Pins

Capture Compare PWM pins (CCP) can be used by the General-Purpose Timer Module to time/count external events using the CCP pin as an input. Alternatively, the GPTM can generate a simple PWM output on the CCP pin.

The TM4C129DNCPDT microcontroller includes twelve 16/32-bit CCP pins that can be programmed to operate in the following modes:

- Capture: The GP Timer is incremented/decremented by programmed events on the CCP input. The GP Timer captures and stores the current timer value when a programmed event occurs.
- Compare: The GP Timer is incremented/decremented by programmed events on the CCP input. The GP Timer compares the current value with a stored value and generates an interrupt when a match occurs.

- PWM: The GP Timer is incremented/decremented by the system clock. A PWM signal is generated based on a match between the counter value and a value stored in a match register and is output on the CCP pin.

1.3.9.5 Hibernation Module (HIB)

The Hibernation module provides logic to switch power off to the main processor and peripherals and to wake on external or time-based events. The Hibernation module includes power-sequencing logic and has the following features:

- 32-bit real-time seconds counter (RTC) with 1/32,768 second resolution and a 15-bit sub-seconds counter
  - 32-bit RTC seconds match register and a 15-bit sub seconds match for timed wake-up and interrupt generation with 1/32,768 second resolution
  - RTC predivider trim for making fine adjustments to the clock rate
- Hardware Calendar Function
  - Year, Month, Day, Day of Week, Hours, Minutes, Seconds
  - Four-year leap compensation
  - 24-hour or AM/PM configuration
- Two mechanisms for power control
  - System power control using discrete external regulator
  - On-chip power control using internal switches under register control
- V_{DD} supplies power when valid, even if $V_{BAT} > V_{DD}$
- Dedicated pin for waking using an external signal
- Capability to configure external reset ($\overline{RST}$) pin and/or up to four GPIO port pins as wake source, with programmable wake level
- Tamper Functionality
  - Support for four tamper inputs
  - Configurable level, weak pullup, and glitch filter
  - Configurable tamper event response
  - Logging of up to four tamper events
  - Optional BBRAM erase on tamper detection
  - Tamper wake from hibernate capability
  - Hibernation clock input failure detect with a switch to the internal oscillator on detection
- RTC operational and hibernation memory valid as long as V_{DD} or V_{BAT} is valid

- Low-battery detection, signaling, and interrupt generation, with optional wake on low battery
- GPIO pin state can be retained during hibernation
- Clock source from an internal low frequency oscillator (HIB LFIOSC) or a 32.768-kHz external crystal or oscillator
- Sixteen 32-bit words of battery-backed memory to save state during hibernation
- Programmable interrupts for:
  - RTC match
  - External wake
  - Low battery

1.3.9.6 Watchdog Timers

A watchdog timer is used to regain control when a system has failed due to a software error or to the failure of an external device to respond in the expected way. The TM4C129DNCPDT Watchdog Timer can generate an interrupt, a non-maskable interrupt, or a reset when a time-out value is reached. In addition, the Watchdog Timer is ARM FiRM-compliant and can be configured to generate an interrupt to the microcontroller on its first time-out, and to generate a reset signal on its second timeout. Once the Watchdog Timer has been configured, the lock register can be written to prevent the timer configuration from being inadvertently altered.

The TM4C129DNCPDT microcontroller has two Watchdog Timer modules: Watchdog Timer 0 uses the system clock for its timer clock; Watchdog Timer 1 uses the PIOSC as its timer clock. The Watchdog Timer module has the following features:

- 32-bit down counter with a programmable load register
- Separate watchdog clock with an enable
- Programmable interrupt generation logic with interrupt masking and optional NMI function
- Lock register protection from runaway software
- Reset generation logic with an enable/disable
- User-enabled stalling when the microcontroller asserts the CPU Halt flag during debug

1.3.9.7 Programmable GPIOs

General-purpose input/output (GPIO) pins offer flexibility for a variety of connections. The TM4C129DNCPDT GPIO module is comprised of 15 physical GPIO blocks, each corresponding to an individual GPIO port. The GPIO module is FiRM-compliant (compliant to the ARM Foundation IP for Real-Time Microcontrollers specification) and supports 0-98 programmable input/output pins. The number of GPIOs available depends on the peripherals being used (see “Signal Tables” on page 37 for the signals available to each GPIO pin).

- Up to 98 GPIOs, depending on configuration
- Highly flexible pin muxing allows use as GPIO or one of several peripheral functions
- 3.3-V-tolerant in input configuration

- Advanced High Performance Bus accesses all ports:
  - Ports A-H and J; Ports K-N and P-Q
- Fast toggle capable of a change every clock cycle for ports on AHB
- Programmable control for GPIO interrupts
  - Interrupt generation masking
  - Edge-triggered on rising, falling, or both
  - Level-sensitive on High or Low values
  - Per-pin interrupts available on Port P and Port Q
- Bit masking in both read and write operations through address lines
- Can be used to initiate an ADC sample sequence or a µDMA transfer
- Pin state can be retained during Hibernation mode; pins on port P can be programmed to wake on level in Hibernation mode
- Pins configured as digital inputs are Schmitt-triggered
- Programmable control for GPIO pad configuration
  - Weak pull-up or pull-down resistors
  - 2-mA, 4-mA, 6-mA, 8-mA, 10-mA and 12-mA pad drive for digital communication; up to four pads can sink 18-mA for high-current applications
  - Slew rate control for 8-mA, 10-mA and 12-mA pad drive
  - Open drain enables
  - Digital input enables

1.3.10 Advanced Motion Control

The TM4C129DNCPDT microcontroller provides motion control functions integrated into the device, including:

- Eight advanced PWM outputs for motion and energy applications
- Four fault inputs to promote low-latency shutdown
- One Quadrature Encoder Input (QEI)

The following provides more detail on these motion control functions.

1.3.10.1 PWM

The TM4C129DNCPDT microcontroller contains one PWM module, with four PWM generator blocks and a control block, for a total of 8 PWM outputs. Pulse width modulation (PWM) is a powerful technique for digitally encoding analog signal levels. High-resolution counters are used to generate a square wave, and the duty cycle of the square wave is modulated to encode an analog signal.

Typical applications include switching power supplies and motor control. The TM4C129DNCPDT PWM module consists of four PWM generator block and a control block. Each PWM generator block contains one timer (16-bit down or up/down counter), two comparators, a PWM signal generator, a dead-band generator, and an interrupt/ADC-trigger selector. Each PWM generator block produces two PWM signals that can either be independent signals or a single pair of complementary signals with dead-band delays inserted.

Each PWM generator has the following features:

- Four fault-condition handling inputs to quickly provide low-latency shutdown and prevent damage to the motor being controlled
- One 16-bit counter
  - Runs in Down or Up/Down mode
  - Output frequency controlled by a 16-bit load value
  - Load value updates can be synchronized
  - Produces output signals at zero and load value
- Two PWM comparators
  - Comparator value updates can be synchronized
  - Produces output signals on match
- PWM signal generator
  - Output PWM signal is constructed based on actions taken as a result of the counter and PWM comparator output signals
  - Produces two independent PWM signals
- Dead-band generator
  - Produces two PWM signals with programmable dead-band delays suitable for driving a half-H bridge
  - Can be bypassed, leaving input PWM signals unmodified
- Can initiate an ADC sample sequence

The control block determines the polarity of the PWM signals and which signals are passed through to the pins. The output of the PWM generation blocks are managed by the output control block before being passed to the device pins. The PWM control block has the following options:

- PWM output enable of each PWM signal
- Optional output inversion of each PWM signal (polarity control)
- Optional fault handling for each PWM signal
- Synchronization of timers in the PWM generator blocks

- Synchronization of timer/comparator updates across the PWM generator blocks
- Extended PWM synchronization of timer/comparator updates across the PWM generator blocks
- Interrupt status summary of the PWM generator blocks
- Extended PWM fault handling, with multiple fault signals, programmable polarities, and filtering
- PWM generators can be operated independently or synchronized with other generators

1.3.10.2 QEI

A quadrature encoder, also known as a 2-channel incremental encoder, converts linear displacement into a pulse signal. By monitoring both the number of pulses and the relative phase of the two signals, the position, direction of rotation, and speed can be tracked. In addition, a third channel, or index signal, can be used to reset the position counter. The TM4C129DNCPDT quadrature encoder with index (QEI) module interprets the code produced by a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, it can capture a running estimate of the velocity of the encoder wheel. The input frequency of the QEI inputs may be as high as 1/4 of the processor frequency (for example, 30 MHz for a 120-MHz system).

The TM4C129DNCPDT microcontroller includes two QEI modules providing control of two motors at the same time with the following features:

- Position integrator that tracks the encoder position
- Programmable noise filter on the inputs
- Velocity capture using built-in timer
- The input frequency of the QEI inputs may be as high as 1/4 of the processor frequency (for example, 12.5 MHz for a 50-MHz system)
- Interrupt generation on:
  - Index pulse
  - Velocity-timer expiration
  - Direction change
  - Quadrature error detection

1.3.11 Analog

The TM4C129DNCPDT microcontroller provides analog functions integrated into the device, including:

- Two 12-bit Analog-to-Digital Converters (ADC), with a total of 20 analog input channels and each with a sample rate of one million samples/second
- Three analog comparators
- On-chip voltage regulator

The following provides more detail on these analog functions.

1.3.11.1 ADC

An analog-to-digital converter (ADC) is a peripheral that converts a continuous analog voltage to a discrete digital number. The TM4C129DNCPDT ADC module features 12-bit conversion resolution and supports 20 input channels plus an internal temperature sensor. Four buffered sample sequencers allow rapid sampling of up to 20 analog input sources without controller intervention. Each sample sequencer provides flexible programming with fully configurable input source, trigger events, interrupt generation, and sequencer priority. Each ADC module has a digital comparator function that allows the conversion value to be diverted to a comparison unit that provides eight digital comparators.

The TM4C129DNCPDT microcontroller provides two ADC modules, each with the following features:

- 20 shared analog input channels
- 12-bit precision ADC
- Single-ended and differential-input configurations
- On-chip internal temperature sensor
- Maximum sample rate of one million samples/second
- Optional phase shift in sample time programmable from 22.5º to 337.5º
- Four programmable sample conversion sequencers from one to eight entries long, with corresponding conversion result FIFOs
- Flexible trigger control
  - Controller (software)
  - Timers
  - Analog Comparators
  - PWM
  - GPIO
- Hardware averaging of up to 64 samples
- Eight digital comparators
- Converter uses signals VREFA+ and GNDA as the voltage reference
- Power and ground for the analog circuitry is separate from the digital power and ground
- Efficient transfers using Micro Direct Memory Access Controller (µDMA)
  - Dedicated channel for each sample sequencer
  - ADC module uses burst requests for DMA
- Global Alternate Clock (ALTCLK) resource or System Clock (SYSCLK) can be used to generate ADC clock

1.3.11.2 Analog Comparators

An analog comparator is a peripheral that compares two analog voltages and provides a logical output that signals the comparison result. The TM4C129DNCPDT microcontroller provides three independent integrated analog comparators that can be configured to drive an output or generate an interrupt or ADC event.

The comparator can provide its output to a device pin, acting as a replacement for an analog comparator on the board, or it can be used to signal the application via interrupts or triggers to the ADC to cause it to start capturing a sample sequence. The interrupt generation and ADC triggering logic is separate. This means, for example, that an interrupt can be generated on a rising edge and the ADC triggered on a falling edge.

The TM4C129DNCPDT microcontroller provides three independent integrated analog comparators with the following functions:

- Compare external pin input to external pin input or to internal programmable voltage reference
- Compare a test voltage against any one of the following voltages:
  - An individual external reference voltage
  - A shared single external reference voltage
  - A shared internal reference voltage

1.3.12 JTAG and ARM Serial Wire Debug

The Joint Test Action Group (JTAG) port is an IEEE standard that defines a Test Access Port and Boundary Scan Architecture for digital integrated circuits and provides a standardized serial interface for controlling the associated test logic. The TAP, Instruction Register (IR), and Data Registers (DR) can be used to test the interconnections of assembled printed circuit boards and obtain manufacturing information on the components. The JTAG Port also provides a means of accessing and controlling design-for-test features such as I/O pin observation and control, scan testing, and debugging. Texas Instruments replaces the ARM SW-DP and JTAG-DP with the ARM Serial Wire JTAG Debug Port (SWJ-DP) interface. The SWJ-DP interface combines the SWD and JTAG debug ports into one module providing all the normal JTAG debug and test functionality plus real-time access to system memory without halting the core or requiring any target resident code. The SWJ-DP interface has the following features:

- IEEE 1149.1-1990 compatible Test Access Port (TAP) controller
- Four-bit Instruction Register (IR) chain for storing JTAG instructions
- IEEE standard instructions: BYPASS, IDCODE, SAMPLE/PRELOAD, and EXTEST
- ARM additional instructions: APACC, DPACC and ABORT
- Integrated ARM Serial Wire Debug (SWD)
  - Serial Wire JTAG Debug Port (SWJ-DP)
  - Flash Patch and Breakpoint (FPB) unit for implementing breakpoints
  - Data Watchpoint and Trace (DWT) unit for implementing watchpoints, trigger resources, and system profiling

– Instrumentation Trace Macrocell (ITM) for support of printf style debugging

– Embedded Trace Macrocell (ETM) for instruction trace capture

– Trace Port Interface Unit (TPIU) for bridging to a Trace Port Analyzer

1.3.13 Packaging and Temperature

- 128-pin RoHS-compliant TQFP package
- Industrial (-40°C to 85°C) ambient temperature range
- Extended (-40°C to 105°C) ambient temperature range

1.4 Kits

The Tiva™ C Series provides the hardware and software tools that engineers need to begin development quickly.

- Reference Design Kits accelerate product development by providing ready-to-run hardware and comprehensive documentation including hardware design files
- Evaluation Kits provide a low-cost and effective means of evaluating TM4C129DNCPDT microcontrollers before purchase
- Development Kits provide you with all the tools you need to develop and prototype embedded applications right out of the box

See the Tiva series website at http://www.ti.com/tiva-c for the latest tools available, or ask your distributor.

1.5 Support Information

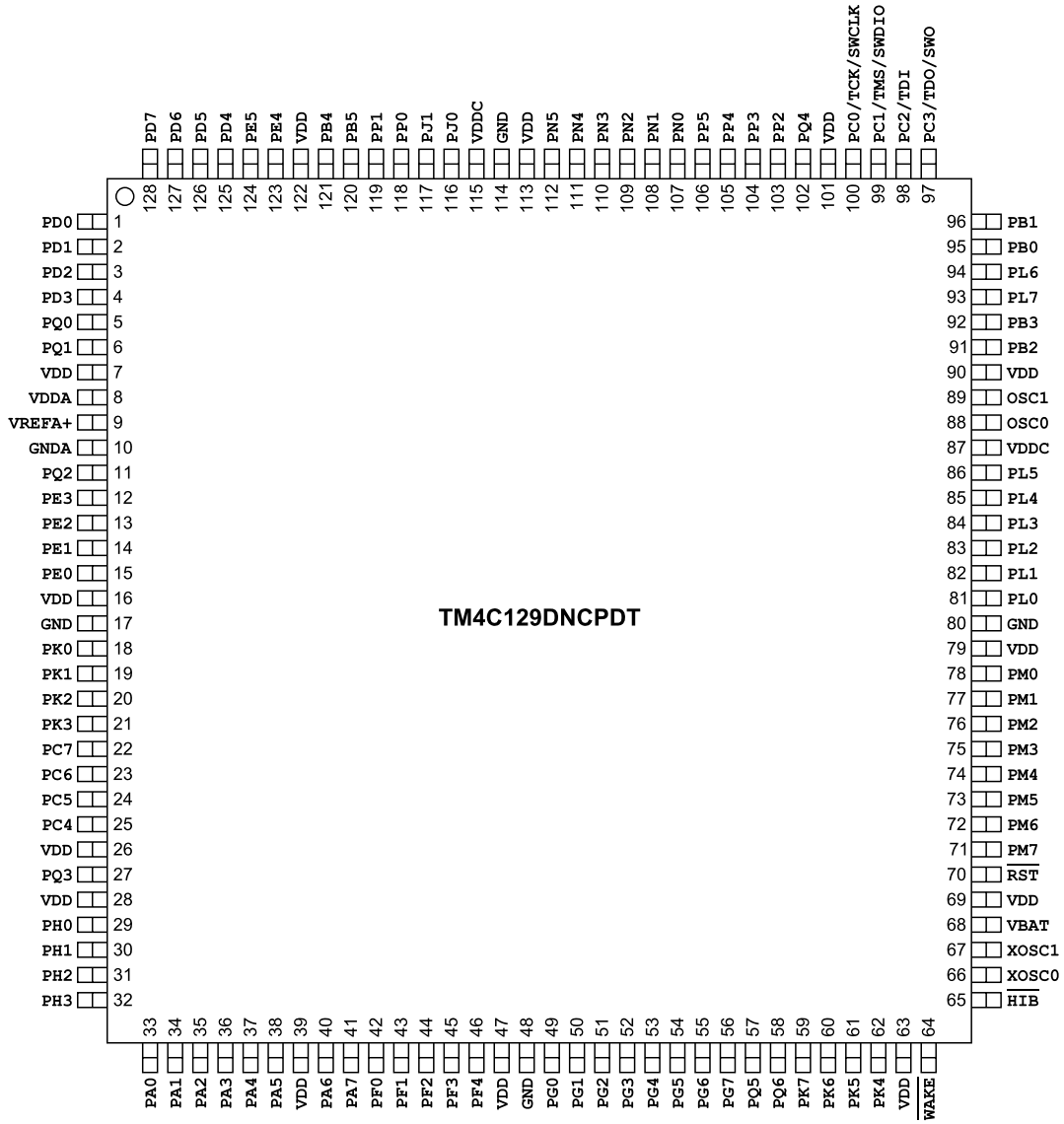
For support on Tiva™ C Series products, contact the TI Worldwide Product Information Center nearest you.

2 Pin Diagram

The TM4C129DNCPDT microcontroller pin diagram is shown below.

Each GPIO signal is identified by its GPIO port unless it defaults to an alternate function on reset. In this case, the GPIO port name is followed by the default alternate function. To see a complete list of possible functions for each pin, see Table 3-5 on page 74.

Figure 2-1. 128-Pin TQFP Package Pin Diagram



3 Signal Tables

The following tables list the signals available for each pin. Signals are configured as GPIOs on reset, except for those noted below. Use the **GPIOAMSEL** register to select analog mode. For a GPIO pin to be used for an alternate digital function, the corresponding bit in the **GPIOAFSEL** register must be set. Further pin muxing options are provided through the PMCx bit field in the **GPIOPCTL** register, which selects one of several available peripheral functions for that GPIO.

Important: All GPIO pins are configured as GPIOs by default with the exception of the pins shown in the table below. A Power-On-Reset ($\overline{POR}$) or asserting $\overline{RST}$ puts the pins back to their default state.

Table 3-1. GPIO Pins With Default Alternate Functions

GPIO Pin	Default State	GPIOAFSEL Bit	GPIOPCTL PMCx Bit Field
PA[1:0]	UART0	0	0x1
PA[5:2]	SSI0	0	0x1
PB[3:2]	I^2C0	0	0x1
PC[3:0]	JTAG/SWD	1	0x3

Table 3-2 on page 38 shows the pin-to-signal-name mapping, including functional characteristics of the signals. Each possible alternate analog and digital function is listed for each pin.

Table 3-3 on page 51 lists the signals in alphabetical order by signal name. If it is possible for a signal to be on multiple pins, each possible pin assignment is listed. The "Pin Mux" column indicates the GPIO and the encoding needed in the PMCx bit field in the **GPIOPCTL** register.

Table 3-4 on page 63 groups the signals by functionality, except for GPIOs. If it is possible for a signal to be on multiple pins, each possible pin assignment is listed.

Table 3-5 on page 74 lists the GPIO pins and their analog and digital alternate functions. The AINx analog signals are not 5-V tolerant and go through an isolation circuit before reaching their circuitry. These signals are configured by clearing the corresponding DEN bit in the **GPIO Digital Enable (GPIODEN)** register and setting the corresponding AMSEL bit in the **GPIO Analog Mode Select (GPIOAMSEL)** register. Other analog signals are 3.3-V tolerant and are connected directly to their circuitry (C0-, C0+, C1-, C1+, C2-, C2+, USB0VBUS, USB0ID). These signals are configured by clearing the DEN bit in the **GPIO Digital Enable (GPIODEN)** register. The digital signals are enabled by setting the appropriate bit in the **GPIO Alternate Function Select (GPIOAFSEL)** and **GPIODEN** registers and configuring the PMCx bit field in the **GPIO Port Control (GPIOPCTL)** register to the numeric enoding shown in the table below. Table entries that are shaded gray are the default values for the corresponding GPIO pin.

Table 3-6 on page 78 lists the signals based on number of possible pin assignments. This table can be used to plan how to configure the pins for a particular functionality. Application Note AN01274 Configuring Tiva™ C Series Microcontrollers with Pin Multiplexing provides an overview of the pin muxing implementation, an explanation of how a system designer defines a pin configuration, and examples of the pin configuration process.

Note: All digital inputs are Schmitt triggered.

3.1 Signals by Pin Number

Table 3-2. Signals by Pin Number

Pin Number	Pin Name	Pin Type	Buffer Type	Description
1	PD0	I/O	TTL	GPIO port D bit 0.
	AIN15	I	Analog	Analog-to-digital converter input 15.
	C0o	O	TTL	Analog comparator 0 output.
	I2C7SCL	I/O	OD	I^2C module 7 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	SSI2XDAT1	I/O	TTL	SSI Module 2 Bi-directional Data Pin 1 (SSI2RX in Legacy SSI Mode).
	T0CCP0	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 0.
2	PD1	I/O	TTL	GPIO port D bit 1.
	AIN14	I	Analog	Analog-to-digital converter input 14.
	C1o	O	TTL	Analog comparator 1 output.
	I2C7SDA	I/O	OD	I^2C module 7 data.
	SSI2XDAT0	I/O	TTL	SSI Module 2 Bi-directional Data Pin 0 (SSI2TX in Legacy SSI Mode).
	T0CCP1	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 1.
3	PD2	I/O	TTL	GPIO port D bit 2.
	AIN13	I	Analog	Analog-to-digital converter input 13.
	C2o	O	TTL	Analog comparator 2 output.
	I2C8SCL	I/O	OD	I^2C module 8 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	SSI2Fss	I/O	TTL	SSI module 2 frame signal.
	T1CCP0	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 0.
4	PD3	I/O	TTL	GPIO port D bit 3.
	AIN12	I	Analog	Analog-to-digital converter input 12.
	I2C8SDA	I/O	OD	I^2C module 8 data.
	SSI2Clk	I/O	TTL	SSI module 2 clock.
	T1CCP1	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 1.
5	PQ0	I/O	TTL	GPIO port Q bit 0.
	EPI0S20	I/O	TTL	EPI module 0 signal 20.
	SSI3Clk	I/O	TTL	SSI module 3 clock.
6	PQ1	I/O	TTL	GPIO port Q bit 1.
	EPI0S21	I/O	TTL	EPI module 0 signal 21.
	SSI3Fss	I/O	TTL	SSI module 3 frame signal.
7	VDD	-	Power	Positive supply for I/O and some logic.
8	VDDA	-	Power	The positive supply for the analog circuits (ADC, Analog Comparators, etc.). These are separated from VDD to minimize the electrical noise contained on VDD from affecting the analog functions. VDDA pins must be supplied with a voltage that meets the specification in , regardless of system implementation.

Table 3-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
9	VREFA+	-	Analog	A reference voltage used to specify the voltage at which the ADC converts to a maximum value. This pin is used in conjunction with GNDA. The voltage that is applied to VREFA+ is the voltage with which an AINn signal is converted to 4095. The VREFA+ voltage is limited to the range specified in the data sheet .
10	GNDA	-	Power	The ground reference for the analog circuits (ADC, Analog Comparators, etc.). These are separated from GND to minimize the electrical noise contained on VDD from affecting the analog functions.
11	PQ2	I/O	TTL	GPIO port Q bit 2.
	EPI0S22	I/O	TTL	EPI module 0 signal 22.
	SSI3XDAT0	I/O	TTL	SSI Module 3 Bi-directional Data Pin 0 (SSI3TX in Legacy SSI Mode).
12	PE3	I/O	TTL	GPIO port E bit 3.
	AIN0	I	Analog	Analog-to-digital converter input 0.
	U1DTR	O	TTL	UART module 1 Data Terminal Ready modem status input signal.
13	PE2	I/O	TTL	GPIO port E bit 2.
	AIN1	I	Analog	Analog-to-digital converter input 1.
	U1DCD	I	TTL	UART module 1 Data Carrier Detect modem status input signal.
14	PE1	I/O	TTL	GPIO port E bit 1.
	AIN2	I	Analog	Analog-to-digital converter input 2.
	U1DSR	I	TTL	UART module 1 Data Set Ready modem output control line.
15	PE0	I/O	TTL	GPIO port E bit 0.
	AIN3	I	Analog	Analog-to-digital converter input 3.
	U1RTS	O	TTL	UART module 1 Request to Send modem flow control output line.
16	VDD	-	Power	Positive supply for I/O and some logic.
17	GND	-	Power	Ground reference for logic and I/O pins.
18	PK0	I/O	TTL	GPIO port K bit 0.
	AIN16	I	Analog	Analog-to-digital converter input 16.
	EPI0S0	I/O	TTL	EPI module 0 signal 0.
	U4Rx	I	TTL	UART module 4 receive.
19	PK1	I/O	TTL	GPIO port K bit 1.
	AIN17	I	Analog	Analog-to-digital converter input 17.
	EPI0S1	I/O	TTL	EPI module 0 signal 1.
	U4Tx	O	TTL	UART module 4 transmit.
20	PK2	I/O	TTL	GPIO port K bit 2.
	AIN18	I	Analog	Analog-to-digital converter input 18.
	EPI0S2	I/O	TTL	EPI module 0 signal 2.
	U4RTS	O	TTL	UART module 4 Request to Send modem flow control output line.
21	PK3	I/O	TTL	GPIO port K bit 3.
	AIN19	I	Analog	Analog-to-digital converter input 19.
	EPI0S3	I/O	TTL	EPI module 0 signal 3.
	U4CTS	I	TTL	UART module 4 Clear To Send modem flow control input signal.

Table 3-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
22	PC7	I/O	TTL	GPIO port C bit 7.
	C0-	I	Analog	Analog comparator 0 negative input.
	EPI0S4	I/O	TTL	EPI module 0 signal 4.
	U5Tx	O	TTL	UART module 5 transmit.
23	PC6	I/O	TTL	GPIO port C bit 6.
	C0+	I	Analog	Analog comparator 0 positive input.
	EPI0S5	I/O	TTL	EPI module 0 signal 5.
	U5Rx	I	TTL	UART module 5 receive.
24	PC5	I/O	TTL	GPIO port C bit 5.
	C1+	I	Analog	Analog comparator 1 positive input.
	EPI0S6	I/O	TTL	EPI module 0 signal 6.
	RTCCLK	O	TTL	Buffered version of the Hibernation module's 32.768-kHz clock. This signal is not output when the part is in Hibernate mode and before being configured after power-on reset.
	U7Tx	O	TTL	UART module 7 transmit.
25	PC4	I/O	TTL	GPIO port C bit 4.
	C1-	I	Analog	Analog comparator 1 negative input.
	EPI0S7	I/O	TTL	EPI module 0 signal 7.
	U7Rx	I	TTL	UART module 7 receive.
26	VDD	-	Power	Positive supply for I/O and some logic.
27	PQ3	I/O	TTL	GPIO port Q bit 3.
	EPI0S23	I/O	TTL	EPI module 0 signal 23.
	SSI3XDAT1	I/O	TTL	SSI Module 3 Bi-directional Data Pin 1 (SSI3RX in Legacy SSI Mode).
28	VDD	-	Power	Positive supply for I/O and some logic.
29	PH0	I/O	TTL	GPIO port H bit 0.
	EPI0S0	I/O	TTL	EPI module 0 signal 0.
	U0RTS	O	TTL	UART module 0 Request to Send modem flow control output signal.
30	PH1	I/O	TTL	GPIO port H bit 1.
	EPI0S1	I/O	TTL	EPI module 0 signal 1.
	U0CTS	I	TTL	UART module 0 Clear To Send modem flow control input signal.
31	PH2	I/O	TTL	GPIO port H bit 2.
	EPI0S2	I/O	TTL	EPI module 0 signal 2.
	U0DCD	I	TTL	UART module 0 Data Carrier Detect modem status input signal.
32	PH3	I/O	TTL	GPIO port H bit 3.
	EPI0S3	I/O	TTL	EPI module 0 signal 3.
	U0DSR	I	TTL	UART module 0 Data Set Ready modem output control line.

Table 3-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
33	PA0	I/O	TTL	GPIO port A bit 0.
	CAN0Rx	I	TTL	CAN module 0 receive.
	I2C9SCL	I/O	OD	I^2C module 9 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	T0CCP0	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 0.
	U0Rx	I	TTL	UART module 0 receive.
34	PA1	I/O	TTL	GPIO port A bit 1.
	CAN0Tx	O	TTL	CAN module 0 transmit.
	I2C9SDA	I/O	OD	I^2C module 9 data.
	T0CCP1	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 1.
	U0Tx	O	TTL	UART module 0 transmit.
35	PA2	I/O	TTL	GPIO port A bit 2.
	I2C8SCL	I/O	OD	I^2C module 8 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	SSI0Clk	I/O	TTL	SSI module 0 clock
	T1CCP0	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 0.
	U4Rx	I	TTL	UART module 4 receive.
36	PA3	I/O	TTL	GPIO port A bit 3.
	I2C8SDA	I/O	OD	I^2C module 8 data.
	SSI0Fss	I/O	TTL	SSI module 0 frame signal
	T1CCP1	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 1.
	U4Tx	O	TTL	UART module 4 transmit.
37	PA4	I/O	TTL	GPIO port A bit 4.
	I2C7SCL	I/O	OD	I^2C module 7 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	SSI0XDAT0	I/O	TTL	SSI Module 0 Bi-directional Data Pin 0 (SSI0TX in Legacy SSI Mode).
	T2CCP0	I/O	TTL	16/32-Bit Timer 2 Capture/Compare/PWM 0.
	U3Rx	I	TTL	UART module 3 receive.
38	PA5	I/O	TTL	GPIO port A bit 5.
	I2C7SDA	I/O	OD	I^2C module 7 data.
	SSI0XDAT1	I/O	TTL	SSI Module 0 Bi-directional Data Pin 1 (SSI0RX in Legacy SSI Mode).
	T2CCP1	I/O	TTL	16/32-Bit Timer 2 Capture/Compare/PWM 1.
	U3Tx	O	TTL	UART module 3 transmit.
39	VDD	-	Power	Positive supply for I/O and some logic.

Table 3-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
40	PA6	I/O	TTL	GPIO port A bit 6.
	EN0RXCK	I	TTL	Ethernet 0 Receive Clock.
	EPI0S8	I/O	TTL	EPI module 0 signal 8.
	I2C6SCL	I/O	OD	I^2C module 6 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	SSI0XDAT2	I/O	TTL	SSI Module 0 Bi-directional Data Pin 2.
	T3CCP0	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 0.
	U2Rx	I	TTL	UART module 2 receive.
	USB0EPEN	O	TTL	Optionally used in Host mode to control an external power source to supply power to the USB bus.
41	PA7	I/O	TTL	GPIO port A bit 7.
	EPI0S9	I/O	TTL	EPI module 0 signal 9.
	I2C6SDA	I/O	OD	I^2C module 6 data.
	SSI0XDAT3	I/O	TTL	SSI Module 0 Bi-directional Data Pin 3.
	T3CCP1	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 1.
	U2Tx	O	TTL	UART module 2 transmit.
	USB0EPEN	O	TTL	Optionally used in Host mode to control an external power source to supply power to the USB bus.
	USB0PFLT	I	TTL	Optionally used in Host mode by an external power source to indicate an error state by that power source.
42	PF0	I/O	TTL	GPIO port F bit 0.
	M0PWM0	O	TTL	Motion Control Module 0 PWM 0. This signal is controlled by Module 0 PWM Generator 0.
	SSI3XDAT1	I/O	TTL	SSI Module 3 Bi-directional Data Pin 1 (SSI3RX in Legacy SSI Mode).
	TRD2	O	TTL	Trace data 2.
43	PF1	I/O	TTL	GPIO port F bit 1.
	M0PWM1	O	TTL	Motion Control Module 0 PWM 1. This signal is controlled by Module 0 PWM Generator 0.
	SSI3XDAT0	I/O	TTL	SSI Module 3 Bi-directional Data Pin 0 (SSI3TX in Legacy SSI Mode).
	TRD1	O	TTL	Trace data 1.
44	PF2	I/O	TTL	GPIO port F bit 2.
	EN0MDC	O	TTL	Ethernet 0 Management Data Clock.
	M0PWM2	O	TTL	Motion Control Module 0 PWM 2. This signal is controlled by Module 0 PWM Generator 1.
	SSI3Fss	I/O	TTL	SSI module 3 frame signal.
	TRD0	O	TTL	Trace data 0.
45	PF3	I/O	TTL	GPIO port F bit 3.
	EN0MDIO	I/O	TTL	Ethernet 0 Management Data Input/Output signal.
	M0PWM3	O	TTL	Motion Control Module 0 PWM 3. This signal is controlled by Module 0 PWM Generator 1.
	SSI3Clk	I/O	TTL	SSI module 3 clock.
	TRCLK	O	TTL	Trace clock.

Table 3-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
46	PF4	I/O	TTL	GPIO port F bit 4.
	M0FAULT0	I	TTL	Motion Control Module 0 PWM Fault 0.
	SSI3XDAT2	I/O	TTL	SSI Module 3 Bi-directional Data Pin 2.
	TRD3	O	TTL	Trace data 3.
47	VDD	-	Power	Positive supply for I/O and some logic.
48	GND	-	Power	Ground reference for logic and I/O pins.
49	PG0	I/O	TTL	GPIO port G bit 0.
	EPI0S11	I/O	TTL	EPI module 0 signal 11.
	I2C1SCL	I/O	OD	I^2C module 1 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	M0PWM4	O	TTL	Motion Control Module 0 PWM 4. This signal is controlled by Module 0 PWM Generator 2.
50	PG1	I/O	TTL	GPIO port G bit 1.
	EPI0S10	I/O	TTL	EPI module 0 signal 10.
	I2C1SDA	I/O	OD	I^2C module 1 data.
	M0PWM5	O	TTL	Motion Control Module 0 PWM 5. This signal is controlled by Module 0 PWM Generator 2.
51	PG2	I/O	TTL	GPIO port G bit 2.
	EN0TXCK	I	TTL	Ethernet 0 Transmit Clock.
	I2C2SCL	I/O	OD	I^2C module 2 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	SSI2XDAT3	I/O	TTL	SSI Module 2 Bi-directional Data Pin 3.
52	PG3	I/O	TTL	GPIO port G bit 3.
	EN0TXEN	O	TTL	Ethernet 0 Transmit Enable.
	I2C2SDA	I/O	OD	I^2C module 2 data.
	SSI2XDAT2	I/O	TTL	SSI Module 2 Bi-directional Data Pin 2.
53	PG4	I/O	TTL	GPIO port G bit 4.
	EN0TXD0	O	TTL	Ethernet 0 Transmit Data 0.
	I2C3SCL	I/O	OD	I^2C module 3 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	SSI2XDAT1	I/O	TTL	SSI Module 2 Bi-directional Data Pin 1 (SSI2RX in Legacy SSI Mode).
	U0CTS	I	TTL	UART module 0 Clear To Send modem flow control input signal.
54	PG5	I/O	TTL	GPIO port G bit 5.
	EN0TXD1	O	TTL	Ethernet 0 Transmit Data 1.
	I2C3SDA	I/O	OD	I^2C module 3 data.
	SSI2XDAT0	I/O	TTL	SSI Module 2 Bi-directional Data Pin 0 (SSI2TX in Legacy SSI Mode).
	U0RTS	O	TTL	UART module 0 Request to Send modem flow control output signal.
55	PG6	I/O	TTL	GPIO port G bit 6.
	EN0RXER	I	TTL	Ethernet 0 Receive Error.
	I2C4SCL	I/O	OD	I^2C module 4 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	SSI2Fss	I/O	TTL	SSI module 2 frame signal.

Table 3-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
56	PG7	I/O	TTL	GPIO port G bit 7.
	EN0RXDV	I	TTL	Ethernet 0 Receive Data Valid.
	I2C4SDA	I/O	OD	I^2C module 4 data.
	SSI2Clk	I/O	TTL	SSI module 2 clock.
57	PQ5	I/O	TTL	GPIO port Q bit 5.
	EN0RXD0	I	TTL	Ethernet 0 Receive Data 0.
	U1Tx	O	TTL	UART module 1 transmit.
58	PQ6	I/O	TTL	GPIO port Q bit 6.
	EN0RXD1	I	TTL	Ethernet 0 Receive Data 1.
	U1DTR	O	TTL	UART module 1 Data Terminal Ready modem status input signal.
59	PK7	I/O	TTL	GPIO port K bit 7.
	EN0TXD3	O	TTL	Ethernet 0 Transmit Data 3.
	EPI0S24	I/O	TTL	EPI module 0 signal 24.
	I2C4SDA	I/O	OD	I^2C module 4 data.
	M0FAULT2	I	TTL	Motion Control Module 0 PWM Fault 2.
	RTCCLK	O	TTL	Buffered version of the Hibernation module's 32.768-kHz clock. This signal is not output when the part is in Hibernate mode and before being configured after power-on reset.
	U0RI	I	TTL	UART module 0 Ring Indicator modem status input signal.
60	PK6	I/O	TTL	GPIO port K bit 6.
	EN0TXD2	O	TTL	Ethernet 0 Transmit Data 2.
	EPI0S25	I/O	TTL	EPI module 0 signal 25.
	I2C4SCL	I/O	OD	I^2C module 4 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	M0FAULT1	I	TTL	Motion Control Module 0 PWM Fault 1.
61	PK5	I/O	TTL	GPIO port K bit 5.
	EN0RXD2	I	TTL	Ethernet 0 Receive Data 2.
	EPI0S31	I/O	TTL	EPI module 0 signal 31.
	I2C3SDA	I/O	OD	I^2C module 3 data.
	M0PWM7	O	TTL	Motion Control Module 0 PWM 7. This signal is controlled by Module 0 PWM Generator 3.
62	PK4	I/O	TTL	GPIO port K bit 4.
	EN0INTRN	I	TTL	Ethernet 0 Interrupt from the Ethernet PHY.
	EN0RXD3	I	TTL	Ethernet 0 Receive Data 3.
	EPI0S32	I/O	TTL	EPI module 0 signal 32.
	I2C3SCL	I/O	OD	I^2C module 3 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	M0PWM6	O	TTL	Motion Control Module 0 PWM 6. This signal is controlled by Module 0 PWM Generator 3.
63	VDD	-	Power	Positive supply for I/O and some logic.
64	$\overline{\text{WAKE}}$	I	TTL	An external input that brings the processor out of Hibernate mode when asserted.
65	$\overline{\text{HIB}}$	O	TTL	An output that indicates the processor is in Hibernate mode.

Table 3-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
66	XOSC0	I	Analog	Hibernation module oscillator crystal input or an external clock reference input. Note that this is either a crystal or a 32.768-kHz oscillator for the Hibernation module RTC.
67	XOSC1	O	Analog	Hibernation module oscillator crystal output. Leave unconnected when using a single-ended clock source.
68	VBAT	-	Power	Power source for the Hibernation module. It is normally connected to the positive terminal of a battery and serves as the battery backup/Hibernation module power-source supply.
69	VDD	-	Power	Positive supply for I/O and some logic.
70	$\overline{\text{RST}}$	I	TTL	System reset input.
71	PM7	I/O	TTL	GPIO port M bit 7.
	EN0COL	I	TTL	Ethernet 0 Collision Detect.
	T5CCP1	I/O	TTL	16/32-Bit Timer 5 Capture/Compare/PWM 1.
	TMPR0	I/O	TTL	Tamper signal 0.
	U0RI	I	TTL	UART module 0 Ring Indicator modem status input signal.
72	PM6	I/O	TTL	GPIO port M bit 6.
	EN0CRS	I	TTL	Ethernet 0 Carrier Sense.
	T5CCP0	I/O	TTL	16/32-Bit Timer 5 Capture/Compare/PWM 0.
	TMPR1	I/O	TTL	Tamper signal 1.
	U0DSR	I	TTL	UART module 0 Data Set Ready modem output control line.
73	PM5	I/O	TTL	GPIO port M bit 5.
	T4CCP1	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 1.
	TMPR2	I/O	TTL	Tamper signal 2.
	U0DCD	I	TTL	UART module 0 Data Carrier Detect modem status input signal.
74	PM4	I/O	TTL	GPIO port M bit 4.
	EN0RREF_CLK	I/O	TTL	Ethernet 0 Reference Clock.
	T4CCP0	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 0.
	TMPR3	I/O	TTL	Tamper signal 3.
	U0CTS	I	TTL	UART module 0 Clear To Send modem flow control input signal.
75	PM3	I/O	TTL	GPIO port M bit 3.
	EPI0S12	I/O	TTL	EPI module 0 signal 12.
	T3CCP1	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 1.
76	PM2	I/O	TTL	GPIO port M bit 2.
	EPI0S13	I/O	TTL	EPI module 0 signal 13.
	T3CCP0	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 0.
77	PM1	I/O	TTL	GPIO port M bit 1.
	EPI0S14	I/O	TTL	EPI module 0 signal 14.
	T2CCP1	I/O	TTL	16/32-Bit Timer 2 Capture/Compare/PWM 1.
78	PM0	I/O	TTL	GPIO port M bit 0.
	EPI0S15	I/O	TTL	EPI module 0 signal 15.
	T2CCP0	I/O	TTL	16/32-Bit Timer 2 Capture/Compare/PWM 0.
79	VDD	-	Power	Positive supply for I/O and some logic.
80	GND	-	Power	Ground reference for logic and I/O pins.

Table 3-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
81	PL0	I/O	TTL	GPIO port L bit 0.
	EPI0S16	I/O	TTL	EPI module 0 signal 16.
	I2C2SDA	I/O	OD	I^2C module 2 data.
	M0FAULT3	I	TTL	Motion Control Module 0 PWM Fault 3.
	USB0D0	I/O	TTL	USB data 0.
82	PL1	I/O	TTL	GPIO port L bit 1.
	EPI0S17	I/O	TTL	EPI module 0 signal 17.
	I2C2SCL	I/O	OD	I^2C module 2 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	PhA0	I	TTL	QEI module 0 phase A.
	USB0D1	I/O	TTL	USB data 1.
83	PL2	I/O	TTL	GPIO port L bit 2.
	C0o	O	TTL	Analog comparator 0 output.
	EPI0S18	I/O	TTL	EPI module 0 signal 18.
	PhB0	I	TTL	QEI module 0 phase B.
	USB0D2	I/O	TTL	USB data 2.
84	PL3	I/O	TTL	GPIO port L bit 3.
	C1o	O	TTL	Analog comparator 1 output.
	EPI0S19	I/O	TTL	EPI module 0 signal 19.
	IDX0	I	TTL	QEI module 0 index.
	USB0D3	I/O	TTL	USB data 3.
85	PL4	I/O	TTL	GPIO port L bit 4.
	EPI0S26	I/O	TTL	EPI module 0 signal 26.
	T0CCP0	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 0.
	USB0D4	I/O	TTL	USB data 4.
86	PL5	I/O	TTL	GPIO port L bit 5.
	EPI0S33	I/O	TTL	EPI module 0 signal 33.
	T0CCP1	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 1.
	USB0D5	I/O	TTL	USB data 5.
87	VDDC	-	Power	Positive supply for most of the logic function, including the processor core and most peripherals. The voltage on this pin is 1.2 V and is supplied by the on-chip LDO. The VDDC pins should only be connected to each other and an external capacitor as specified in the data sheet.
88	OSC0	I	Analog	Main oscillator crystal input or an external clock reference input.
89	OSC1	O	Analog	Main oscillator crystal output. Leave unconnected when using a single-ended clock source.
90	VDD	-	Power	Positive supply for I/O and some logic.

Table 3-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
91	PB2	I/O	TTL	GPIO port B bit 2.
	EN0MDC	O	TTL	Ethernet 0 Management Data Clock.
	EPI0S27	I/O	TTL	EPI module 0 signal 27.
	I2C0SCL	I/O	OD	I^2C module 0 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	T5CCP0	I/O	TTL	16/32-Bit Timer 5 Capture/Compare/PWM 0.
	USB0STP	O	TTL	Asserted by the USB controller to signal the end of a USB transmit packet or register write operation.
92	PB3	I/O	TTL	GPIO port B bit 3.
	EN0MDIO	I/O	TTL	Ethernet 0 Management Data Input/Output signal.
	EPI0S28	I/O	TTL	EPI module 0 signal 28.
	I2C0SDA	I/O	OD	I^2C module 0 data.
	T5CCP1	I/O	TTL	16/32-Bit Timer 5 Capture/Compare/PWM 1.
	USB0CLK	O	TTL	60-MHz clock to the external PHY.
93	PL7	I/O	TTL	GPIO port L bit 7.
	T1CCP1	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 1.
	USB0DM	I/O	Analog	Bidirectional differential data pin (D- per USB specification) for USB0.
94	PL6	I/O	TTL	GPIO port L bit 6.
	T1CCP0	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 0.
	USB0DP	I/O	Analog	Bidirectional differential data pin (D+ per USB specification) for USB0.
95	PB0	I/O	TTL	GPIO port B bit 0.
	CAN1Rx	I	TTL	CAN module 1 receive.
	I2C5SCL	I/O	OD	I^2C module 5 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	T4CCP0	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 0.
	U1Rx	I	TTL	UART module 1 receive.
	USB0ID	I	Analog	This signal senses the state of the USB ID signal. The USB PHY enables an integrated pull-up, and an external element (USB connector) indicates the initial state of the USB controller (pulled down is the A side of the cable and pulled up is the B side).
96	PB1	I/O	TTL	GPIO port B bit 1.
	CAN1Tx	O	TTL	CAN module 1 transmit.
	I2C5SDA	I/O	OD	I^2C module 5 data.
	T4CCP1	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 1.
	U1Tx	O	TTL	UART module 1 transmit.
	USB0VBUS	I/O	Analog	This signal is used during the session request protocol. This signal allows the USB PHY to both sense the voltage level of VBUS, and pull up VBUS momentarily during VBUS pulsing.
97	PC3	I/O	TTL	GPIO port C bit 3.
	SWO	O	TTL	JTAG TDO and SWO.
	TDO	O	TTL	JTAG TDO and SWO.

Table 3-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
98	PC2	I/O	TTL	GPIO port C bit 2.
	TDI	I	TTL	JTAG TDI.
99	PC1	I/O	TTL	GPIO port C bit 1.
	SWDIO	I/O	TTL	JTAG TMS and SWDIO.
	TMS	I	TTL	JTAG TMS and SWDIO.
100	PC0	I/O	TTL	GPIO port C bit 0.
	SWCLK	I	TTL	JTAG/SWD CLK.
	TCK	I	TTL	JTAG/SWD CLK.
101	VDD	-	Power	Positive supply for I/O and some logic.
102	PQ4	I/O	TTL	GPIO port Q bit 4.
	DIVSCLK	O	TTL	An optionally divided reference clock output based on a selected clock source.
	U1Rx	I	TTL	UART module 1 receive.
103	PP2	I/O	TTL	GPIO port P bit 2.
	EPI0S29	I/O	TTL	EPI module 0 signal 29.
	U0DTR	O	TTL	UART module 0 Data Terminal Ready modem status input signal.
	USB0NXT	O	TTL	Asserted by the external PHY to throttle all data types.
104	PP3	I/O	TTL	GPIO port P bit 3.
	EPI0S30	I/O	TTL	EPI module 0 signal 30.
	RTCCLK	O	TTL	Buffered version of the Hibernation module's 32.768-kHz clock. This signal is not output when the part is in Hibernate mode and before being configured after power-on reset.
	U0DCD	I	TTL	UART module 0 Data Carrier Detect modem status input signal.
	U1CTS	I	TTL	UART module 1 Clear To Send modem flow control input signal.
	USB0DIR	O	TTL	Indicates that the external PHY is able to accept data from the USB controller.
105	PP4	I/O	TTL	GPIO port P bit 4.
	U0DSR	I	TTL	UART module 0 Data Set Ready modem output control line.
	U3RTS	O	TTL	UART module 3 Request to Send modem flow control output line.
	USB0D7	I/O	TTL	USB data 7.
106	PP5	I/O	TTL	GPIO port P bit 5.
	I2C2SCL	I/O	OD	I^2C module 2 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	U3CTS	I	TTL	UART module 3 Clear To Send modem flow control input signal.
	USB0D6	I/O	TTL	USB data 6.
107	PN0	I/O	TTL	GPIO port N bit 0.
	U1RTS	O	TTL	UART module 1 Request to Send modem flow control output line.
108	PN1	I/O	TTL	GPIO port N bit 1.
	U1CTS	I	TTL	UART module 1 Clear To Send modem flow control input signal.
109	PN2	I/O	TTL	GPIO port N bit 2.
	EPI0S29	I/O	TTL	EPI module 0 signal 29.
	U1DCD	I	TTL	UART module 1 Data Carrier Detect modem status input signal.
	U2RTS	O	TTL	UART module 2 Request to Send modem flow control output line.

Table 3-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
110	PN3	I/O	TTL	GPIO port N bit 3.
	EPI0S30	I/O	TTL	EPI module 0 signal 30.
	U1DSR	I	TTL	UART module 1 Data Set Ready modem output control line.
	U2CTS	I	TTL	UART module 2 Clear To Send modem flow control input signal.
111	PN4	I/O	TTL	GPIO port N bit 4.
	EPI0S34	I/O	TTL	EPI module 0 signal 34.
	I2C2SDA	I/O	OD	I^2C module 2 data.
	U1DTR	O	TTL	UART module 1 Data Terminal Ready modem status input signal.
	U3RTS	O	TTL	UART module 3 Request to Send modem flow control output line.
112	PN5	I/O	TTL	GPIO port N bit 5.
	EPI0S35	I/O	TTL	EPI module 0 signal 35.
	I2C2SCL	I/O	OD	I^2C module 2 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	U1RI	I	TTL	UART module 1 Ring Indicator modem status input signal.
	U3CTS	I	TTL	UART module 3 Clear To Send modem flow control input signal.
113	VDD	-	Power	Positive supply for I/O and some logic.
114	GND	-	Power	Ground reference for logic and I/O pins.
115	VDDC	-	Power	Positive supply for most of the logic function, including the processor core and most peripherals. The voltage on this pin is 1.2 V and is supplied by the on-chip LDO. The VDDC pins should only be connected to each other and an external capacitor as specified in the data sheet.
116	PJ0	I/O	TTL	GPIO port J bit 0.
	U3Rx	I	TTL	UART module 3 receive.
117	PJ1	I/O	TTL	GPIO port J bit 1.
	U3Tx	O	TTL	UART module 3 transmit.
118	PP0	I/O	TTL	GPIO port P bit 0.
	C2+	I	Analog	Analog comparator 2 positive input.
	EN0INTRN	I	TTL	Ethernet 0 Interrupt from the Ethernet PHY.
	SSI3XDAT2	I/O	TTL	SSI Module 3 Bi-directional Data Pin 2.
	U6Rx	I	TTL	UART module 6 receive.
119	PP1	I/O	TTL	GPIO port P bit 1.
	C2-	I	Analog	Analog comparator 2 negative input.
	SSI3XDAT3	I/O	TTL	SSI Module 3 Bi-directional Data Pin 3.
	U6Tx	O	TTL	UART module 6 transmit.
120	PB5	I/O	TTL	GPIO port B bit 5.
	AIN11	I	Analog	Analog-to-digital converter input 11.
	I2C5SDA	I/O	OD	I^2C module 5 data.
	SSI1Clk	I/O	TTL	SSI module 1 clock.
	U0RTS	O	TTL	UART module 0 Request to Send modem flow control output signal.

Table 3-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
121	PB4	I/O	TTL	GPIO port B bit 4.
	AIN10	I	Analog	Analog-to-digital converter input 10.
	I2C5SCL	I/O	OD	I^2C module 5 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	SSI1Fss	I/O	TTL	SSI module 1 frame signal.
	U0CTS	I	TTL	UART module 0 Clear To Send modem flow control input signal.
122	VDD	-	Power	Positive supply for I/O and some logic.
123	PE4	I/O	TTL	GPIO port E bit 4.
	AIN9	I	Analog	Analog-to-digital converter input 9.
	SSI1XDAT0	I/O	TTL	SSI Module 1 Bi-directional Data Pin 0 (SSI1TX in Legacy SSI Mode).
	U1RI	I	TTL	UART module 1 Ring Indicator modem status input signal.
124	PE5	I/O	TTL	GPIO port E bit 5.
	AIN8	I	Analog	Analog-to-digital converter input 8.
	SSI1XDAT1	I/O	TTL	SSI Module 1 Bi-directional Data Pin 1 (SSI1RX in Legacy SSI Mode).
125	PD4	I/O	TTL	GPIO port D bit 4.
	AIN7	I	Analog	Analog-to-digital converter input 7.
	SSI1XDAT2	I/O	TTL	SSI Module 1 Bi-directional Data Pin 2.
	T3CCP0	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 0.
	U2Rx	I	TTL	UART module 2 receive.
126	PD5	I/O	TTL	GPIO port D bit 5.
	AIN6	I	Analog	Analog-to-digital converter input 6.
	SSI1XDAT3	I/O	TTL	SSI Module 1 Bi-directional Data Pin 3.
	T3CCP1	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 1.
	U2Tx	O	TTL	UART module 2 transmit.
127	PD6	I/O	TTL	GPIO port D bit 6.
	AIN5	I	Analog	Analog-to-digital converter input 5.
	SSI2XDAT3	I/O	TTL	SSI Module 2 Bi-directional Data Pin 3.
	T4CCP0	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 0.
	U2RTS	O	TTL	UART module 2 Request to Send modem flow control output line.
	USB0EPEN	O	TTL	Optionally used in Host mode to control an external power source to supply power to the USB bus.
128	PD7	I/O	TTL	GPIO port D bit 7.
	AIN4	I	Analog	Analog-to-digital converter input 4.
	NMI	I	TTL	Non-maskable interrupt.
	SSI2XDAT2	I/O	TTL	SSI Module 2 Bi-directional Data Pin 2.
	T4CCP1	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 1.
	U2CTS	I	TTL	UART module 2 Clear To Send modem flow control input signal.
	USB0PFLT	I	TTL	Optionally used in Host mode by an external power source to indicate an error state by that power source.

3.2 Signals by Signal Name

Table 3-3. Signals by Signal Name

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
AIN0	12	PE3	I	Analog	Analog-to-digital converter input 0.
AIN1	13	PE2	I	Analog	Analog-to-digital converter input 1.
AIN2	14	PE1	I	Analog	Analog-to-digital converter input 2.
AIN3	15	PE0	I	Analog	Analog-to-digital converter input 3.
AIN4	128	PD7	I	Analog	Analog-to-digital converter input 4.
AIN5	127	PD6	I	Analog	Analog-to-digital converter input 5.
AIN6	126	PD5	I	Analog	Analog-to-digital converter input 6.
AIN7	125	PD4	I	Analog	Analog-to-digital converter input 7.
AIN8	124	PE5	I	Analog	Analog-to-digital converter input 8.
AIN9	123	PE4	I	Analog	Analog-to-digital converter input 9.
AIN10	121	PB4	I	Analog	Analog-to-digital converter input 10.
AIN11	120	PB5	I	Analog	Analog-to-digital converter input 11.
AIN12	4	PD3	I	Analog	Analog-to-digital converter input 12.
AIN13	3	PD2	I	Analog	Analog-to-digital converter input 13.
AIN14	2	PD1	I	Analog	Analog-to-digital converter input 14.
AIN15	1	PD0	I	Analog	Analog-to-digital converter input 15.
AIN16	18	PK0	I	Analog	Analog-to-digital converter input 16.
AIN17	19	PK1	I	Analog	Analog-to-digital converter input 17.
AIN18	20	PK2	I	Analog	Analog-to-digital converter input 18.
AIN19	21	PK3	I	Analog	Analog-to-digital converter input 19.
C0+	23	PC6	I	Analog	Analog comparator 0 positive input.
C0-	22	PC7	I	Analog	Analog comparator 0 negative input.
C0o	1 83	PD0 (5) PL2 (5)	O	TTL	Analog comparator 0 output.
C1+	24	PC5	I	Analog	Analog comparator 1 positive input.
C1-	25	PC4	I	Analog	Analog comparator 1 negative input.
C1o	2 84	PD1 (5) PL3 (5)	O	TTL	Analog comparator 1 output.
C2+	118	PP0	I	Analog	Analog comparator 2 positive input.
C2-	119	PP1	I	Analog	Analog comparator 2 negative input.
C2o	3	PD2 (5)	O	TTL	Analog comparator 2 output.
CAN0Rx	33	PA0 (7)	I	TTL	CAN module 0 receive.
CAN0Tx	34	PA1 (7)	O	TTL	CAN module 0 transmit.
CAN1Rx	95	PB0 (7)	I	TTL	CAN module 1 receive.
CAN1Tx	96	PB1 (7)	O	TTL	CAN module 1 transmit.
DIVSCLK	102	PQ4 (7)	O	TTL	An optionally divided reference clock output based on a selected clock source.
EN0COL	71	PM7 (14)	I	TTL	Ethernet 0 Collision Detect.
EN0CRS	72	PM6 (14)	I	TTL	Ethernet 0 Carrier Sense.

Table 3-3. Signals by Signal Name *(continued)*

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
EN0INTRN	62 118	PK4 (7) PP0 (7)	I	TTL	Ethernet 0 Interrupt from the Ethernet PHY.
EN0MDC	44 91	PF2 (5) PB2 (5)	O	TTL	Ethernet 0 Management Data Clock.
EN0MDIO	45 92	PF3 (5) PB3 (5)	I/O	TTL	Ethernet 0 Management Data Input/Output signal.
EN0RREF_CLK	74	PM4 (14)	I/O	TTL	Ethernet 0 Reference Clock.
EN0RXCK	40	PA6 (14)	I	TTL	Ethernet 0 Receive Clock.
EN0RXD0	57	PQ5 (14)	I	TTL	Ethernet 0 Receive Data 0.
EN0RXD1	58	PQ6 (14)	I	TTL	Ethernet 0 Receive Data 1.
EN0RXD2	61	PK5 (14)	I	TTL	Ethernet 0 Receive Data 2.
EN0RXD3	62	PK4 (14)	I	TTL	Ethernet 0 Receive Data 3.
EN0RXDV	56	PG7 (14)	I	TTL	Ethernet 0 Receive Data Valid.
EN0RXER	55	PG6 (14)	I	TTL	Ethernet 0 Receive Error.
EN0TXCK	51	PG2 (14)	I	TTL	Ethernet 0 Transmit Clock.
EN0TXD0	53	PG4 (14)	O	TTL	Ethernet 0 Transmit Data 0.
EN0TXD1	54	PG5 (14)	O	TTL	Ethernet 0 Transmit Data 1.
EN0TXD2	60	PK6 (14)	O	TTL	Ethernet 0 Transmit Data 2.
EN0TXD3	59	PK7 (14)	O	TTL	Ethernet 0 Transmit Data 3.
EN0TXEN	52	PG3 (14)	O	TTL	Ethernet 0 Transmit Enable.
EPI0S0	18 29	PK0 (15) PH0 (15)	I/O	TTL	EPI module 0 signal 0.
EPI0S1	19 30	PK1 (15) PH1 (15)	I/O	TTL	EPI module 0 signal 1.
EPI0S2	20 31	PK2 (15) PH2 (15)	I/O	TTL	EPI module 0 signal 2.
EPI0S3	21 32	PK3 (15) PH3 (15)	I/O	TTL	EPI module 0 signal 3.
EPI0S4	22	PC7 (15)	I/O	TTL	EPI module 0 signal 4.
EPI0S5	23	PC6 (15)	I/O	TTL	EPI module 0 signal 5.
EPI0S6	24	PC5 (15)	I/O	TTL	EPI module 0 signal 6.
EPI0S7	25	PC4 (15)	I/O	TTL	EPI module 0 signal 7.
EPI0S8	40	PA6 (15)	I/O	TTL	EPI module 0 signal 8.
EPI0S9	41	PA7 (15)	I/O	TTL	EPI module 0 signal 9.
EPI0S10	50	PG1 (15)	I/O	TTL	EPI module 0 signal 10.
EPI0S11	49	PG0 (15)	I/O	TTL	EPI module 0 signal 11.
EPI0S12	75	PM3 (15)	I/O	TTL	EPI module 0 signal 12.
EPI0S13	76	PM2 (15)	I/O	TTL	EPI module 0 signal 13.
EPI0S14	77	PM1 (15)	I/O	TTL	EPI module 0 signal 14.
EPI0S15	78	PM0 (15)	I/O	TTL	EPI module 0 signal 15.
EPI0S16	81	PL0 (15)	I/O	TTL	EPI module 0 signal 16.
EPI0S17	82	PL1 (15)	I/O	TTL	EPI module 0 signal 17.
EPI0S18	83	PL2 (15)	I/O	TTL	EPI module 0 signal 18.

Table 3-3. Signals by Signal Name *(continued)*

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
EPI0S19	84	PL3 (15)	I/O	TTL	EPI module 0 signal 19.
EPI0S20	5	PQ0 (15)	I/O	TTL	EPI module 0 signal 20.
EPI0S21	6	PQ1 (15)	I/O	TTL	EPI module 0 signal 21.
EPI0S22	11	PQ2 (15)	I/O	TTL	EPI module 0 signal 22.
EPI0S23	27	PQ3 (15)	I/O	TTL	EPI module 0 signal 23.
EPI0S24	59	PK7 (15)	I/O	TTL	EPI module 0 signal 24.
EPI0S25	60	PK6 (15)	I/O	TTL	EPI module 0 signal 25.
EPI0S26	85	PL4 (15)	I/O	TTL	EPI module 0 signal 26.
EPI0S27	91	PB2 (15)	I/O	TTL	EPI module 0 signal 27.
EPI0S28	92	PB3 (15)	I/O	TTL	EPI module 0 signal 28.
EPI0S29	103 109	PP2 (15) PN2 (15)	I/O	TTL	EPI module 0 signal 29.
EPI0S30	104 110	PP3 (15) PN3 (15)	I/O	TTL	EPI module 0 signal 30.
EPI0S31	61	PK5 (15)	I/O	TTL	EPI module 0 signal 31.
EPI0S32	62	PK4 (15)	I/O	TTL	EPI module 0 signal 32.
EPI0S33	86	PL5 (15)	I/O	TTL	EPI module 0 signal 33.
EPI0S34	111	PN4 (15)	I/O	TTL	EPI module 0 signal 34.
EPI0S35	112	PN5 (15)	I/O	TTL	EPI module 0 signal 35.
GND	17 48 80 114	fixed	-	Power	Ground reference for logic and I/O pins.
GNDA	10	fixed	-	Power	The ground reference for the analog circuits (ADC, Analog Comparators, etc.). These are separated from GND to minimize the electrical noise contained on VDD from affecting the analog functions.
HIB	65	fixed	O	TTL	An output that indicates the processor is in Hibernate mode.
I2C0SCL	91	PB2 (2)	I/O	OD	I^2C module 0 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
I2C0SDA	92	PB3 (2)	I/O	OD	I^2C module 0 data.
I2C1SCL	49	PG0 (2)	I/O	OD	I^2C module 1 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
I2C1SDA	50	PG1 (2)	I/O	OD	I^2C module 1 data.
I2C2SCL	51 82 106 112	PG2 (2) PL1 (2) PP5 (2) PN5 (3)	I/O	OD	I^2C module 2 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
I2C2SDA	52 81 111	PG3 (2) PL0 (2) PN4 (3)	I/O	OD	I^2C module 2 data.
I2C3SCL	53 62	PG4 (2) PK4 (2)	I/O	OD	I^2C module 3 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.

Table 3-3. Signals by Signal Name *(continued)*

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
I2C3SDA	54 61	PG5 (2) PK5 (2)	I/O	OD	I^2C module 3 data.
I2C4SCL	55 60	PG6 (2) PK6 (2)	I/O	OD	I^2C module 4 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
I2C4SDA	56 59	PG7 (2) PK7 (2)	I/O	OD	I^2C module 4 data.
I2C5SCL	95 121	PB0 (2) PB4 (2)	I/O	OD	I^2C module 5 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
I2C5SDA	96 120	PB1 (2) PB5 (2)	I/O	OD	I^2C module 5 data.
I2C6SCL	40	PA6 (2)	I/O	OD	I^2C module 6 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
I2C6SDA	41	PA7 (2)	I/O	OD	I^2C module 6 data.
I2C7SCL	1 37	PD0 (2) PA4 (2)	I/O	OD	I^2C module 7 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
I2C7SDA	2 38	PD1 (2) PA5 (2)	I/O	OD	I^2C module 7 data.
I2C8SCL	3 35	PD2 (2) PA2 (2)	I/O	OD	I^2C module 8 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
I2C8SDA	4 36	PD3 (2) PA3 (2)	I/O	OD	I^2C module 8 data.
I2C9SCL	33	PA0 (2)	I/O	OD	I^2C module 9 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
I2C9SDA	34	PA1 (2)	I/O	OD	I^2C module 9 data.
IDX0	84	PL3 (6)	I	TTL	QEI module 0 index.
M0FAULT0	46	PF4 (6)	I	TTL	Motion Control Module 0 PWM Fault 0.
M0FAULT1	60	PK6 (6)	I	TTL	Motion Control Module 0 PWM Fault 1.
M0FAULT2	59	PK7 (6)	I	TTL	Motion Control Module 0 PWM Fault 2.
M0FAULT3	81	PL0 (6)	I	TTL	Motion Control Module 0 PWM Fault 3.
M0PWM0	42	PF0 (6)	O	TTL	Motion Control Module 0 PWM 0. This signal is controlled by Module 0 PWM Generator 0.
M0PWM1	43	PF1 (6)	O	TTL	Motion Control Module 0 PWM 1. This signal is controlled by Module 0 PWM Generator 0.
M0PWM2	44	PF2 (6)	O	TTL	Motion Control Module 0 PWM 2. This signal is controlled by Module 0 PWM Generator 1.
M0PWM3	45	PF3 (6)	O	TTL	Motion Control Module 0 PWM 3. This signal is controlled by Module 0 PWM Generator 1.
M0PWM4	49	PG0 (6)	O	TTL	Motion Control Module 0 PWM 4. This signal is controlled by Module 0 PWM Generator 2.
M0PWM5	50	PG1 (6)	O	TTL	Motion Control Module 0 PWM 5. This signal is controlled by Module 0 PWM Generator 2.

Table 3-3. Signals by Signal Name *(continued)*

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
M0PWM6	62	PK4 (6)	O	TTL	Motion Control Module 0 PWM 6. This signal is controlled by Module 0 PWM Generator 3.
M0PWM7	61	PK5 (6)	O	TTL	Motion Control Module 0 PWM 7. This signal is controlled by Module 0 PWM Generator 3.
NMI	128	PD7 (8)	I	TTL	Non-maskable interrupt.
OSC0	88	fixed	I	Analog	Main oscillator crystal input or an external clock reference input.
OSC1	89	fixed	O	Analog	Main oscillator crystal output. Leave unconnected when using a single-ended clock source.
PA0	33	-	I/O	TTL	GPIO port A bit 0.
PA1	34	-	I/O	TTL	GPIO port A bit 1.
PA2	35	-	I/O	TTL	GPIO port A bit 2.
PA3	36	-	I/O	TTL	GPIO port A bit 3.
PA4	37	-	I/O	TTL	GPIO port A bit 4.
PA5	38	-	I/O	TTL	GPIO port A bit 5.
PA6	40	-	I/O	TTL	GPIO port A bit 6.
PA7	41	-	I/O	TTL	GPIO port A bit 7.
PB0	95	-	I/O	TTL	GPIO port B bit 0.
PB1	96	-	I/O	TTL	GPIO port B bit 1.
PB2	91	-	I/O	TTL	GPIO port B bit 2.
PB3	92	-	I/O	TTL	GPIO port B bit 3.
PB4	121	-	I/O	TTL	GPIO port B bit 4.
PB5	120	-	I/O	TTL	GPIO port B bit 5.
PC0	100	-	I/O	TTL	GPIO port C bit 0.
PC1	99	-	I/O	TTL	GPIO port C bit 1.
PC2	98	-	I/O	TTL	GPIO port C bit 2.
PC3	97	-	I/O	TTL	GPIO port C bit 3.
PC4	25	-	I/O	TTL	GPIO port C bit 4.
PC5	24	-	I/O	TTL	GPIO port C bit 5.
PC6	23	-	I/O	TTL	GPIO port C bit 6.
PC7	22	-	I/O	TTL	GPIO port C bit 7.
PD0	1	-	I/O	TTL	GPIO port D bit 0.
PD1	2	-	I/O	TTL	GPIO port D bit 1.
PD2	3	-	I/O	TTL	GPIO port D bit 2.
PD3	4	-	I/O	TTL	GPIO port D bit 3.
PD4	125	-	I/O	TTL	GPIO port D bit 4.
PD5	126	-	I/O	TTL	GPIO port D bit 5.
PD6	127	-	I/O	TTL	GPIO port D bit 6.
PD7	128	-	I/O	TTL	GPIO port D bit 7.
PE0	15	-	I/O	TTL	GPIO port E bit 0.
PE1	14	-	I/O	TTL	GPIO port E bit 1.
PE2	13	-	I/O	TTL	GPIO port E bit 2.

Table 3-3. Signals by Signal Name *(continued)*

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
PE3	12	-	I/O	TTL	GPIO port E bit 3.
PE4	123	-	I/O	TTL	GPIO port E bit 4.
PE5	124	-	I/O	TTL	GPIO port E bit 5.
PF0	42	-	I/O	TTL	GPIO port F bit 0.
PF1	43	-	I/O	TTL	GPIO port F bit 1.
PF2	44	-	I/O	TTL	GPIO port F bit 2.
PF3	45	-	I/O	TTL	GPIO port F bit 3.
PF4	46	-	I/O	TTL	GPIO port F bit 4.
PG0	49	-	I/O	TTL	GPIO port G bit 0.
PG1	50	-	I/O	TTL	GPIO port G bit 1.
PG2	51	-	I/O	TTL	GPIO port G bit 2.
PG3	52	-	I/O	TTL	GPIO port G bit 3.
PG4	53	-	I/O	TTL	GPIO port G bit 4.
PG5	54	-	I/O	TTL	GPIO port G bit 5.
PG6	55	-	I/O	TTL	GPIO port G bit 6.
PG7	56	-	I/O	TTL	GPIO port G bit 7.
PH0	29	-	I/O	TTL	GPIO port H bit 0.
PH1	30	-	I/O	TTL	GPIO port H bit 1.
PH2	31	-	I/O	TTL	GPIO port H bit 2.
PH3	32	-	I/O	TTL	GPIO port H bit 3.
PhA0	82	PL1 (6)	I	TTL	QEI module 0 phase A.
PhB0	83	PL2 (6)	I	TTL	QEI module 0 phase B.
PJ0	116	-	I/O	TTL	GPIO port J bit 0.
PJ1	117	-	I/O	TTL	GPIO port J bit 1.
PK0	18	-	I/O	TTL	GPIO port K bit 0.
PK1	19	-	I/O	TTL	GPIO port K bit 1.
PK2	20	-	I/O	TTL	GPIO port K bit 2.
PK3	21	-	I/O	TTL	GPIO port K bit 3.
PK4	62	-	I/O	TTL	GPIO port K bit 4.
PK5	61	-	I/O	TTL	GPIO port K bit 5.
PK6	60	-	I/O	TTL	GPIO port K bit 6.
PK7	59	-	I/O	TTL	GPIO port K bit 7.
PL0	81	-	I/O	TTL	GPIO port L bit 0.
PL1	82	-	I/O	TTL	GPIO port L bit 1.
PL2	83	-	I/O	TTL	GPIO port L bit 2.
PL3	84	-	I/O	TTL	GPIO port L bit 3.
PL4	85	-	I/O	TTL	GPIO port L bit 4.
PL5	86	-	I/O	TTL	GPIO port L bit 5.
PL6	94	-	I/O	TTL	GPIO port L bit 6.
PL7	93	-	I/O	TTL	GPIO port L bit 7.
PM0	78	-	I/O	TTL	GPIO port M bit 0.

Table 3-3. Signals by Signal Name *(continued)*

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
PM1	77	-	I/O	TTL	GPIO port M bit 1.
PM2	76	-	I/O	TTL	GPIO port M bit 2.
PM3	75	-	I/O	TTL	GPIO port M bit 3.
PM4	74	-	I/O	TTL	GPIO port M bit 4.
PM5	73	-	I/O	TTL	GPIO port M bit 5.
PM6	72	-	I/O	TTL	GPIO port M bit 6.
PM7	71	-	I/O	TTL	GPIO port M bit 7.
PN0	107	-	I/O	TTL	GPIO port N bit 0.
PN1	108	-	I/O	TTL	GPIO port N bit 1.
PN2	109	-	I/O	TTL	GPIO port N bit 2.
PN3	110	-	I/O	TTL	GPIO port N bit 3.
PN4	111	-	I/O	TTL	GPIO port N bit 4.
PN5	112	-	I/O	TTL	GPIO port N bit 5.
PP0	118	-	I/O	TTL	GPIO port P bit 0.
PP1	119	-	I/O	TTL	GPIO port P bit 1.
PP2	103	-	I/O	TTL	GPIO port P bit 2.
PP3	104	-	I/O	TTL	GPIO port P bit 3.
PP4	105	-	I/O	TTL	GPIO port P bit 4.
PP5	106	-	I/O	TTL	GPIO port P bit 5.
PQ0	5	-	I/O	TTL	GPIO port Q bit 0.
PQ1	6	-	I/O	TTL	GPIO port Q bit 1.
PQ2	11	-	I/O	TTL	GPIO port Q bit 2.
PQ3	27	-	I/O	TTL	GPIO port Q bit 3.
PQ4	102	-	I/O	TTL	GPIO port Q bit 4.
PQ5	57	-	I/O	TTL	GPIO port Q bit 5.
PQ6	58	-	I/O	TTL	GPIO port Q bit 6.
RST	70	fixed	I	TTL	System reset input.
RTCCLK	24 59 104	PC5 (7) PK7 (5) PP3 (7)	O	TTL	Buffered version of the Hibernation module's 32.768-kHz clock. This signal is not output when the part is in Hibernate mode and before being configured after power-on reset.
SSI0Clk	35	PA2 (15)	I/O	TTL	SSI module 0 clock
SSI0Fss	36	PA3 (15)	I/O	TTL	SSI module 0 frame signal
SSI0XDAT0	37	PA4 (15)	I/O	TTL	SSI Module 0 Bi-directional Data Pin 0 (SSI0TX in Legacy SSI Mode).
SSI0XDAT1	38	PA5 (15)	I/O	TTL	SSI Module 0 Bi-directional Data Pin 1 (SSI0RX in Legacy SSI Mode).
SSI0XDAT2	40	PA6 (13)	I/O	TTL	SSI Module 0 Bi-directional Data Pin 2.
SSI0XDAT3	41	PA7 (13)	I/O	TTL	SSI Module 0 Bi-directional Data Pin 3.
SSI1Clk	120	PB5 (15)	I/O	TTL	SSI module 1 clock.
SSI1Fss	121	PB4 (15)	I/O	TTL	SSI module 1 frame signal.

Table 3-3. Signals by Signal Name *(continued)*

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
SSI1XDAT0	123	PE4 (15)	I/O	TTL	SSI Module 1 Bi-directional Data Pin 0 (SSI1TX in Legacy SSI Mode).
SSI1XDAT1	124	PE5 (15)	I/O	TTL	SSI Module 1 Bi-directional Data Pin 1 (SSI1RX in Legacy SSI Mode).
SSI1XDAT2	125	PD4 (15)	I/O	TTL	SSI Module 1 Bi-directional Data Pin 2.
SSI1XDAT3	126	PD5 (15)	I/O	TTL	SSI Module 1 Bi-directional Data Pin 3.
SSI2Clk	4 56	PD3 (15) PG7 (15)	I/O	TTL	SSI module 2 clock.
SSI2Fss	3 55	PD2 (15) PG6 (15)	I/O	TTL	SSI module 2 frame signal.
SSI2XDAT0	2 54	PD1 (15) PG5 (15)	I/O	TTL	SSI Module 2 Bi-directional Data Pin 0 (SSI2TX in Legacy SSI Mode).
SSI2XDAT1	1 53	PD0 (15) PG4 (15)	I/O	TTL	SSI Module 2 Bi-directional Data Pin 1 (SSI2RX in Legacy SSI Mode).
SSI2XDAT2	52 128	PG3 (15) PD7 (15)	I/O	TTL	SSI Module 2 Bi-directional Data Pin 2.
SSI2XDAT3	51 127	PG2 (15) PD6 (15)	I/O	TTL	SSI Module 2 Bi-directional Data Pin 3.
SSI3Clk	5 45	PQ0 (14) PF3 (14)	I/O	TTL	SSI module 3 clock.
SSI3Fss	6 44	PQ1 (14) PF2 (14)	I/O	TTL	SSI module 3 frame signal.
SSI3XDAT0	11 43	PQ2 (14) PF1 (14)	I/O	TTL	SSI Module 3 Bi-directional Data Pin 0 (SSI3TX in Legacy SSI Mode).
SSI3XDAT1	27 42	PQ3 (14) PF0 (14)	I/O	TTL	SSI Module 3 Bi-directional Data Pin 1 (SSI3RX in Legacy SSI Mode).
SSI3XDAT2	46 118	PF4 (14) PP0 (15)	I/O	TTL	SSI Module 3 Bi-directional Data Pin 2.
SSI3XDAT3	119	PP1 (15)	I/O	TTL	SSI Module 3 Bi-directional Data Pin 3.
SWCLK	100	PC0 (1)	I	TTL	JTAG/SWD CLK.
SWDIO	99	PC1 (1)	I/O	TTL	JTAG TMS and SWDIO.
SWO	97	PC3 (1)	O	TTL	JTAG TDO and SWO.
T0CCP0	1 33 85	PD0 (3) PA0 (3) PL4 (3)	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 0.
T0CCP1	2 34 86	PD1 (3) PA1 (3) PL5 (3)	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 1.
T1CCP0	3 35 94	PD2 (3) PA2 (3) PL6 (3)	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 0.
T1CCP1	4 36 93	PD3 (3) PA3 (3) PL7 (3)	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 1.
T2CCP0	37 78	PA4 (3) PM0 (3)	I/O	TTL	16/32-Bit Timer 2 Capture/Compare/PWM 0.
T2CCP1	38 77	PA5 (3) PM1 (3)	I/O	TTL	16/32-Bit Timer 2 Capture/Compare/PWM 1.

Table 3-3. Signals by Signal Name *(continued)*

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
T3CCP0	40 76 125	PA6 (3) PM2 (3) PD4 (3)	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 0.
T3CCP1	41 75 126	PA7 (3) PM3 (3) PD5 (3)	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 1.
T4CCP0	74 95 127	PM4 (3) PB0 (3) PD6 (3)	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 0.
T4CCP1	73 96 128	PM5 (3) PB1 (3) PD7 (3)	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 1.
T5CCP0	72 91	PM6 (3) PB2 (3)	I/O	TTL	16/32-Bit Timer 5 Capture/Compare/PWM 0.
T5CCP1	71 92	PM7 (3) PB3 (3)	I/O	TTL	16/32-Bit Timer 5 Capture/Compare/PWM 1.
TCK	100	PC0 (1)	I	TTL	JTAG/SWD CLK.
TDI	98	PC2 (1)	I	TTL	JTAG TDI.
TDO	97	PC3 (1)	O	TTL	JTAG TDO and SWO.
TMPR0	71	PM7	I/O	TTL	Tamper signal 0.
TMPR1	72	PM6	I/O	TTL	Tamper signal 1.
TMPR2	73	PM5	I/O	TTL	Tamper signal 2.
TMPR3	74	PM4	I/O	TTL	Tamper signal 3.
TMS	99	PC1 (1)	I	TTL	JTAG TMS and SWDIO.
TRCLK	45	PF3 (15)	O	TTL	Trace clock.
TRD0	44	PF2 (15)	O	TTL	Trace data 0.
TRD1	43	PF1 (15)	O	TTL	Trace data 1.
TRD2	42	PF0 (15)	O	TTL	Trace data 2.
TRD3	46	PF4 (15)	O	TTL	Trace data 3.
U0CTS	30 53 74 121	PH1 (1) PG4 (1) PM4 (1) PB4 (1)	I	TTL	UART module 0 Clear To Send modem flow control input signal.
U0DCD	31 73 104	PH2 (1) PM5 (1) PP3 (2)	I	TTL	UART module 0 Data Carrier Detect modem status input signal.
U0DSR	32 72 105	PH3 (1) PM6 (1) PP4 (2)	I	TTL	UART module 0 Data Set Ready modem output control line.
U0DTR	103	PP2 (1)	O	TTL	UART module 0 Data Terminal Ready modem status input signal.
U0RI	59 71	PK7 (1) PM7 (1)	I	TTL	UART module 0 Ring Indicator modem status input signal.
U0RTS	29 54 120	PH0 (1) PG5 (1) PB5 (1)	O	TTL	UART module 0 Request to Send modem flow control output signal.
U0Rx	33	PA0 (1)	I	TTL	UART module 0 receive.

Table 3-3. Signals by Signal Name *(continued)*

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
U0Tx	34	PA1 (1)	O	TTL	UART module 0 transmit.
U1CTS	104 108	PP3 (1) PN1 (1)	I	TTL	UART module 1 Clear To Send modem flow control input signal.
U1DCD	13 109	PE2 (1) PN2 (1)	I	TTL	UART module 1 Data Carrier Detect modem status input signal.
U1DSR	14 110	PE1 (1) PN3 (1)	I	TTL	UART module 1 Data Set Ready modem output control line.
U1DTR	12 58 111	PE3 (1) PQ6 (1) PN4 (1)	O	TTL	UART module 1 Data Terminal Ready modem status input signal.
U1RI	112 123	PN5 (1) PE4 (1)	I	TTL	UART module 1 Ring Indicator modem status input signal.
U1RTS	15 107	PE0 (1) PN0 (1)	O	TTL	UART module 1 Request to Send modem flow control output line.
U1Rx	95 102	PB0 (1) PQ4 (1)	I	TTL	UART module 1 receive.
U1Tx	57 96	PQ5 (1) PB1 (1)	O	TTL	UART module 1 transmit.
U2CTS	110 128	PN3 (2) PD7 (1)	I	TTL	UART module 2 Clear To Send modem flow control input signal.
U2RTS	109 127	PN2 (2) PD6 (1)	O	TTL	UART module 2 Request to Send modem flow control output line.
U2Rx	40 125	PA6 (1) PD4 (1)	I	TTL	UART module 2 receive.
U2Tx	41 126	PA7 (1) PD5 (1)	O	TTL	UART module 2 transmit.
U3CTS	106 112	PP5 (1) PN5 (2)	I	TTL	UART module 3 Clear To Send modem flow control input signal.
U3RTS	105 111	PP4 (1) PN4 (2)	O	TTL	UART module 3 Request to Send modem flow control output line.
U3Rx	37 116	PA4 (1) PJ0 (1)	I	TTL	UART module 3 receive.
U3Tx	38 117	PA5 (1) PJ1 (1)	O	TTL	UART module 3 transmit.
U4CTS	21	PK3 (1)	I	TTL	UART module 4 Clear To Send modem flow control input signal.
U4RTS	20	PK2 (1)	O	TTL	UART module 4 Request to Send modem flow control output line.
U4Rx	18 35	PK0 (1) PA2 (1)	I	TTL	UART module 4 receive.
U4Tx	19 36	PK1 (1) PA3 (1)	O	TTL	UART module 4 transmit.
U5Rx	23	PC6 (1)	I	TTL	UART module 5 receive.
U5Tx	22	PC7 (1)	O	TTL	UART module 5 transmit.
U6Rx	118	PP0 (1)	I	TTL	UART module 6 receive.
U6Tx	119	PP1 (1)	O	TTL	UART module 6 transmit.
U7Rx	25	PC4 (1)	I	TTL	UART module 7 receive.

Table 3-3. Signals by Signal Name *(continued)*

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
U7Tx	24	PC5 (1)	O	TTL	UART module 7 transmit.
USB0CLK	92	PB3 (14)	O	TTL	60-MHz clock to the external PHY.
USB0D0	81	PL0 (14)	I/O	TTL	USB data 0.
USB0D1	82	PL1 (14)	I/O	TTL	USB data 1.
USB0D2	83	PL2 (14)	I/O	TTL	USB data 2.
USB0D3	84	PL3 (14)	I/O	TTL	USB data 3.
USB0D4	85	PL4 (14)	I/O	TTL	USB data 4.
USB0D5	86	PL5 (14)	I/O	TTL	USB data 5.
USB0D6	106	PP5 (14)	I/O	TTL	USB data 6.
USB0D7	105	PP4 (14)	I/O	TTL	USB data 7.
USB0DIR	104	PP3 (14)	O	TTL	Indicates that the external PHY is able to accept data from the USB controller.
USB0DM	93	PL7	I/O	Analog	Bidirectional differential data pin (D- per USB specification) for USB0.
USB0DP	94	PL6	I/O	Analog	Bidirectional differential data pin (D+ per USB specification) for USB0.
USB0EPEN	40 41 127	PA6 (5) PA7 (11) PD6 (5)	O	TTL	Optionally used in Host mode to control an external power source to supply power to the USB bus.
USB0ID	95	PB0	I	Analog	This signal senses the state of the USB ID signal. The USB PHY enables an integrated pull-up, and an external element (USB connector) indicates the initial state of the USB controller (pulled down is the A side of the cable and pulled up is the B side).
USB0NXT	103	PP2 (14)	O	TTL	Asserted by the external PHY to throttle all data types.
USB0PFLT	41 128	PA7 (5) PD7 (5)	I	TTL	Optionally used in Host mode by an external power source to indicate an error state by that power source.
USB0STP	91	PB2 (14)	O	TTL	Asserted by the USB controller to signal the end of a USB transmit packet or register write operation.
USB0VBUS	96	PB1	I/O	Analog	This signal is used during the session request protocol. This signal allows the USB PHY to both sense the voltage level of VBUS, and pull up VBUS momentarily during VBUS pulsing.
VBAT	68	fixed	-	Power	Power source for the Hibernation module. It is normally connected to the positive terminal of a battery and serves as the battery backup/Hibernation module power-source supply.

Table 3-3. Signals by Signal Name *(continued)*

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
VDD	7 16 26 28 39 47 63 69 79 90 101 113 122	fixed	-	Power	Positive supply for I/O and some logic.
VDDA	8	fixed	-	Power	The positive supply for the analog circuits (ADC, Analog Comparators, etc.). These are separated from VDD to minimize the electrical noise contained on VDD from affecting the analog functions. VDDA pins must be supplied with a voltage that meets the specification in , regardless of system implementation.
VDDC	87 115	fixed	-	Power	Positive supply for most of the logic function, including the processor core and most peripherals. The voltage on this pin is 1.2 V and is supplied by the on-chip LDO. The VDDC pins should only be connected to each other and an external capacitor as specified in the data sheet.
VREFA+	9	fixed	-	Analog	A reference voltage used to specify the voltage at which the ADC converts to a maximum value. This pin is used in conjunction with GNDA. The voltage that is applied to VREFA+ is the voltage with which an AINn signal is converted to 4095. The VREFA+ voltage is limited to the range specified in the data sheet .
$\overline{\text{WAKE}}$	64	fixed	I	TTL	An external input that brings the processor out of Hibernate mode when asserted.
XOSC0	66	fixed	I	Analog	Hibernation module oscillator crystal input or an external clock reference input. Note that this is either a crystal or a 32.768-kHz oscillator for the Hibernation module RTC.
XOSC1	67	fixed	O	Analog	Hibernation module oscillator crystal output. Leave unconnected when using a single-ended clock source.

3.3 Signals by Function, Except for GPIO

Table 3-4. Signals by Function, Except for GPIO

Function	Pin Name	Pin Number	Pin Type	Buffer Type	Description
ADC	AIN0	12	I	Analog	Analog-to-digital converter input 0.
	AIN1	13	I	Analog	Analog-to-digital converter input 1.
	AIN2	14	I	Analog	Analog-to-digital converter input 2.
	AIN3	15	I	Analog	Analog-to-digital converter input 3.
	AIN4	128	I	Analog	Analog-to-digital converter input 4.
	AIN5	127	I	Analog	Analog-to-digital converter input 5.
	AIN6	126	I	Analog	Analog-to-digital converter input 6.
	AIN7	125	I	Analog	Analog-to-digital converter input 7.
	AIN8	124	I	Analog	Analog-to-digital converter input 8.
	AIN9	123	I	Analog	Analog-to-digital converter input 9.
	AIN10	121	I	Analog	Analog-to-digital converter input 10.
	AIN11	120	I	Analog	Analog-to-digital converter input 11.
	AIN12	4	I	Analog	Analog-to-digital converter input 12.
	AIN13	3	I	Analog	Analog-to-digital converter input 13.
	AIN14	2	I	Analog	Analog-to-digital converter input 14.
	AIN15	1	I	Analog	Analog-to-digital converter input 15.
	AIN16	18	I	Analog	Analog-to-digital converter input 16.
	AIN17	19	I	Analog	Analog-to-digital converter input 17.
	AIN18	20	I	Analog	Analog-to-digital converter input 18.
	AIN19	21	I	Analog	Analog-to-digital converter input 19.
	VREFA+	9	-	Analog	A reference voltage used to specify the voltage at which the ADC converts to a maximum value. This pin is used in conjunction with GNDA. The voltage that is applied to VREFA+ is the voltage with which an AINn signal is converted to 4095. The VREFA+ voltage is limited to the range specified in the data sheet .
Analog Comparators	C0+	23	I	Analog	Analog comparator 0 positive input.
	C0-	22	I	Analog	Analog comparator 0 negative input.
	C0o	1 83	O	TTL	Analog comparator 0 output.
	C1+	24	I	Analog	Analog comparator 1 positive input.
	C1-	25	I	Analog	Analog comparator 1 negative input.
	C1o	2 84	O	TTL	Analog comparator 1 output.
	C2+	118	I	Analog	Analog comparator 2 positive input.
	C2-	119	I	Analog	Analog comparator 2 negative input.
	C2o	3	O	TTL	Analog comparator 2 output.
Controller Area Network	CAN0Rx	33	I	TTL	CAN module 0 receive.
	CAN0Tx	34	O	TTL	CAN module 0 transmit.
	CAN1Rx	95	I	TTL	CAN module 1 receive.
	CAN1Tx	96	O	TTL	CAN module 1 transmit.

Table 3-4. Signals by Function, Except for GPIO *(continued)*

Function	Pin Name	Pin Number	Pin Type	Buffer Type	Description
Core	TRCLK	45	O	TTL	Trace clock.
	TRD0	44	O	TTL	Trace data 0.
	TRD1	43	O	TTL	Trace data 1.
	TRD2	42	O	TTL	Trace data 2.
	TRD3	46	O	TTL	Trace data 3.
Ethernet	EN0COL	71	I	TTL	Ethernet 0 Collision Detect.
	EN0CRS	72	I	TTL	Ethernet 0 Carrier Sense.
	EN0INTRN	62 118	I	TTL	Ethernet 0 Interrupt from the Ethernet PHY.
	EN0MDC	44 91	O	TTL	Ethernet 0 Management Data Clock.
	EN0MDIO	45 92	I/O	TTL	Ethernet 0 Management Data Input/Output signal.
	EN0RREF_CLK	74	I/O	TTL	Ethernet 0 Reference Clock.
	EN0RXCK	40	I	TTL	Ethernet 0 Receive Clock.
	EN0RXD0	57	I	TTL	Ethernet 0 Receive Data 0.
	EN0RXD1	58	I	TTL	Ethernet 0 Receive Data 1.
	EN0RXD2	61	I	TTL	Ethernet 0 Receive Data 2.
	EN0RXD3	62	I	TTL	Ethernet 0 Receive Data 3.
	EN0RXDV	56	I	TTL	Ethernet 0 Receive Data Valid.
	EN0RXER	55	I	TTL	Ethernet 0 Receive Error.
	EN0TXCK	51	I	TTL	Ethernet 0 Transmit Clock.
	EN0TXD0	53	O	TTL	Ethernet 0 Transmit Data 0.
	EN0TXD1	54	O	TTL	Ethernet 0 Transmit Data 1.
	EN0TXD2	60	O	TTL	Ethernet 0 Transmit Data 2.
	EN0TXD3	59	O	TTL	Ethernet 0 Transmit Data 3.
	EN0TXEN	52	O	TTL	Ethernet 0 Transmit Enable.

Table 3-4. Signals by Function, Except for GPIO *(continued)*

Function	Pin Name	Pin Number	Pin Type	Buffer Type	Description
External Peripheral Interface	EPI0S0	18 29	I/O	TTL	EPI module 0 signal 0.
	EPI0S1	19 30	I/O	TTL	EPI module 0 signal 1.
	EPI0S2	20 31	I/O	TTL	EPI module 0 signal 2.
	EPI0S3	21 32	I/O	TTL	EPI module 0 signal 3.
	EPI0S4	22	I/O	TTL	EPI module 0 signal 4.
	EPI0S5	23	I/O	TTL	EPI module 0 signal 5.
	EPI0S6	24	I/O	TTL	EPI module 0 signal 6.
	EPI0S7	25	I/O	TTL	EPI module 0 signal 7.
	EPI0S8	40	I/O	TTL	EPI module 0 signal 8.
	EPI0S9	41	I/O	TTL	EPI module 0 signal 9.
	EPI0S10	50	I/O	TTL	EPI module 0 signal 10.
	EPI0S11	49	I/O	TTL	EPI module 0 signal 11.
	EPI0S12	75	I/O	TTL	EPI module 0 signal 12.
	EPI0S13	76	I/O	TTL	EPI module 0 signal 13.
	EPI0S14	77	I/O	TTL	EPI module 0 signal 14.
	EPI0S15	78	I/O	TTL	EPI module 0 signal 15.
	EPI0S16	81	I/O	TTL	EPI module 0 signal 16.
	EPI0S17	82	I/O	TTL	EPI module 0 signal 17.
	EPI0S18	83	I/O	TTL	EPI module 0 signal 18.
	EPI0S19	84	I/O	TTL	EPI module 0 signal 19.
	EPI0S20	5	I/O	TTL	EPI module 0 signal 20.
	EPI0S21	6	I/O	TTL	EPI module 0 signal 21.
	EPI0S22	11	I/O	TTL	EPI module 0 signal 22.
	EPI0S23	27	I/O	TTL	EPI module 0 signal 23.
	EPI0S24	59	I/O	TTL	EPI module 0 signal 24.
	EPI0S25	60	I/O	TTL	EPI module 0 signal 25.
	EPI0S26	85	I/O	TTL	EPI module 0 signal 26.
	EPI0S27	91	I/O	TTL	EPI module 0 signal 27.
	EPI0S28	92	I/O	TTL	EPI module 0 signal 28.
	EPI0S29	103 109	I/O	TTL	EPI module 0 signal 29.
	EPI0S30	104 110	I/O	TTL	EPI module 0 signal 30.
	EPI0S31	61	I/O	TTL	EPI module 0 signal 31.
	EPI0S32	62	I/O	TTL	EPI module 0 signal 32.
	EPI0S33	86	I/O	TTL	EPI module 0 signal 33.
	EPI0S34	111	I/O	TTL	EPI module 0 signal 34.
	EPI0S35	112	I/O	TTL	EPI module 0 signal 35.

Table 3-4. Signals by Function, Except for GPIO *(continued)*

Function	Pin Name	Pin Number	Pin Type	Buffer Type	Description
General-Purpose Timers	T0CCP0	1 33 85	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 0.
	T0CCP1	2 34 86	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 1.
	T1CCP0	3 35 94	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 0.
	T1CCP1	4 36 93	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 1.
	T2CCP0	37 78	I/O	TTL	16/32-Bit Timer 2 Capture/Compare/PWM 0.
	T2CCP1	38 77	I/O	TTL	16/32-Bit Timer 2 Capture/Compare/PWM 1.
	T3CCP0	40 76 125	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 0.
	T3CCP1	41 75 126	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 1.
	T4CCP0	74 95 127	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 0.
	T4CCP1	73 96 128	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 1.
	T5CCP0	72 91	I/O	TTL	16/32-Bit Timer 5 Capture/Compare/PWM 0.
	T5CCP1	71 92	I/O	TTL	16/32-Bit Timer 5 Capture/Compare/PWM 1.

Table 3-4. Signals by Function, Except for GPIO *(continued)*

Function	Pin Name	Pin Number	Pin Type	Buffer Type	Description
Hibernate	HIB	65	O	TTL	An output that indicates the processor is in Hibernate mode.
	RTCCLK	24 59 104	O	TTL	Buffered version of the Hibernation module's 32.768-kHz clock. This signal is not output when the part is in Hibernate mode and before being configured after power-on reset.
	TMPR0	71	I/O	TTL	Tamper signal 0.
	TMPR1	72	I/O	TTL	Tamper signal 1.
	TMPR2	73	I/O	TTL	Tamper signal 2.
	TMPR3	74	I/O	TTL	Tamper signal 3.
	VBAT	68	-	Power	Power source for the Hibernation module. It is normally connected to the positive terminal of a battery and serves as the battery backup/Hibernation module power-source supply.
	WAKE	64	I	TTL	An external input that brings the processor out of Hibernate mode when asserted.
	XOSC0	66	I	Analog	Hibernation module oscillator crystal input or an external clock reference input. Note that this is either a crystal or a 32.768-kHz oscillator for the Hibernation module RTC.
	XOSC1	67	O	Analog	Hibernation module oscillator crystal output. Leave unconnected when using a single-ended clock source.

Table 3-4. Signals by Function, Except for GPIO *(continued)*

Function	Pin Name	Pin Number	Pin Type	Buffer Type	Description
I2C	I2C0SCL	91	I/O	OD	I^2C module 0 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	I2C0SDA	92	I/O	OD	I^2C module 0 data.
	I2C1SCL	49	I/O	OD	I^2C module 1 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	I2C1SDA	50	I/O	OD	I^2C module 1 data.
	I2C2SCL	51 82 106 112	I/O	OD	I^2C module 2 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	I2C2SDA	52 81 111	I/O	OD	I^2C module 2 data.
	I2C3SCL	53 62	I/O	OD	I^2C module 3 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	I2C3SDA	54 61	I/O	OD	I^2C module 3 data.
	I2C4SCL	55 60	I/O	OD	I^2C module 4 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	I2C4SDA	56 59	I/O	OD	I^2C module 4 data.
	I2C5SCL	95 121	I/O	OD	I^2C module 5 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	I2C5SDA	96 120	I/O	OD	I^2C module 5 data.
	I2C6SCL	40	I/O	OD	I^2C module 6 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	I2C6SDA	41	I/O	OD	I^2C module 6 data.
	I2C7SCL	1 37	I/O	OD	I^2C module 7 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	I2C7SDA	2 38	I/O	OD	I^2C module 7 data.
	I2C8SCL	3 35	I/O	OD	I^2C module 8 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	I2C8SDA	4 36	I/O	OD	I^2C module 8 data.
	I2C9SCL	33	I/O	OD	I^2C module 9 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	I2C9SDA	34	I/O	OD	I^2C module 9 data.

Table 3-4. Signals by Function, Except for GPIO *(continued)*

Function	Pin Name	Pin Number	Pin Type	Buffer Type	Description
JTAG/SWD/SWO	SWCLK	100	I	TTL	JTAG/SWD CLK.
	SWDIO	99	I/O	TTL	JTAG TMS and SWDIO.
	SWO	97	O	TTL	JTAG TDO and SWO.
	TCK	100	I	TTL	JTAG/SWD CLK.
	TDI	98	I	TTL	JTAG TDI.
	TDO	97	O	TTL	JTAG TDO and SWO.
	TMS	99	I	TTL	JTAG TMS and SWDIO.
PWM	M0FAULT0	46	I	TTL	Motion Control Module 0 PWM Fault 0.
	M0FAULT1	60	I	TTL	Motion Control Module 0 PWM Fault 1.
	M0FAULT2	59	I	TTL	Motion Control Module 0 PWM Fault 2.
	M0FAULT3	81	I	TTL	Motion Control Module 0 PWM Fault 3.
	M0PWM0	42	O	TTL	Motion Control Module 0 PWM 0. This signal is controlled by Module 0 PWM Generator 0.
	M0PWM1	43	O	TTL	Motion Control Module 0 PWM 1. This signal is controlled by Module 0 PWM Generator 0.
	M0PWM2	44	O	TTL	Motion Control Module 0 PWM 2. This signal is controlled by Module 0 PWM Generator 1.
	M0PWM3	45	O	TTL	Motion Control Module 0 PWM 3. This signal is controlled by Module 0 PWM Generator 1.
	M0PWM4	49	O	TTL	Motion Control Module 0 PWM 4. This signal is controlled by Module 0 PWM Generator 2.
	M0PWM5	50	O	TTL	Motion Control Module 0 PWM 5. This signal is controlled by Module 0 PWM Generator 2.
	M0PWM6	62	O	TTL	Motion Control Module 0 PWM 6. This signal is controlled by Module 0 PWM Generator 3.
	M0PWM7	61	O	TTL	Motion Control Module 0 PWM 7. This signal is controlled by Module 0 PWM Generator 3.

Table 3-4. Signals by Function, Except for GPIO *(continued)*

Function	Pin Name	Pin Number	Pin Type	Buffer Type	Description
Power	GND	17 48 80 114	-	Power	Ground reference for logic and I/O pins.
	GNDA	10	-	Power	The ground reference for the analog circuits (ADC, Analog Comparators, etc.). These are separated from GND to minimize the electrical noise contained on VDD from affecting the analog functions.
	VDD	7 16 26 28 39 47 63 69 79 90 101 113 122	-	Power	Positive supply for I/O and some logic.
	VDDA	8	-	Power	The positive supply for the analog circuits (ADC, Analog Comparators, etc.). These are separated from VDD to minimize the electrical noise contained on VDD from affecting the analog functions. VDDA pins must be supplied with a voltage that meets the specification in , regardless of system implementation.
	VDDC	87 115	-	Power	Positive supply for most of the logic function, including the processor core and most peripherals. The voltage on this pin is 1.2 V and is supplied by the on-chip LDO. The VDDC pins should only be connected to each other and an external capacitor as specified in the data sheet.
QEI	IDX0	84	I	TTL	QEI module 0 index.
	PhA0	82	I	TTL	QEI module 0 phase A.
	PhB0	83	I	TTL	QEI module 0 phase B.

Table 3-4. Signals by Function, Except for GPIO *(continued)*

Function	Pin Name	Pin Number	Pin Type	Buffer Type	Description
SSI	SSI0Clk	35	I/O	TTL	SSI module 0 clock
	SSI0Fss	36	I/O	TTL	SSI module 0 frame signal
	SSI0XDAT0	37	I/O	TTL	SSI Module 0 Bi-directional Data Pin 0 (SSI0TX in Legacy SSI Mode).
	SSI0XDAT1	38	I/O	TTL	SSI Module 0 Bi-directional Data Pin 1 (SSI0RX in Legacy SSI Mode).
	SSI0XDAT2	40	I/O	TTL	SSI Module 0 Bi-directional Data Pin 2.
	SSI0XDAT3	41	I/O	TTL	SSI Module 0 Bi-directional Data Pin 3.
	SSI1Clk	120	I/O	TTL	SSI module 1 clock.
	SSI1Fss	121	I/O	TTL	SSI module 1 frame signal.
	SSI1XDAT0	123	I/O	TTL	SSI Module 1 Bi-directional Data Pin 0 (SSI1TX in Legacy SSI Mode).
	SSI1XDAT1	124	I/O	TTL	SSI Module 1 Bi-directional Data Pin 1 (SSI1RX in Legacy SSI Mode).
	SSI1XDAT2	125	I/O	TTL	SSI Module 1 Bi-directional Data Pin 2.
	SSI1XDAT3	126	I/O	TTL	SSI Module 1 Bi-directional Data Pin 3.
	SSI2Clk	4 56	I/O	TTL	SSI module 2 clock.
	SSI2Fss	3 55	I/O	TTL	SSI module 2 frame signal.
	SSI2XDAT0	2 54	I/O	TTL	SSI Module 2 Bi-directional Data Pin 0 (SSI2TX in Legacy SSI Mode).
	SSI2XDAT1	1 53	I/O	TTL	SSI Module 2 Bi-directional Data Pin 1 (SSI2RX in Legacy SSI Mode).
	SSI2XDAT2	52 128	I/O	TTL	SSI Module 2 Bi-directional Data Pin 2.
	SSI2XDAT3	51 127	I/O	TTL	SSI Module 2 Bi-directional Data Pin 3.
	SSI3Clk	5 45	I/O	TTL	SSI module 3 clock.
	SSI3Fss	6 44	I/O	TTL	SSI module 3 frame signal.
	SSI3XDAT0	11 43	I/O	TTL	SSI Module 3 Bi-directional Data Pin 0 (SSI3TX in Legacy SSI Mode).
	SSI3XDAT1	27 42	I/O	TTL	SSI Module 3 Bi-directional Data Pin 1 (SSI3RX in Legacy SSI Mode).
	SSI3XDAT2	46 118	I/O	TTL	SSI Module 3 Bi-directional Data Pin 2.
	SSI3XDAT3	119	I/O	TTL	SSI Module 3 Bi-directional Data Pin 3.
System Control & Clocks	DIVSCLK	102	O	TTL	An optionally divided reference clock output based on a selected clock source.
	NMI	128	I	TTL	Non-maskable interrupt.
	OSC0	88	I	Analog	Main oscillator crystal input or an external clock reference input.
	OSC1	89	O	Analog	Main oscillator crystal output. Leave unconnected when using a single-ended clock source.
	$\overline{\text{RST}}$	70	I	TTL	System reset input.

Table 3-4. Signals by Function, Except for GPIO *(continued)*

Function	Pin Name	Pin Number	Pin Type	Buffer Type	Description
UART	U0CTS	30 53 74 121	I	TTL	UART module 0 Clear To Send modem flow control input signal.
	U0DCD	31 73 104	I	TTL	UART module 0 Data Carrier Detect modem status input signal.
	U0DSR	32 72 105	I	TTL	UART module 0 Data Set Ready modem output control line.
	U0DTR	103	O	TTL	UART module 0 Data Terminal Ready modem status input signal.
	U0RI	59 71	I	TTL	UART module 0 Ring Indicator modem status input signal.
	U0RTS	29 54 120	O	TTL	UART module 0 Request to Send modem flow control output signal.
	U0Rx	33	I	TTL	UART module 0 receive.
	U0Tx	34	O	TTL	UART module 0 transmit.
	U1CTS	104 108	I	TTL	UART module 1 Clear To Send modem flow control input signal.
	U1DCD	13 109	I	TTL	UART module 1 Data Carrier Detect modem status input signal.
	U1DSR	14 110	I	TTL	UART module 1 Data Set Ready modem output control line.
	U1DTR	12 58 111	O	TTL	UART module 1 Data Terminal Ready modem status input signal.
	U1RI	112 123	I	TTL	UART module 1 Ring Indicator modem status input signal.
	U1RTS	15 107	O	TTL	UART module 1 Request to Send modem flow control output line.
	U1Rx	95 102	I	TTL	UART module 1 receive.
	U1Tx	57 96	O	TTL	UART module 1 transmit.
	U2CTS	110 128	I	TTL	UART module 2 Clear To Send modem flow control input signal.
	U2RTS	109 127	O	TTL	UART module 2 Request to Send modem flow control output line.
	U2Rx	40 125	I	TTL	UART module 2 receive.
	U2Tx	41 126	O	TTL	UART module 2 transmit.
	U3CTS	106 112	I	TTL	UART module 3 Clear To Send modem flow control input signal.
	U3RTS	105 111	O	TTL	UART module 3 Request to Send modem flow control output line.
	U3Rx	37 116	I	TTL	UART module 3 receive.

Table 3-4. Signals by Function, Except for GPIO *(continued)*

Function	Pin Name	Pin Number	Pin Type	Buffer Type	Description
	U3Tx	38 117	O	TTL	UART module 3 transmit.
	U4CTS	21	I	TTL	UART module 4 Clear To Send modem flow control input signal.
	U4RTS	20	O	TTL	UART module 4 Request to Send modem flow control output line.
	U4Rx	18 35	I	TTL	UART module 4 receive.
	U4Tx	19 36	O	TTL	UART module 4 transmit.
	U5Rx	23	I	TTL	UART module 5 receive.
	U5Tx	22	O	TTL	UART module 5 transmit.
	U6Rx	118	I	TTL	UART module 6 receive.
	U6Tx	119	O	TTL	UART module 6 transmit.
	U7Rx	25	I	TTL	UART module 7 receive.
	U7Tx	24	O	TTL	UART module 7 transmit.

Table 3-4. Signals by Function, Except for GPIO *(continued)*

Function	Pin Name	Pin Number	Pin Type	Buffer Type	Description
USB	USB0CLK	92	O	TTL	60-MHz clock to the external PHY.
	USB0D0	81	I/O	TTL	USB data 0.
	USB0D1	82	I/O	TTL	USB data 1.
	USB0D2	83	I/O	TTL	USB data 2.
	USB0D3	84	I/O	TTL	USB data 3.
	USB0D4	85	I/O	TTL	USB data 4.
	USB0D5	86	I/O	TTL	USB data 5.
	USB0D6	106	I/O	TTL	USB data 6.
	USB0D7	105	I/O	TTL	USB data 7.
	USB0DIR	104	O	TTL	Indicates that the external PHY is able to accept data from the USB controller.
	USB0DM	93	I/O	Analog	Bidirectional differential data pin (D- per USB specification) for USB0.
	USB0DP	94	I/O	Analog	Bidirectional differential data pin (D+ per USB specification) for USB0.
	USB0EPEN	40 41 127	O	TTL	Optionally used in Host mode to control an external power source to supply power to the USB bus.
	USB0ID	95	I	Analog	This signal senses the state of the USB ID signal. The USB PHY enables an integrated pull-up, and an external element (USB connector) indicates the initial state of the USB controller (pulled down is the A side of the cable and pulled up is the B side).
	USB0NXT	103	O	TTL	Asserted by the external PHY to throttle all data types.
	USB0PFLT	41 128	I	TTL	Optionally used in Host mode by an external power source to indicate an error state by that power source.
	USB0STP	91	O	TTL	Asserted by the USB controller to signal the end of a USB transmit packet or register write operation.
	USB0VBUS	96	I/O	Analog	This signal is used during the session request protocol. This signal allows the USB PHY to both sense the voltage level of VBUS, and pull up VBUS momentarily during VBUS pulsing.

3.4 GPIO Pins and Alternate Functions

Table 3-5. GPIO Pins and Alternate Functions

IO	Pin	Analog or Special Function[a]	Digital Function (GPIOPCTL PMCx Bit Field Encoding)[b]											
			1	2	3	4	5	6	7	8	11	13	14	15
PA0	33	-	U0Rx	I2C9SCL	T0CCP0	-	-	-	CAN0Rx	-	-	-	-	-
PA1	34	-	U0Tx	I2C9SDA	T0CCP1	-	-	-	CAN0Tx	-	-	-	-	-
PA2	35	-	U4Rx	I2C8SCL	T1CCP0	-	-	-	-	-	-	-	-	SSI0Clk
PA3	36	-	U4Tx	I2C8SDA	T1CCP1	-	-	-	-	-	-	-	-	SSI0Fss
PA4	37	-	U3Rx	I2C7SCL	T2CCP0	-	-	-	-	-	-	-	-	SSI0XDAT0

Table 3-5. GPIO Pins and Alternate Functions *(continued)*

IO	Pin	Analog or Special Function[a]	Digital Function (GPIOPCTL PMCx Bit Field Encoding)[b]											
			1	2	3	4	5	6	7	8	11	13	14	15
PA5	38	-	U3Tx	I2C7SDA	T2CCP1	-	-	-	-	-	-	-	-	SSI0XDAT1
PA6	40	-	U2Rx	I2C6SCL	T3CCP0	-	USB0EPEN	-	-	-	-	SSI0XDAT2	EN0RXCK	EPI0S8
PA7	41	-	U2Tx	I2C6SDA	T3CCP1	-	USB0PFLT	-	-	-	USB0EPEN	SSI0XDAT3	-	EPI0S9
PB0	95	USB0ID	U1Rx	I2C5SCL	T4CCP0	-	-	-	CAN1Rx	-	-	-	-	-
PB1	96	USB0VBUS	U1Tx	I2C5SDA	T4CCP1	-	-	-	CAN1Tx	-	-	-	-	-
PB2	91	-	-	I2C0SCL	T5CCP0	-	EN0MDC	-	-	-	-	-	USB0STP	EPI0S27
PB3	92	-	-	I2C0SDA	T5CCP1	-	EN0MDIO	-	-	-	-	-	USB0CLK	EPI0S28
PB4	121	AIN10	U0CTS	I2C5SCL	-	-	-	-	-	-	-	-	-	SSI1Fss
PB5	120	AIN11	U0RTS	I2C5SDA	-	-	-	-	-	-	-	-	-	SSI1Clk
PC0	100	-	TCK SWCLK	-	-	-	-	-	-	-	-	-	-	-
PC1	99	-	TMS SWDIO	-	-	-	-	-	-	-	-	-	-	-
PC2	98	-	TDI	-	-	-	-	-	-	-	-	-	-	-
PC3	97	-	TDO SWO	-	-	-	-	-	-	-	-	-	-	-
PC4	25	C1-	U7Rx	-	-	-	-	-	-	-	-	-	-	EPI0S7
PC5	24	C1+	U7Tx	-	-	-	-	-	RTCCLK	-	-	-	-	EPI0S6
PC6	23	C0+	U5Rx	-	-	-	-	-	-	-	-	-	-	EPI0S5
PC7	22	C0-	U5Tx	-	-	-	-	-	-	-	-	-	-	EPI0S4
PD0	1	AIN15	-	I2C7SCL	T0CCP0	-	C0o	-	-	-	-	-	-	SSI2XDAT1
PD1	2	AIN14	-	I2C7SDA	T0CCP1	-	C1o	-	-	-	-	-	-	SSI2XDAT0
PD2	3	AIN13	-	I2C8SCL	T1CCP0	-	C2o	-	-	-	-	-	-	SSI2Fss
PD3	4	AIN12	-	I2C8SDA	T1CCP1	-	-	-	-	-	-	-	-	SSI2Clk
PD4	125	AIN7	U2Rx	-	T3CCP0	-	-	-	-	-	-	-	-	SSI1XDAT2
PD5	126	AIN6	U2Tx	-	T3CCP1	-	-	-	-	-	-	-	-	SSI1XDAT3
PD6	127	AIN5	U2RTS	-	T4CCP0	-	USB0EPEN	-	-	-	-	-	-	SSI2XDAT3
PD7	128	AIN4	U2CTS	-	T4CCP1	-	USB0PFLT	-	-	NMI	-	-	-	SSI2XDAT2
PE0	15	AIN3	U1RTS	-	-	-	-	-	-	-	-	-	-	-
PE1	14	AIN2	U1DSR	-	-	-	-	-	-	-	-	-	-	-
PE2	13	AIN1	U1DCD	-	-	-	-	-	-	-	-	-	-	-
PE3	12	AIN0	U1DTR	-	-	-	-	-	-	-	-	-	-	-
PE4	123	AIN9	U1RI	-	-	-	-	-	-	-	-	-	-	SSI1XDAT0
PE5	124	AIN8	-	-	-	-	-	-	-	-	-	-	-	SSI1XDAT1
PF0	42	-	-	-	-	-	-	M0PWM0	-	-	-	-	SSI3XDAT1	TRD2
PF1	43	-	-	-	-	-	-	M0PWM1	-	-	-	-	SSI3XDAT0	TRD1
PF2	44	-	-	-	-	-	EN0MDC	M0PWM2	-	-	-	-	SSI3Fss	TRD0
PF3	45	-	-	-	-	-	EN0MDIO	M0PWM3	-	-	-	-	SSI3Clk	TRCLK
PF4	46	-	-	-	-	-	-	M0FAULT0	-	-	-	-	SSI3XDAT2	TRD3
PG0	49	-	-	I2C1SCL	-	-	-	M0PWM4	-	-	-	-	-	EPI0S11

Table 3-5. GPIO Pins and Alternate Functions *(continued)*

IO	Pin	Analog or Special Function[a]	Digital Function (GPIOPCTL PMCx Bit Field Encoding)[b]											
			1	2	3	4	5	6	7	8	11	13	14	15
PG1	50	-	-	I2C1SDA	-	-	-	M0PWM5	-	-	-	-	-	EPI0S10
PG2	51	-	-	I2C2SCL	-	-	-	-	-	-	-	-	EN0TXCK	SSI2XDAT3
PG3	52	-	-	I2C2SDA	-	-	-	-	-	-	-	-	EN0TXEN	SSI2XDAT2
PG4	53	-	U0CTS	I2C3SCL	-	-	-	-	-	-	-	-	EN0TXD0	SSI2XDAT1
PG5	54	-	U0RTS	I2C3SDA	-	-	-	-	-	-	-	-	EN0TXD1	SSI2XDAT0
PG6	55	-	-	I2C4SCL	-	-	-	-	-	-	-	-	EN0RXER	SSI2Fss
PG7	56	-	-	I2C4SDA	-	-	-	-	-	-	-	-	EN0RXDV	SSI2Clk
PH0	29	-	U0RTS	-	-	-	-	-	-	-	-	-	-	EPI0S0
PH1	30	-	U0CTS	-	-	-	-	-	-	-	-	-	-	EPI0S1
PH2	31	-	U0DCD	-	-	-	-	-	-	-	-	-	-	EPI0S2
PH3	32	-	U0DSR	-	-	-	-	-	-	-	-	-	-	EPI0S3
PJ0	116	-	U3Rx	-	-	-	-	-	-	-	-	-	-	-
PJ1	117	-	U3Tx	-	-	-	-	-	-	-	-	-	-	-
PK0	18	AIN16	U4Rx	-	-	-	-	-	-	-	-	-	-	EPI0S0
PK1	19	AIN17	U4Tx	-	-	-	-	-	-	-	-	-	-	EPI0S1
PK2	20	AIN18	U4RTS	-	-	-	-	-	-	-	-	-	-	EPI0S2
PK3	21	AIN19	U4CTS	-	-	-	-	-	-	-	-	-	-	EPI0S3
PK4	62	-	-	I2C3SCL	-	-	-	M0PWM6	EN0INTRN	-	-	-	EN0RXD3	EPI0S32
PK5	61	-	-	I2C3SDA	-	-	-	M0PWM7	-	-	-	-	EN0RXD2	EPI0S31
PK6	60	-	-	I2C4SCL	-	-	-	M0FAULT1	-	-	-	-	EN0TXD2	EPI0S25
PK7	59	-	U0RI	I2C4SDA	-	-	RTCCLK	M0FAULT2	-	-	-	-	EN0TXD3	EPI0S24
PL0	81	-	-	I2C2SDA	-	-	-	M0FAULT3	-	-	-	-	USB0D0	EPI0S16
PL1	82	-	-	I2C2SCL	-	-	-	PhA0	-	-	-	-	USB0D1	EPI0S17
PL2	83	-	-	-	-	-	C0o	PhB0	-	-	-	-	USB0D2	EPI0S18
PL3	84	-	-	-	-	-	C1o	IDX0	-	-	-	-	USB0D3	EPI0S19
PL4	85	-	-	-	T0CCP0	-	-	-	-	-	-	-	USB0D4	EPI0S26
PL5	86	-	-	-	T0CCP1	-	-	-	-	-	-	-	USB0D5	EPI0S33
PL6	94	USB0DP	-	-	T1CCP0	-	-	-	-	-	-	-	-	-
PL7	93	USB0DM	-	-	T1CCP1	-	-	-	-	-	-	-	-	-
PM0	78	-	-	-	T2CCP0	-	-	-	-	-	-	-	-	EPI0S15
PM1	77	-	-	-	T2CCP1	-	-	-	-	-	-	-	-	EPI0S14
PM2	76	-	-	-	T3CCP0	-	-	-	-	-	-	-	-	EPI0S13
PM3	75	-	-	-	T3CCP1	-	-	-	-	-	-	-	-	EPI0S12
PM4	74	TMPR3	U0CTS	-	T4CCP0	-	-	-	-	-	-	-	EN0RREF_CLK	-
PM5	73	TMPR2	U0DCD	-	T4CCP1	-	-	-	-	-	-	-	-	-
PM6	72	TMPR1	U0DSR	-	T5CCP0	-	-	-	-	-	-	-	EN0CRS	-
PM7	71	TMPR0	U0RI	-	T5CCP1	-	-	-	-	-	-	-	EN0COL	-
PN0	107	-	U1RTS	-	-	-	-	-	-	-	-	-	-	-
PN1	108	-	U1CTS	-	-	-	-	-	-	-	-	-	-	-

Table 3-5. GPIO Pins and Alternate Functions *(continued)*

IO	Pin	Analog or Special Function[a]	Digital Function (GPIOPCTL PMCx Bit Field Encoding)[b]											
			1	2	3	4	5	6	7	8	11	13	14	15
PN2	109	-	U1DCD	U2RTS	-	-	-	-	-	-	-	-	-	EPI0S29
PN3	110	-	U1DSR	U2CTS	-	-	-	-	-	-	-	-	-	EPI0S30
PN4	111	-	U1DTR	U3RTS	I2C2SDA	-	-	-	-	-	-	-	-	EPI0S34
PN5	112	-	U1RI	U3CTS	I2C2SCL	-	-	-	-	-	-	-	-	EPI0S35
PP0	118	C2+	U6Rx	-	-	-	-	-	EN0INTRN	-	-	-	-	SSI3XDAT2
PP1	119	C2-	U6Tx	-	-	-	-	-	-	-	-	-	-	SSI3XDAT3
PP2	103	-	U0DTR	-	-	-	-	-	-	-	-	-	USB0NXT	EPI0S29
PP3	104	-	U1CTS	U0DCD	-	-	-	-	RTCCLK	-	-	-	USB0DIR	EPI0S30
PP4	105	-	U3RTS	U0DSR	-	-	-	-	-	-	-	-	USB0D7	-
PP5	106	-	U3CTS	I2C2SCL	-	-	-	-	-	-	-	-	USB0D6	-
PQ0	5	-	-	-	-	-	-	-	-	-	-	-	SSI3Clk	EPI0S20
PQ1	6	-	-	-	-	-	-	-	-	-	-	-	SSI3Fss	EPI0S21
PQ2	11	-	-	-	-	-	-	-	-	-	-	-	SSI3XDAT0	EPI0S22
PQ3	27	-	-	-	-	-	-	-	-	-	-	-	SSI3XDAT1	EPI0S23
PQ4	102	-	U1Rx	-	-	-	-	-	DIVSCLK	-	-	-	-	-
PQ5	57	-	U1Tx	-	-	-	-	-	-	-	-	-	EN0RXD0	-
PQ6	58	-	U1DTR	-	-	-	-	-	-	-	-	-	EN0RXD1	-

a. The TMPRn signals are digital signals enabled and configured by the Hibernation module. All other signals listed in this column are analog signals.

b. The digital signals that are shaded gray are the power-on default values for the corresponding GPIO pin. Encodings 9, 10, and 12 are not used on this device.

3.5 Possible Pin Assignments for Alternate Functions

Table 3-6. Possible Pin Assignments for Alternate Functions

# of Possible Assignments	Alternate Function	GPIO Function
one	AIN0	PE3
	AIN1	PE2
	AIN10	PB4
	AIN11	PB5
	AIN12	PD3
	AIN13	PD2
	AIN14	PD1
	AIN15	PD0
	AIN16	PK0
	AIN17	PK1
	AIN18	PK2
	AIN19	PK3
	AIN2	PE1
	AIN3	PE0
	AIN4	PD7
	AIN5	PD6
	AIN6	PD5
	AIN7	PD4
	AIN8	PE5
	AIN9	PE4
	C0+	PC6
	C0-	PC7
	C1+	PC5
	C1-	PC4
	C2+	PP0
	C2-	PP1
	C2o	PD2
	CAN0Rx	PA0
	CAN0Tx	PA1
	CAN1Rx	PB0
	CAN1Tx	PB1
	DIVSCLK	PQ4
	EN0COL	PM7
	EN0CRS	PM6
	EN0RREF_CLK	PM4
	EN0RXCK	PA6
	EN0RXD0	PQ5
	EN0RXD1	PQ6
	EN0RXD2	PK5

Table 3-6. Possible Pin Assignments for Alternate Functions *(continued)*

# of Possible Assignments	Alternate Function	GPIO Function
	EN0RXD3	PK4
	EN0RXDV	PG7
	EN0RXER	PG6
	EN0TXCK	PG2
	EN0TXD0	PG4
	EN0TXD1	PG5
	EN0TXD2	PK6
	EN0TXD3	PK7
	EN0TXEN	PG3
	EPI0S10	PG1
	EPI0S11	PG0
	EPI0S12	PM3
	EPI0S13	PM2
	EPI0S14	PM1
	EPI0S15	PM0
	EPI0S16	PL0
	EPI0S17	PL1
	EPI0S18	PL2
	EPI0S19	PL3
	EPI0S20	PQ0
	EPI0S21	PQ1
	EPI0S22	PQ2
	EPI0S23	PQ3
	EPI0S24	PK7
	EPI0S25	PK6
	EPI0S26	PL4
	EPI0S27	PB2
	EPI0S28	PB3
	EPI0S31	PK5
	EPI0S32	PK4
	EPI0S33	PL5
	EPI0S34	PN4
	EPI0S35	PN5
	EPI0S4	PC7
	EPI0S5	PC6
	EPI0S6	PC5
	EPI0S7	PC4
	EPI0S8	PA6
	EPI0S9	PA7
	I2C0SCL	PB2
	I2C0SDA	PB3

Table 3-6. Possible Pin Assignments for Alternate Functions *(continued)*

# of Possible Assignments	Alternate Function	GPIO Function
	I2C1SCL	PG0
	I2C1SDA	PG1
	I2C6SCL	PA6
	I2C6SDA	PA7
	I2C9SCL	PA0
	I2C9SDA	PA1
	IDX0	PL3
	M0FAULT0	PF4
	M0FAULT1	PK6
	M0FAULT2	PK7
	M0FAULT3	PL0
	M0PWM0	PF0
	M0PWM1	PF1
	M0PWM2	PF2
	M0PWM3	PF3
	M0PWM4	PG0
	M0PWM5	PG1
	M0PWM6	PK4
	M0PWM7	PK5
	NMI	PD7
	PhA0	PL1
	PhB0	PL2
	SSI0Clk	PA2
	SSI0Fss	PA3
	SSI0XDAT0	PA4
	SSI0XDAT1	PA5
	SSI0XDAT2	PA6
	SSI0XDAT3	PA7
	SSI1Clk	PB5
	SSI1Fss	PB4
	SSI1XDAT0	PE4
	SSI1XDAT1	PE5
	SSI1XDAT2	PD4
	SSI1XDAT3	PD5
	SSI3XDAT3	PP1
	SWCLK	PC0
	SWDIO	PC1
	SWO	PC3
	TCK	PC0
	TDI	PC2
	TDO	PC3

Table 3-6. Possible Pin Assignments for Alternate Functions *(continued)*

# of Possible Assignments	Alternate Function	GPIO Function
	TMPR0	PM7
	TMPR1	PM6
	TMPR2	PM5
	TMPR3	PM4
	TMS	PC1
	TRCLK	PF3
	TRD0	PF2
	TRD1	PF1
	TRD2	PF0
	TRD3	PF4
	U0DTR	PP2
	U0Rx	PA0
	U0Tx	PA1
	U4CTS	PK3
	U4RTS	PK2
	U5Rx	PC6
	U5Tx	PC7
	U6Rx	PP0
	U6Tx	PP1
	U7Rx	PC4
	U7Tx	PC5
	USB0CLK	PB3
	USB0D0	PL0
	USB0D1	PL1
	USB0D2	PL2
	USB0D3	PL3
	USB0D4	PL4
	USB0D5	PL5
	USB0D6	PP5
	USB0D7	PP4
	USB0DIR	PP3
	USB0DM	PL7
	USB0DP	PL6
	USB0ID	PB0
	USB0NXT	PP2
	USB0STP	PB2
	USB0VBUS	PB1

Table 3-6. Possible Pin Assignments for Alternate Functions *(continued)*

# of Possible Assignments	Alternate Function	GPIO Function
two	C0o	PD0 PL2
	C1o	PD1 PL3
	EN0INTRN	PK4 PP0
	EN0MDC	PB2 PF2
	EN0MDIO	PB3 PF3
	EPI0S0	PH0 PK0
	EPI0S1	PH1 PK1
	EPI0S2	PH2 PK2
	EPI0S29	PN2 PP2
	EPI0S3	PH3 PK3
	EPI0S30	PN3 PP3
	I2C3SCL	PG4 PK4
	I2C3SDA	PG5 PK5
	I2C4SCL	PG6 PK6
	I2C4SDA	PG7 PK7
	I2C5SCL	PB0 PB4
	I2C5SDA	PB1 PB5
	I2C7SCL	PA4 PD0
	I2C7SDA	PA5 PD1
	I2C8SCL	PA2 PD2
	I2C8SDA	PA3 PD3
	SSI2Clk	PD3 PG7
	SSI2Fss	PD2 PG6
	SSI2XDAT0	PD1 PG5
	SSI2XDAT1	PD0 PG4
	SSI2XDAT2	PD7 PG3
	SSI2XDAT3	PD6 PG2
	SSI3Clk	PF3 PQ0
	SSI3Fss	PF2 PQ1
	SSI3XDAT0	PF1 PQ2
	SSI3XDAT1	PF0 PQ3
	SSI3XDAT2	PF4 PP0
	T2CCP0	PA4 PM0
	T2CCP1	PA5 PM1
	T5CCP0	PB2 PM6
	T5CCP1	PB3 PM7
	U0RI	PK7 PM7
	U1CTS	PN1 PP3
	U1DCD	PE2 PN2
	U1DSR	PE1 PN3
	U1RI	PE4 PN5

Table 3-6. Possible Pin Assignments for Alternate Functions *(continued)*

# of Possible Assignments	Alternate Function	GPIO Function
	U1RTS	PE0 PN0
	U1Rx	PB0 PQ4
	U1Tx	PB1 PQ5
	U2CTS	PD7 PN3
	U2RTS	PD6 PN2
	U2Rx	PA6 PD4
	U2Tx	PA7 PD5
	U3CTS	PN5 PP5
	U3RTS	PN4 PP4
	U3Rx	PA4 PJ0
	U3Tx	PA5 PJ1
	U4Rx	PA2 PK0
	U4Tx	PA3 PK1
	USB0PFLT	PA7 PD7
three	I2C2SDA	PG3 PL0 PN4
	RTCCLK	PC5 PK7 PP3
	T0CCP0	PA0 PD0 PL4
	T0CCP1	PA1 PD1 PL5
	T1CCP0	PA2 PD2 PL6
	T1CCP1	PA3 PD3 PL7
	T3CCP0	PA6 PD4 PM2
	T3CCP1	PA7 PD5 PM3
	T4CCP0	PB0 PD6 PM4
	T4CCP1	PB1 PD7 PM5
	U0DCD	PH2 PM5 PP3
	U0DSR	PH3 PM6 PP4
	U0RTS	PB5 PG5 PH0
	U1DTR	PE3 PN4 PQ6
	USB0EPEN	PA6 PA7 PD6
four	I2C2SCL	PG2 PL1 PN5 PP5
	U0CTS	PB4 PG4 PH1 PM4

3.6 Connections for Unused Signals

Table 3-7 on page 84 shows how to handle signals for functions that are not used in a particular system implementation for devices that are in a 128-pin TQFP package. Two options are shown in the table: an acceptable practice and a preferred practice for reduced power consumption and improved EMC characteristics. If a module is not used in a system, and its inputs are grounded, it is important that the clock to the module is never enabled by setting the corresponding bit in the **RCGCx** register.

Table 3-7. Connections for Unused Signals (128-Pin TQFP)

Function	Signal Name	Pin Number	Acceptable Practice	Preferred Practice
ADC	VREFA+	9	VDDA	VDDA
GPIO	PA1(UART0TX)	34	NC	GND[a]
	PA4 (SSI0XDAT0)	37	NC	GND[b]
	All unused GPIOs	-	NC	GND
Hibernate	HIB	65	NC	NC
	VBAT	68	NC	VDD
	WAKE	64	NC	GND
	XOSC0	66	NC	GND
	XOSC1	67	NC	NC
No Connects	NC	-	NC	NC
System Control	OSC0	88	NC	GND
	OSC1	89	NC	NC
	RST	70	VDD	Pull up as shown in the data sheet
USB	USB0DM / PL7	93	NC	Pull-down to GND with 1K resistor[c]
	USB0DP / PL6	94	NC	Pull-down to GND with 1K resistor[c]

a. PA1 (UART0TX) may be enabled as an output by the ROM boot loader if no code is present in the flash and PA0 (UART0RX) receives a valid boot signature. Ensure that this condition will not occur if PA1 is to be connected directly to GND.

b. PA4 (SSI0XDAT0) may be enabled as an output by the ROM boot loader if no code is present in the flash and the SSI0x (PA2, PA3, PA5) receives a valid boot signature. Ensure that this condition will not occur if PA4 is to be connected directly to GND.

c. The ROM boot loader may configure these pins as USB pins if no code is present in the flash therefore they should not be directly connected to ground.

A Package Information

A.1 Orderable Devices

Figure A-1. Key to Part Numbers

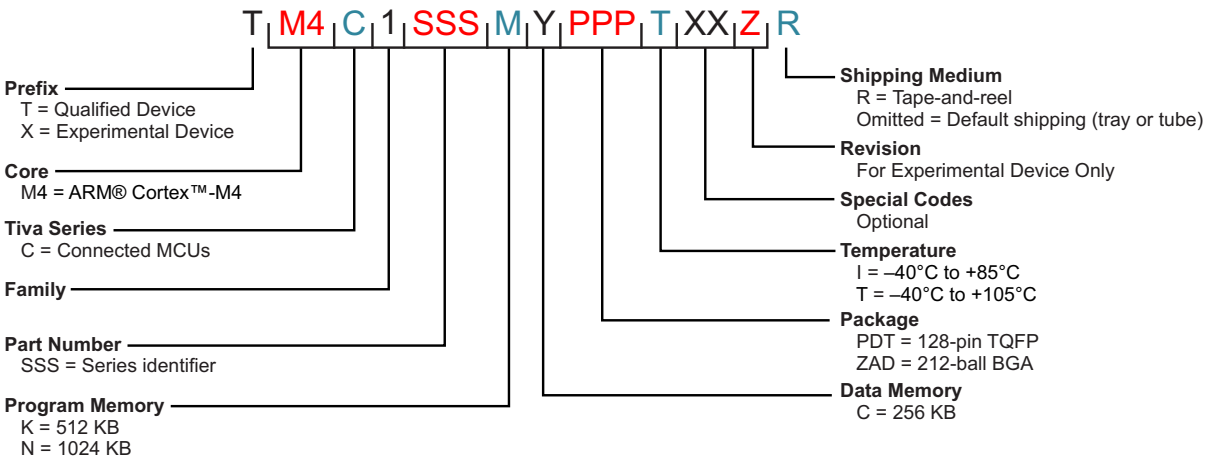


Table A-1. Orderable Part Numbers

Part Number	Description
TM4C129DNCPDTI	Tiva™ C Series TM4C129DNCPDT Microcontroller Industrial Temperature 128-pin TQFP
TM4C129DNCPDTIR	Tiva™ C Series TM4C129DNCPDT Microcontroller Industrial Temperature 128-pin TQFP Tape-and-reel
TM4C129DNCPDTT	Tiva™ C Series TM4C129DNCPDT Microcontroller Extended Temperature 128-pin TQFP
TM4C129DNCPDTTR	Tiva™ C Series TM4C129DNCPDT Microcontroller Extended Temperature 128-pin TQFP Tape-and-reel

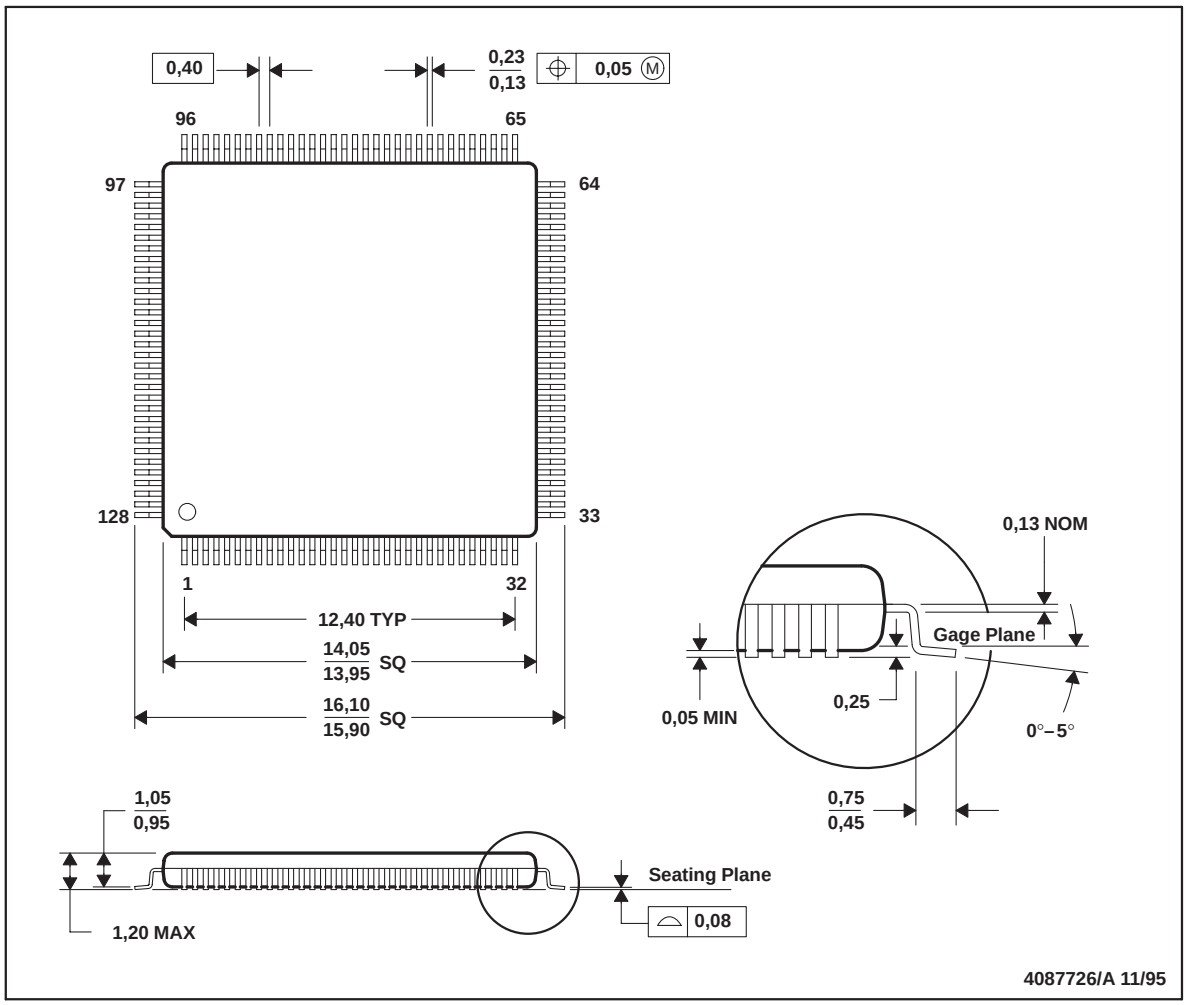
A.2 Packaging Diagram

Figure A-2. TM4C129DNCPDT 128-Pin TQFP Package Diagram

MECHANICAL DATA

MPQF013 – NOVEMBER 1995

PDT (S-PQFP-G128) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265