N-Channel 55 V (D-S) 175 °C MOSFET

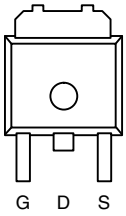
PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a]
55	0.0200 at V_{GS} = 10 V	35
	0.0260 at V_{GS} = 4.5 V	30

FEATURES

- TrenchFET® Power MOSFETS
- 175 °C Rated Maximum Junction Temperature
- Low Input Capacitance
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Available
RoHS* COMPLIANT

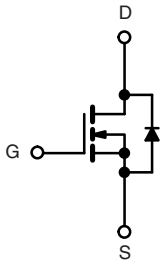
TO-252



Drain Connected to Tab

Top View

Ordering Information:
SUD35N05-26L-E3 (Lead (Pb)-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	55	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 175 °C)[b]	T_C = 25 °C	I_D	35	A
	T_C = 100 °C		25	
Pulsed Drain Current		I_{DM}	80	
Continuous Source Current (Diode Conduction)[a]		I_S	35	
Maximum Power Dissipation	T_C = 25 °C	P_D	50[c]	W
	T_A = 25 °C		7.5[b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Junction-to-Ambient[b]	t ≤ 10 s	R_{thJA}	17	20	°C/W
	Steady State		50	60	
Junction-to-Case		R_{thJC}	2.5	3	
Junction-to-Lead		R_{thJL}	5	6	

Notes:
a. Package limited.
b. Surface mounted on 1" x1" FR4 board, t ≤ 10 s.
c. See SOA curve for voltage derating.

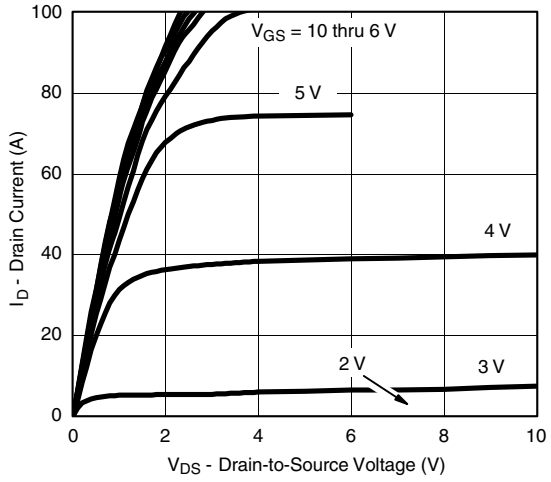
* Pb containing terminations are not RoHS compliant, exemptions may apply.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ[a]**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{BR}	V_{GS} = 0 V, I_D = 250 µA	55			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1			
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 44 V, V_{GS} = 0 V			1	µA
		V_{DS} = 44 V, V_{GS} = 0 V, T_J = 125 °C			50	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 5 V	35			A
Drain-Source On-State Resistance[b]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A		0.0165	0.0200	Ω
		V_{GS} = 10 V, I_D = 10 A, T_J = 125 °C			0.0350	
		V_{GS} = 4.5 V, I_D = 15 A		0.0215	0.0260	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 20 A		25		S
Dynamic[a]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		885		pF
Output Capacitance	C_{oss}			185		
Reverse Transfer Capacitance	C_{rss}			80		
Total Gate Charge[c]	Q_g	V_{DS} = 25 V, V_{GS} = 5 V, I_D = 35 A		10.5	13	nC
Gate-Source Charge[c]	Q_{gs}			4		
Gate-Drain Charge[c]	Q_{gd}			4.8		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 25 V, R_L = 0.3 Ω I_D ≅ 35 A, V_{GEN} = 10 V, R_G = 2.5 Ω		5	8	ns
Rise Time[c]	t_r			18	30	
Turn-Off Delay Time[c]	$t_{d(off)}$			20	30	
Fall Time[c]	t_f			100	150	
Source-Drain Diode Ratings and Characteristic (T_C = 25 °C)						
Continuous Current	I_S				35	A
Pulsed Current	I_{SM}				80	
Diode Forward Voltage[b]	V_{SD}	I_F = 80 A, V_{GS} = 0 V			1.5	V
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 35 A, di/dt = 100 A/µs		25	40	ns

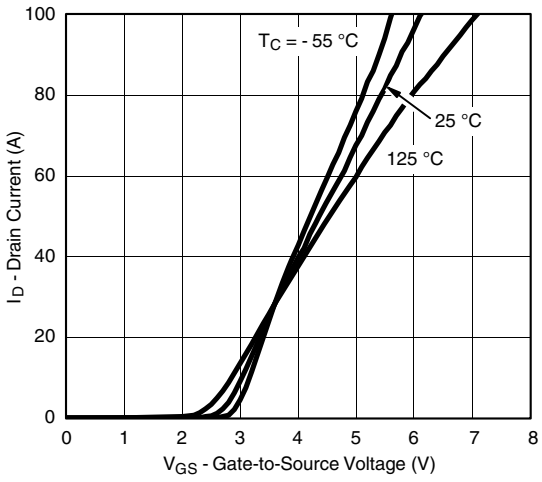
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

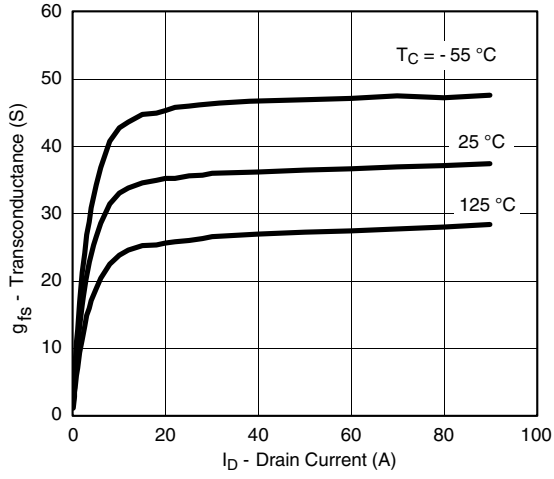
TYPICAL CHARACTERISTICS (25 °C unless noted)



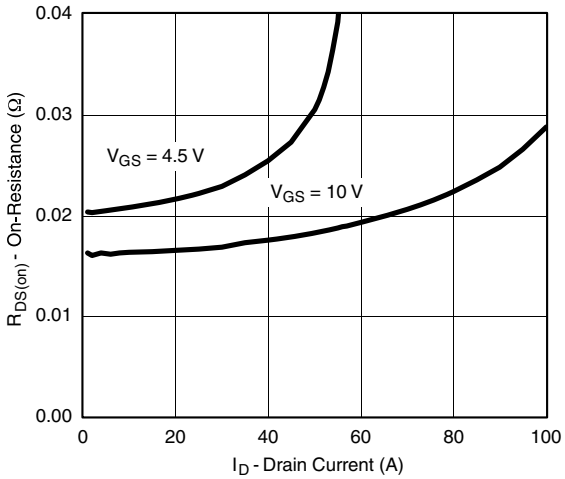
Output Characteristics



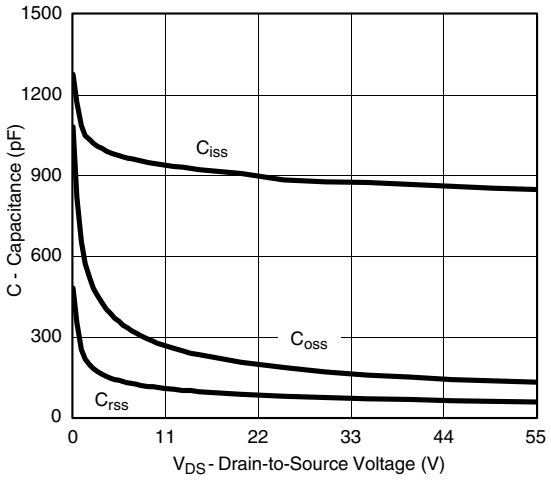
Transfer Characteristics



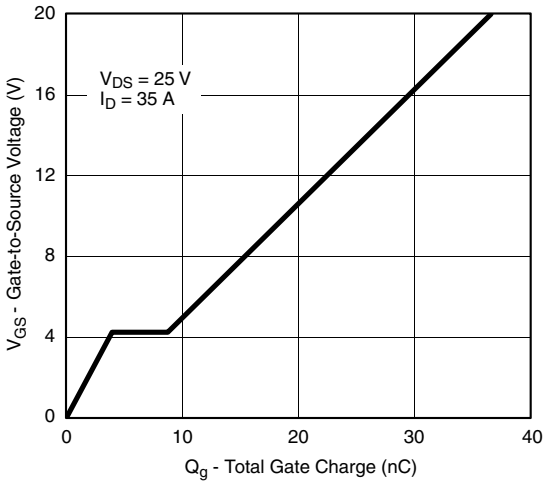
Transconductance



On-Resistance vs. Drain Current

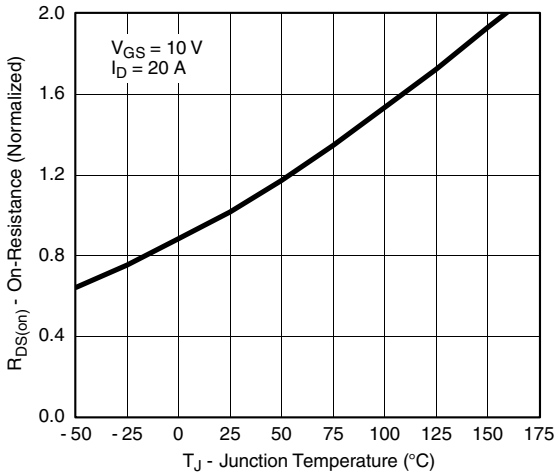


Capacitance

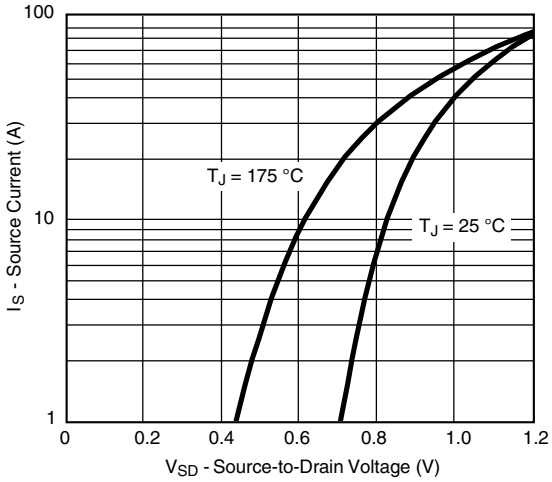


Gate Charge

TYPICAL CHARACTERISTICS (25 °C unless noted)

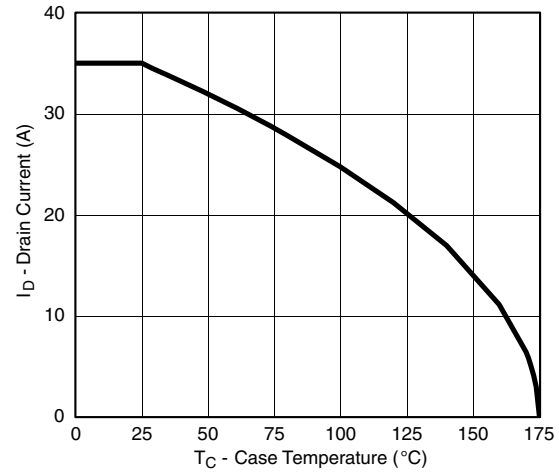


On-Resistance vs. Junction Temperature

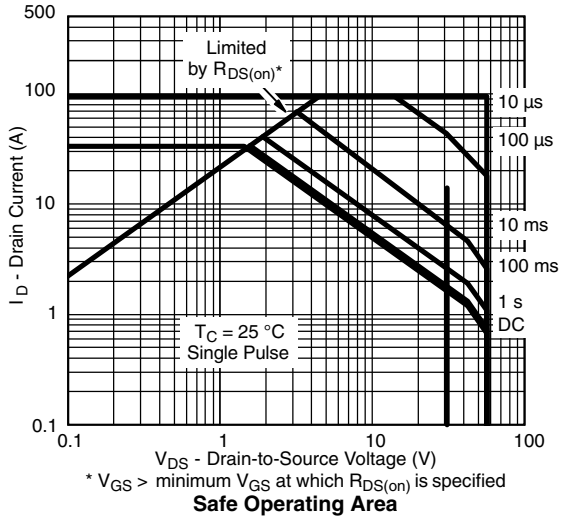


Source-Drain Diode Forward Voltage

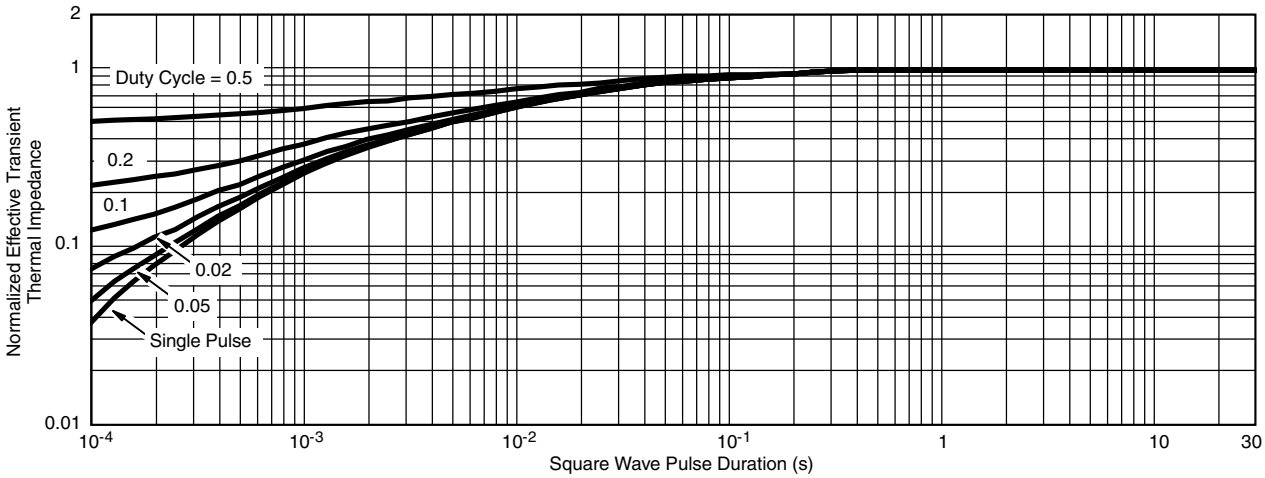
THERMAL RATINGS



Max. Avalanche and Drain Current vs. Case Temperature



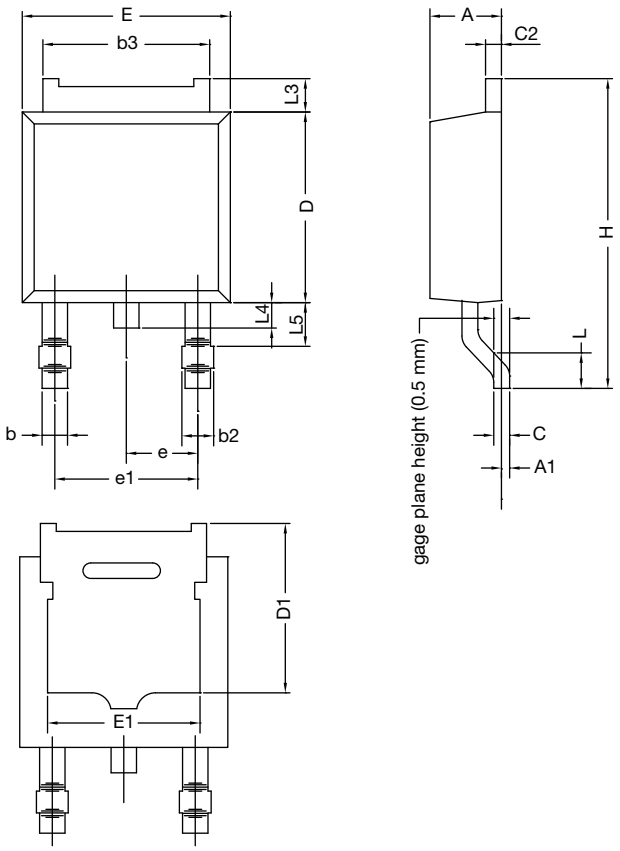
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71443.

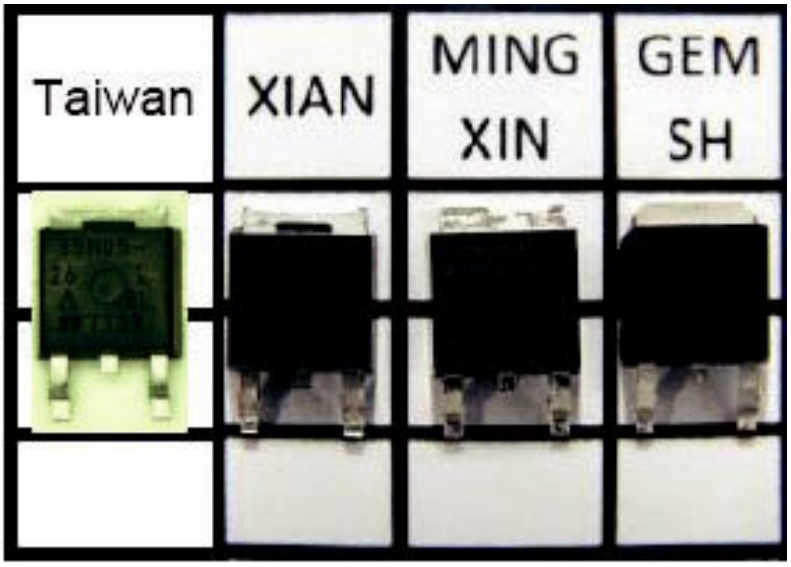
TO-252AA Case Outline



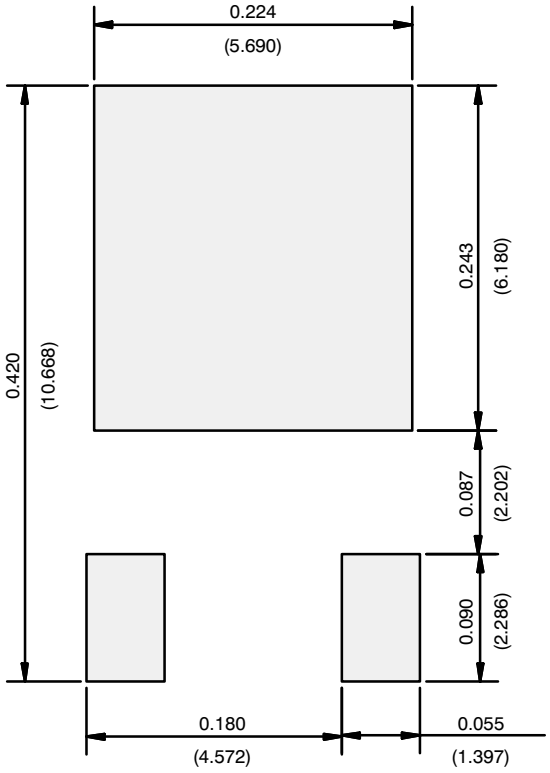
	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T13-0359-Rev. O, 03-Jun-13 DWG: 5347				

Notes

- Dimension L3 is for reference only.
- Xi'an, Mingxin, and GEM SH actual photo.



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

Return to Index

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