Application Report
SWCA116C–September 2011–Revised October 2012

TPS65911x Schematic Checklist

ABSTRACT

This application note for TPS65911x, a power companion device for application processors (see the device data sheet) lists the connection details for each pin. The ball details include a brief explanation of the function of each pin or signal and whether the signal is analog or digital. Use this information to check the connectivity for each ball on a system schematic.

In addition to this list, customers are advised to use the information in the data sheet, (TI literature number SWCS046).

NOTE: Customer must ensure that the power-up sequence for the application processor is met. This document does not cover the details of the power-up sequence for TPS65911 or the application processor. Refer to the device data sheet and the reference designs for the application processors for the correct power-up sequence requirements.

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Table 1. TPS65911x Schematic Checklist

Name	BGA Pin	Type	I/O [1]	Description	Recommended Connection [2]	Not Used Features
VDDIO	N7	Power	I	Digital I/Os supply	Connect to system I/O supply: an external I/O supply or I/O supply provided by TPS65911x (usually VIO).	N/A
SDA_SDI	M5	Digital	I/O	I^2C bidirectional data signal/serial peripheral interface data input (multiplexed)	1.2-k pullup to I/O supply	N/A
SCL_SCK	M4	Digital	I/O	I^2C bidirectional clock signal/serial peripheral interface clock input (multiplexed)	1.2-k pullup to I/O supply	N/A
SLEEP	F1	Digital	I	ACTIVE-to-SLEEP state transition control signal	Connected to processor control pin (that is, GPIO or any other low-power mode control pin)	GND
PWRHOLD	N1	Digital	I	Switch on, switch off control signal/GPI, mode defined in EEPROM	Switch-on, switch-off mode: Can be connected to an external signal for PMIC power-up/power-down control or If control is not required, then can be tied to VRTC	Floating (internal pulldown)
					GPI: Connect based on system requirement	Floating
PWRON	E4	Digital	I	External switch-on control (on button)	Push-button. PWRON transition low will power up PMIC	Floating (internal pullup)
NRESPWRON	H4	Digital	O	Power off reset	Connect to reset input of the processor or any other similar function to show device power up is complete	N/A
INT1	L3	Digital	O	Interrupt flag	Connect to the processor interrupt pin or a GPIO (optional)	Floating
NRESPWRON2	C7	Digital	O, OD	Second NRESPWRON output	Pullup to I/O supply	Floating
BOOT1	J5	Digital	I	Power-up sequence selection	Connect to VRTC for the EEPROM boot up sequence	N/A
CLK32KOUT	F4	Digital	O	32-kHz clock output	To processor 32K clock input	Floating
OSC32KIN	F8	Analog	I	32-kHz crystal oscillator	To crystal (if used)	Can be floating if using internal RC (defined in EEPROM)
OSC32KOUT	F7	Analog	I	32-kHz Crystal oscillator	To crystal (if used)	Can be floating if using internal RC (defined in EEPROM)
VREF	G8	Analog	O	Bandgap voltage	Connect to 0.1-µF capacitor to REFGND. Capacitor close to device	N/A
REFGND	G7	Analog	I/O	Reference ground	Connect to AGND (clean ground), same as 32K crystal GND	N/A
TESTV	B8	Analog	O	Analog test output (DFT)	Floating	Floating

(1) I = Input; O = Output; OD = Open Drain

(2) VBAT is the battery or any input source other than preregulation. The maximum level is 5.5 V.

Table 1. TPS65911x Schematic Checklist (continued)

Name	BGA Pin	Type	I/O [1]	Description	Recommended Connection [2]	Not Used Features
VBACKUP	D7	Power	I	Backup battery input	Backup battery - supercap or rechargeable coincell	Connected to GND (preferred) or VCC7
VCC1	E1/F2/F3	Power	I	VDD1 DC-DC power input	Connect to VBAT with a 10-µF capacitor	Connected to VCC7 or GND
GND1	C1/C2/D3	Power	I/O	VDD1 DC-DC power ground	GND	GND
SW1	D2/D1/E2	Power	O	VDD1 DC-DC switched output	Connected to a 2.2-µH inductor and a 10-µF capacitor to ground	Floating
VFB1	D4	Analog	I	VDD1 feedback voltage	Connected to a 2.2-µH inductor (other node that is away from the device)	GND or floating
VCC2	G2/G1	Power	I	VDD2 DC-DC power input	Connec to VBAT with a 10-µF capacitor	Connected to VCC7 or GND
GND2	J2/J1	Power	I/O	VDD2 DC-DC power ground	GND	GND
SW2	H2/H1	Power	O	VDD2 DC-DC switched output	Connected to a 2.2-µH inductor and a 10-µF capacitor to ground	Floating
VFB2	K2	Analog	I	VDD2 DC-DC feedback voltage	Connected to a 2.2-µH inductor (other node that is away from the device)	GND or floating
VCCIO	L7/L8	Power	I	VIO DC-DC power Input	Connec to VBAT with a 10-µF capacitor	Connected to VCC7 or GND
GNDIO	J7/J8	Power	I/O	VIO DC-DC power ground	GND	GND
SWIO	K8/K7	Power	O	VIO DC-DC switched output	Connected to a 2.2-µH inductor and a 10-µF capacitor to ground	Floating
VFBIO	H8	Analog	I	VIO feedback voltage	Connected to a 2.2-µH inductor (other node that is away from the device)	GND or floating
VCC3	N3	Power	I	LDO6, LDO7, and LDO8 power input	Connec to VBAT with a 4.7-µF capacitor	GND if other LDOs are not used (LDO6, LDO7, and LDO8 share this as a common input)
LDO8	M1	Power	O	LDO regulator output	Connect to a 2.2-µF filter capacitor	Floating
LDO7	M3	Power	O	LDO regulator output	Connect to a 2.2-µF filter capacitor	Floating
LDO6	M2	Power	O	LDO regulator output	Connect to a 2.2-µF filter capacitor	Floating
VCC4	L1	Power	I	LDO5 power input	Connec to VBAT with a 4.7-µF capacitor	GND if LDO5 is not used
LDO5	K1	Power	O	LDO regulator output	Connect to a 2.2-µF filter capacitor	Floating
VCC5	D8	Power	I	LDO3 and LDO4 power input	Connec to VBAT with a 4.7-µF capacitor	GND if not used by LDO3 or LDO4
LDO3	E7	Power	O	LDO regulator output	Connect to a 2.2-µF filter capacitor	Floating
LDO4	C8	Power	O	LDO regulator output	Connect to a 2.2-µF filter capacitor	Floating
VRTC	B5	Power	O	LDO regulator output	2.2 µF to GND	N/A

Table 1. TPS65911x Schematic Checklist (continued)

Name	BGA Pin	Type	I/O [1]	Description	Recommended Connection [2]	Not Used Features
VCC6	N5	Power	I	LDO1 and LDO2 power input	3.6-V (maximum) input. Needs external input or preregulated output from TPS65911x	GND if LDO output is not used (LDO1 and LDO2)
LDO1	N6	Power	O	LDO regulator output	Connect to a 2.2-µF filter capacitor	Floating
LDO2	N4	Power	O	LDO regulator output	Connect to a 2.2-µF filter capacitor	Floating
VCC7	B6	Power	I	VRTC power input and analog references supply	VBAT (5.5-V maximum) or other preregulated supply. Must be first supply provided for TPS65911x.	N/A
AGND	H5/H6/ D6/E5/ E6/F5/ G4/J4/J 6/K3	Power	I/O	Analog ground	AGND	N/A
AGND2	N8/J3/ M8	Power	I/O	Analog ground	AGND	N/A
DGND	B2/B1/ A1	Power	I/O	Digital ground	GND	N/A
EN2	M6	Digital	I/O	Enable for supplies/voltage scaling dedicated I^2C data	Processor I^2C for SmartReflex™ control with external pullup to VIO or connected to GPIO for DC-DC/LDO control	Floating
EN1	M7	Digital	I/O	Enable for supplies/voltage scaling dedicated I^2C clock	Processor I^2C for SmartReflex control with external pullup to VIO or connected to GPIO for DC-DC/LDO control	Floating
GPIO0	L5	Digital	I/O	GPIO, push-pull/OD as output. Default: defined in EEPROM	Connect to 120-kΩ PU to VDDIO (if configured as push-pull then pullup not required)	Floating
GPIO1	F6	Digital	I/O, OD	GPIO/LED1 output. Default: GPI	Depends on system. (If used as GPIO then 120-kΩ pullup is required.)	Floating
GPIO2	L2	Digital	I/O, OD	GPIO/DC-DC clock synchronization. Default: defined in EEPROM	Depends on system. (If used as GPIO then 120-kΩ pullup is required.)	Floating
GPIO3	B7	Digital	I/O, OD	GPIO/LED2 output. Default: GPI	Depends on system. (If used as GPIO then 120-kΩ pullup is required.)	Floating
GPIO4	H7	Digital	I/O, OD	GPIO. Default: GPI	Depends on system. (If used as GPIO then 120-kΩ pullup is required.)	Floating
GPIO5	G6	Digital	I/O, OD	GPIO. Default: GPI	Depends on system. (If used as GPIO then 120-kΩ pullup is required.)	Floating
GPIO6	G3	Digital	I/O; OD	GPIO. Default: defined in EEPROM	Depends on system. (If used as GPIO then 120-kΩ pullup is required.)	Floating
GPIO7	L4	Digital	I/O, OD	GPIO. Default: defined in EEPROM	Depends on system. (If used as GPIO then 120-kΩ pullup is required.)	Floating
GPIO8	K5	Digital	I/O, OD	GPIO. Default: GPI	Depends on system. (If used as GPIO then 120-kΩ pullup is required.)	Floating

Table 1. TPS65911x Schematic Checklist (continued)

Name	BGA Pin	Type	I/O [1]	Description	Recommended Connection [2]	Not Used Features
PWRDN	N2	Analog	I	Reset input; that is, for thermal reset	Test point or optionally a jumper connected to GND for a reset. Can be floating on production platform.	Floating or based on implementation. That is, if PWRDN is active low in EEPROM then tie to VRTC to avoid device reset.
HDRST	L6	Digital	I	Cold reset	Test point or optionally a 3-pin test point to connect to GND and VRTC.	Floating
VCCS	E8	Analog	I/O	Input for two comparators	Main supply of TPS65911x or multiple-cell battery through resistive divider	N/A
VBST	A2	Analog	I	VDDCtrl, supply for high-side FET driver	See Figure 1 in the data sheet and the corresponding external components table.	Floating
DRVH	A3	Analog	O	VDDCtrl, high-side FET driver output		Floating
SW	A4	Analog	I	VDDCtrl, switch node		Floating
V5IN	A5	Power	I	VDDCtrl, 5-V input	5-V input	GND or VCC7
DRVL	A6	Analog	O	VDDCtrl, FET driver output	See Figure 1 in the data sheet and the corresponding external components table.	Floating
VOUT	B4	Analog	I	VDDCtrl, feedback input		GND
TRIP	B3	Analog	I	VDDCtrl, OCL detection threshold pin		GND
VFB	C5	Analog	I	VDDCtrl, slew rate control capacitance		GND or floating
PGOOD	C4	Analog	O, OD	VDDCtrl, internal signal, leave floating (controller trimming only)	Floating	Floating
GNDC	A8/A7	Power	I/O	VDDCtrl, controller gnd	GND	N/A
TRAN	C6	Analog	I	Internal functional pin, leave floating (controller trimming only)	Floating	Floating
EN	D5	Analog	I	Internal functional pin, leave floating	Floating	Floating

Revision History

The following table summarizes the TPS65911x Schematic Checklist versions.

Note: Numbering may vary from previous versions.

Version	Literature Number	Date	Notes
*	SWCA116	September 2011	See (1)
A	SWCA116A	December 2011	See (2)
B	SWCA116B	December 2011	See (3)
C	SWCA116C	October 2012	See (4)

(1) TPS65911x Schematic Checklist, (SWCA116) - initial release.

(2) TPS65911x Schematic Checklist, (SWCA116A)"
- add missing balls
- update VBACKUP not used features - changed connection from GND to VCC7

(3) TPS65911x Schematic Checklist, (SWCA116B)"
- Update VBACKUP not used features - changed connection from VCC7 to GND (preferred) or VCC7

(4) TPS65911x Schematic Checklist, (SWCA116C)"
- Fix revision B history error

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