

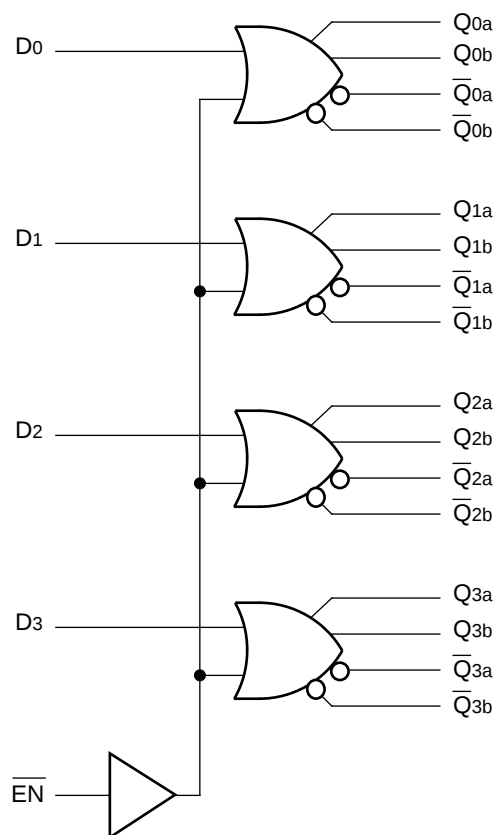
FEATURES

- 600ps max. propagation delay
- Extended 100E VEE range of -4.2V to -5.5V
- Common enable input
- Fully compatible with industry standard 10KH, 100K I/O levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E112
- Available in 28-pin PLCC package

DESCRIPTION

The SY10/100E112 are quad drivers designed for use in new, high-performance ECL systems. The E112 has two pairs of OR/NOR outputs from each gate and a common, buffered enable input. The data input can also be used as an ECL memory address fan-out driver, although the E111 is designed specifically for this purpose, and offers lower skew than the E112. For memory address driver applications where scan capabilities are required, please refer to the SY10/100E212 device.

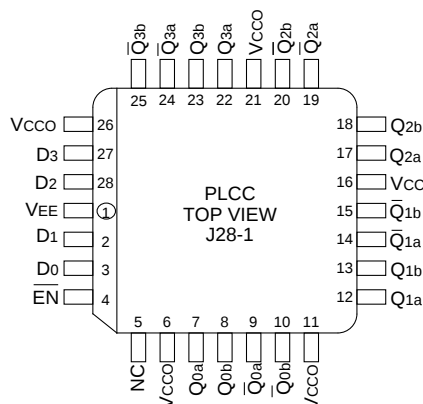
BLOCK DIAGRAM



PIN NAMES

Pin	Function
D0-D3	Data Inputs
$\overline{EN}$	Enable Input
Q_{na}, Q_{nb}	True Outputs
$\overline{Q}_{na}, \overline{Q}_{nb}$	Inverting Outputs
VCCO	Vcc to Output

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E112JI	J28-1	Industrial	SY10E112JI	Sn-Pb
SY10E112JITR ⁽²⁾	J28-1	Industrial	SY10E112JI	Sn-Pb
SY100E112JI	J28-1	Industrial	SY100E112JI	Sn-Pb
SY100E112JITR ⁽²⁾	J28-1	Industrial	SY100E112JI	Sn-Pb
SY10E112JC	J28-1	Commercial	SY10E112JC	Sn-Pb
SY10E112JCTR ⁽²⁾	J28-1	Commercial	SY10E112JC	Sn-Pb
SY100E112JC	J28-1	Commercial	SY100E112JC	Sn-Pb
SY100E112JCTR ⁽²⁾	J28-1	Commercial	SY100E112JC	Sn-Pb
SY10E112JY ⁽³⁾	J28-1	Industrial	SY10E112JY with Pb-Free bar-line indicator	Matte-Sn
SY10E112JYTR ^(2, 3)	J28-1	Industrial	SY10E112JY with Pb-Free bar-line indicator	Matte-Sn
SY100E112JY ⁽³⁾	J28-1	Industrial	SY100E112JY with Pb-Free bar-line indicator	Matte-Sn
SY100E112JYTR ^(2, 3)	J28-1	Industrial	SY100E112JY with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

TRUTH TABLE

EN	Q _n	$\overline{Q}_n$
L	D _n	$\overline{D}_n$
H	H	L

DC ELECTRICAL CHARACTERISTICSV_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

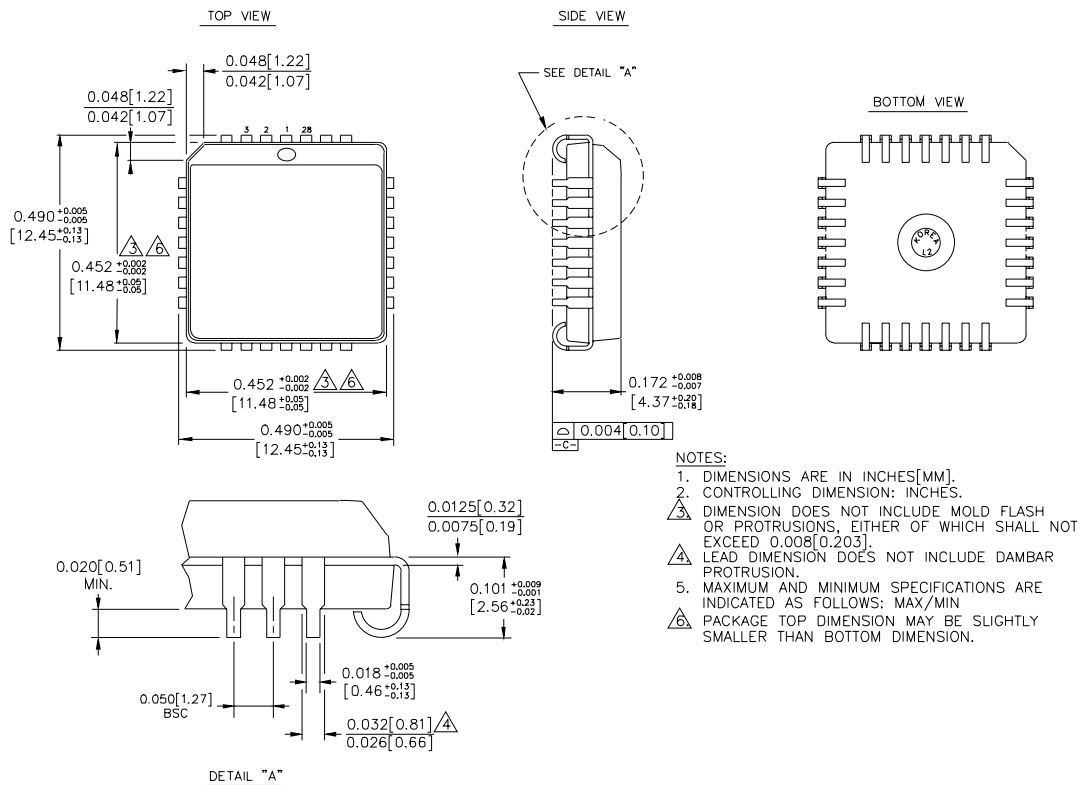
Symbol	Parameter	T _A = -40°C			T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I _{IH}	Input HIGH Current EN D	—	—	150	—	—	150	—	—	150	—	—	150	μA
		—	—	200	—	—	200	—	—	200	—	—	200	
I _{EE}	Power Supply Current													mA
	10E	—	47	56	—	47	56	—	47	56	—	47	56	
	100E	—	47	56	—	47	56	—	47	56	—	54	65	

AC ELECTRICAL CHARACTERISTICSV_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T _A = -40°C			T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t _{PD}	Propagation Delay to Output D EN	200 275	400 450	600 675	200 275	400 450	600 675	200 275	400 450	600 675	200 275	400 450	600 675	ps
t _{skew}	Within-Device Skew D _n to Q _n , $\overline{Q}_n^{(1)}$ Q _{na} to Q _{nb} ⁽²⁾	— —	80 40	— —	— —	80 40	— —	— —	80 40	— —	— —	80 40	— —	ps
t _r t _f	Rise/Fall Time 20% to 80%	275	425	700	275	425	700	275	425	700	275	425	700	ps

Notes:

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Skew defined between common OR or common NOR outputs of a single gate.

28-PIN PLCC (J28-1)

Rev. 03

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