FOUR-CHANNEL AUTOMOTIVE DIGITAL AMPLIFIERS

Check for Samples: TAS5414C-Q1, TAS5424C-Q1

FEATURES

- **TAS5414C-Q1 – Single-Ended Input**
- **TAS5424C-Q1 – Differential Input**
- **Four-Channel Digital Power Amplifier**
- **Four Analog Inputs, Four BTL Power Outputs**
- **Typical Output Power at 10% THD+N**
  - **28 W/Ch Into 4 Ω at 14.4 V**
  - **50 W/Ch Into 2 Ω at 14.4 V**
  - **79 W/Ch Into 4 Ω at 24 V**
  - **150 W/Ch Into 2 Ω at 24 V (PBTL)**
- **Channels Can Be Paralleled (PBTL) for High-Current Applications**
- **THD+N < 0.02%, 1 kHz, 1 W Into 4 Ω**
- **Patented Pop- and Click-Reduction Technology**
  - **Soft Muting With Gain Ramp Control**
  - **Common-Mode Ramping**
- **Patented AM Interference Avoidance**
- **Patented Cycle-by-Cycle Current Limit**
- **75-dB PSRR**
- **Four-Address I^2C Serial Interface for Device Configuration and Control**
- **Channel Gains: 12-dB, 20-dB, 26-dB, 32-dB**
- **Load Diagnostic Functions:**
  - **Output Open and Shorted Load**
  - **Output-to-Power and -to-Ground Shorts**
  - **Patented Tweeter Detection**
- **Protection and Monitoring Functions:**
  - **Short-Circuit Protection**
  - **Load-Dump Protection to 50 V**
  - **Fortuitous Open-Ground and -Power Tolerant**
  - **Patented Output DC Level Detection While Music Playing**
  - **Overtemperature Protection**
  - **Over- and Undervoltage Conditions**
  - **Clip Detection**
- **44-Pin PSOP3 (DKE) Power SOP Package With Heat Slug Up for TAS5424C-Q1**
- **64-Pin QFP (PHD) Power Package With Heat Slug Up for TAS5414C-Q1**
- **Designed for Automotive EMC Requirements**
- **Qualified According to AEC-Q100**
- **ISO9000:2002 TS16949 Certified**
- **–40°C to 105°C Ambient Temperature Range**

APPLICATIONS

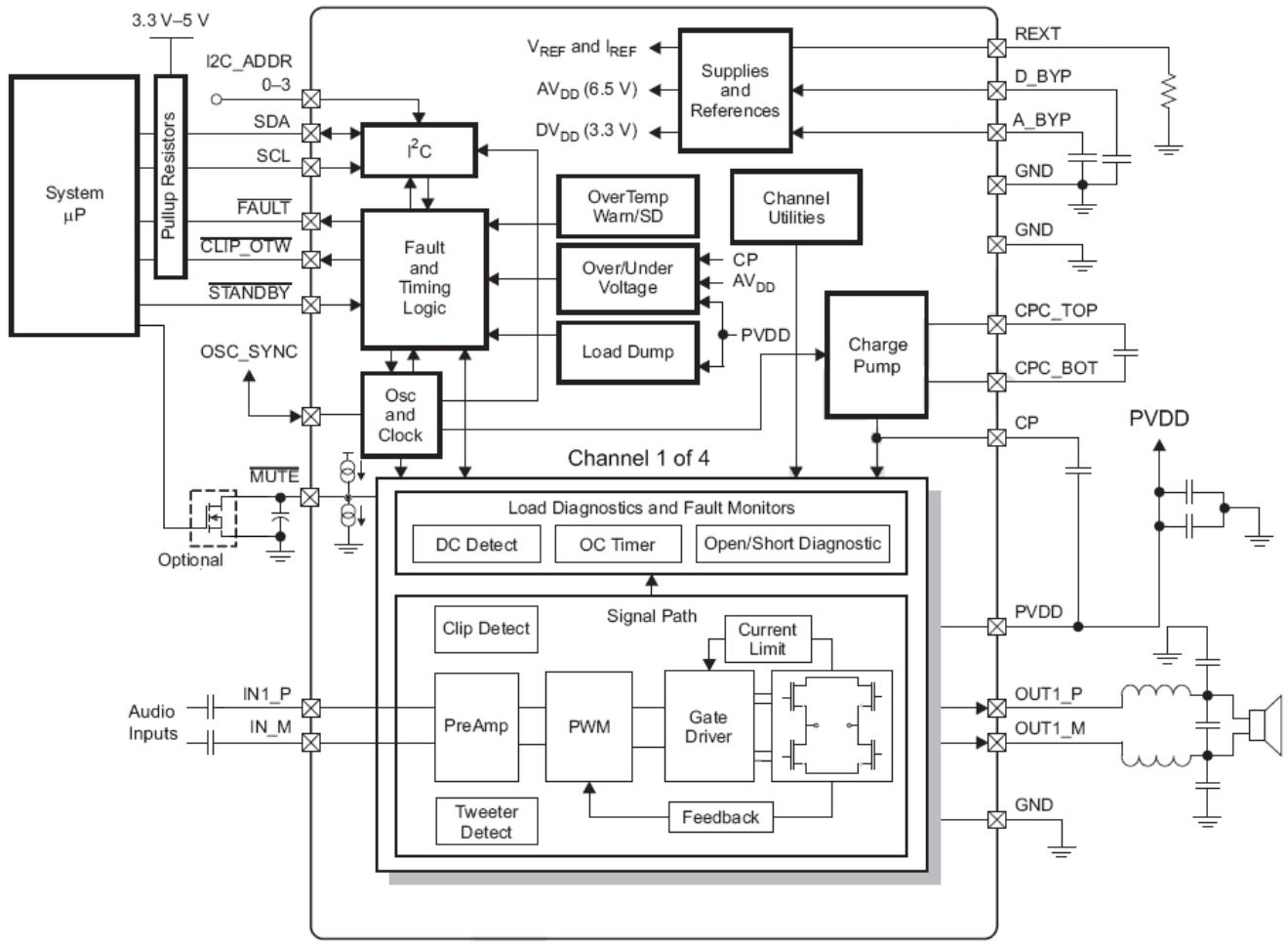
OEM/Retail Head Units and Amplifier Modules Where Feature Densities and System Configurations Require Reduction in Heat From the Audio Power Amplifier

DESCRIPTION

The TAS5414C-Q1 and TAS5424C-Q1 are four-channel digital audio amplifiers designed for use in automotive head units and external amplifier modules. They provide four channels at 23 W continuously into 4 Ω at less than 1% THD+N from a 14.4-V supply. Each channel can also deliver 38 W into 2 Ω at 1% THD+N. The TAS5414C-Q1 uses single-ended analog inputs, whereas the TAS5424C-Q1 employs differential inputs for increased immunity to common-mode system noise. The digital PWM topology of the device provides dramatic improvements in efficiency over traditional linear amplifier solutions. This reduces the power dissipated by the amplifier by a factor of ten under typical music playback conditions. The device incorporates all the functionality needed to perform in the demanding OEM applications area. The devices have built-in load diagnostic functions for detecting and diagnosing misconnected outputs to help to reduce test time during the manufacturing process.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS AND FUNCTIONS

The pin assignments are shown as follows.

DKE Package
(Top View)

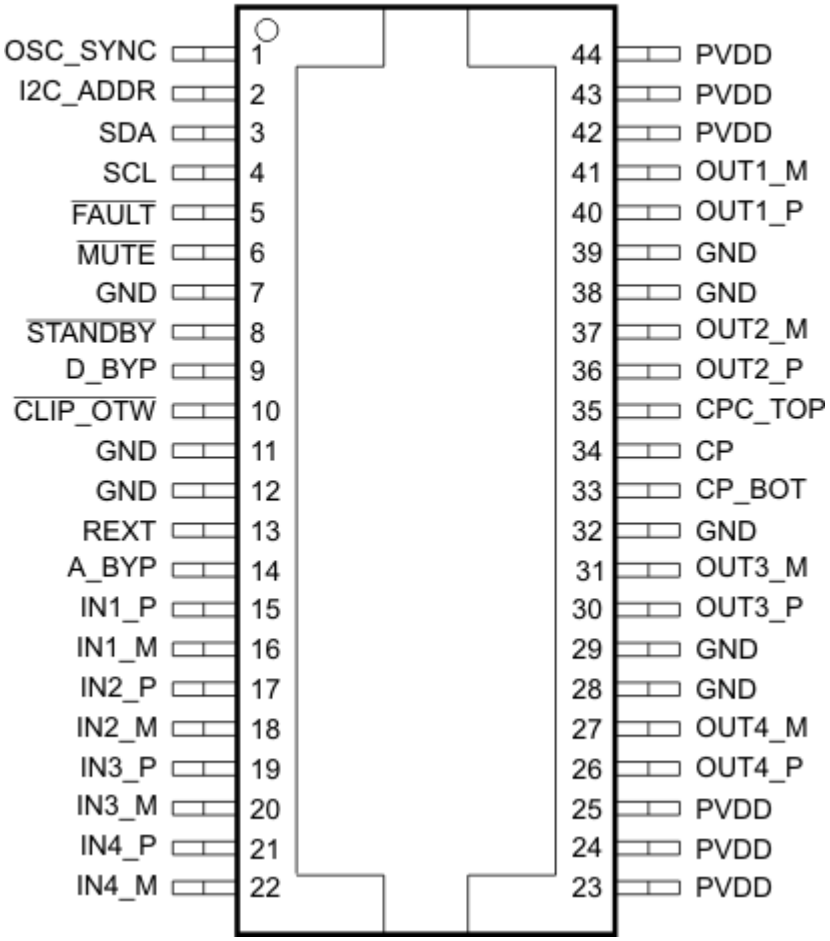


Figure 1. TAS5424C-Q1 44-Pin Package

PHD Package
(Top View)

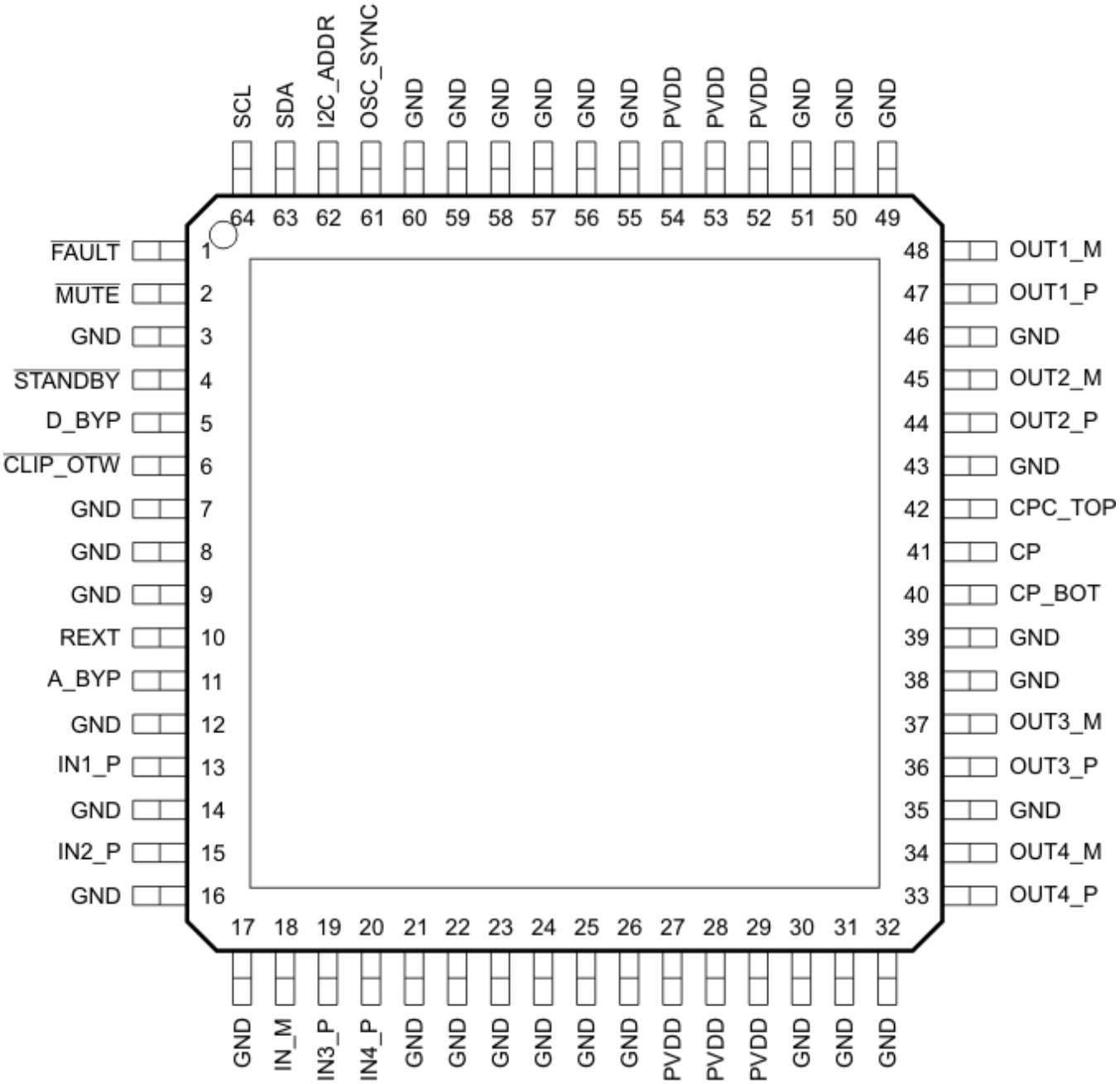


Figure 2. TAS5414C-Q1 64-Pin Package

Table 1. PIN FUNCTIONS

PIN			TYPE	DESCRIPTION
NAME	DKE PACKAGE	PHD PACKAGE		
	TAS5424C-Q1 NO.	TAS5414C-Q1 NO.		
A_BYP	14	11	PBY	Bypass pin for the AVDD analog regulator
$\overline{\text{CLIP\_OTW}}$	10	6	DO	Reports CLIP, OTW, or both. It also reports tweeter detection during tweeter mode. Open-drain
CP	34	41	CP	Top of main storage capacitor for charge pump (bottom goes to PVDD)
CPC_BOT	33	40	CP	Bottom of flying capacitor for charge pump
CPC_TOP	35	42	CP	Top of flying capacitor for charge pump
D_BYP	9	5	PBY	Bypass pin for DVDD regulator output
$\overline{\text{FAULT}}$	5	1	DO	Global fault output (open drain): UV, OV, OTSD, OCSD, DC
GND	7, 11, 12, 28, 29, 32, 38, 39	3, 7, 8, 9, 12, 14, 16, 17, 21, 22, 23, 24, 25, 26, 30, 31, 32, 35, 38, 39, 43, 46, 49, 50, 51, 55, 56, 57, 58, 59, 60	GND	Ground
I2C_ADDR	2	62	AI	I^2C address bit
IN1_M	16	N/A	AI	Inverting analog input for channel 1 (TAS5424C-Q1 only)
IN1_P	15	13	AI	Non-inverting analog input for channel 1
IN2_M	18	N/A	AI	Inverting analog input for channel 2 (TAS5424C-Q1 only)
IN2_P	17	15	AI	Non-inverting analog input for channel 2
IN3_M	20	N/A	AI	Inverting analog input for channel 3 (TAS5424C-Q1 only)
IN3_P	19	19	AI	Non-inverting analog input for channel 3
IN4_M	22	N/A	AI	Inverting analog input for channel 4 (TAS5424C-Q1 only)
IN4_P	21	20	AI	Non-inverting analog input for channel 4
IN_M	N/A	18	ARTN	Signal return for the four analog channel inputs (TAS5414C-Q1 only)
$\overline{\text{MUTE}}$	6	2	AI	Gain ramp control: mute (low), play (high)
OSC_SYNC	1	61	DI/DO	Oscillator input from master or output to slave amplifiers
OUT1_M	41	48	PO	– polarity output for bridge 1
OUT1_P	40	47	PO	+ polarity output for bridge 1
OUT2_M	37	45	PO	– polarity output for bridge 2
OUT2_P	36	44	PO	+ polarity output for bridge 2
OUT3_M	31	37	PO	– polarity output for bridge 3
OUT3_P	30	36	PO	+ polarity output for bridge 3
OUT4_M	27	34	PO	– polarity output for bridge 4
OUT4_P	26	33	PO	+ polarity output for bridge 4
PVDD	23, 24, 25, 42, 43, 44	27, 28, 29, 52, 53, 54	PWR	PVDD supply
REXT	13	10	AI	Precision resistor pin to set analog reference
SCL	4	64	DI	I^2C clock input from system I^2C master
SDA	3	63	DI/DO	I^2C data I/O for communication with system I^2C master
$\overline{\text{STANDBY}}$	8	4	DI	Active-low STANDBY pin. Standby (low), power up (high)

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			VALUE		UNIT
			MIN	MAX	
PVDD	DC supply voltage range	Relative to GND	–0.3	30	V
$PVDD_{MAX}$	Pulsed supply voltage range	t ≤ 100 ms exposure	–1	50	V
$PVDD_{RAMP}$	Supply voltage ramp rate			15	V/ms
I_{PVDD}	Externally imposed dc supply current per PVDD or GND pin			±12	A
I_{PVDD_MAX}	Pulsed supply current per PVDD pin (one shot)	t < 100 ms		17	A
I_O	Maximum allowed dc current per output pin			±13.5	A
I_{O_MAX} (1)	Pulsed output current per output pin (single pulse)	t < 100 ms		±17	A
I_{IN_MAX}	Maximum current, all digital and analog input pins (2)	DC or pulsed		±1	mA
I_{MUTE_MAX}	Maximum current on $\overline{MUTE}$ pin	DC or pulsed		±20	mA
I_{IN_ODMAX}	Maximum sink current for open-drain pins			7	mA
V_{LOGIC}	Input voltage range for pin relative to GND (SCL, SDA, I2C_ADDR pins)	Supply voltage range: 6V < PVDD < 24 V	–0.3	6	V
V_{MUTE}	Voltage range for $\overline{MUTE}$ pin relative to GND	Supply voltage range: 6 V < PVDD < 24 V	–0.3	7.5	V
$V_{STANDBY}$	Input voltage range for $\overline{STANDBY}$ pin	Supply voltage range: 6 V < PVDD < 24 V	–0.3	5.5	V
V_{OSC_SYNC}	Input voltage range for OSC_SYNC pin relative to GND	Supply voltage range: 6 V < PVDD < 24 V	–0.3	3.6	V
V_{GND}	Maximum voltage between GND pins			±0.3	V
$V_{AIN\_AC\_MAX\_5414}$	Maximum ac-coupled input voltage for TAS5414C-Q1 (2), analog input pins	Supply voltage range: 6 V < PVDD < 24 V		1.9	Vrms
$V_{AIN\_AC\_MAX\_5424}$	Maximum ac-coupled differential input voltage for TAS5424C-Q1 (2), analog input pins	Supply voltage range: 6 V < PVDD < 24 V		3.8	Vrms
T_J	Maximum operating junction temperature range		–55	150	°C
T_{stg}	Storage temperature range		–55	150	°C

(1) Pulsed current ratings are maximum survivable currents externally applied to the device. The device may encounter high currents during reverse-battery, fortuitous open-ground, and fortuitous open-supply fault conditions.
(2) See the *Application Information* section for information on analog input voltage and ac coupling.

THERMAL CHARACTERISTICS

PARAMETER		VALUE (Typical)	UNIT
$R_{\theta JC}$	Junction-to-case (heat slug) thermal resistance, DKE package	1	°C/W
$R_{\theta JC}$	Junction-to-case (heat slug) thermal resistance, PHD package	1.2	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	This device is not intended to be used without a heatsink. Therefore, $R_{\theta JA}$ is not specified. See the *Thermal Information* section.	
	Exposed pad dimensions, DKE package	13.8 × 5.8	mm
	Exposed pad dimensions, PHD package	8 × 8	

ELECTROSTATIC DISCHARGE (ESD)

PARAMETER	Package	Pins	VALUE (Typical)	UNIT
Human Body Model (HBM) AEC-Q100-002	All	All	3000	V
Changed Device Model (CDM) AEC-Q100-011	DKE	Corner pins excluding OSC_SYNC	1000	V
		All other pins (including OSC_SYNC) except CP pin	500	
		CP pin (Non-Corner Pin)	400	
	PHD	Corner pins excluding SCL	750	V
		All pins (including SCL) except CP and CP_Top	600	
		CP and CP_Top pins	400	

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	TYP	MAX	UNIT
$PVDD_{OP}$	DC supply voltage range relative to GND		6	14.4	24	V
V_{AIN_5414} (2)	Analog audio input signal level (TAS5414C-Q1)	AC-coupled input voltage	0		0.25–1(3)	Vrms
V_{AIN_5424} (2)	Analog audio input signal level (TAS5424C-Q1)	AC-coupled input voltage	0		0.5–2(3)	Vrms
T_A	Ambient temperature		–40		105	°C
T_J	Junction temperature	An adequate heat sink is required to keep T_J within specified range.	–40		115	°C
R_L	Nominal speaker load impedance		2	4		Ω
V_{PU}	Pullup voltage supply (for open-drain logic outputs)		3	3.3 or 5	5.5	V
R_{PU_EXT}	External pullup resistor on open-drain logic outputs	Resistor connected between open-drain logic output and V_{PU} supply	10		50	kΩ
R_{PU_I2C}	I^2C pullup resistance on SDA and SCL pins		1	4.7	10	kΩ
R_{I2C_ADD}	Total resistance of voltage divider for I^2C address slave 1 or slave 2, connected between D_BYP and GND pins		10		50	kΩ
R_{REXT}	External resistance on REXT pin	1% tolerance required	19.8	20	20.2	kΩ
C_{D_BYP} , C_{A_BYP}	External capacitance on D_BYP and A_BYP pins		10		120	nF
C_{OUT}	External capacitance to GND on OUT_X pins			150	680	nF
C_{IN}	External capacitance to analog input pin in series with input signal			0.47		µF
C_{FLY}	Flying capacitor on charge pump		0.47	1	1.5	µF
C_P	Charge pump capacitor	50V needed for Load Dump	0.47	1	1.5	µF
C_{MUTE}	$\overline{MUTE}$ pin capacitor		100	220	1000	nF
$C_{OSCSYNC\_MAX}$	Allowed loading capacitance on OSC_SYNC pin			75		pF

(1) The *Recommended Operating Conditions* table specifies only that the device is functional in the given range. See the *Electrical Characteristics* table for specified performance limits.
(2) Signal input for full unclipped output with gains of 32 dB, 26 dB, 20 dB, and 12 dB
(3) Maximum recommended input voltage is determined by the gain setting.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise noted): T_{Case} = 25°C, PVDD = 14.4 V, R_L = 4 Ω, f_S = 417 kHz, P_{out} = 1 W/ch, Rext = 20 kΩ, AES17 filter, default I^2C settings, master-mode operation (see application diagram)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CURRENT						
I_{PVDD_IDLE}	PVDD idle current	All four channels in MUTE mode		170	220	mA
I_{PVDD_Hi-Z}		All four channels in Hi-Z mode		93		
I_{PVDD_STBY}	PVDD standby current	STANDBY mode, $T_J \le 85°C$		2	10	µA
OUTPUT POWER						
P_{OUT}	Output power per channel	4 Ω, PVDD = 14.4 V, THD+N ≤ 1%, 1 kHz, T_c = 75°C		23		W
		4 Ω, PVDD = 14.4 V, THD+N = 10%, 1 kHz, T_c = 75°C	25	28		
		4 Ω, PVDD = 24 V, THD+N = 10%, 1 kHz, T_c = 75°C	63	79		
		2 Ω, PVDD = 14.4 V, THD+N = 1%, 1 kHz, T_c = 75°C		38		
		2 Ω, PVDD = 14.4 V, THD+N = 10%, 1 kHz, T_c = 75°C	40	50		
		PBTL 2-Ω operation, PVDD = 24 V, THD+N = 10%, 1 kHz, T_c = 75°C		150		
		PBTL 1-Ω operation, PVDD = 14.4 V, THD+N = 10%, 1 kHz, T_c = 75°C		90		
EFF_P	Power efficiency	4 channels operating, 23-W output power/ch, L = 10 µH, $T_J \le 85°C$		90%		
AUDIO PERFORMANCE						
V_{NOISE}	Noise voltage at output	Zero input, and A-weighting		60	100	µV
	Channel crosstalk	P = 1 W, f = 1 kHz, enhanced crosstalk enabled via I^2C (reg. 0x10)	70	85		dB
$CMRR_{5424}$	Common-mode rejection ratio (TAS5424C-Q1)	f = 1 kHz, 1 Vrms referenced to GND, G = 26 dB	60	75		dB
PSRR	Power-supply rejection ratio	PVDD = 14.4 Vdc + 1 Vrms, f = 1 kHz	60	75		dB
THD+N	Total harmonic distortion + noise	P = 1 W, f = 1 kHz		0.02%	0.1%	
f_S	Switching frequency	Switching frequency selectable for AM interference avoidance	336	357	378	kHz
			392	417	442	
			470	500	530	
R_{AIN}	Analog input resistance	Internal shunt resistance on each input pin	63	85	106	kΩ
V_{IN_CM}	Common-mode input voltage	AC-coupled common-mode input voltage (zero differential input)		1.3		Vrms
V_{CM_INT}	Internal common-mode input bias voltage	Internal bias applied to IN_M pin		3.3		V
G	Voltage gain (V_O/V_{IN})	Source impedance = 0 Ω, gain measurement taken at 1 W of power per channel	11	12	13	dB
			19	20	21	
			25	26	27	
			31	32	33	
G_{CH}	Channel-to-channel variation	Any gain commanded	–1	0	1	dB
PWM OUTPUT STAGE						
$R_{DS(on)}$	FET drain-to-source resistance	Not including bond wire resistance, T_J = 25°C		65	90	mΩ
V_{O_OFFSET}	Output offset voltage	Zero input signal, G = 26 dB		±10	±50	mV
PVDD OVERVOLTAGE (OV) PROTECTION						
V_{OV_SET}	PVDD overvoltage shutdown set		24.6	26.4	28.2	V
V_{OV_CLEAR}	PVDD overvoltage shutdown clear		24.4	25.9	27.4	V
PVDD UNDERVOLTAGE (UV) PROTECTION						
V_{UV_SET}	PVDD undervoltage shutdown set		4.9	5.3	5.6	V
V_{UV_CLEAR}	PVDD undervoltage shutdown clear		6.2	6.6	7	V
AVDD						
V_{A_BYP}	A_BYP pin voltage			6.5		V
$V_{A\_BYP\_UV\_SET}$	A_BYP UV voltage			4.8		V
$V_{A\_BYP\_UV\_CLEAR}$	Recovery voltage A_BYP UV			5.3		V
DVDD						
V_{D_BYP}	D_BYP pin voltage			3.3		V

ELECTRICAL CHARACTERISTICS (continued)

Test conditions (unless otherwise noted): T_{Case} = 25°C, PVDD = 14.4 V, R_L = 4 Ω, f_S = 417 kHz, P_{out} = 1 W/ch, Rext = 20 kΩ, AES17 filter, default I^2C settings, master-mode operation (see application diagram)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-ON RESET (POR)						
V_{POR}	PVDD voltage for POR	I^2C active above this voltage			4	V
V_{POR_HY}	PVDD recovery hysteresis voltage for POR			0.1		V
REXT						
V_{REXT}	Rext pin voltage			1.27		V
CHARGE PUMP (CP)						
V_{CPUV_SET}	CP undervoltage			4.8		V
V_{CPUV_CLEAR}	Recovery voltage for CP UV			4.9		V
OVERTEMPERATURE (OT) PROTECTION						
T_{OTW1_CLEAR}	Junction temperature for overtemperature warning		96	112	128	°C
T_{OTW1_SET} / T_{OTW2_CLEAR}			106	122	138	°C
T_{OTW2_SET} / T_{OTW3_CLEAR}			116	132	148	°C
T_{OTW3_SET} / T_{OTSD_CLEAR}			126	142	158	°C
T_{OTSD}	Junction temperature for overtemperature shutdown		136	152	168	°C
T_{FB}	Junction temperature for overtemperature foldback	Per channel	130	150	170	°C
CURRENT LIMITING PROTECTION						
I_{LIM}	Current limit (load current)	Level 1	5.5	7.3	9	A
		Level 2 (default)	10.6	12.7	15	
OVERCURRENT (OC) SHUTDOWN PROTECTION						
I_{MAX}	Maximum current (peak output current)	Level 1	7.8	9.8	12.2	A
		Level 2 (default), Any short to supply, ground, or other channels	11.9	14.8	17.7	
TWEETER DETECT						
I_{TH_TW}	Load-current threshold for tweeter detect		330	445	560	mA
I_{LIM_TW}	Load-current limit for tweeter detect			2.1		A
STANDBY MODE						
V_{IH}	$\overline{\text{STANDBY}}$ input voltage for logic-level high		2			V
V_{IL}	$\overline{\text{STANDBY}}$ input voltage for logic-level low				0.7	V
I_{STBY}	$\overline{\text{STANDBY}}$ pin current			0.1	0.2	μA
MUTE MODE						
G_{MUTE}	Output attenuation	$\overline{\text{MUTE}}$ pin ≤ 0.5 V for 200ms or I^2C Mute Enabled		100		dB
DC DETECT						
$V_{TH\_DC\_TOL}$	DC detect threshold tolerance			25		%
t_{DCD}	DC detect step-response time for four channels				5.3	s
CLIP_OTW REPORT						
$V_{OH\_CLIPOTW}$	$\overline{\text{CLIP\_OTW}}$ pin output voltage for logic level high (open-drain logic output)	External 47-kΩ pullup resistor to 3 V–5.5 V	2.4			V
$V_{OL\_CLIPOTW}$	$\overline{\text{CLIP\_OTW}}$ pin output voltage for logic level low (open-drain logic output)				0.5	V
$t_{DELAY\_CLIPDET}$	$\overline{\text{CLIP\_OTW}}$ signal delay when output clipping detected				20	μs
FAULT REPORT						
V_{OH_FAULT}	$\overline{\text{FAULT}}$ pin output voltage for logic-level high (open-drain logic output)	External 47-kΩ pullup resistor to 3 V–5.5 V	2.4			V
V_{OL_FAULT}	$\overline{\text{FAULT}}$ pin output voltage for logic-level low (open-drain logic output)				0.5	

ELECTRICAL CHARACTERISTICS (continued)

Test conditions (unless otherwise noted): T_{Case} = 25°C, PVDD = 14.4 V, R_L = 4 Ω, f_S = 417 kHz, P_{out} = 1 W/ch, Rext = 20 kΩ, AES17 filter, default I^2C settings, master-mode operation (see application diagram)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN, SHORT DIAGNOSTICS						
R_{S2P}, R_{S2G}	Maximum resistance to detect a short from OUT pin(s) to PVDD or ground				200	Ω
R_{OPEN_LOAD}	Minimum load resistance to detect open circuit	Including speaker wires	300	740	1300	Ω
$R_{SHORTED\_LOAD}$	Maximum load resistance to detect short circuit	Including speaker wires	0.5	1	1.5	Ω
I^2C ADDRESS DECODER						
$t_{LATCH\_I2CADDR}$	Time delay to latch I^2C address after POR			300		µs
V_{I2C_ADDR}	Voltage on I2C_ADDR pin for address 0	Connect to GND	0%	0%	15%	V_{D_BYP}
	Voltage on I2C_ADDR pin for address 1	External resistors in series between D_BYP and GND as a voltage divider	25%	35%	45%	
	Voltage on I2C_ADDR pin for address 2		55%	65%	75%	
	Voltage on I2C_ADDR pin for address 3	Connect to D_BYP	85%	100%	100%	
I^2C						
t_{HOLD_I2C}	Power-on hold time before I^2C communication	$\overline{\text{STANDBY}}$ high		1		ms
f_{SCL}	SCL clock frequency				400	kHz
V_{IH}	SCL pin input voltage for logic-level high	R_{PU_I2C} = 5-kΩ pullup, supply voltage = 3.3 V or 5 V	2.1		5.5	V
V_{IL}	SCL pin input voltage for logic-level low		–0.5		1.1	V
V_{OH}	SDA pin output voltage for logic-level high	I^2C read, R_{I2C} = 5-kΩ pullup, supply voltage = 3.3 V or 5 V	2.4			V
V_O	SDA pin output voltage for logic-level low	I^2C read, 3-mA sink current			0.4	V
V_{IH}	SDA pin input voltage for logic-level high	I^2C write, R_{I2C} = 5-kΩ pullup, supply voltage = 3.3 V or 5 V	2.1		5.5	V
V_{IL}	SDA pin input voltage for logic-level low	I^2C write, R_{I2C} = 5-kΩ pullup, supply voltage = 3.3 V or 5 V	–0.5		1.1	V
C_I	Capacitance for SCL and SDA pins				10	pF
OSCILLATOR						
V_{OH}	OSC_SYNC pin output voltage for logic-level high	I2C_ADDR pin set to MASTER mode	2.4			V
V_{OL}	OSC_SYNC pin output voltage for logic-level low				0.5	V
V_{IH}	OSC_SYNC pin input voltage for logic-level high	I2C_ADDR pin set to SLAVE mode	2			V
V_{IL}	OSC_SYNC pin input voltage for logic-level low				0.8	V
f_{OSC_SYNC}	OSC_SYNC pin clock frequency	I2C_ADDR pin set to MASTER mode, f_S = 500 kHz	3.76	4	4.24	MHz
		I2C_ADDR pin set to MASTER mode, f_S = 417 kHz	3.13	3.33	3.63	
		I2C_ADDR pin set to MASTER mode, f_S = 357 kHz	2.68	2.85	3.0	

TIMING REQUIREMENTS FOR I²C INTERFACE SIGNALS

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
t_r	Rise time for both SDA and SCL signals			300	ns
t_f	Fall time for both SDA and SCL signals			300	ns
$t_{w(H)}$	SCL pulse duration, high	0.6			µs
$t_{w(L)}$	SCL pulse duration, low	1.3			µs
t_{su2}	Setup time for START condition	0.6			µs
t_{h2}	START condition hold time until generation of first clock pulse	0.6			µs
t_{su1}	Data setup time	100			ns
t_{h1}	Data hold time	0 (1)			ns
t_{su3}	Setup time for STOP condition	0.6			µs
C_B	Load capacitance for each bus line			400	pF

(1) A device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

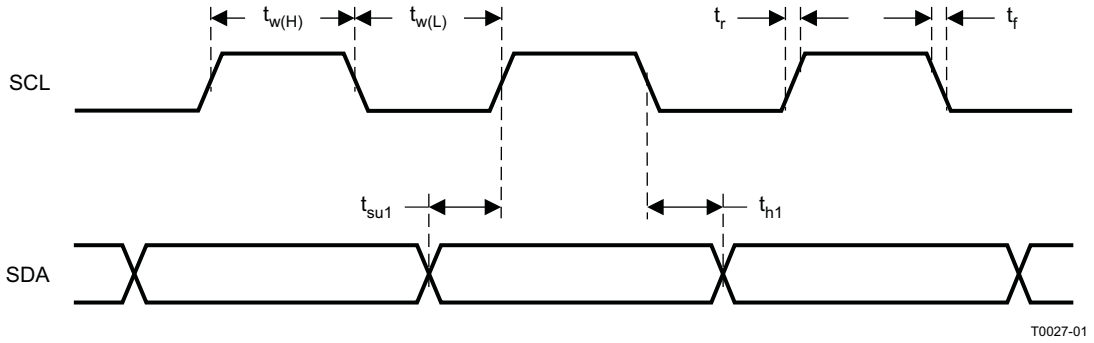


Figure 3. SCL and SDA Timing

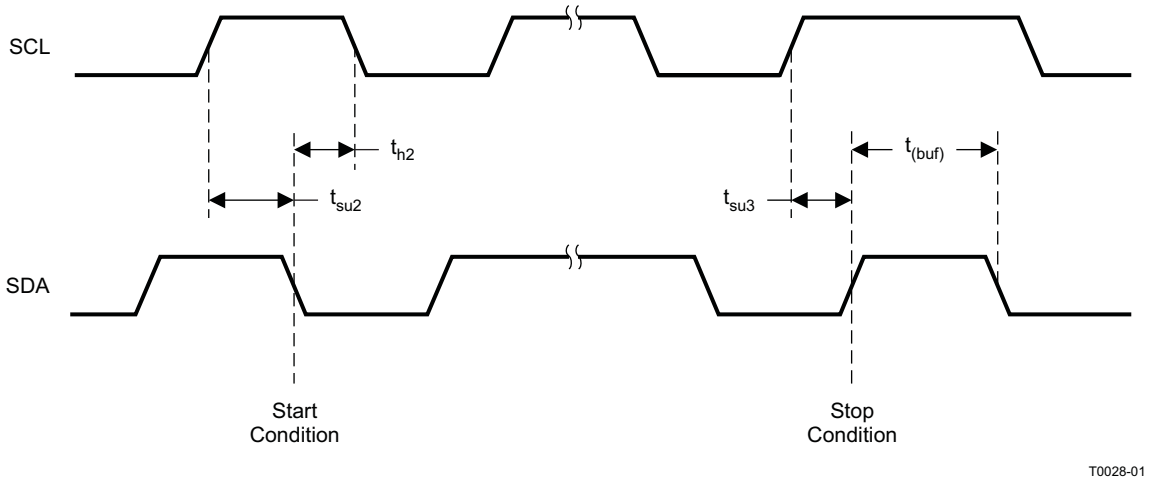


Figure 4. Timing for Start and Stop Conditions

TYPICAL CHARACTERISTICS

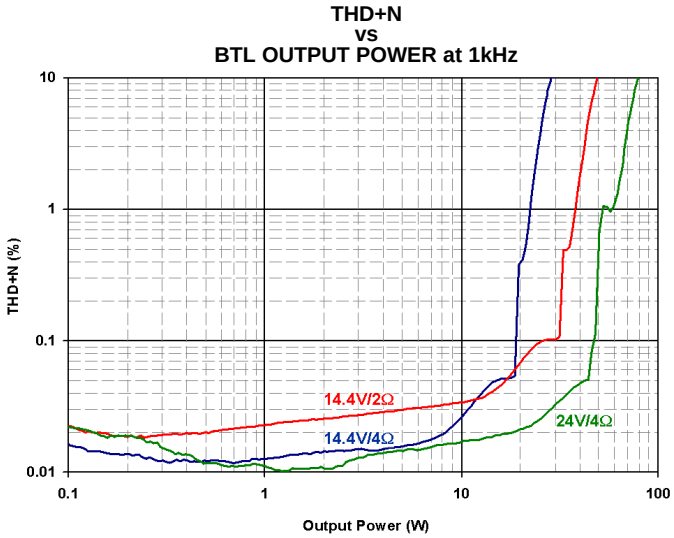


Figure 5.

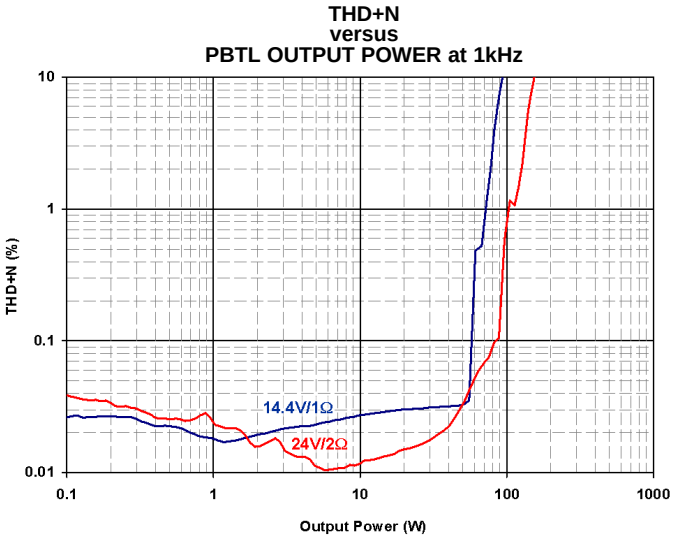


Figure 6.

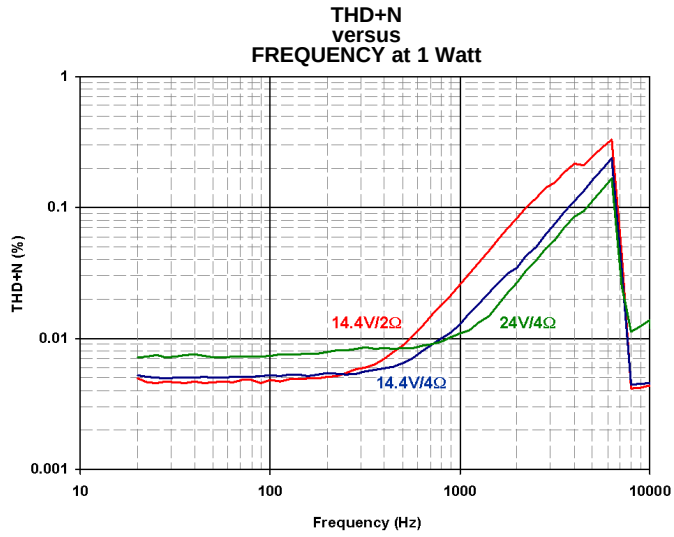


Figure 7.

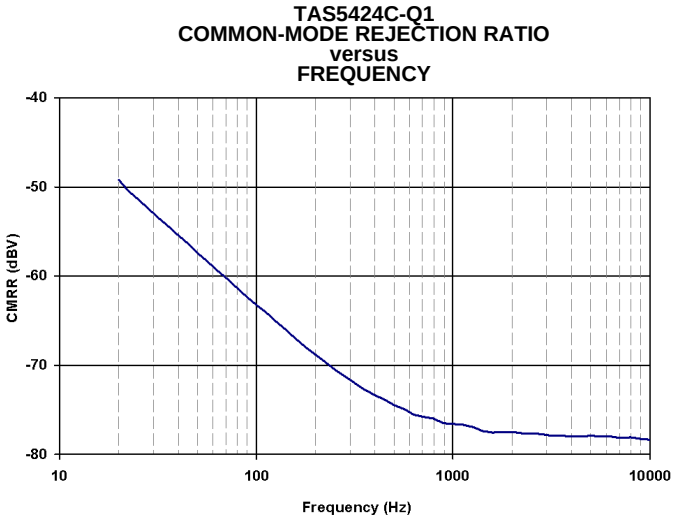


Figure 8.

TYPICAL CHARACTERISTICS (continued)

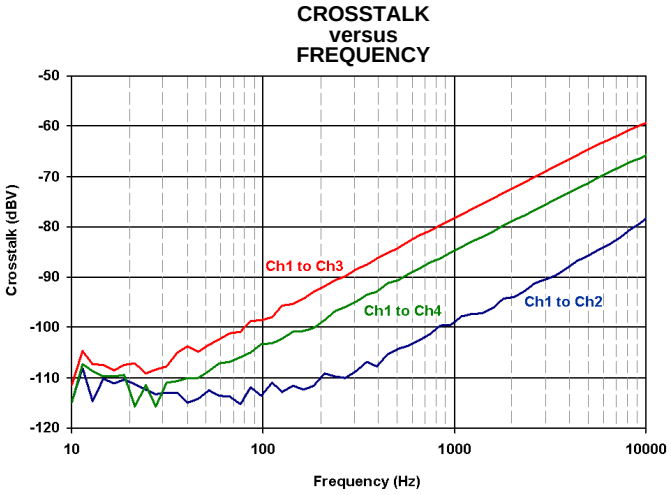


Figure 9.

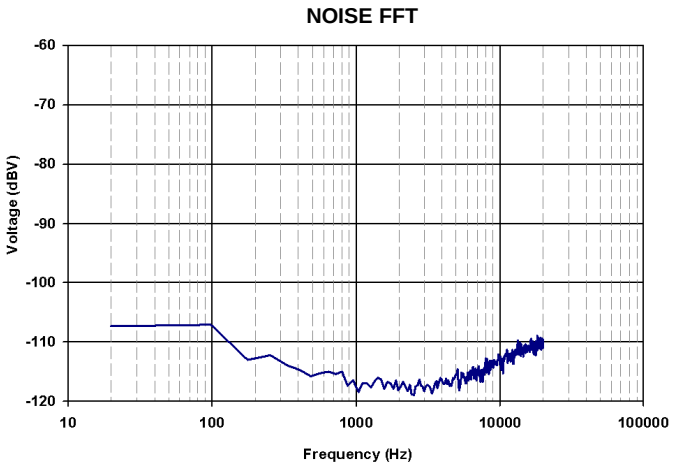


Figure 10.

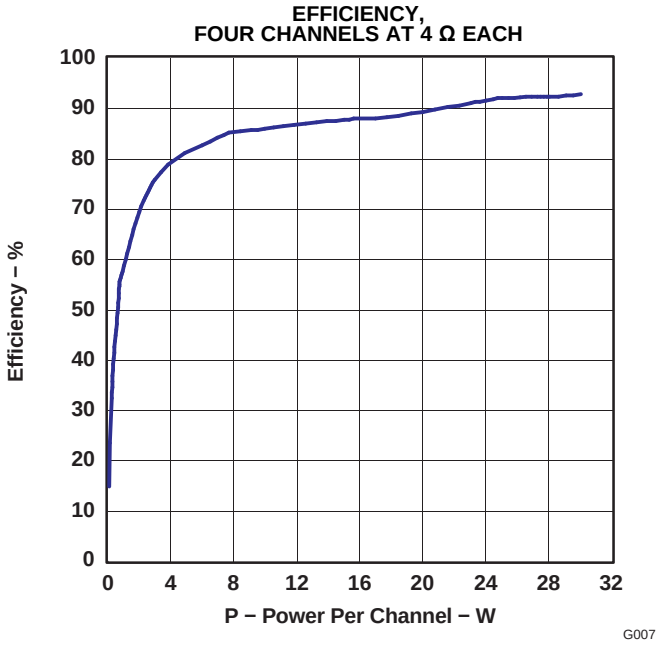


Figure 11.

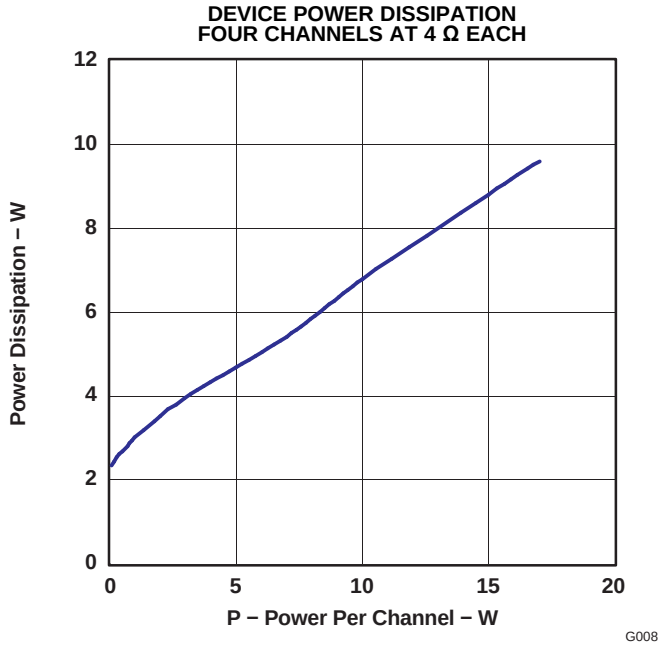


Figure 12.

DESCRIPTION OF OPERATION

OVERVIEW

The TAS5414C-Q1 and TAS5424C-Q1 are single-chip, four-channel, analog-input audio amplifiers for use in the automotive environment. The design uses an ultra-efficient class-D technology developed by Texas Instruments, but with changes needed by the automotive industry. This technology allows for reduced power consumption, reduced heat, and reduced peak currents in the electrical system. The device realizes an audio sound system design with smaller size and lower weight than traditional class-AB solutions.

There are eight core design blocks:

- Preamplifier
- PWM
- Gate drive
- Power FETs
- Diagnostics
- Protection
- Power supply
- I^2C serial communication bus

Preamplifier

The preamplifier is a high-input-impedance, low-noise, low-offset-voltage input stage with adjustable gain. The high input impedance allows the use of low-cost input capacitors while still achieving extended low-frequency response. A dedicated, internally regulated supply pwoers the preamplifier, giving it excellent noise immunity and channel separation. The preamplifier also includes:

1. **Mute Pop-and-Click Control**— The device ramps the gain gradually when ib receiving a mute or play command. The start or stopping of switching in a class-D amplifier can cause another form of click and pop. The TAS5414C-Q1 and TAS5424C-Q1 incorporate a patented method to reduce the pop energy during the switching startup and shutdown sequence. Fault conditions require rapid protection response by the TAS5414C-Q1and the TAS5424C-Q1, which do not have time to ramp the gain down in a pop-free manner. The device transitions into Hi-Z mode when encountering an OV, UV, OC, OT, or dc fault. Also, activation of the $\overline{\text{STANDBY}}$ pin may not be pop-free.
2. **Gain Control**—Setting of gains for the four channels occurs in the preamplifier via I^2C control registers, outside of the global feedback resistors of the device, thus allowing for stability of the system at all gain settings with properly loaded conditions.

Pulse-Width Modulator (PWM)

The PWM converts the analog signal from the preamplifier into a switched signal of varying duty cycle. This is the critical stage that defines the class-D architecture. In the TAS5414C-Q1 and TAS5424C-Q1, the modulator is an advanced design with high bandwidth, low noise, low distortion, excellent stability, and full 0–100% modulation capability. The patented PWM uses clipping recovery circuitry to eliminate the deep saturation characteristic of PWMs when the input signal exceeds the modulator waveform.

Gate Drive

The gate driver accepts the low-voltage PWM signal and level-shifts it to drive a high-current, full-bridge, power FET stage. The device uses proprietary techniques to optimize EMI and audio performance.

Power FETs

The BTL output for each channel comprises four rugged N-channel 30-V 65-mΩ FETs for high efficiency and maximum power transfer to the load. These FETs can handle large voltage transients during load dump.

Load Diagnostics

The device incorporates load diagnostic circuitry designed to help pinpoint the nature of output misconnections during installation. The TAS5414C-Q1 and the TAS5424C-Q1 include functions for detecting and determining the status of output connections. The devices support the following diagnostics:

- Short to GND
- Short to PVDD
- Short across load
- Open load
- Tweeter detection

Reporting to the system of the presence of any of the short or open conditions occurs via I^2C register read. One can read the tweeter-detect status from the CLIP_OTW pin when properly configured.

1. **Output Short and Open Diagnostics**—The device contains circuitry designed to detect shorts and open conditions on the outputs. Invocation of the load diagnostic function can only occur when the output is in the Hi-Z mode. There are four phases of test during load diagnostics and two levels of test. In the full level, all channels must be in the Hi-Z state. Testing covers all four phases on each channel, all four channels at the same time. When fewer than four channels are in Hi-Z, the reduced level of test is the only available option. In the reduced level, the only tests available are short to PVDD and short to GND. Load diagnostics can occur at power up before moving the amplifier out of Hi-Z mode. If the amplifier is already in play mode, it must *Mute* and then *Hi-Z* before performing the load diagnostic. By performing the mute function, the normal pop- and click-free transitions occur before the diagnostics begin. Performance of the diagnostics is as shown in Figure 13. Figure 14 shows the impedance ranges for the open-load and shorted-load diagnostics. Reading the results of the diagnostics is from the diagnostic register via I^2C for each channel. With the default settings and MUTE capacitor, the S2G and S2P phase take approximately 20 ms each, the OL phase takes approximately 100 ms, and the SL takes approximately 230 ms. In I^2C register 0x10, bit D4 can extend the test time for S2P and S2G to 80 ms each. To prevent false S2G and S2P faults, this time extension is necessary if the output pins have a capacitance higher than 680 nF to ground .

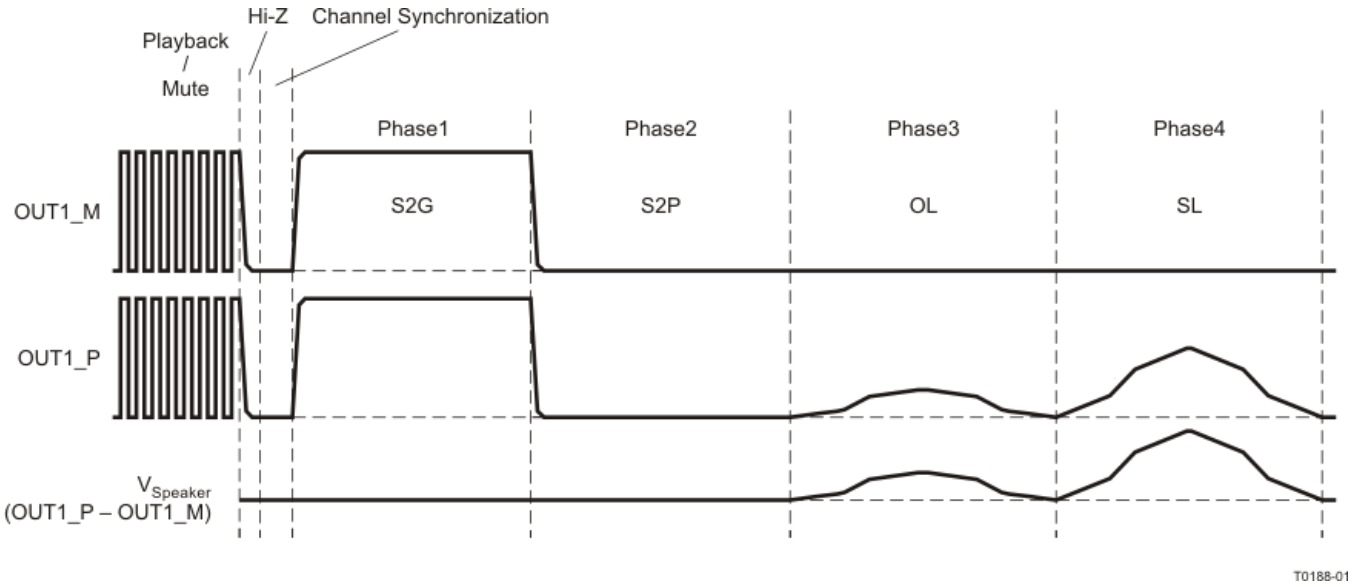


Figure 13. Load Diagnostics Sequence of Events

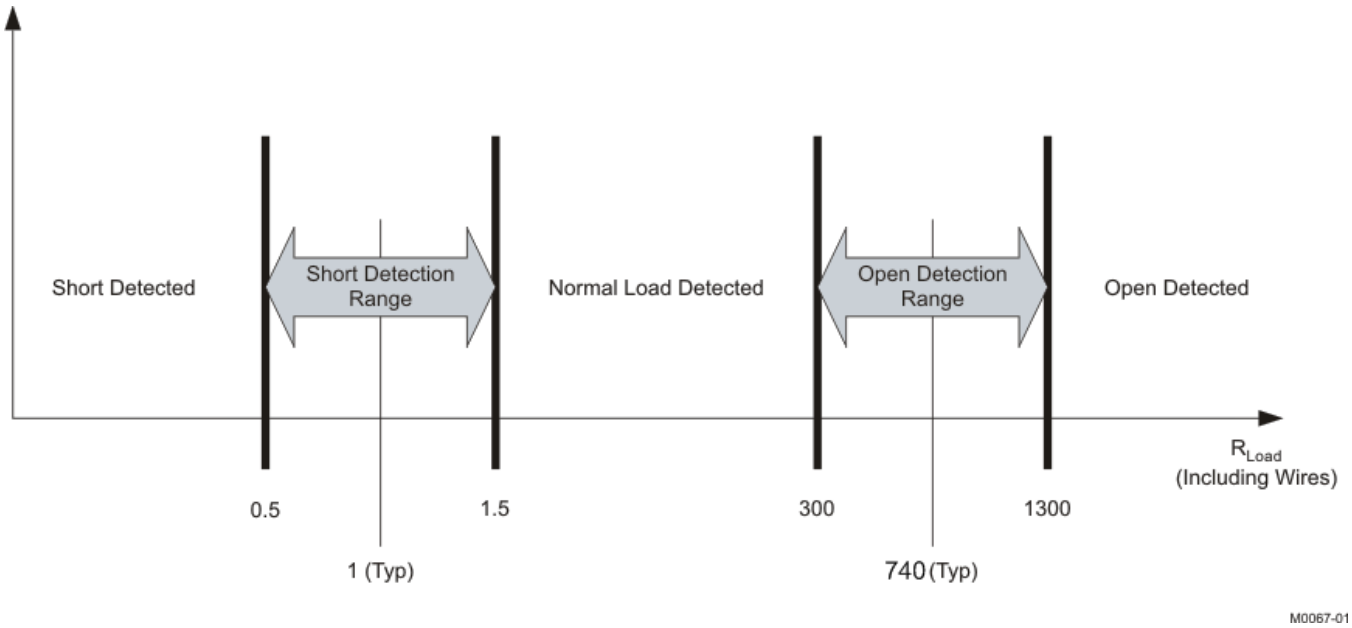


Figure 14. Open- and Shorted-Load Detection

2. **Tweeter Detection**—Tweeter detection is an alternate operating mode used to determine the proper connection of a frequency-dependent load (such as a speaker with a crossover). Invoking of weeter detection is via I^2C, with individual testing of all four channels recommended. Tweeter detection uses the average cycle-by-cycle current limit circuit (see *CBC* section) to measure the current delivered to the load. The proper implementation of this diagnostic function depends on the amplitude of a user-supplied test signal and on the impedance-versus-frequency curve of the acoustic load. The system (external to the TAS5414C-Q1 and TAS5424C-Q1) must generate a signal to which the load responds. The frequency and amplitude of this signal must be calibrated by the user to result in a current draw that is greater than the tweeter detection threshold when the load under test is present, and less than the detection threshold if the load is unconnected. The current level for the tweeter detection threshold, as well as the maximum current that can safely be delivered to a load when in tweeter-detection mode, is in the Electrical Characteristics section of the data sheet. Reporting of the tweeter-detection results is on the $\overline{\text{CLIP\_OTW}}$ pin during the application of the test signal. With tweeter detection activated (indicating that the tested load is present), pulses on the $\overline{\text{CLIP\_OTW}}$ pin begin to toggle. The pulses on the $\overline{\text{CLIP\_OTW}}$ pins report low whenever the current exceeds the detection threshold, and the pin remains low until the current no longer exceeds the threshold. The minimum low-pulse period that one can expect is equal to one period of the switching frequency. Having an input signal that increases the duration of detector activation (for example, increasing the amplitude of the input signal) increases the amount of time for which the pin reports low.
NOTE: Because tweeter detection is an alternate *operating mode*, place the channels to be tested in Play mode (via register 0x0C) after tweeter detection has been activated in order to commence the detection process. Additionally, set up the $\overline{\text{CLIP\_OTW}}$ pin via register 0x0A to report the results of tweeter detection.

Protection and Monitoring

1. **Cycle-By-Cycle Current Limit (CBC)**—The CBC current-limiting circuit terminates each PWM pulse to limit the output current flow to the average current limit (I_{LIM}) threshold. The overall effect on the audio in the case of a current overload is quite similar to a voltage-clipping event, temporarily limiting power at the peaks of the musical signal and normal operation continues without disruption on removal of the overload. The TAS5414C-Q1 and TAS5424C-Q1 do not prematurely shut down in this condition. All four channels continue in play mode and pass signal.
2. **Overcurrent Shutdown (OCSD)**—Under severe short-circuit events, such as a short to PVDD or ground, the device uses a peak-current detector, and the affected channel shuts down in 200 µs to 390 µs if the conditions are severe enough. The shutdown speed depends on a number of factors, such as the impedance of the short circuit, supply voltage, and switching frequency. Only the shorted channels shut down in such a scenario. The user may restart the affected channel via I^2C. An OCSD event activates the fault pin, and the

I²C fault register saves a record of the affected channels. If the supply or ground short is strong enough to exceed the peak current threshold but not severe enough to trigger the OCSD, the peak current limiter prevents excess current from damaging the output FETs, and operation returns to normal after the short is removed.

3. **DC Detect**—This circuit detects a dc offset at the output of the amplifier continuously during normal operation. If the dc offset reaches the level defined in the I²C registers for the specified time period, the circuit triggers. By default, a dc detection event does not shut the output down. Disabling and enabling the shutdown function is via I²C. If enabled, the triggered channel shuts down, but the others remain playing, but with the FAULT pin asserted. The I²C registers define the dc level.
4. **Clip Detect**—The clip detect circuit alerts the user to the presence of a 100% duty-cycle PWM due to a clipped waveform. When this occurs, a signal passed to the CLIP_OTW pin asserts it until the 100% duty-cycle PWM signal is no longer present. All four channels connect to the same CLIP_OTW pin. Through I²C, one can change the CLIP_OTW signal clip-only, OTW-only, or both. A fourth mode, used only during diagnostics, is the option to report tweeter detection events on this pin (see the *Tweeter Detection* section). The microcontroller in the system can monitor the signal at the CLIP_OTW pin, and may have a configuration that reduces the volume to all four channels in an active clipping-prevention circuit.
5. **Overtemperature Warning (OTW), Overtemperature Shutdown (OTSD) and Thermal Foldback**—By default, the CLIP_OTW pin setting indicates an OTW. One can make changes via I²C commands. If selected to indicate a temperature warning, CLIP_OTW pin assertion occurs when the die temperature reaches warning level 1 as shown in the electrical specifications. The OTW has three temperature thresholds with a 10°C hysteresis. I²C register 0x04 indicates each threshold in bits 5, 6, and 7. The device still functions until the temperature reaches the OTSD threshold, at which time the outputs go into Hi-Z mode and the device asserts the FAULT pin. I²C is still active in the event of an OTSD, and one can read the registers for faults, but all audio ceases abruptly. After the OTSD resets, one can turn the device back on through I²C. The OTW indication remains until the temperature drops below warning level 1. The thermal foldback decreases the channel gain.
6. **Undervoltage (UV) and Power-on-Reset (POR)**—The undervoltage (UV) protection detects low voltages on PVDD, AVDD, and CP. In the event of an undervoltage, the device asserts the FAULT pin and updates the I²C registerd, depending on which voltage caused the event. Power-on reset (POR) occurs when PVDD drops low enough. A POR event causes the I²C to go into a high-impedance state. After the device recovers from the POR event, the device re-initialization occur via I²C.
7. **Overvoltage (OV) and Load Dump**—The OV protection detects high voltages on PVDD. If PVDD reaches the overvoltage threshold, the device asserts the FAULT pin iand updates the I²C register. The device can withstand 50-V load-dump voltage spikes.

Power Supply

A car battery that can have a large voltage range most commonly provides the power for the device. PVDD is a filtered battery voltage, and it is the supply for the output FETS and the low-side FET gate driver. The supply for the high-side FET gate driver comes from a charge pump (CP). The charge pump supplies the gate-drive voltage for all four channels. AVDD, provided by an internal linear regulator powers the analog circuitry. This supply requires 0.1-µF, 10-V external bypass capacitor at the A_BYP pin. TI recommends not connecting any external components except the bypass capacitor to this pin. DVDD, which comes from an internal linear regulator, powers the digital circuitry. The D_BYP pin requires a 0.1-µF, 10-V external bypass capacitor. TI recommends not connecting any external components except the bypass capacitor to this pin.

The TAS5414C-Q1 and TAS5424C-Q1 can withstand fortuitous open-ground and -power conditions. Fortuitous open ground usually occurs when a speaker wire shorts to ground, allowing for a second ground path through the body diode in the output FETs. The diagnostic capability allows debugging of the speakers and speaker wires, eliminating the need to remove the amplifier to diagnose the problem.

I²C Serial Communication Bus

The device communicates with the system processor via the I²C serial communication bus as an I²C slave-only device. The processor can poll the device via I²C to determine the operating status. All reports of fault conditions and detections are via I²C. There are also numerous features and operating conditions that one can set via I²C.

The I²C bus allows control of the following configurations:

- Independent gain control of each channel. The gain can be set to 12 dB, 20 dB, 26 dB, and 32 dB.

- Select the AM non-interference switching frequency
- Select the functionality of the OTW_CLIP pin
- Enable or disable the dc-detect function with selectable threshold
- Place a channel in Hi-Z (switching stopped) mode (mute)
- Select tweeter detect, set the detection threshold, and initiate the function
- Initiate the open- and shorted-load diagnostic
- Reset faults and return to normal switching operation from Hi-Z mode (unmute)

In addition to the standard SDA and SCL pins for the I^2C bus, the TAS5414C-Q1 and the TAS5424C-Q1 include a single pin that allows up to four devices to work together in a system with no additional hardware required for communication or synchronization. The I2C_ADDR pin sets the device in master or slave mode and selects the I^2C address for that device. Tie I2C_ADDR to DGND for master, to 1.2 Vdc for slave 1, to 2.4 Vdc for slave 2, and to D_BYP for slave 3. The OSC_SYNC pin is for synchronizing the internal clock oscillators, thereby avoid beat frequencies. One can apply an external oscillator to this pin for external control of the switching frequency.

Table 2. Table 7. I2C_ADDR Pin Connection

I2C_ADDR VALUE	I2C_ADDR PIN CONNECTION	I^2C ADDRESSES
0 (OSC MASTER)	To SGND pin	0xD8/D9
1 (OSC SLAVE1)	35% DVDD (resistive voltage divider between D_BYP pin and SGND pin)(1)	0xDA/DB
2 (OSC SLAVE2)	65% DVDD (resistive voltage divider between D_BYP pin and SGND pin)(1)	0xDC/DD
3 (OSC SLAVE3)	To D_BYP pin	0xDE/DF

(1) TI recommends R_{I2C_ADDR} resistors with 5% or better tolerance.

I^2C Bus Protocol

The TAS5414C-Q1 and TAS5424C-Q1 have a bidirectional serial control interface that is compatible with the Inter IC (I^2C) bus protocol and supports 400-kbps data transfer rates for random and sequential write and read operations. This is a slave-only device that does not support a multimaster bus environment or wait-state insertion. The control interface programs the registers of the device and reads device status.

The I^2C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data transfer on the bus is serial, one bit at a time. The transfer of address and data is in byte (8-bit) format with the most-significant bit (MSB) transferred first. In addition, the receiving device acknowledges each byte transferred on the bus with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is HIGH to indicate a start and stop conditions. A HIGH-to-LOW transition on SDA indicates a start, and a LOW-to-HIGH transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. Figure 15 shows these conditions. The master generates the 7-bit slave address and the read/write bit to open communication with another device and then wait for an acknowledge condition. The TAS5414C-Q1 and TAS5424C-Q1 hold SDA LOW during the acknowledge-clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/$\overline{W}$ bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. There must be an external pullup resistor for the SDA and SCL signals to set the HIGH level for the bus. There is no limit on the number of bytes that one can transmit between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus.

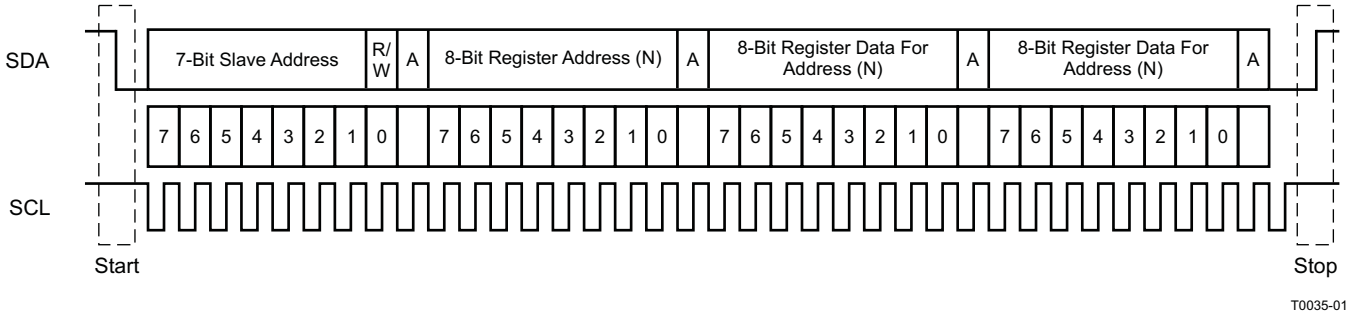


Figure 15. Typical I²C Sequence

Use the I2C_ADDR pin (pin 2) to program the device for one of four addresses. These four addresses are licensed I²C addresses and do not conflict with other licensed I²C audio devices. To communicate with the TAS5414C-Q1 and the TAS5424C-Q1, the I²C master uses addresses shown in Figure 15. Transmission of read and write data can be via single-byte or multiple-byte data transfers.

Random Write

As shown in Figure 16, a random write or single-byte write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a single-byte write data transfer, the read/write bit is a 0. After receiving the correct I²C device address and the read/write bit, the device responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the internal memory address being accessed. After receiving the address byte, the device again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5414C-Q1 or TAS5424C-Q1 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte write transfer.

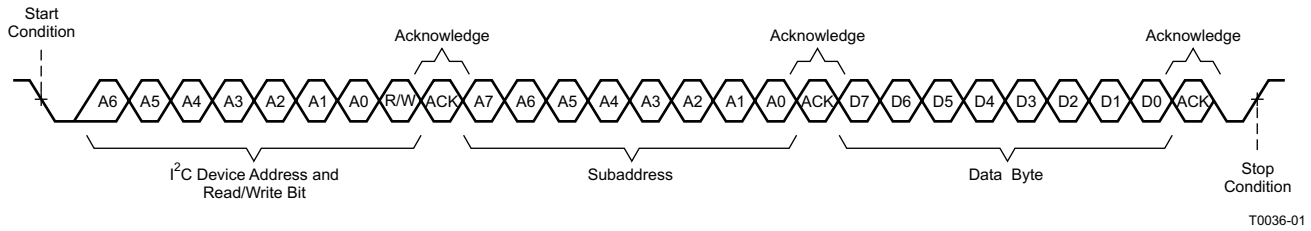


Figure 16. Random-Write Transfer

Sequential Write

A sequential write transfer is identical to a single-byte data-write transfer except for the transmisson of multiple data bytes by the master device to TAS5414C-Q1 or TAS5424C-Q1 as shown in Figure 17. After receiving each data byte, the device responds with an acknowledge bit and automatically increments the I²C subaddress by one.

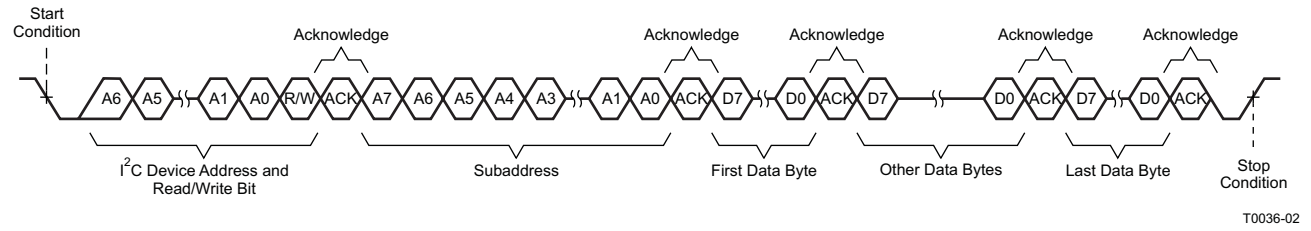


Figure 17. Sequential Write Transfer

Random Read

As shown in Figure 18, a random read or single-byte read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. For the single-byte read transfer, the master device transmits both a write followed by a read. Initially, a write transfers the address byte or bytes of the internal memory address to be read. Thus, the read/write bit is a 0. After receiving the address and the read/write bit, the TAS5414C-Q1 or TAS5424C-Q1 responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the device address and the read/write bit again. This time the read/write bit is a 1, indicating a read transfer. After receiving the address and the read/write bit, the device again responds with an acknowledge bit. Next, the TAS5414C-Q1 or TAS5424C-Q1 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte read transfer.

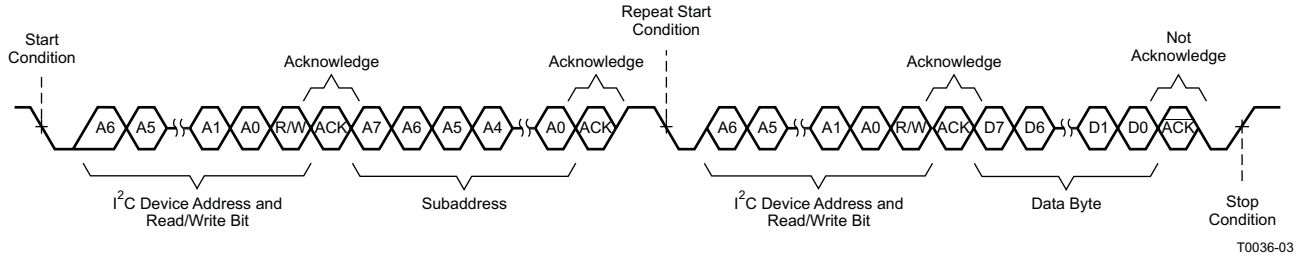


Figure 18. Random Read Transfer

Sequential Read

A sequential read transfer is identical to a single-byte read transfer except for the transmission of multiple data bytes by the TAS5414C-Q1 or TAS5424C-Q1 to the master device as shown in Figure 19. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte and automatically increments the I²C subaddress by one. After receiving the last data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the transfer.

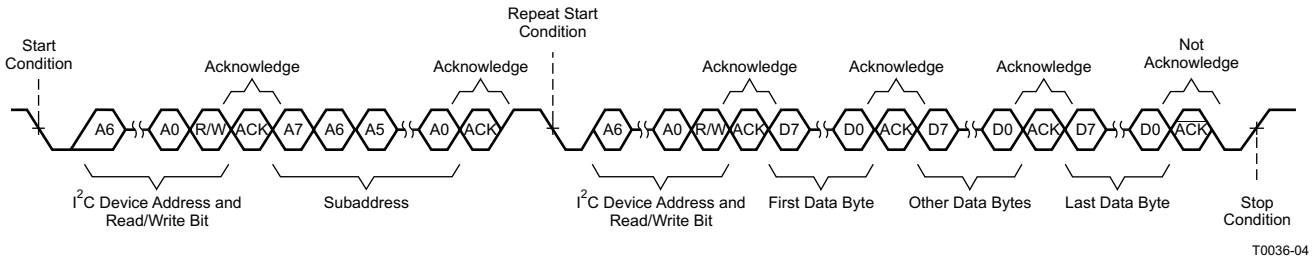


Figure 19. Sequential Read Transfer

Table 3. TAS5414C-Q1 and TAS5424C-Q1 I²C Addresses

I2C_ADDR VALUE		FIXED ADDRESS					SELECTABLE WITH ADDRESS PIN		READ/WRITE BIT	I²C ADDRESS
		MSB	6	5	4	3	2	1	LSB	
0 (OSC MASTER)	I²C WRITE	1	1	0	1	1	0	0	0	0xD8
	I²C READ	1	1	0	1	1	0	0	1	0xD9
1 (OSC SLAVE1)	I²C WRITE	1	1	0	1	1	0	1	0	0xDA
	I²C READ	1	1	0	1	1	0	1	1	0xDB
2 (OSC SLAVE2)	I²C WRITE	1	1	0	1	1	1	0	0	0xDC
	I²C READ	1	1	0	1	1	1	0	1	0xDD
3 (OSC SLAVE3)	I²C WRITE	1	1	0	1	1	1	1	0	0xDE
	I²C READ	1	1	0	1	1	1	1	1	0xDF

Table 4. I²C Address Register Definitions

ADDRESS	TYPE	REGISTER DESCRIPTION
0x00	Read	Latched fault register 1, global and channel fault
0x01	Read	Latched fault register 2, dc offset and overcurrent detect
0x02	Read	Latched diagnostic register 1, load diagnostics
0x03	Read	Latched diagnostic register 2, load diagnostics
0x04	Read	External status register 1, temperature and voltage detect
0x05	Read	External status register 2, Hi-Z and low-low state
0x06	Read	External status register 3, mute and play modes
0x07	Read	External status register 4, load diagnostics
0x08	Read, Write	External control register 1, channel gain select
0x09	Read, Write	External control register 2, overcurrent control
0x0A	Read, Write	External control register 3, switching frequency and clip pin select
0x0B	Read, Write	External control register 4, load diagnostic, master mode select
0x0C	Read, Write	External control register 5, output state control
0x0D	Read, Write	External control register 6, output state control
0x0E, 0x0F	–	Not used
0x10	Read, Write	External control register 7, dc detect threshold selection
0x13	Read	External status register 5, overtemperature shutdown and thermal foldback

Table 5. Fault Register 1 (0x00) Protection

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No protection-created faults, default value
–	–	–	–	–	–	–	1	Overtemperature warning has occurred.
–	–	–	–	–	–	1	–	DC offset has occurred in any channel.
–	–	–	–	–	1	–	–	Overcurrent shutdown has occurred in any channel.
–	–	–	–	1	–	–	–	Overtemperature shutdown has occurred.
–	–	–	1	–	–	–	–	Charge-pump undervoltage has occurred.
–	–	1	–	–	–	–	–	AVDD, analog voltage, undervoltage has occurred.
–	1	–	–	–	–	–	–	PVDD undervoltage has occurred.
1	–	–	–	–	–	–	–	PVDD overvoltage has occurred.

Table 6. Fault Register 2 (0x01) Protection

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No protection-created faults, default value
–	–	–	–	–	–	–	1	Overcurrent shutdown channel 1 has occurred.

Table 6. Fault Register 2 (0x01) Protection (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	–	–	–	1	–	Overcurrent shutdown channel 2 has occurred.
–	–	–	–	–	1	–	–	Overcurrent shutdown channel 3 has occurred.
–	–	–	–	1	–	–	–	Overcurrent shutdown channel 4 has occurred.
–	–	–	1	–	–	–	–	DC offset channel 1 has occurred.
–	–	1	–	–	–	–	–	DC offset channel 2 has occurred.
–	1	–	–	–	–	–	–	DC offset channel 3 has occurred.
1	–	–	–	–	–	–	–	DC offset channel 4 has occurred.

Table 7. Diagnostic Register 1 (0x02) Load Diagnostics

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No load-diagnostic-created faults, default value
–	–	–	–	–	–	–	1	Output short to ground channel 1 has occurred.
–	–	–	–	–	–	1	–	Output short to PVDD channel 1 has occurred.
–	–	–	–	–	1	–	–	Shorted load channel 1 has occurred.
–	–	–	–	1	–	–	–	Open load channel 1 has occurred.
–	–	–	1	–	–	–	–	Output short to ground channel 2 has occurred.
–	–	1	–	–	–	–	–	Output short to PVDD channel 2 has occurred.
–	1	–	–	–	–	–	–	Shorted load channel 2 has occurred.
1	–	–	–	–	–	–	–	Open load channel 2 has occurred.

Table 8. Diagnostic Register 2 (0x03) Load Diagnostics

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No load-diagnostic-created faults, default value
–	–	–	–	–	–	–	1	Output short to ground channel 3 has occurred.
–	–	–	–	–	–	1	–	Output short to PVDD channel 3 has occurred.
–	–	–	–	–	1	–	–	Shorted load channel 3 has occurred.
–	–	–	–	1	–	–	–	Open load channel 3 has occurred.
–	–	–	1	–	–	–	–	Output short to ground channel 4 has occurred.
–	–	1	–	–	–	–	–	Output short to PVDD channel 4 has occurred.
–	1	–	–	–	–	–	–	Shorted load channel 4 has occurred.
1	–	–	–	–	–	–	–	Open load channel 4 has occurred.

Table 9. External Status Register 1 (0x04) Fault Detection

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No protection-created faults are present, default value.
–	–	–	–	–	–	–	1	PVDD overvoltage fault is present.
–	–	–	–	–	–	1	–	PVDD undervoltage fault is present.
–	–	–	–	–	1	–	–	AVDD, analog voltage fault is present.
–	–	–	–	1	–	–	–	Charge-pump voltage fault is present.
–	–	–	1	–	–	–	–	Overtemperature shutdown is present.
0	0	1	–	–	–	–	–	Overtemperature warning
0	1	1	–	–	–	–	–	Overtemperature warning level 1
1	0	1	–	–	–	–	–	Overtemperature warning level 2
1	1	1	–	–	–	–	–	Overtemperature warning level 3

Table 10. External Status Register 2 (0x05) Output State of Individual Channels

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	1	1	1	1	Output is in Hi-Z mode, not in low-low mode(1), default value.
–	–	–	–	–	–	–	0	Channel 1 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)
–	–	–	–	–	–	0	–	Channel 2 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)
–	–	–	–	–	0	–	–	Channel 3 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)
–	–	–	–	0	–	–	–	Channel 4 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)
–	–	–	1	–	–	–	–	Channel 1 low-low mode (0 = not low-low, 1 = low-low)(1)
–	–	1	–	–	–	–	–	Channel 2 low-low mode (0 = not low-low, 1 = low-low)(1)
–	1	–	–	–	–	–	–	Channel 3 low-low mode (0 = not low-low, 1 = low-low)(1)
1	–	–	–	–	–	–	–	Channel 4 low-low mode (0 = not low-low, 1 = low-low)(1)

(1) *Low-low* is defined as both outputs actively pulled to ground.

Table 11. External Status Register 3 (0x06) Play and Mute Modes

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	Mute mode is disabled, play mode disabled, default value, (Hi-Z mode).
–	–	–	–	–	–	–	1	Channel 1 play mode is enabled.
–	–	–	–	–	–	1	–	Channel 2 play mode is enabled.
–	–	–	–	–	1	–	–	Channel 3 play mode is enabled.
–	–	–	–	1	–	–	–	Channel 4 play mode is enabled.
–	–	–	1	–	–	–	–	Channel 1 mute mode is enabled.
–	–	1	–	–	–	–	–	Channel 2 mute mode is enabled.
–	1	–	–	–	–	–	–	Channel 3 mute mode is enabled.
1	–	–	–	–	–	–	–	Channel 4 mute mode is enabled.

Table 12. External Status Register 4 (0x07) Load Diagnostics

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No channels are set in load diagnostics mode, default value.
–	–	–	–	–	–	–	1	Channel 1 is in load diagnostics mode.
–	–	–	–	–	–	1	–	Channel 2 is in load diagnostics mode.
–	–	–	–	–	1	–	–	Channel 3 is in load diagnostics mode.
–	–	–	–	1	–	–	–	Channel 4 is in load diagnostics mode.
–	–	–	1	–	–	–	–	Channel 1 is in overtemperature foldback.
–	–	1	–	–	–	–	–	Channel 2 is in overtemperature foldback.
–	1	–	–	–	–	–	–	Channel 3 is in overtemperature foldback.
1	–	–	–	–	–	–	–	Channel 4 is in overtemperature foldback.

Table 13. External Control Register 1 (0x08) Gain Select

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	0	1	0	1	0	1	0	Set gain for all channels to 26 dB, default value.
–	–	–	–	–	–	0	0	Set channel 1 gain to 12 dB.
–	–	–	–	–	–	0	1	Set channel 1 gain to 20 dB.
–	–	–	–	–	–	1	1	Set channel 1 gain to 32 dB.
–	–	–	–	0	0	–	–	Set channel 2 gain to 12 dB.
–	–	–	–	0	1	–	–	Set channel 2 gain to 20 dB.
–	–	–	–	1	1	–	–	Set channel 2 gain to 32 dB.
–	–	0	0	–	–	–	–	Set channel 3 gain to 12 dB.
–	–	0	1	–	–	–	–	Set channel 3 gain to 20 dB.
–	–	1	1	–	–	–	–	Set channel 3 gain to 32 dB.

Table 13. External Control Register 1 (0x08) Gain Select (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	–	–	–	–	–	–	Set channel 4 gain to 12 dB.
0	1	–	–	–	–	–	–	Set channel 4 gain to 20 dB.
1	1	–	–	–	–	–	–	Set channel 4 gain to 32 dB.

Table 14. External Control Register 2 (0x09) Overcurrent Control

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	1	1	1	0	0	0	0	Current limit level 2 for all channels, thermal foldback is active.
–	–	–	–	–	–	–	1	Disable thermal foldback
–	–	–	0	–	–	–	–	Set channel 1 overcurrent limit (0 - level 1, 1 - level 2)
–	–	0	–	–	–	–	–	Set channel 2 overcurrent limit (0 - level 1, 1 - level 2)
–	0	–	–	–	–	–	–	Set channel 3 overcurrent limit (0 - level 1, 1 - level 2)
0	–	–	–	–	–	–	–	Set channel 4 overcurrent limit (0 - level 1, 1 - level 2)
–	–	–	–	1	1	1	–	Reserved

Table 15. External Control Register 3 (0x0A) Switching Frequency Select and Clip_OTW Configuration

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	1	1	0	1	Set f_S = 417 kHz, report clip and OTW, 45° phase, disable hard stop, CLIP_OTW pin does not report thermal foldback.
–	–	–	–	–	–	0	0	Set f_S = 500 kHz
–	–	–	–	–	–	1	0	Set f_S = 357 kHz
–	–	–	–	–	–	1	1	Invalid frequency selection (do not set)
–	–	–	–	0	0	–	–	Configure $\overline{\text{CLIP\_OTW}}$ pin to report tweeter detect only.
–	–	–	–	0	1	–	–	Configure $\overline{\text{CLIP\_OTW}}$ pin to report clip detect only.
–	–	–	–	1	0	–	–	Configure $\overline{\text{CLIP\_OTW}}$ pin to report overtemperature warning only.
–	–	–	1	–	–	–	–	Enable hard-stop mode.
–	–	1	–	–	–	–	–	Set f_S to a 180° phase difference between adjacent channels.
–	1	–	–	–	–	–	–	Send sync pulse from OSC_SYNC pin (device must be in master mode).
1	–	–	–	1	–	–	–	Configure $\overline{\text{CLIP\_OTW}}$ pin to report thermal foldback

Table 16. External Control Register 4 (0x0B) Load Diagnostics and Master/Slave Control

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	1	0	1	0	0	0	0	Clock output disabled, master clock mode, dc detection enabled, load diagnostics disabled
–	–	–	–	–	–	–	1	Run channel 1 load diagnostics
–	–	–	–	–	–	1	–	Run channel 2 load diagnostics
–	–	–	–	–	1	–	–	Run channel 3 load diagnostics
–	–	–	–	1	–	–	–	Run channel 4 load diagnostics
–	–	–	0	–	–	–	–	Disable dc detection on all channels
–	–	1	–	–	–	–	–	Enable tweeter-detect mode
–	0	–	–	–	–	–	–	Enable slave mode (external oscillator is necessary)
1	–	–	–	–	–	–	–	Enable clock output on OSC_SYNC pin (valid only in master mode)

Table 17. External Control Register 5 (0x0C) Output Control

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	1	1	1	1	1	All channels, Hi-Z, mute, reset disabled, dc detect is enabled
–	–	–	–	–	–	–	0	Set channel 1 to mute mode, non-Hi-Z
–	–	–	–	–	–	0	–	Set channel 2 to mute mode, non-Hi-Z

Table 17. External Control Register 5 (0x0C) Output Control (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	–	–	0	–	–	Set channel 3 to mute mode, non-Hi-Z
–	–	–	–	0	–	–	–	Set channel 4 to mute mode, non-Hi-Z
–	–	–	0	–	–	–	–	Set non-Hi-Z channels to play mode, (unmute)
–	–	1	–	–	–	–	–	DC detect shutdown disabled, but still reports a fault
–	1	–	–	–	–	–	–	Reserved
1	–	–	–	–	–	–	–	Reset device

Table 18. External Control Register 6 (0x0D) Output Control

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	Low-low state disabled, all channels
–	–	–	–	–	–	–	1	Set channel 1 to low-low state
–	–	–	–	–	–	1	–	Set channel 2 to low-low state
–	–	–	–	–	1	–	–	Set channel 3 to low-low state
–	–	–	–	1	–	–	–	Set channel 4 to low-low state
–	–	–	1	–	–	–	–	Connect channel 1 and channel 2 for parallel BTL mode
–	–	1	–	–	–	–	–	Connect channel 3 and channel 4 for parallel BTL mode
1	1	–	–	–	–	–	–	Reserved

Table 19. External Control Register 7 (0x10) Miscellaneous Selection

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	1	Normal speed CM ramp, normal S2P & S2G timing, no delay between LDG phases, Crosstalk Enhancement Disabled, Default DC detect value (1.6V)
–	–	–	–	–	–	0	0	Minimum DC detect value (0.8 V)
–	–	–	–	–	–	1	0	Maximum DC detect value (2.4 V)
–	–	–	–	–	1	–	–	Enable crosstalk enhancement
–	–	–	–	1	–	–	–	Adds a 20-ms delay between load diagnostic phases
–	–	–	1	–	–	–	–	Short-to-power (S2P) and short-to-ground (S2G) load-diagnostic phases take 4x longer
–	–	1	–	–	–	–	–	Slow common-mode ramp, increase the default time by 3x
–	1	–	–	–	–	–	–	Reserved
1	–	–	–	–	–	–	–	Slower common-mode (CM) ramp-down from mute mode

Table 20. External Status Register 5 (0x13) Overtemperature and Thermal Foldback Status

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	Default overtemperature foldback status, no channel is in foldback
–	–	–	–	–	–	–	1	Channel 1 in thermal foldback
–	–	–	–	–	–	1	–	Channel 2 in thermal foldback
–	–	–	–	–	1	–	–	Channel 3 in thermal foldback
–	–	–	–	1	–	–	–	Channel 4 in thermal foldback
–	–	–	1	–	–	–	–	Channel 1 in overtemperature shutdown
–	–	1	–	–	–	–	–	Channel 2 in overtemperature shutdown
–	1	–	–	–	–	–	–	Channel 3 in overtemperature shutdown
1	–	–	–	–	–	–	–	Channel 4 in overtemperature shutdown

Hardware Control Pins

There are four discrete hardware pins for real-time control and indication of device status.

$\overline{\text{FAULT}}$ pin: This active-low open-drain output pin indicates the presence of a fault condition that requires the device to go into the Hi-Z mode or standby mode. On assertion of this pin, the device has protected itself and the system from potential damage. One can read the exact nature of the fault via I^2C with the exception of PVDD undervoltage faults below POR, in which case the I^2C bus is no longer operational. However, the fault is still indicated due to $\overline{\text{FAULT}}$ pin assertion.

$\overline{\text{CLIP\_OTW}}$ pin: Configured via I^2C, this active-low open-drain pin\ indicates one of the following conditions: overtemperature warning, the detection of clipping, or the logical OR of both of these conditions. During tweeter detect diagnostics, assertion of this pin also occurs when a tweeter is present. If overtemperature warning is set, the device can indicate thermal foldback on this pin too.

$\overline{\text{MUTE}}$ pin: This active-low pin is used for hardware control of the mute-unmute function for all four channels. Capacitor C_{MUTE} controls the time constant for the gain ramp needed to produce a pop- and click-free mute function. For pop- and click-free operation, implementation of the mute function should be through I^2C commands. The use of a hard mute with an external transistor does not ensure pop- and click-free operation, and TI does not recommended it except as an *emergency hard mute* function in case of a loss of I^2C control. Sharing the C_{MUTE} capacitor between multiple devices is disallowed.

$\overline{\text{STANDBY}}$ pin: On assertion of this active-low pin, the device goes into a complete shutdown, and the typical current-draw limit is 2 µA, typical. $\overline{\text{STANDBY}}$ can be used to shut down the device rapidly. If all channels are in Hi-Z, the device enters standby in approximately 1 ms; if, not a quick ramp-down occurs that takes approximately 20 ms. The outputs ramp down quickly if not already in Hi-Z, so externally biasing the $\overline{\text{MUTE}}$ pin prevents the device from entering standby. All I^2C register content is lost and the I^2C bus goes into the high-impedance state on assertion of the $\overline{\text{STANDBY}}$ pin.

EMI Considerations

Automotive-level EMI performance depends on both careful integrated circuit design and good system-level design. Controlling sources of electromagnetic interference (EMI) was a major consideration in all aspects of the design.

The design has minimal parasitic inductances due to the short leads on the package. This dramatically reduces the EMI that results from current passing from the die to the system PCB. Each channel also operates at a different phase. The phase between channels is I^2C selectable to either 45° or 180°, to reduce EMI caused by high-current switching. The design also incorporates circuitry that optimizes output transitions that cause EMI.

AM Radio Avoidance

To reduce interference in the AM radio band, the device has the ability to change the switching frequency via I^2C commands. Table 21 lists the recommended frequencies. The fundamental frequency and its second harmonic straddle the AM radio band listed. This eliminates the tones that can be present due to demodulation of the switching frequency by the AM radio.

Table 21. Recommended Switching Frequencies for AM Mode Operation

US		EUROPEAN	
AM FREQUENCY (kHz)	SWITCHING FREQUENCY (kHz)	AM FREQUENCY (kHz)	SWITCHING FREQUENCY (kHz)
540–670	417	522–675	417
680–980	500	676–945	500
990–1180	417	946–1188	417
1190–1420	500	1189–1422	500
1430–1580	417	1423–1584	417
1590–1700	500	1585–1701	500

Operating Modes and Faults

The following tables depict the operating modes and faults.

Table 22. Operating Modes

STATE NAME	OUTPUT FETS	CHARGE PUMP	OSCILLATOR	I^2C	AVDD and DVDD
STANDBY	Hi-Z, floating	Stopped	Stopped	Stopped	OFF
Hi-Z	Hi-Z, weak pulldown	Active	Active	Active	ON
Mute	Switching at 50%	Active	Active	Active	ON
Normal operation	Switching with audio	Active	Active	Active	ON

Table 23. Global Faults and Actions

FAULT OR EVENT	FAULT OR EVENT CATEGORY	MONITORING MODES	REPORTING METHOD	ACTION TYPE	ACTION RESULT	LATCHED OR SELF-CLEARING
POR	Voltage fault	All	$\overline{\text{FAULT}}$ pin	Hard mute (no ramp)	Standby	Self-clearing
UV		Hi-Z, mute, normal	I^2C + $\overline{\text{FAULT}}$ pin		Hi-Z	Latched
CP UV						
OV						
Load dump		All	$\overline{\text{FAULT}}$ pin		Standby	Self-clearing
OTW	Thermal warning	Hi-Z, mute, normal	I^2C + $\overline{\text{CLIP\_OTW}}$ pin	None	None	Self-clearing
OTSD	Thermal fault	Hi-Z, mute, normal	I^2C + $\overline{\text{FAULT}}$ pin	Hard mute (no ramp)	Standby	Latched

Table 24. Channel Faults and Actions

FAULT/ EVENT	FAULT OR EVENT CATEGORY	MONITORING MODES	REPORTING METHOD	ACTION TYPE	ACTION RESULT	LATCHED OR SELF-CLEARING
Open-short diagnostic	Diagnostic	Hi-Z (I^2C activated)	I^2C	None	None	Latched
Clipping	Warning	Mute / Play	$\overline{\text{CLIP\_OTW}}$ pin	None	None	Self-clearing
CBC load current limit	Online protection			Current Limit	Start OC timer	Self-clearing
OC fault	Output channel fault		I^2C + $\overline{\text{FAULT}}$ pin	Hard mute	Hi-Z	Latched
DC detect				Hard mute	Hi-Z	Latched
OT Foldback	Warning		I^2C + $\overline{\text{CLIP\_OTW}}$ pin	Reduce Gain	None	Self-clearing

Audio Shutdown and Restart Sequence

The gain ramp of the filtered output signal and the updating of the I^2C registers correspond to the MUTE pin voltage during the ramping process. The value of the external capacitor on the MUTE pin dictates the length of time that the MUTE pin takes to complete its ramp. With the default 220-nF capacitor, the turnon common-mode ramp takes approximately 26 ms and the gain ramp takes approximately 76 ms.

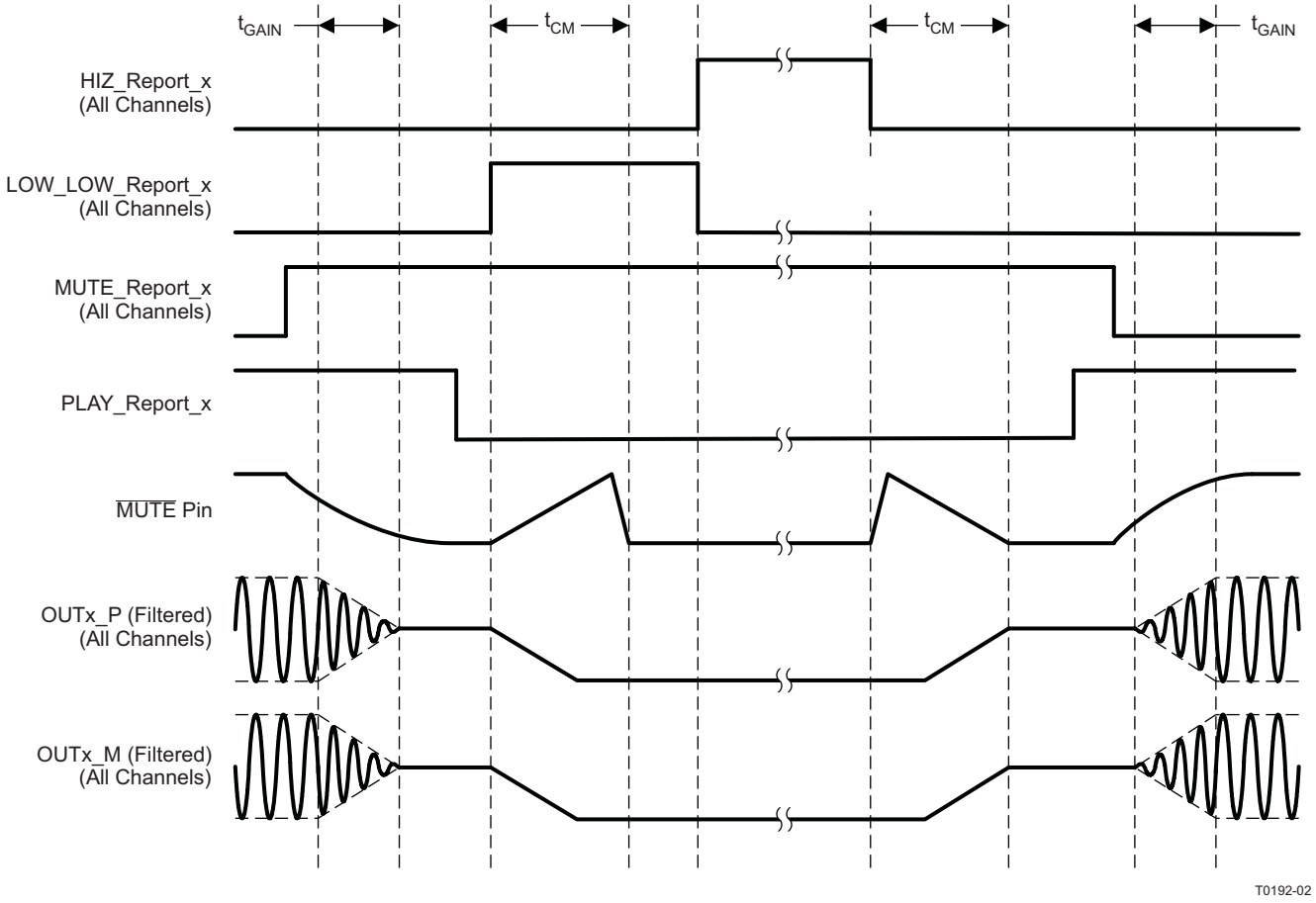


Figure 20. Timing Diagram for Click- and Pop-Free Shutdown and Restart Sequence

Latched-Fault Shutdown and Restart Sequence Control

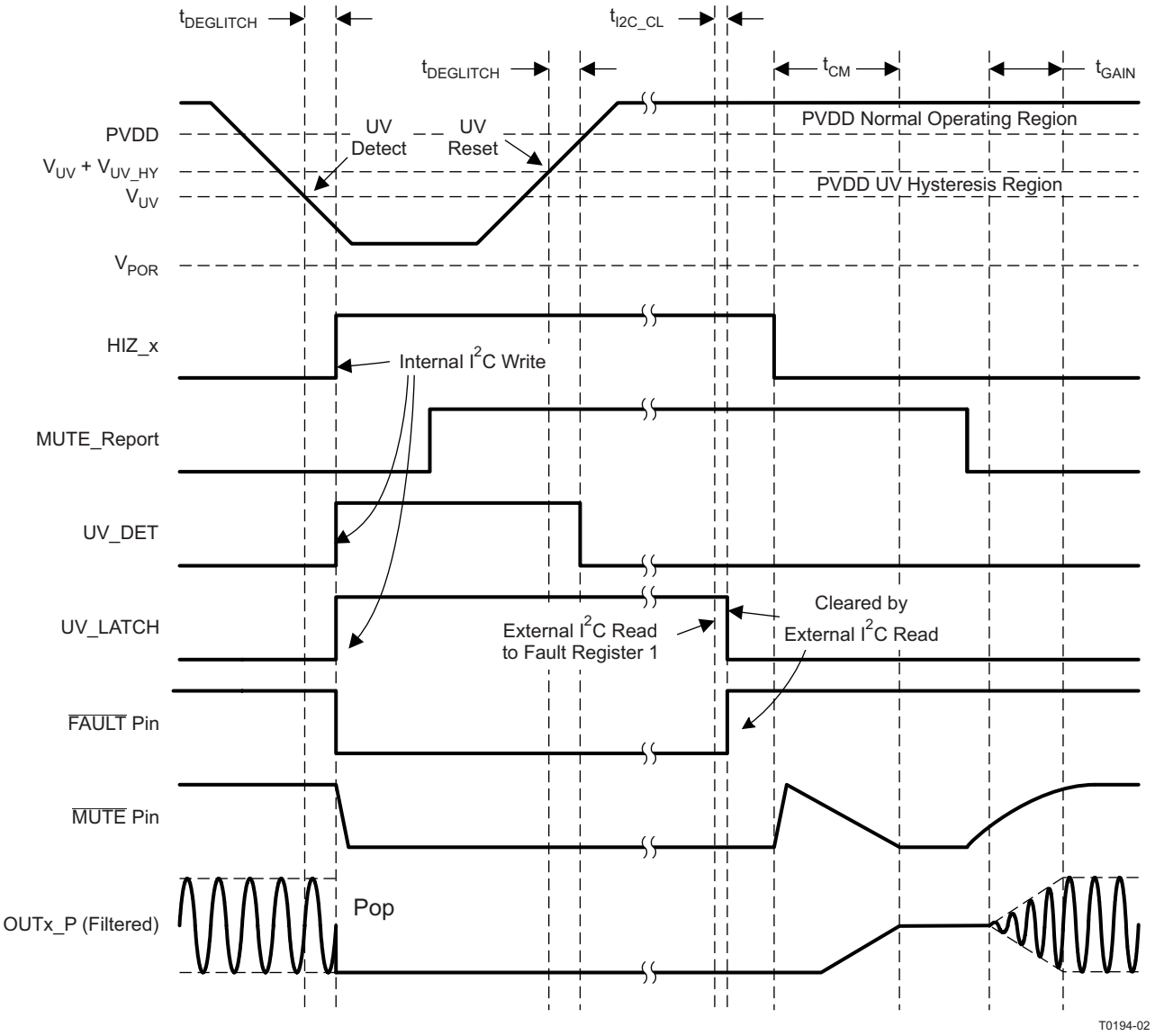


Figure 21. Timing Diagram for Latched-Global-Fault Shutdown and Restart (UV Shutdown and Recovery)

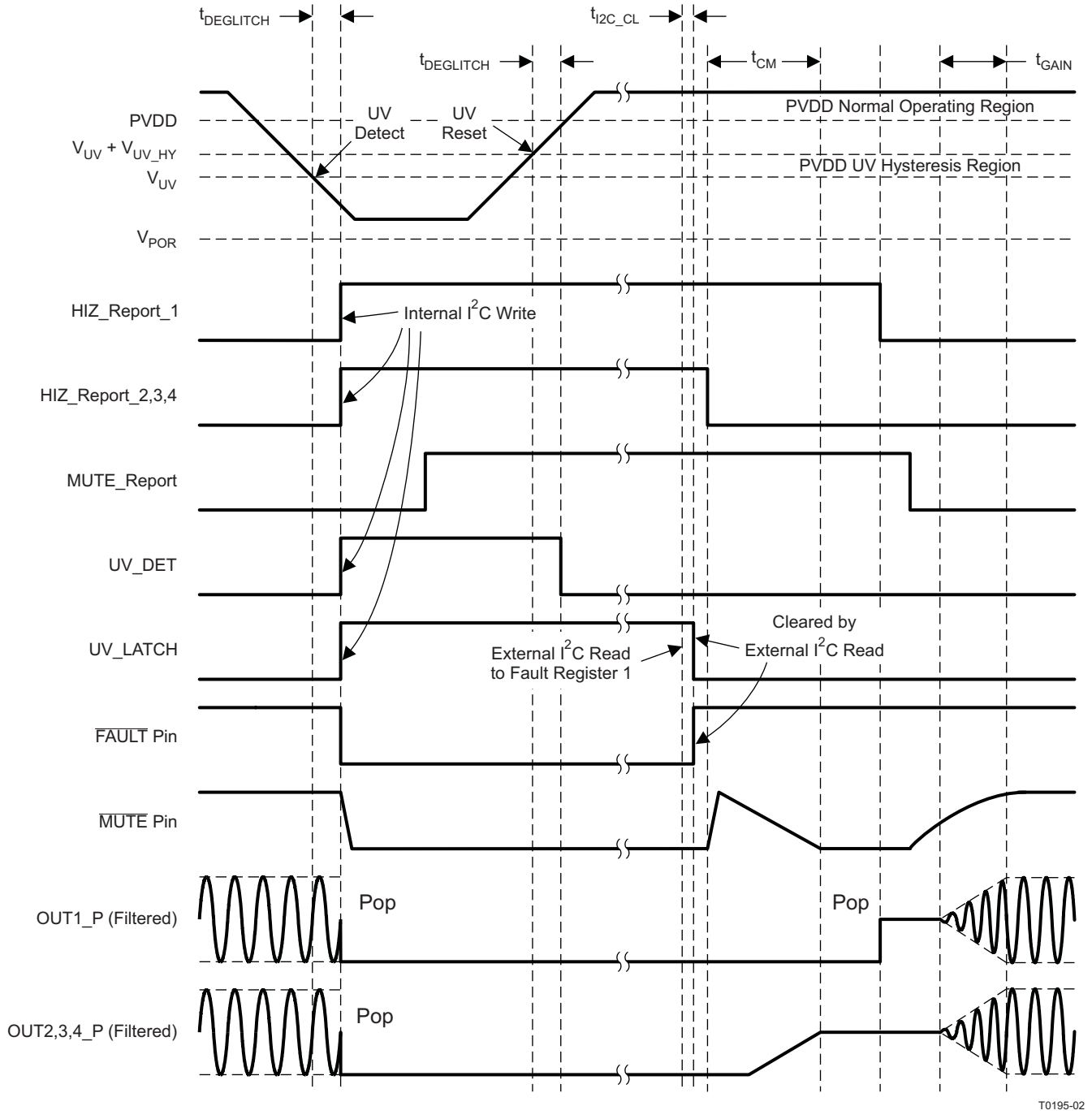


Figure 22. Timing Diagram for Latched-Global-Fault Shutdown and Individual-Channel Restart (UV Shutdown and Recovery)

APPLICATION INFORMATION

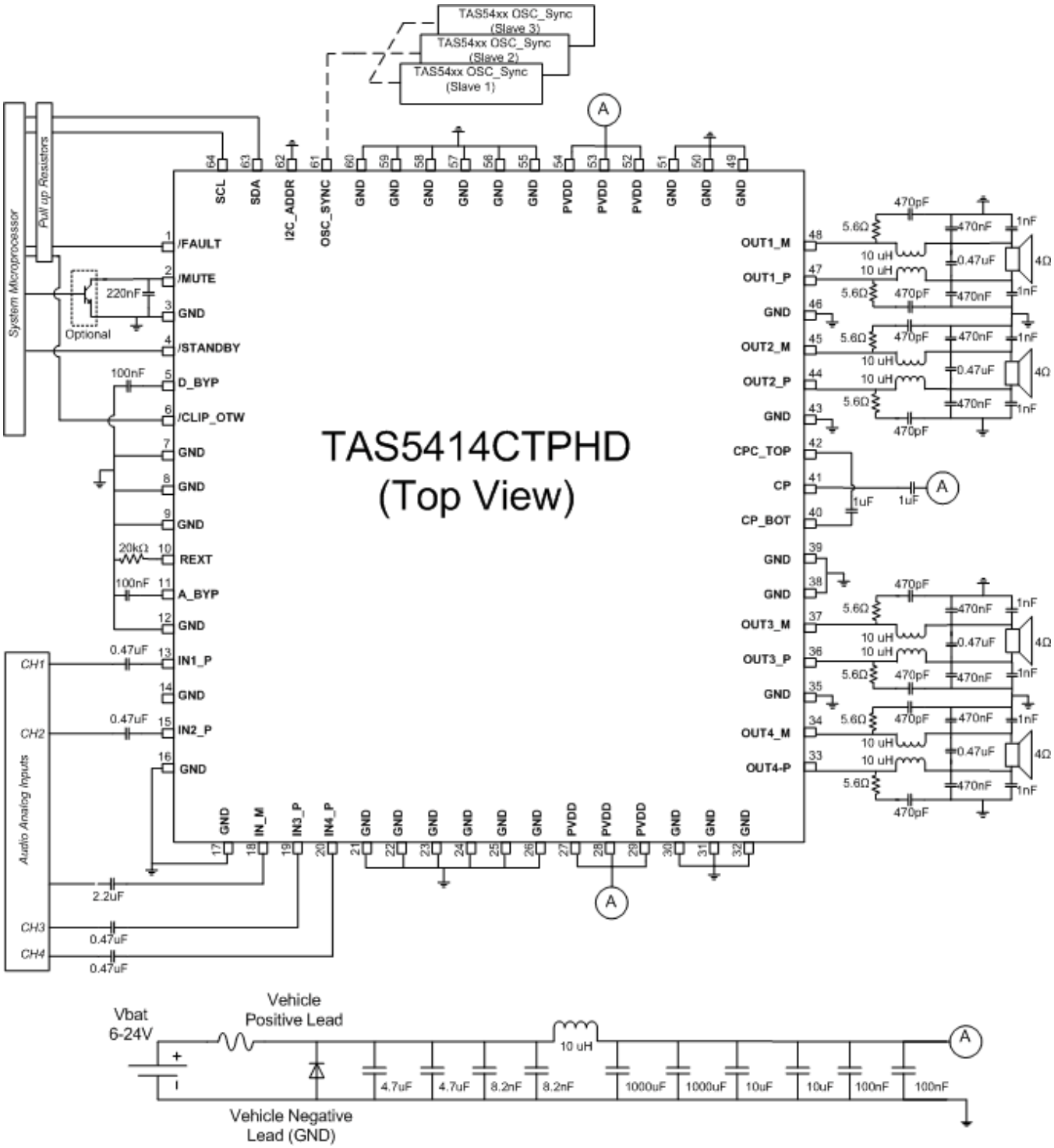


Figure 23. TAS5414C-Q1 Typical Application Schematic

Parallel Operation (PBTL)

The device can drive more current by paralleling BTL channels on the load side of the LC output filter. Parallel operation requires identical I^2C settings for any two paralleled channels in order to have reliable system performance and even power dissipation on multiple channels. For smooth power up, power down, and mute operation, the same control commands (such as mute, play, Hi-Z, and so on) should be sent to the paralleled channels at the same time. The device also supports load diagnostics for parallel connection. There is no support for paralleling on the device side of the LC output filter, which can result in device failure. When paralleling channels, use the parallel BTL I^2C control bits in register 0x0D. Parallel channels 1 and 2, and/or channels 3 and 4. Setting these bits allows the thermal foldback to react on both channels equally.

Input Filter Design

For the TAS5424C-Q1 device, the input filters for the P and M inputs of a single channel should be identical. For the TAS5414C-Q1, the IN_M pin should have an impedance to GND that is equivalent to the parallel combination of the input impedances of all IN_P channels combined, including any source impedance from the previous stage in the system design. For example, if each of the four IN_P channels have a 1-µF dc blocking capacitor, 1 kΩ of series resistance due to an input RC filter, and 1 kΩ of source resistance from the DAC supplying the audio signal, then the IN_M channel should have a 4-µF capacitor in series with a 500-Ω resistor to GND (4 × 1 µF in parallel = 4 µF; 4 × 2 kΩ in parallel = 500 Ω).

Demodulation Filter Design

The amplifier outputs are driven by high-current LDMOS transistors in an H-bridge configuration. These transistors are either fully off or on. The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the audio signal. TI recommends the use of a second-order LC filter to recover the audio signal. The main purpose of the demodulation filter is to attenuate the high-frequency components of the output signals that are out of the audio band. Design of the demodulation filter significantly affects the audio performance of the power amplifier. Therefore, to meet the system THD+N needs, carefully consider the selection of the inductors used in the output filter. The rule is that the inductance should stay above 10% of the inductance value within the range of peak current seen at maximum output power in the system design.

Line Driver Applications

In many automotive audio applications, the end user would like to use the same head unit to drive either a speaker (with several ohms of impedance) or an external amplifier (with several kilohms of impedance). The design is capable of supporting both applications; however, the one must design the output filter and system to handle the expected output load conditions.

Thermal Information

The design of the thermally augmented package is for interface directly to heat sinks using a thermal interface compound (for example, Arctic Silver, Ceramique thermal compound). The heat sink then absorbs heat from the ICs and couples it to the local air. With proper thermal management this process can reach equilibrium at a lower temperature and heat can be continually removed from the ICs. Because of the device efficiency, heat sinks can be smaller than those required for linear amplifiers of equivalent performance.

$R_{\theta JA}$ is a system thermal resistance from junction to ambient air. As such, it is a system parameter with the following components:

- $R_{\theta JC}$ (the thermal resistance from junction to case, or in this case the heat slug)
- Thermal resistance of the thermal grease
- Thermal resistance of the heat sink

One can calculate the thermal resistance of the thermal grease from the exposed heat slug area and the manufacturer's value for the area thermal resistance of the thermal grease (expressed in °C-in^2/W or °C-mm^2/W). The area thermal resistance of the example thermal grease with a 0.001-inch (0.0254-mm) thick layer is about 0.007°C-in^2/W (4.52°C-mm^2/W). The approximate exposed heat slug size is as follows:

44-pin PSOP3	0.124 in^2 (80 mm^2)
64-pin QFP	0.099 in^2 (64 mm^2)

Dividing the example area thermal resistance of the thermal grease by the area of the heat slug gives the actual resistance through the thermal grease for both parts:

44-pin PSOP3	0.06°C/W
64-pin QFP	0.07°C/W

The thermal resistance of thermal pads is generally considerably higher than a thin thermal-grease layer. Thermal tape has an even higher thermal resistance and should not be used at all. The heat-sink vendor generally predicts heat sink thermal resistance, either modeled using a continuous-flow dynamics (CFD) model, or measured.

Thus, for a single monaural channel in the IC, the system $R_{\theta JA}$ = $R_{\theta JC}$ + thermal-grease resistance + heat-sink resistance.

The following table indicates modeled parameters for one device on a heat sink. The junction temperature setting is at 115°C while delivering 20 watts per channel into 4-Ω loads with no clipping. The assumed thickness of the thermal grease is about 0.001 inches (0.0254 mm).

Device	64-Pin QFP
Ambient temperature	25°C
Power to load	20 W × 4
Power dissipation	1.9 W × 4
ΔT inside package	7.6°C
ΔT through thermal grease	0.46°C
Required heatsink thermal resistance	10.78°C/W
Junction temperature	115°C
System $R_{\theta JA}$	11.85°C/W
$R_{\theta JA}$ × power dissipation	90°C

Electrical Connection of Heat Slug and Heat Sink

Electrically connect the heat sink attached to the heat slug of the device to GND, or leave it floating. Do not connect the heat slug to any other electrical node.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5414CTPHDRQ1	ACTIVE	HTQFP	PHD	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	TAS5414CTQ1	Samples
TAS5424CTDKERQ1	PREVIEW	HSSOP	DKE	44	500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	-40 to 105	TAS5424CQ1	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

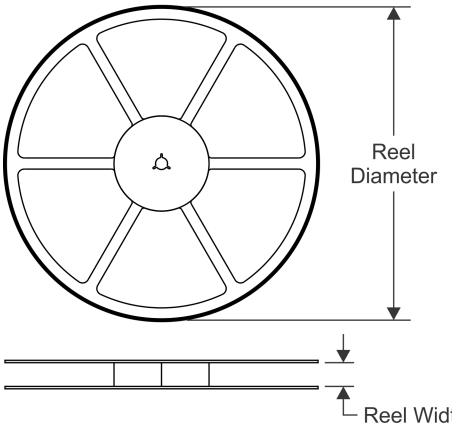
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

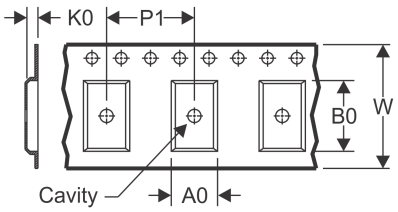
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

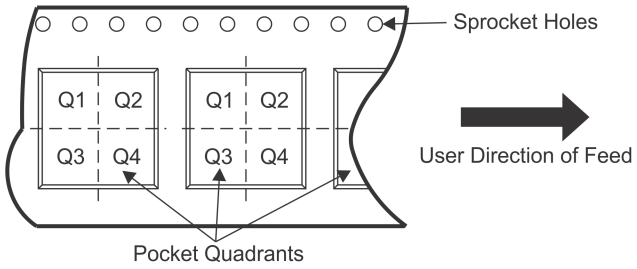


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

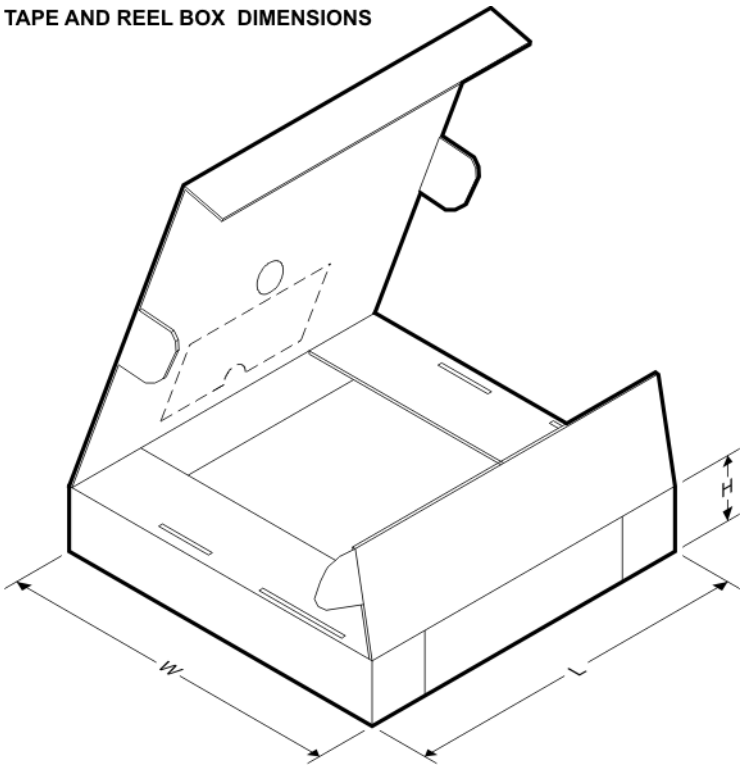
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5414CTPHDRQ1	HTQFP	PHD	64	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

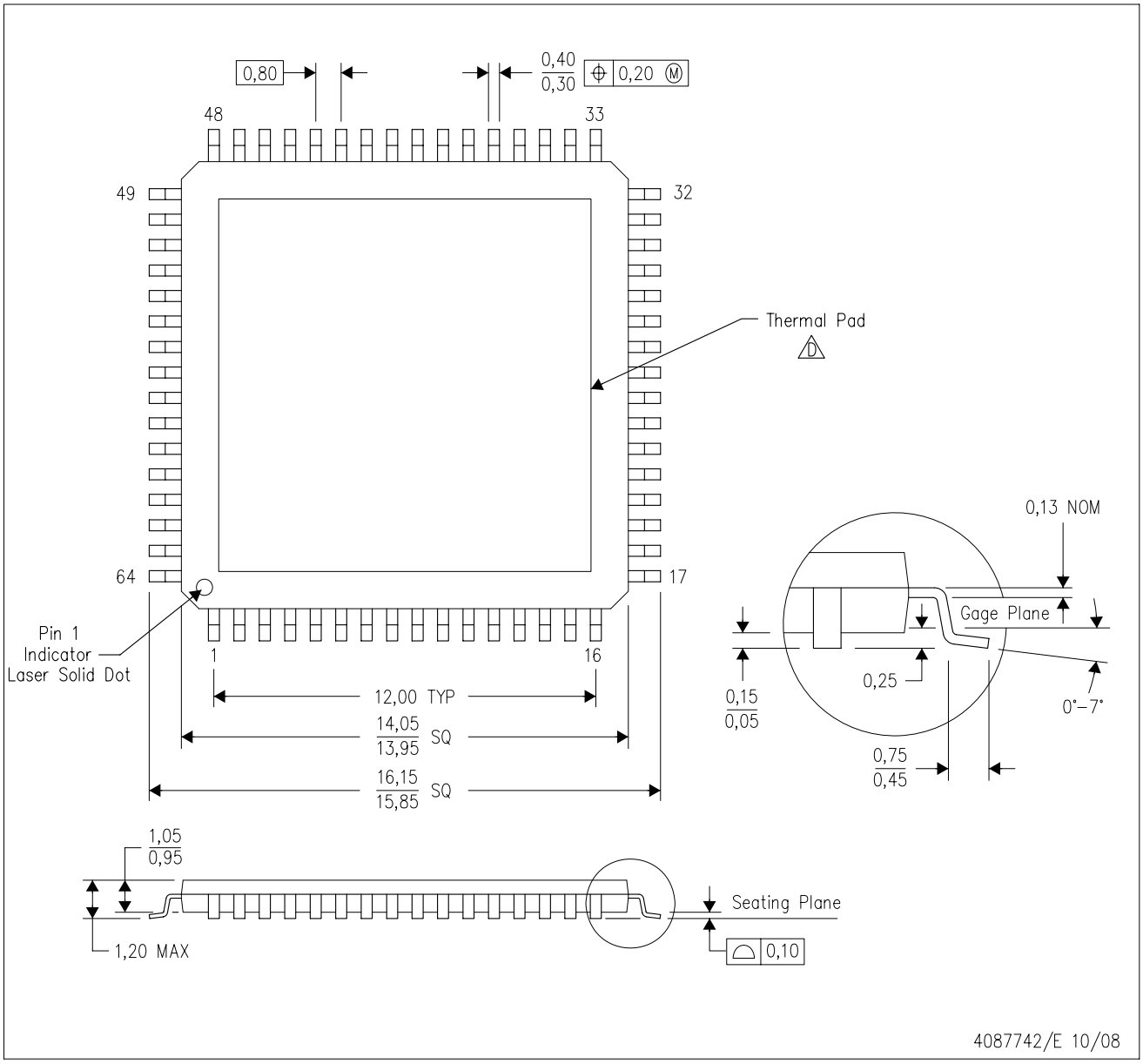
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5414CTPHDRQ1	HTQFP	PHD	64	1000	367.0	367.0	45.0

PHD (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be attached directly to an external heatsink. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

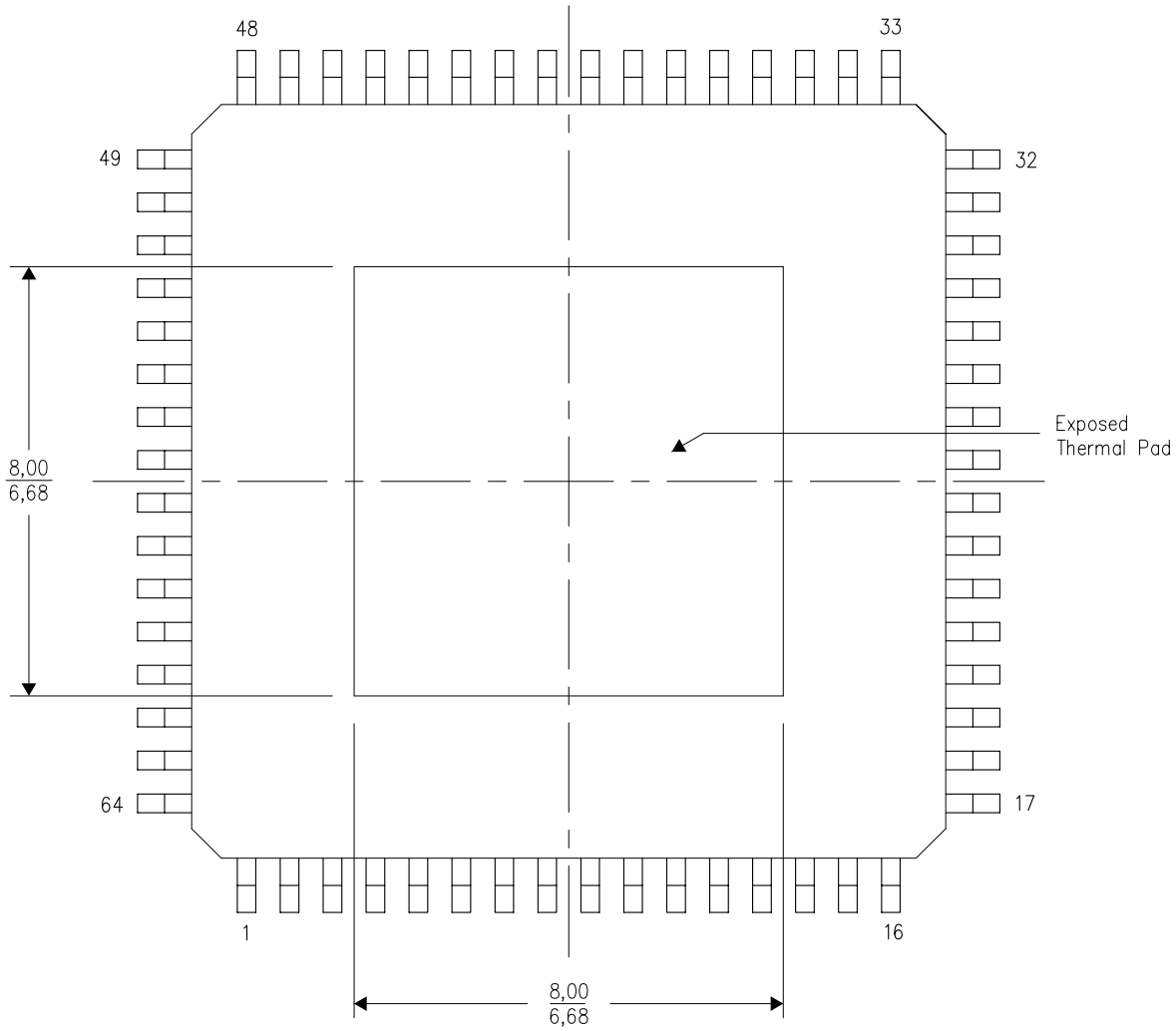
PHD (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206328–3/H 04/11

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

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