General Purpose I²S Input Class D Amplifier

Check for Samples: TAS5760L

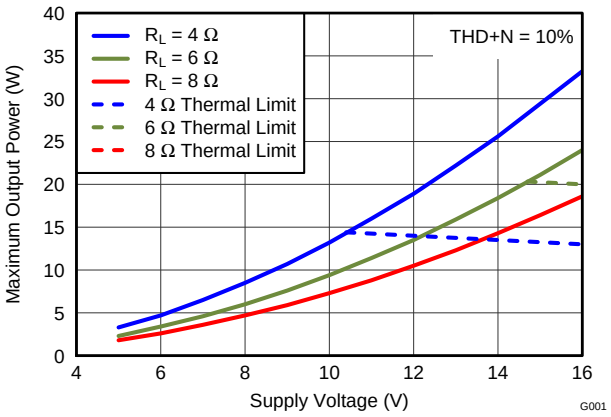
FEATURES

- **Audio I/O Configuration:**
  - **Single Stereo I²S Input**
  - **Stereo Bridge Tied Load (BTL) or Mono Parallel Bridge Tied Load (PBTL) Operation**
  - **32, 44.1, 48, 88.2, 96 kHz Sample Rates**
- **General Operational Features:**
  - **Selectable Hardware or Software Control**
  - **Integrated Digital Output Clipper**
  - **Programmable I²C Address (1101100[R/W] or 1101101[R/W])**
  - **Closed Loop Amplifier Architecture**
  - **Adjustable Switching Frequency for Speaker Amplifier**
- **Robustness Features:**
  - **Clock Error, DC and Short Circuit Protection**
  - **Over Temperature and Programmable Overcurrent Protection**
- **Audio Performance (PVDD = 12V, R_{SPK} = 8Ω, SPK_GAIN[1:0] Pins = 01)**
  - **Idle Channel Noise = 65 µVrms (A-Wtd)**
  - **THD+N = 0.09 % (at 1 W, 1 kHz)**
  - **SNR = 100 dB A-Wtd (Ref. to THD+N = 1%)**

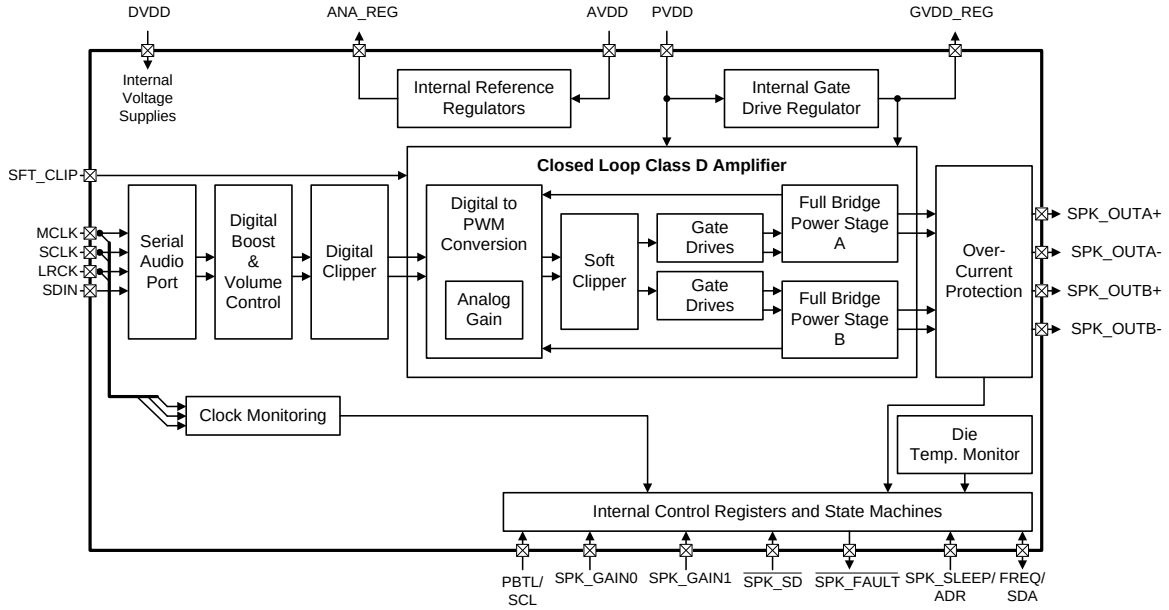
APPLICATIONS

- **LCD/LED TV and Multi-Purpose Monitors**
- **Sound Bars, Docking Stations, PC Audio**
- **General Purpose Audio Equipment**

Power at 10% THD+N vs PVDD



NOTE: Thermal Limits were determined via the TAS5760xxEVM



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION

The TAS5760L is a stereo I²S input device which includes hardware and software (I²C) control modes, integrated digital clipper, several gain options, and a wide power supply operating range to enable use in a multitude of applications. The TAS5760L operates with a nominal supply voltage from 4.5 to 15 VDC.

An optimal mix of thermal performance and device cost is provided in the 120 mΩ $R_{DS(ON)}$ of the output MOSFETs. Additionally, a thermally enhanced 48-Pin TSSOP provides excellent operation in the elevated ambient temperatures found in modern consumer electronic devices.

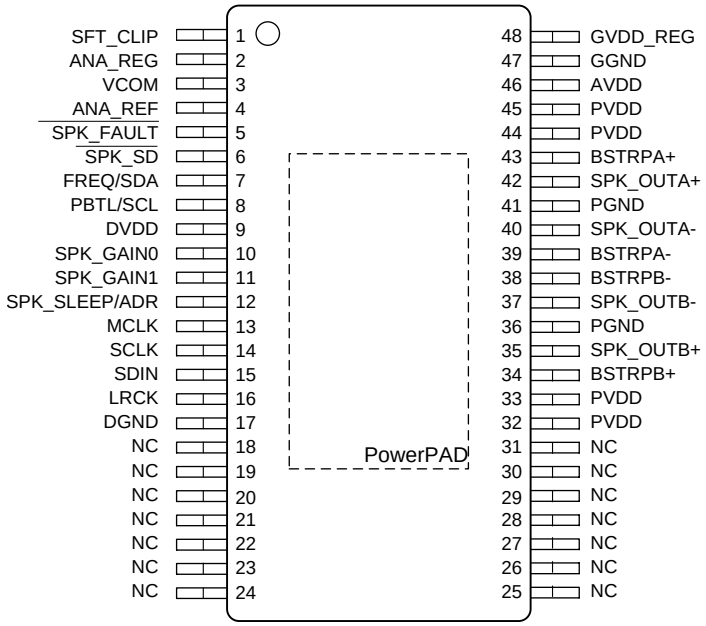
The entire TAS5760xx family is pin to pin compatible in the 48-Pin TSSOP package. Alternatively, to achieve the smallest possible solutions size for applications where pin to pin compatibility and a headphone or line driver are not required, a 32-Pin TSSOP package is offered for the TAS5760M and TAS5760L devices. The I²C register map in all of the TAS5760xx family is identical, to ensure low development overhead when choosing between devices based upon system level requirements.

TAS5760xx FAMILY INFORMATION

Device	Description	Package
TAS5760MDDCA	Flexible, general purpose I²S input class D Amplifier with integrated headphone / line driver and integrated digital clipper, which supports PVDD levels ≤ 24 V	48 Pin, 0.5mm Lead-Pitch, Pad-down TSSOP (DCA)
TAS5760MDCA	Flexible, general purpose I²S input class D Amplifier with integrated digital clipper, which supports PVDD levels ≤ 24 V	48 Pin, 0.5mm Lead-Pitch, Pad-down TSSOP (DCA)
TAS5760MDAP		32 Pin, 0.65mm Lead Pitch, Pad-down TSSOP (DAP)
TAS5760LDDCA	Flexible, general purpose I²S input class D Amplifier with integrated headphone / line driver and integrated digital clipper, which supports PVDD levels ≤ 15V	48 Pin, 0.5mm Lead-Pitch, Pad-down TSSOP (DCA)
TAS5760LDCA	Flexible, general purpose I²S input class D Amplifier with integrated digital clipper, which supports PVDD levels ≤ 15V	48 Pin, 0.5mm Lead-Pitch, Pad-down TSSOP (DCA)
TAS5760LDAP		32 Pin, 0.65mm Lead Pitch, Pad-down TSSOP (DAP)

PINOUT AND PIN DESCRIPTIONS

TSSOP PACKAGE
DCA-48
(TOP VIEW)



Pin Descriptions

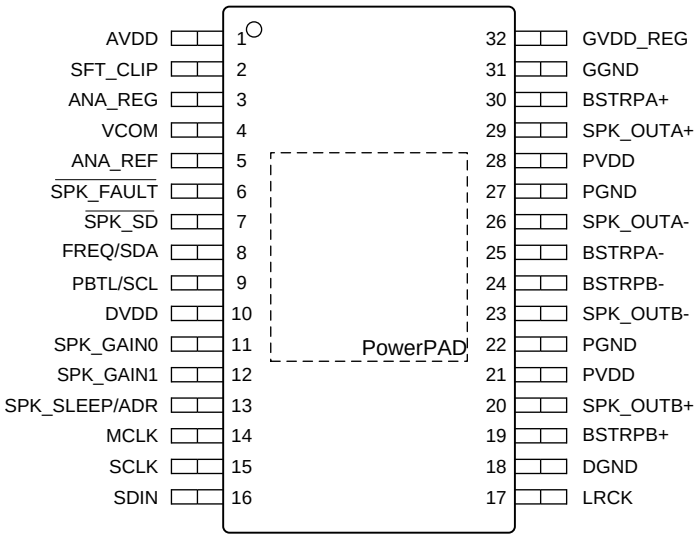
TAS5760L Name	No.	Type(1)	Internal Termination	Description
AVDD	46	P	-	Power supply for internal analog circuitry
ANA_REF	4	P	-	Connection point for internal reference used by ANA_REG and VCOM filter capacitors
ANA_REG	2	P	-	Voltage regulator derived from AVDD supply (NOTE: This terminal is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry)
BSTRPA-	39	P	-	Connection point for the SPK_OUTA- bootstrap capacitor, which is used to create a power supply for the high-side gate drive for SPK_OUTA-
BSTRPA+	43	P	-	Connection point for the SPK_OUTA+ bootstrap capacitor, which is used to create a power supply for the high-side gate drive for SPK_OUTA
BSTRPB-	38	P	-	Connection point for the SPK_OUTB- bootstrap capacitor, which is used to create a power supply for the high-side gate drive for SPK_OUTB-
BSTRPB+	34	P	-	Connection point for the SPK_OUTB+ bootstrap capacitor, which is used to create a power supply for the high-side gate drive for SPK_OUTB+
DGND	17	G	-	Ground for digital circuitry (NOTE: This terminal should be connected to the system ground)
DVDD	9	P	-	Power supply for the internal digital circuitry
FREQ/SDA	7	DI	Weak Pull-Down	Dual function terminal that functions as an I²C data input terminal in I²C Control Mode or as a Frequency Select terminal when in Hardware Control Mode.
GGND	47	G	-	Ground for gate drive circuitry (this terminal should be connected to the system ground)
GVDD_REG	48	P	-	Voltage regulator derived from PVDD supply (NOTE: This terminal is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry)
LRCK	16	DI	Weak Pull-Down	Word select clock for the digital signal that is active on the serial port's input data line

(1) AI = Analog input, AO = Analog output, DI = Digital Input, DO = Digital Output, P = Power, G = Ground (0V)

Pin Descriptions (continued)

TAS5760L Name	No.	Type(1)	Internal Termination	Description
MCLK	13	DI	Weak Pull-Down	Master Clock used for internal clock tree, sub-circuit/state machine, and Serial Audio Port clocking
NC	18-31	-	-	Not connected inside the device (all "no connect" terminals should be connected to ground for best thermal performance, however they can be used as routing channels if required.)
PBTL/SCL	8	DI	Weak Pull-Down	Dual function terminal that functions as an I²C clock input terminal in I²C Control Mode or configures the device to operate in pre-filter Parallel Bridge Tied Load (PBTL) mode when in Hardware Control Mode
PGND	36, 41	G	-	Ground for power device circuitry (NOTE: This terminal should be connected to the system ground)
PVDD	32, 33, 44, 45	P	-	Power Supply for internal power circuitry
SCLK	14	DI	Weak Pull-Down	Bit clock for the digital signal that is active on the serial data port's input data line
SDIN	15	DI	Weak Pull-Down	Data line to the serial data port
SFT_CLIP	1	AI	-	sets the maximum output voltage before clipping
$\overline{\text{SPK\_FAULT}}$	5	DO	-	Speaker amplifier fault terminal, which is pulled "LOW" when an internal fault occurs
SPK_GAIN0	10	DI	Weak Pull-Down	Adjusts the LSB of the multi-bit gain of the speaker amplifier
SPK_GAIN1	11	DI	Weak Pull-Down	Adjusts the MSB of the multi-bit gain of the speaker amplifier
SPK_SLEEP/ADR	12	DI	Weak Pull-Up	In Hardware Control Mode, places the speaker amplifier in sleep mode. In Software Control Mode, is used to determine the I²C Address of the device
SPK_OUTA-	40	AO	-	Negative terminal for differential speaker amplifier output "A"
SPK_OUTA+	42	AO	-	Positive terminal for differential speaker amplifier output "A"
SPK_OUTB-	37	AO	-	Negative terminal for differential speaker amplifier output "B"
SPK_OUTB+	35	AO	-	Positive terminal for differential speaker amplifier output "B"
$\overline{\text{SPK\_SD}}$	6	AO	-	Places the speaker amplifier in shutdown
VCOM	3	P	-	Bias voltage for internal PWM conversion block
PowerPAD™	-	G	-	Provides both electrical and thermal connection from the device to the board. A matching ground pad must be provided on the PCB and the device connected to it via solder. For proper electrical operation, this ground pad must be connected to the system ground.

TSSOP PACKAGE
DAP-32
(TOP VIEW)



Pin Descriptions

TAS5760L Name	No.	Type(1)	Internal Termination	Description
AVDD	1	P	-	Power supply for internal analog circuitry
ANA_REF	5	P	-	Connection point for internal reference used by ANA_REG and VCOM filter capacitors
ANA_REG	3	P	-	Voltage regulator derived from AVDD supply (NOTE: This terminal is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry)
BSTRPA-	25	P	-	Connection point for the SPK_OUTA- bootstrap capacitor, which is used to create a power supply for the high-side gate drive for SPK_OUTA-
BSTRPA+	30	P	-	Connection point for the SPK_OUTA+ bootstrap capacitor, which is used to create a power supply for the high-side gate drive for SPK_OUTA
BSTRPB-	24	P	-	Connection point for the SPK_OUTB- bootstrap capacitor, which is used to create a power supply for the high-side gate drive for SPK_OUTB-
BSTRPB+	19	P	-	Connection point for the SPK_OUTB+ bootstrap capacitor, which is used to create a power supply for the high-side gate drive for SPK_OUTB+
DGND	18	G	-	Ground for digital circuitry (NOTE: This terminal should be connected to the system ground)
DVDD	10	P	-	Power supply for the internal digital circuitry
FREQ/SDA	8	DI	Weak Pull-Down	Dual function terminal that functions as an I²C data input terminal in I²C Control Mode or as a Frequency Select terminal when in Hardware Control Mode.
GGND	31	G	-	Ground for gate drive circuitry (this terminal should be connected to the system ground)
GVDD_REG	32	P	-	Voltage regulator derived from PVDD supply (NOTE: This terminal is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry)
LRCK	17	DI	Weak Pull-Down	Word select clock for the digital signal that is active on the serial port's input data line
MCLK	14	DI	Weak Pull-Down	Master Clock used for internal clock tree, sub-circuit/state machine, and Serial Audio Port clocking
PBTL/SCL	9	DI	Weak Pull-Down	Dual function terminal that functions as an I²C clock input terminal in I²C Control Mode or configures the device to operate in pre-filter Parallel Bridge Tied Load (PBTL) mode when in Hardware Control Mode

(1) AI = Analog input, AO = Analog output, DI = Digital Input, DO = Digital Output, P = Power, G = Ground (0V)

Pin Descriptions (continued)

TAS5760L Name	No.	Type(1)	Internal Termination	Description
PGND	22, 27	G	-	Ground for power device circuitry (NOTE: This terminal should be connected to the system ground)
PVDD	21, 28	P	-	Power Supply for internal power circuitry
SCLK	15	DI	Weak Pull-Down	Bit clock for the digital signal that is active on the serial data port's input data line
SDIN	16	DI	Weak Pull-Down	Data line to the serial data port
SFT_CLIP	2	AI	-	sets the maximum output voltage before clipping
$\overline{\text{SPK\_FAULT}}$	6	DO	Open Drain	Fault terminal, which is pulled "LOW" when an internal fault occurs
SPK_GAIN0	11	DI	Weak Pull-Down	Adjusts the LSB of the multi-bit gain of the speaker amplifier
SPK_GAIN1	12	DI	Weak Pull-Down	Adjusts the MSB of the multi-bit gain of the speaker amplifier
SPK_SLEEP/ADR	13	DI	Weak Pull-Up	Places the speaker amplifier in mute
SPK_OUTA-	26	AO	-	Negative terminal for differential speaker amplifier output "A"
SPK_OUTA+	29	AO	-	Positive terminal for differential speaker amplifier output "A"
SPK_OUTB-	23	AO	-	Negative terminal for differential speaker amplifier output "B"
SPK_OUTB+	20	AO	-	Positive terminal for differential speaker amplifier output "B"
$\overline{\text{SPK\_SD}}$	7	DI	-	Places the device in shutdown when pulled "LOW"
VCOM	4	P	-	Bias voltage for internal PWM conversion block
PowerPAD™	-	G	-	Provides both electrical and thermal connection from the device to the board. A matching ground pad must be provided on the PCB and the device connected to it via solder

ABSOLUTE MAXIMUM RATINGS(2)

over operating free-air temperature range (unless otherwise noted)

Parameter		Min	Max	Unit
Temperature	Ambient Operating Temperature, T_A	–25	85	°C
	Ambient Storage Temperature, T_S	–40	125	°C
Supply Voltage	AVDD Supply	–0.3	20	V
	PVDD Supply	–0.3	20	V
	DVDD Supply	–0.3	4	V
DVDD Referenced Digital Input Voltages	Digital Inputs referenced to DVDD supply	-0.5	DVDD + 0.5	V
Speaker Amplifier Output Voltage	V_{SPK_OUTxx}, measured at the output pin	-0.3	22	V

(2) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

THERMAL METRIC(1)		TAS5760L		UNIT
		48 Pin DCA(1)	48 Pin DCA(2)	
θ_{JA}	Junction-to-ambient thermal resistance	60.3	30.2	°C/W
$\theta_{JC(bottom)}$	Junction-to-case (bottom) thermal resistance	16.0	14.3	°C/W
θ_{JB}	Junction-to-board thermal resistance	12.0	12.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.9	12.7	°C/W
$\theta_{JC(top)}$	Junction-to-case (top) thermal resistance	0.8	0.7	°C/W

(1) JEDEC Standard 2 Layer Board
(2) JEDEC Standard 4 Layer Board

THERMAL CHARACTERISTICS- 32 PIN DAP PACKAGE OPTION

THERMAL METRIC(1)		TAS5760L 32 Pin DAP JEDEC Standard 2 Layer Board	TAS5760L 32 Pin DAP JEDEC Standard 4 Layer Board	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	60.3	31.9	°C/W
$\theta_{JC(top)}$	Junction-to-case (top) thermal resistance	16.0	16.0	°C/W
θ_{JB}	Junction-to-board thermal resistance	12.0	17.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.9	16.8	°C/W
$\theta_{JC(bottom)}$	Junction-to-case (bottom) thermal resistance	0.8	0.81	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
T_A	Ambient Operating Temperature		–25	-	85	°C
AVDD	AVDD Supply		4.5	-	16.5	V
PVDD	PVDD Supply		4.5	-	16.5	V

RECOMMENDED OPERATING CONDITIONS (continued)

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
DVDD	DVDD Supply		2.8	-	3.63	V
$VIH_{(DR)}$	Input Logic "HIGH" for DVDD Referenced Digital Inputs		-	DVDD	-	V
$VIL_{(DR)}$	Input Logic "LOW" for DVDD Referenced Digital Inputs		-	0	-	V
$R_{SPK\ (BTL)}$	Minimum Speaker Load in BTL Mode		4	-	-	Ω
$R_{SPK\ (PBTL)}$	Minimum Speaker Load in PBTL Mode		2	-	-	Ω

ELECTRICAL SPECIFICATIONS AND CHARACTERISTICS

DIGITAL I/O PINS

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{IH1}	Input Logic "HIGH" threshold for DVDD Referenced Digital Inputs	All digital pins	70	-	-	%DVDD
V_{IL1}	Input Logic "LOW" threshold for DVDD Referenced Digital Inputs	All digital pins	-	-	30	%DVDD
$\|I_{IH}\|_1$	Input Logic "HIGH" Current Level	All digital pins	-	-	15	µA
$\|I_{IL}\|_1$	Input Logic "LOW" Current Level	All digital pins	-	-	-15	µA
V_{OH}	Output Logic "HIGH" Voltage Level	I_{OH} = 2 mA	90	-	-	%DVDD
V_{OL}	Output Logic "LOW" Voltage Level	I_{OH} = -2 mA	-	-	10	%DVDD

MASTER CLOCK

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
D_{MCLK}	Allowable MCLK Duty Cycle		45	50	55	%
f_{MCLK}	Supported MCLK Frequencies	Values include: 128, 192, 256, 384, 512.	128	-	512	x f_S

SERIAL AUDIO PORT

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
D_{SCLK}	Allowable SCLK Duty Cycle		45	50	55	%
	Required LRCK to SCLK Rising Edge		15	-	-	ns
t_{HLD}	Required SDIN Hold Time after SCLK Rising Edge		15	-	-	ns
t_{su}	Required SDIN Setup Time before SCLK Rising Edge		15	-	-	ns
f_S	Supported Input Sample Rates	Sample rates above 48kHz supported by "double speed mode," which is activated through the I²C control port	32	-	96	kHz
f_{SCLK}	Supported SCLK Frequencies	Values include: 32, 48, 64	32	-	64	x f_S

PROTECTION CIRCUITRY

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
$OVE_{RTHRES(PVDD)}$	PVDD Over-Voltage Error Threshold	PVDD Rising	-	18	-	V
$OVE_{FTHRES(PVDD)}$	PVDD Over-Voltage Error Threshold	PVDD Falling	-	17.3	-	V
$UVE_{FTHRES(PVDD)}$	PVDD Under-Voltage Error (UVE) Threshold	PVDD Falling	-	3.95	-	V
$UVE_{RTHRES(PVDD)}$	PVDD UVE Threshold (PVDD Rising)	PVDD Rising	-	4.15	-	V
OTE_{THRES}	Over-Temperature Error (OTE) Threshold		-	150	-	°C
OTE_{HYST}	Over-Temperature Error (OTE) Hysteresis		-	15	-	°C
OCE_{THRES}	Over-Current Error (OCE) Threshold for each BTL Output	PVDD= 15V, T_A = 25 °C	-	7	-	A
DCE_{THRES}	DC Error (DCE) Threshold	PVDD= 12V, T_A = 25 °C	-	2.6	-	V
$T_{\overline{SPK\_FAULT}}$	Speaker Amplifier Fault Time Out period	DC Detect Error	-	650	-	ms
		OTE or OCP Fault		1.3		s

SPEAKER AMPLIFIER IN ALL MODES

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
AV_{00}	Speaker Amplifier Gain with SPK_GAIN[1:0] Pins = 00	Hardware Control Mode (Additional gain settings available in Software Control Mode)(1)	-	25.2	-	dBV
AV_{01}	Speaker Amplifier Gain with SPK_GAIN[1:0] Pins = 01	Hardware Control Mode (Additional gain settings available in Software Control Mode)(1)	-	28.6	-	dBV
AV_{10}	Speaker Amplifier Gain with SPK_GAIN[1:0] Pins = 10	Hardware Control Mode (Additional gain settings available in Software Control Mode)(1)	-	30	-	dBV
AV_{11}	Speaker Amplifier Gain with SPK_GAIN[1:0] Pins = 11	(This setting places the device in Software Control Mode)	-	(Set via I²C)	-	-
$\lvert VOS\rvert_{(SPK\_AMP)}$	Speaker Amplifier DC Offset	BTL, Worst case over voltage, gain settings	-	-	10	mV
		PBTL, Worst case over voltage, gain settings	-	-	15	mV
$f_{SPK\_AMP(0)}$	Speaker Amplifier Switching Frequency when PWM_FREQ Pin = 0	(Hardware Control Mode. Additional switching rates available in Software Control Mode.)	-	16	-	x f_S
$f_{SPK\_AMP(1)}$	Speaker Amplifier Switching Frequency when PWM_FREQ Pin = 1	(Hardware Control Mode. Additional switching rates available in Software Control Mode.)	-	8	-	x f_S
$R_{DS(ON)}$	On Resistance of Output MOSFET (both high-side and low-side)	PVDD = 15 V, TA = 25 °C, Die Only	-	120	-	mΩ
		PVDD= 15V, TA = 25 °C, Includes: Die, Bond Wires, Leadframe	-	150	-	mΩ

(1) The digital boost block contributes +6dB of gain to this value. The audio signal must be kept below -6dB to avoid clipping the digital audio path.

SPEAKER AMPLIFIER IN ALL MODES (continued)

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
f_C	-3dB Corner Frequency of High-Pass Filter	f_S = 44.1 kHz	-	3.7	-	Hz
		f_S = 48 kHz	-	4	-	
		f_S = 88.2 kHz	-	7.4	-	
		f_S = 96 kHz	-	8	-	

SPEAKER AMPLIFIER IN STEREO BRIDGE TIED LOAD (BTL) MODE

input signal is 1 kHz Sine, specifications are over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
$ICN_{(SPK)}$	Idle Channel Noise	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8Ω, A-Weighted	-	66	-	µVrms
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8Ω, A-Weighted	-	75	-	µVrms
$P_{O(SPK)}$	Maximum Instantaneous Output Power Per. Ch.	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 4Ω, THD+N = 0.1%,	-	14.2	-	W
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8Ω, THD+N = 0.1%	-	8	-	W
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 4Ω, THD+N = 0.1%,	-	21.9	-	W
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8Ω, THD+N = 0.1%	-	12.5	-	W
$P_{O(SPK)}$	Maximum Continuous Output Power Per. Ch. (1)	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 4Ω, THD+N = 0.1%,	-	14	-	W
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8Ω, THD+N = 0.1%	-	8	-	W
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 4Ω, THD+N = 0.1%,	-	13.25	-	W
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8Ω, THD+N = 0.1%	-	12.5	-	W
$SNR_{(SPK)}$	Signal to Noise Ratio (Referenced to THD+N = 1%)	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8Ω, A-Weighted, -60dBFS Input	-	99.7	-	dB
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8Ω, A-Weighted, -60dBFS Input	-	98.2	-	dB
$THD+N_{(SPK)}$	Total Harmonic Distortion and Noise	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 4Ω, Po = 1 W	-	0.02	-	%
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8Ω, Po = 1 W	-	0.03	-	%
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 4Ω, Po = 1 W	-	0.03	-	%
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8Ω, Po = 1 W	-	0.03	-	%
$X\text{-}Talk_{(SPK)}$	Cross-talk (worst case between LtoR and RtoL coupling)	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8Ω, Input Signal 250 mVrms, 1kHz Sine	-	-92	-	dB
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8Ω, Input Signal 250 mVrms, 1kHz Sine	-	-93	-	dB

(1) The continuous power output of any amplifier is determined by the thermal performance of the amplifier as well as limitations placed on it by the system around it, such as the PCB configuration and the ambient operating temperature. The performance characteristics listed in this section are achievable on the TAS5760L's EVM, which is representative of the poplular "2 Layers / 1oz Copper" PCB configuration in a size that is representative of the amount of area often provided to the amplifier section of popular consumer audio electronics. As can be seen in the instantaneous power portion of this table, more power can be delivered from the TAS5760L if steps are taken to pull more heat out of the device. For instance, using a board with more layers or adding a small heatsink will result in an increase of continuous power, up to and including the instantaneous power level. This behavior can also been seen in the POUT vs. PVDD plots shown in the typical performance plots section of this data sheet.

SPEAKER AMPLIFIER IN MONO PARALLEL BRIDGE TIED LOAD (PBTL) MODE

input signal is 1 kHz Sine, specifications are over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
ICN	Idle Channel Noise	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8Ω, A-Weighted	-	69	-	µVrms
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8Ω, A-Weighted	-	85	-	µVrms
$P_{O(SPK)}$	Maximum Instantaneous Output Power	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 2Ω, THD+N = 0.1%,	-	28.6	-	W
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 4Ω, THD+N = 0.1%,	-	15.9	-	W
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8Ω, THD+N = 0.1%	-	8.4	-	W
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 2Ω, THD+N = 0.1%,	-	43.2	-	W
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 4Ω, THD+N = 0.1%,	-	25	-	W
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8Ω, THD+N = 0.1%	-	13.3	-	W
$P_{O(SPK)}$	Maximum Continuous Output Power(1)	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 2Ω, THD+N = 0.1%,	-	30	-	W
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 4Ω, THD+N = 0.1%,	-	15.9	-	W
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8Ω, THD+N = 0.1%	-	8.4	-	W
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 2Ω, THD+N = 0.1%,	-	28.5	-	W
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 4Ω, THD+N = 0.1%,	-	25	-	W
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8Ω, THD+N = 0.1%	-	13.3	-	W
SNR	Signal to Noise Ratio (Referenced to THD+N = 1%)	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8Ω, A-Weighted, -60dBFS Input	-	100.4	-	dB
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8Ω, A-Weighted, -60dBFS Input	-	99.5	-	dB
$THD+N_{(SPK)}$	Total Harmonic Distortion and Noise	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 2Ω, Po = 1 W	-	0.03	-	%
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 4Ω, Po = 1 W	-	0.02	-	%
		PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8Ω, Po = 1 W	-	0.02	-	%
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 2Ω, Po = 1 W	-	0.03	-	%
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 4Ω, Po = 1 W	-	0.02	-	%
		PVDD = 15 V, SPK_GAIN[1:0] Pins = 01, R_{SPK} = 8Ω, Po = 1 W	-	0.02	-	%

(1) The continuous power output of any amplifier is determined by the thermal performance of the amplifier as well as limitations placed on it by the system around it, such as the PCB configuration and the ambient operating temperature. The performance characteristics listed in this section are achievable on the TAS5760L's EVM, which is representative of the poplular "2 Layers / 1oz Copper" PCB configuration in a size that is representative of the amount of area often provided to the amplifier section of popular consumer audio electronics. As can be seen in the instantaneous power portion of this table, more power can be delivered from the TAS5760L if steps are taken to pull more heat out of the device. For instance, using a board with more layers or adding a small heatsink will result in an increase of continuous power, up to and including the instantaneous power level. This behavior can also been seen in the POUT vs. PVDD plots shown in the typical performance plots section of this data sheet.

I²C CONTROL PORT

specifications are over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Units
$C_{L(I^2C)}$	Allowable Load Capacitance for Each I²C Line		-	-	400	pF
f_{SCL}	Support SCL frequency	No Wait States	-	-	400	kHz

I²C CONTROL PORT (continued)

specifications are over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Units
t_{buf}	Bus Free time between stop and start conditions		1.3	-	-	µS
$t_{f(I^2C)}$	Rise Time, SCL and SDA		-	-	300	ns
$t_{h1(I^2C)}$	Hold Time, SCL to SDA		0	-	-	ns
$t_{h2(I^2C)}$	Hold Time, start condition to SCL		0.6	-	-	µs
$t_{I^2C(start)}$	I²C Startup Time		-	-	12	mS
$t_{r(I^2C)}$	Rise Time, SCL and SDA		-	-	300	ns
$t_{su1(I^2C)}$	Setup Time, SDA to SCL		100	-	-	ns
$t_{su2(I^2C)}$	Setup Time, SCL to start condition		0.6	-	-	µS
$t_{su3(I^2C)}$	Setup Time, SCL to stop condition		0.6	-	-	µS
$T_{w(H)}$	Required Pulse Duration, SCL High		0.6	-	-	µS
$T_{w(L)}$	Required Pulse Duration, SCL "LOW"		1.3	-	-	µS

TYPICAL IDLE, MUTE, SHUTDOWN, OPERATIONAL POWER CONSUMPTION

input signal is 1 kHz Sine, specifications are over operating free-air temperature range (unless otherwise noted)

V_{PVDD} [V]	R_{SPK} [Ω]	Speaker Amplifier State		$I_{PVDD+AVDD}$ [mA]	I_{DVDD} [mA]	P_{DISS} [W]
6	4	f_{SPK_AMP} = 384kHz	Idle	23.48	3.73	0.15
	8			23.44	3.72	0.15
	4		Mute	23.53	3.72	0.15
	8			23.46	3.72	0.15
	4		Sleep	13.26	0.48	0.08
	8			13.27	0.53	0.08
	4		Shutdown	0.046	0.04	0
	8			0.046	0.03	0
	4	f_{SPK_AMP} = 768kHz	Idle	30.94	3.71	0.2
	8			30.94	3.71	0.2
	4		Mute	29.37	3.71	0.19
	8			29.39	3.71	0.19
	4		Sleep	13.24	0.5	0.08
	8			13.23	0.52	0.08
	4		Shutdown	0.046	0.03	0
	8			0.046	0.03	0
	4	f_{SPK_AMP} = 1152kHz	Idle	39.39	3.7	0.25
	8			39.43	3.7	0.25
	4		Mute	36.91	3.7	0.23
	8			36.9	3.69	0.23
	4		Sleep	13.17	0.53	0.08
	8			13.13	0.45	0.08
	4		Shutdown	0.046	0.03	0
	8			0.046	0.03	0

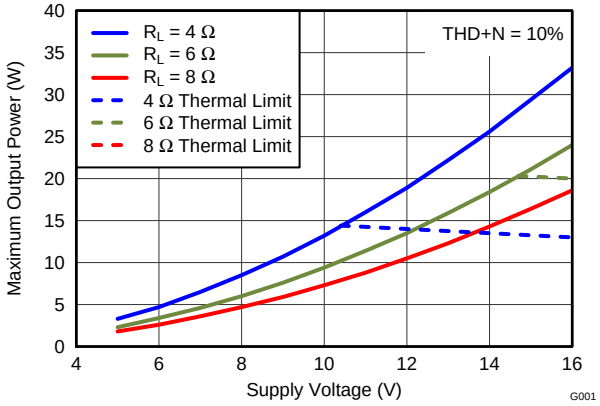
TYPICAL IDLE, MUTE, SHUTDOWN, OPERATIONAL POWER CONSUMPTION (continued)

input signal is 1 kHz Sine, specifications are over operating free-air temperature range (unless otherwise noted)

V_{PVDD} [V]	R_{SPK} [Ω]	Speaker Amplifier State		$I_{PVDD+AVDD}$ [mA]	I_{DVDD} [mA]	P_{DISS} [W]
12	4	f_{SPK_AMP} = 384kHz	Idle	32.95	3.74	0.41
	8			32.93	3.73	0.41
	4		Mute	32.98	3.73	0.41
	8			32.97	3.73	0.41
	4		Sleep	12.71	0.47	0.15
	8			12.75	0.5	0.15
	4		Shutdown	0.053	0.04	0
	8			0.053	0.04	0
	4	f_{SPK_AMP} = 768kHz	Idle	44.84	3.73	0.55
	8			44.82	3.73	0.55
	4		Mute	42.71	3.72	0.52
	8			42.66	3.72	0.52
	4		Sleep	12.71	0.49	0.15
	8			12.73	0.52	0.15
	4		Shutdown	0.063	0.03	0
	8			0.053	0.03	0
	4	f_{SPK_AMP} = 1152kHz	Idle	59.3	3.73	0.72
	8			59.3	3.73	0.72
	4		Mute	55.74	3.72	0.68
	8			55.74	3.72	0.68
	4		Sleep	12.67	0.49	0.15
	8			12.61	0.43	0.15
	4		Shutdown	0.053	0.02	0
	8			0.053	0.03	0

TYPICAL SPEAKER AMPLIFIER PERFORMANCE CHARACTERISTICS (Stereo BTL Mode)

At T_A = 25°C, f_{SPK_AMP} = 384kHz, input signal is 1 kHz Sine, unless otherwise noted.
Filter used for 8 Ω = 22 µH + 0.68 µF, Filter used for 6 Ω = 15 µH + 0.68 µF, Filter used for 4 Ω = 10 µH + 0.68 µF unless otherwise noted.



NOTE: Thermal Limits are referenced to TAS5760xxEVM Rev D

Figure 1. Output Power vs PVDD

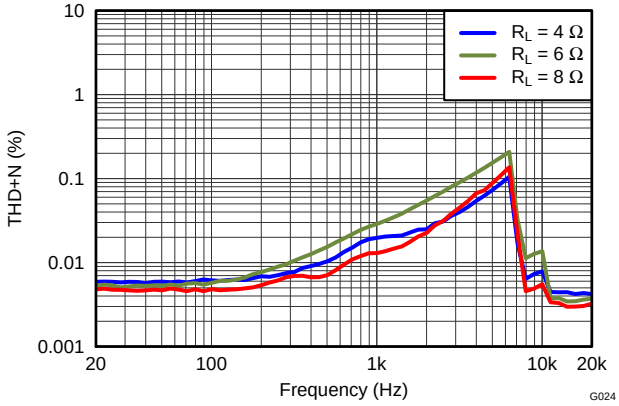


Figure 2. THD+N vs Frequency with PVDD = 12 V, P_{OSPK} = 1 W

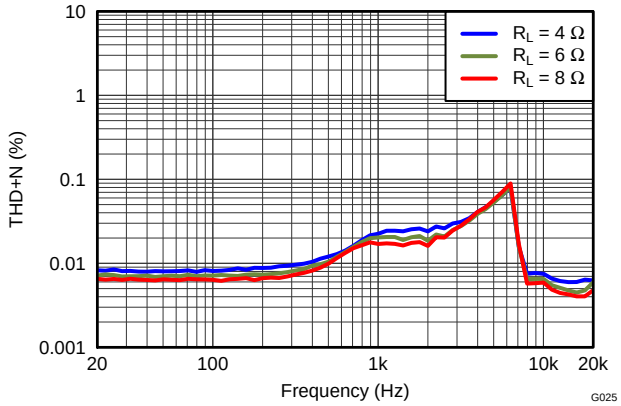


Figure 3. THD+N vs Frequency with PVDD = 12 V, P_{OSPK} = 1 W

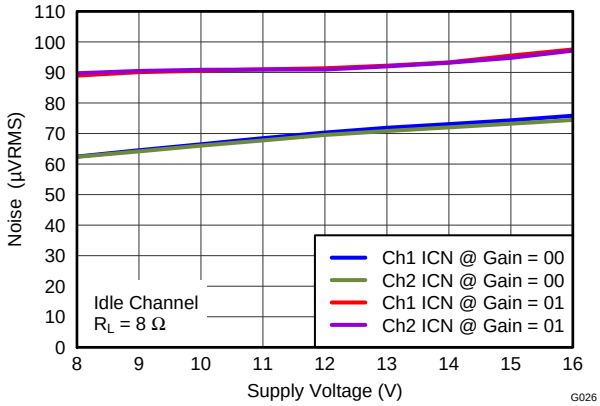


Figure 4. Idle Channel Noise vs PVDD

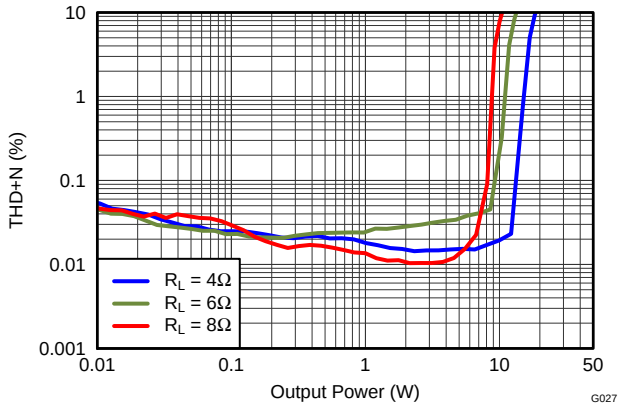


Figure 5. THD+N vs Output Power with PVDD = 12 V, Both Channels Driven

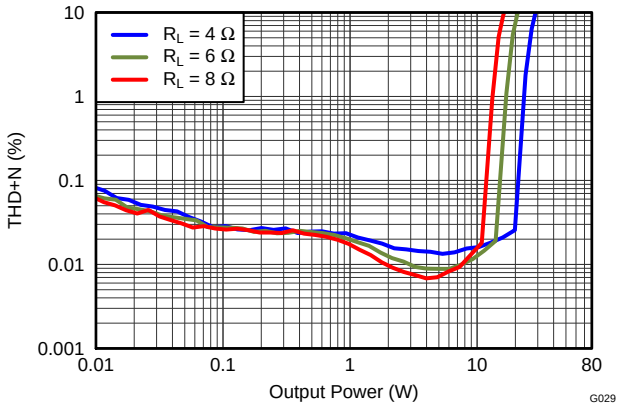


Figure 6. THD+N vs Output Power with PVDD = 12 V, Both Channels Driven

TYPICAL SPEAKER AMPLIFIER PERFORMANCE CHARACTERISTICS (Stereo BTL Mode) (continued)

At T_A = 25°C, f_{SPK_AMP} = 384kHz, input signal is 1 kHz Sine, unless otherwise noted.

Filter used for 8 Ω = 22 µH + 0.68 µF, Filter used for 6 Ω = 15 µH + 0.68 µF, Filter used for 4 Ω = 10 µH + 0.68 µF unless otherwise noted.

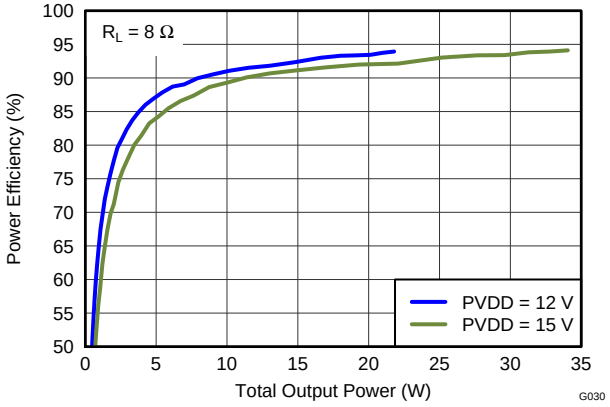


Figure 7. Efficiency vs Output Power

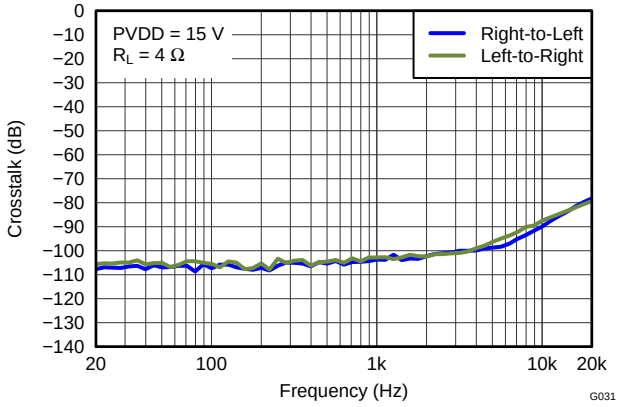


Figure 8. Crosstalk vs Frequency

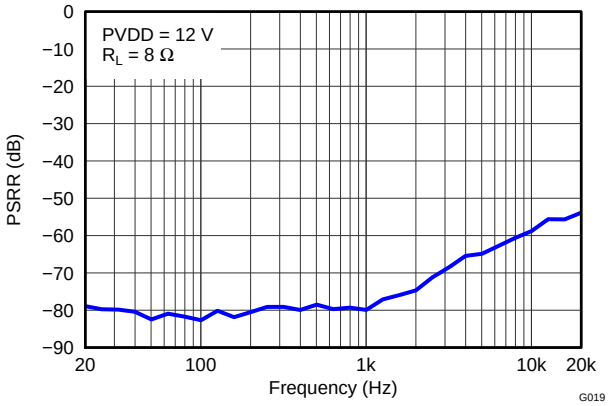


Figure 9. PVDD PSRR vs Frequency

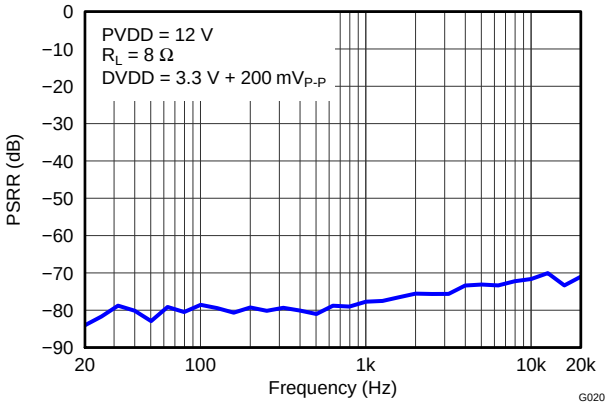


Figure 10. DVDD PSRR vs Frequency

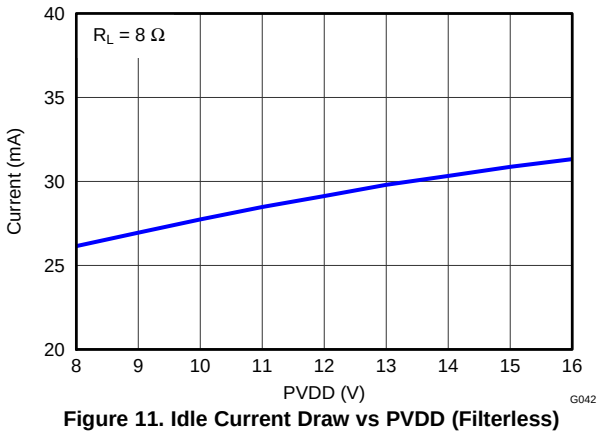


Figure 11. Idle Current Draw vs PVDD (Filterless)

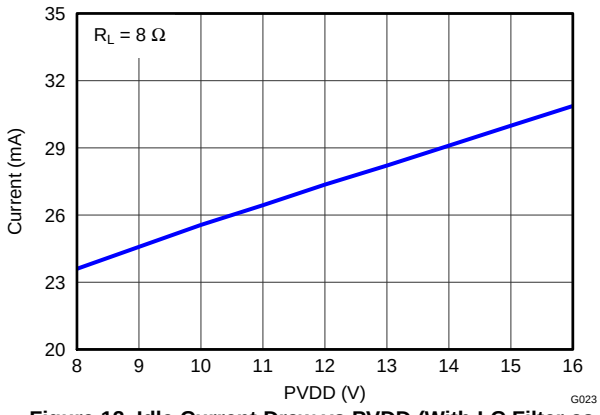


Figure 12. Idle Current Draw vs PVDD (With LC Filter as shown on the EVM)

TYPICAL SPEAKER AMPLIFIER PERFORMANCE CHARACTERISTICS (Stereo BTL Mode) (continued)

At T_A = 25°C, f_{SPK_AMP} = 384kHz, input signal is 1 kHz Sine, unless otherwise noted.

Filter used for 8 Ω = 22 µH + 0.68 µF, Filter used for 6 Ω = 15 µH + 0.68 µF, Filter used for 4 Ω = 10 µH + 0.68 µF unless otherwise noted.

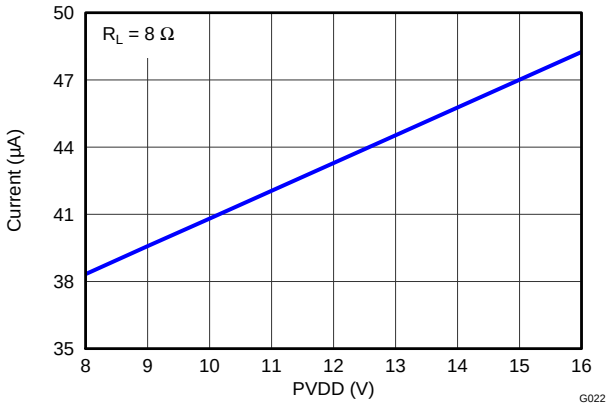
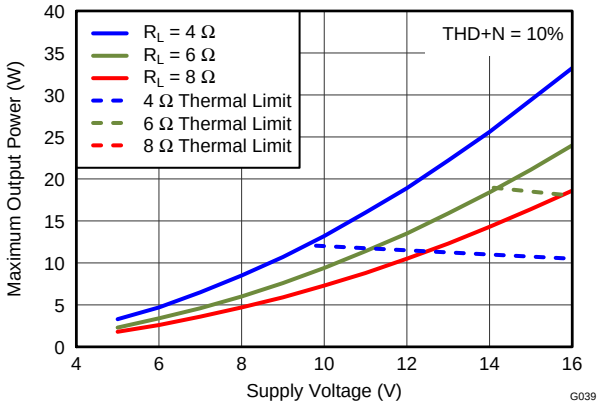


Figure 13. Shutdown Current Draw vs PVDD (Filterless)

TYPICAL SPEAKER AMPLIFIER PERFORMANCE CHARACTERISTICS (Stereo BTL Mode) (continued)

At T_A = 25°C, f_{SPK_AMP} = 768 kHz, input signal is 1 kHz Sine, unless otherwise noted.
Filter used for 8 Ω = 22 µH + 0.68 µF, Filter used for 6 Ω = 15 µH + 0.68 µF, Filter used for 4 Ω = 10 µH + 0.68 µF unless otherwise noted.



NOTE: Thermal Limits are referenced to TAS5760xxEVM Rev D

Figure 14. Output Power vs PVDD

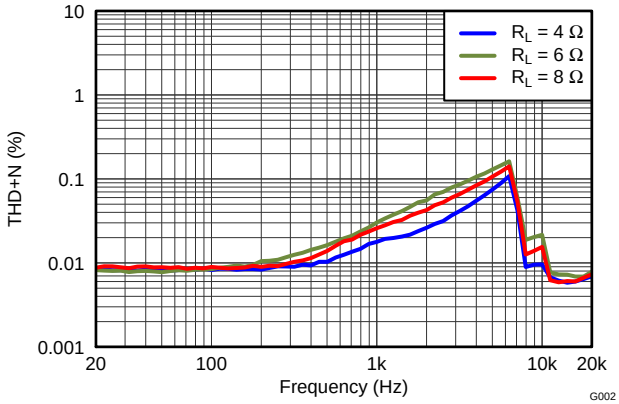


Figure 15. THD+N vs Frequency with PVDD = 12 V, P_{OSPK} = 1 W

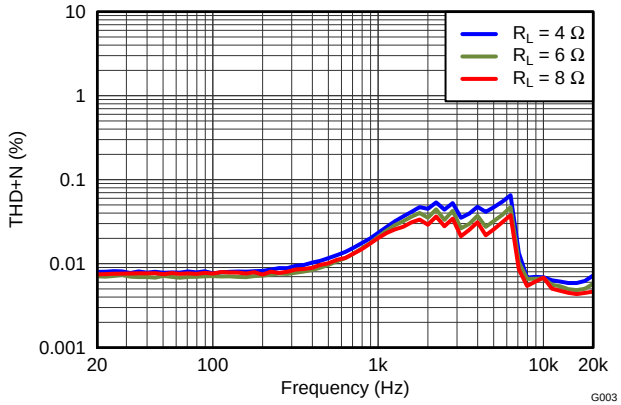


Figure 16. THD+N vs Frequency with PVDD = 12 V, P_{OSPK} = 1 W

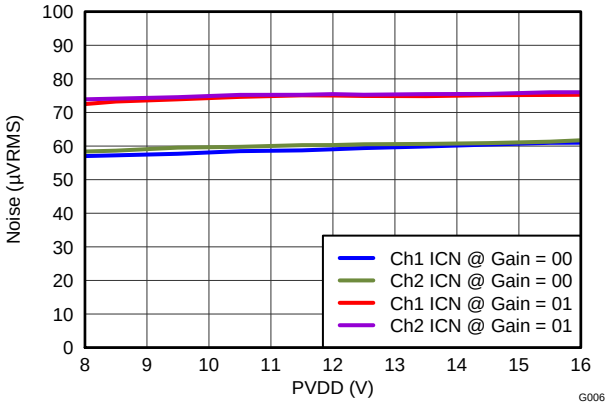


Figure 17. Idle Channel Noise vs PVDD

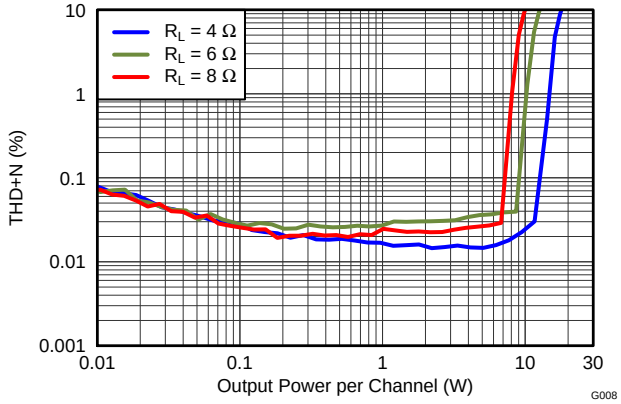


Figure 18. THD+N vs Output Power with PVDD = 12 V, Both Channels Driven

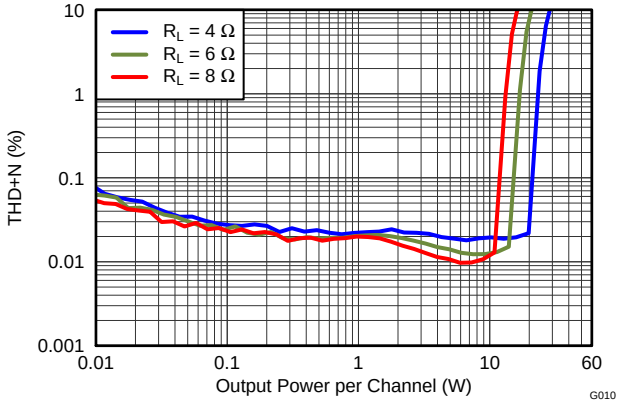


Figure 19. THD+N vs Output Power with PVDD = 12 V, Both Channels Driven

TYPICAL SPEAKER AMPLIFIER PERFORMANCE CHARACTERISTICS (Stereo BTL Mode) (continued)

At T_A = 25°C, f_{SPK_AMP} = 768 kHz, input signal is 1 kHz Sine, unless otherwise noted.

Filter used for 8 Ω = 22 µH + 0.68 µF, Filter used for 6 Ω = 15 µH + 0.68 µF, Filter used for 4 Ω = 10 µH + 0.68 µF unless otherwise noted.

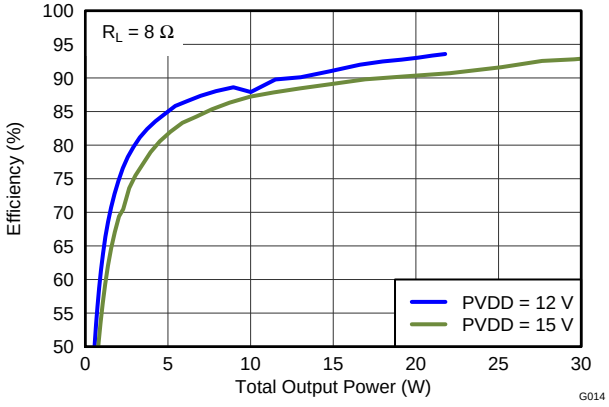


Figure 20. Efficiency vs Output Power

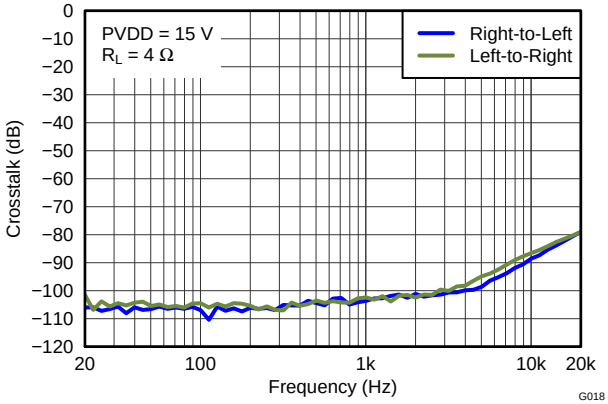


Figure 21. Crosstalk vs Frequency

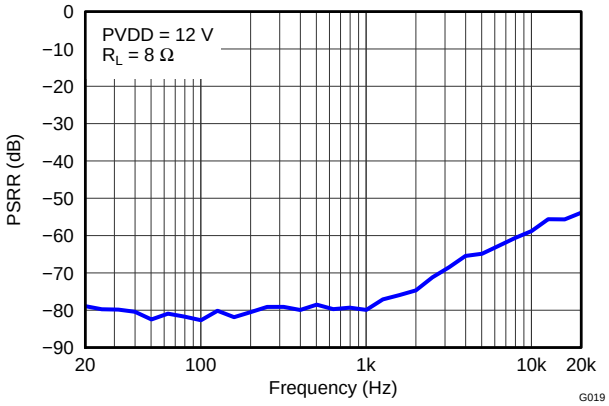


Figure 22. PVDD PSRR vs Frequency

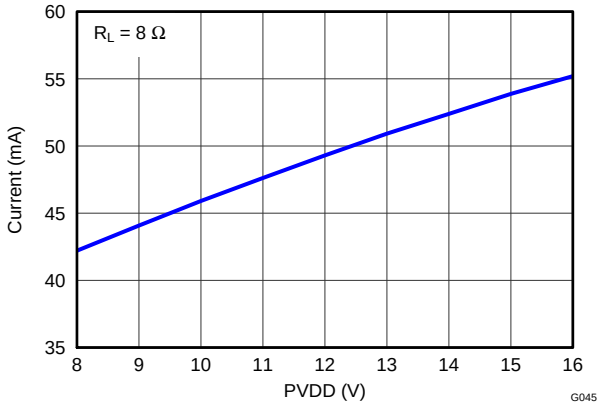


Figure 23. Idle Current Draw vs PVDD (Filterless)

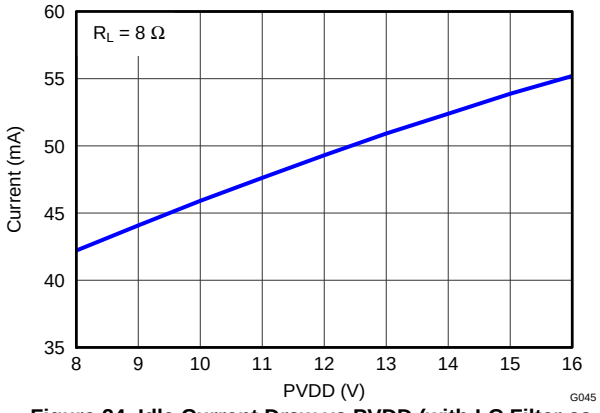


Figure 24. Idle Current Draw vs PVDD (with LC Filter as shown on EVM)

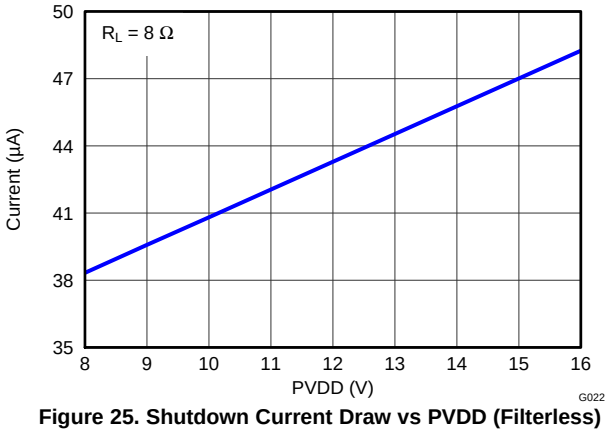


Figure 25. Shutdown Current Draw vs PVDD (Filterless)

TYPICAL PERFORMANCE CHARACTERISTICS (Mono PBTL Mode)

At T_A = 25°C, f_{SPK_AMP} = 384 kHz, input signal is 1 kHz Sine unless otherwise noted.

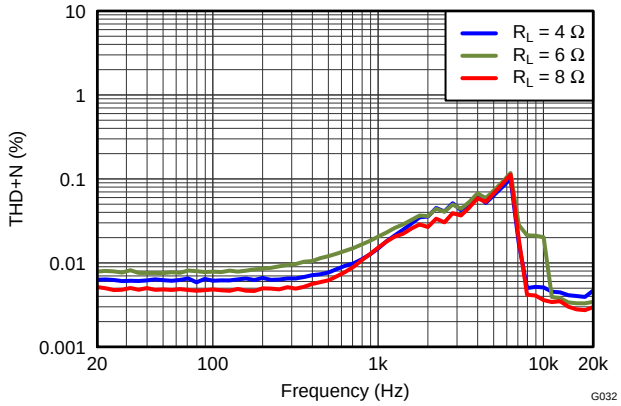


Figure 26. THD+N vs Frequency with PVDD = 12 V, P_{OSPK} = 1 W

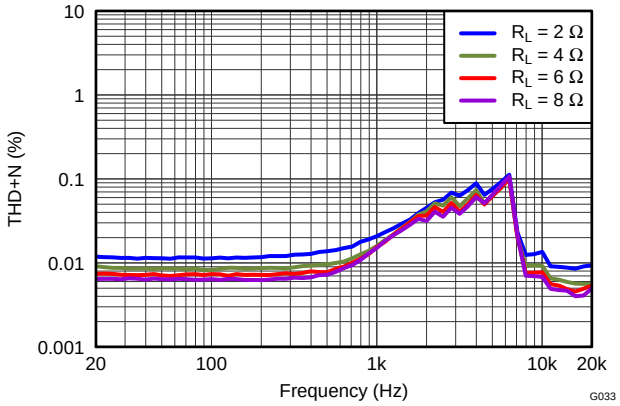


Figure 27. THD+N vs Frequency with PVDD = 12 V, P_{OSPK} = 1 W

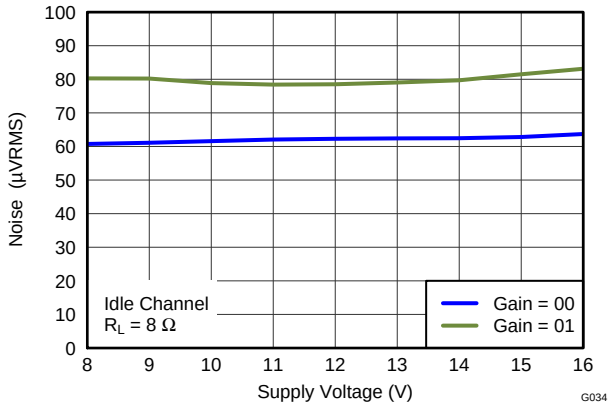


Figure 28. Idle Channel Noise vs PVDD

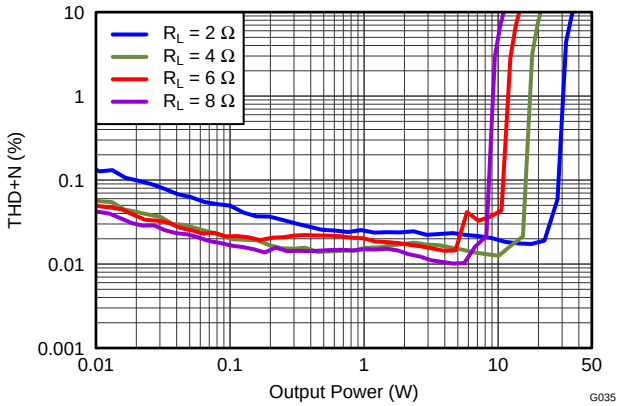


Figure 29. THD+N vs Output Power with PVDD = 12 V with 1 kHz Sine Input

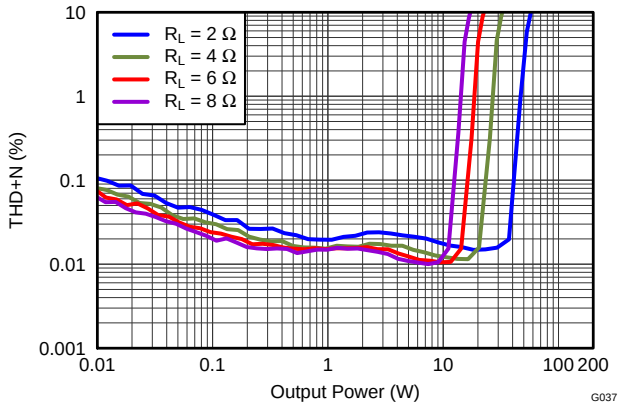


Figure 30. THD+N vs Output Power with PVDD = 12 V with 1 kHz Sine Input

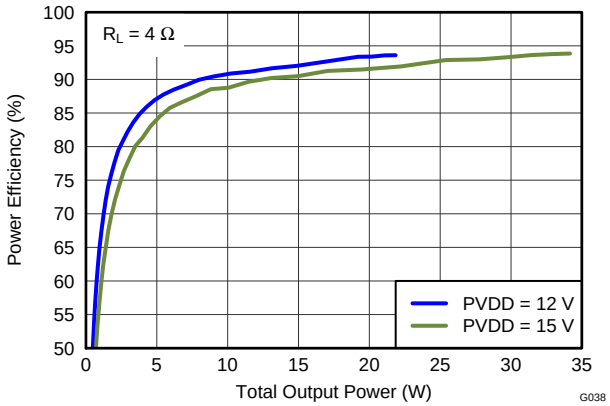


Figure 31. Efficiency vs Output Power

TYPICAL PERFORMANCE CHARACTERISTICS (Mono PBTL Mode) (continued)

At T_A = 25°C, f_{SPK_AMP} = 768 kHz, input signal is 1 kHz Sine unless otherwise noted.

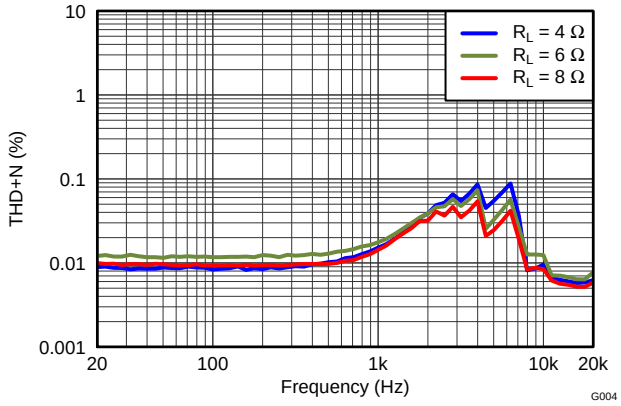


Figure 32. THD+N vs Frequency with PVDD = 12 V, P_{OSPK} = 1 W

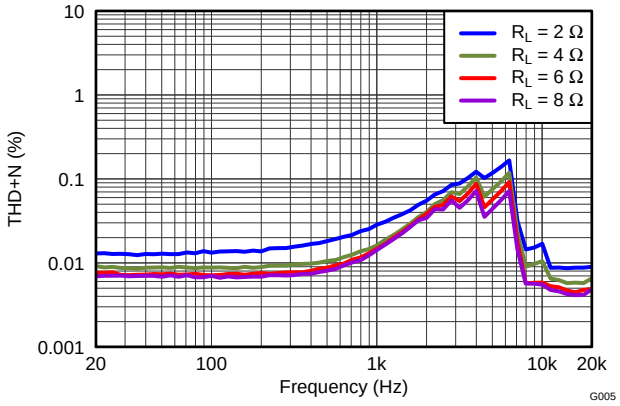


Figure 33. THD+N vs Frequency with PVDD = 12 V, P_{OSPK} = 1 W

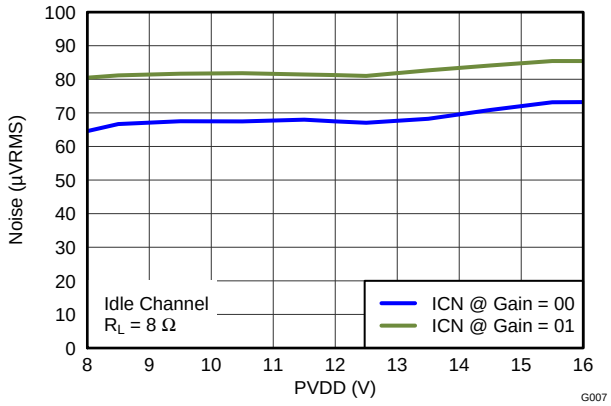


Figure 34. Idle Channel Noise vs PVDD

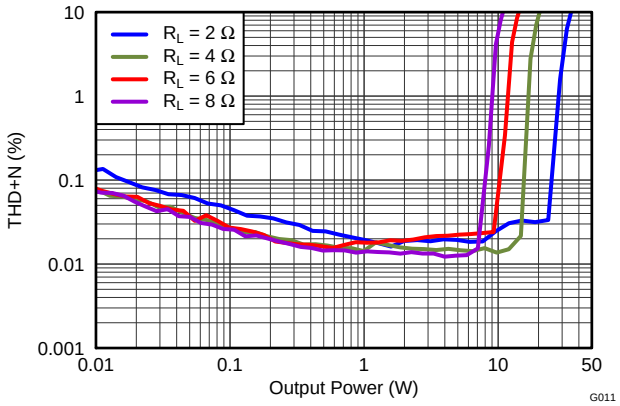


Figure 35. THD+N vs Output Power with PVDD = 12 V

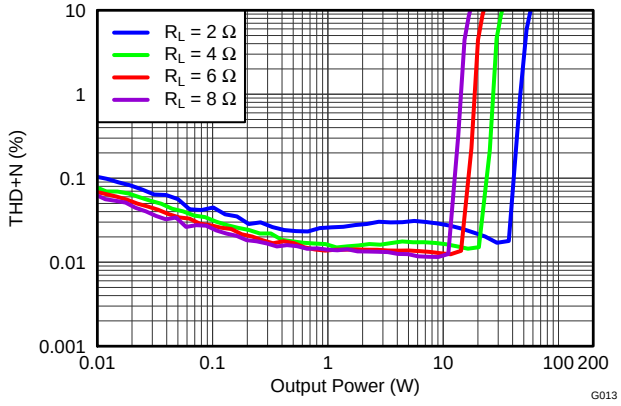


Figure 36. THD+N vs Output Power with PVDD = 12 V

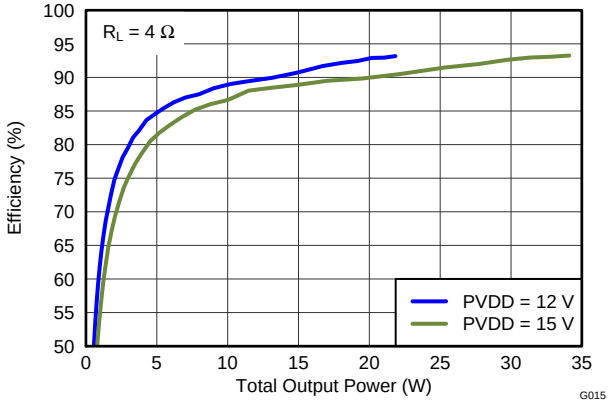
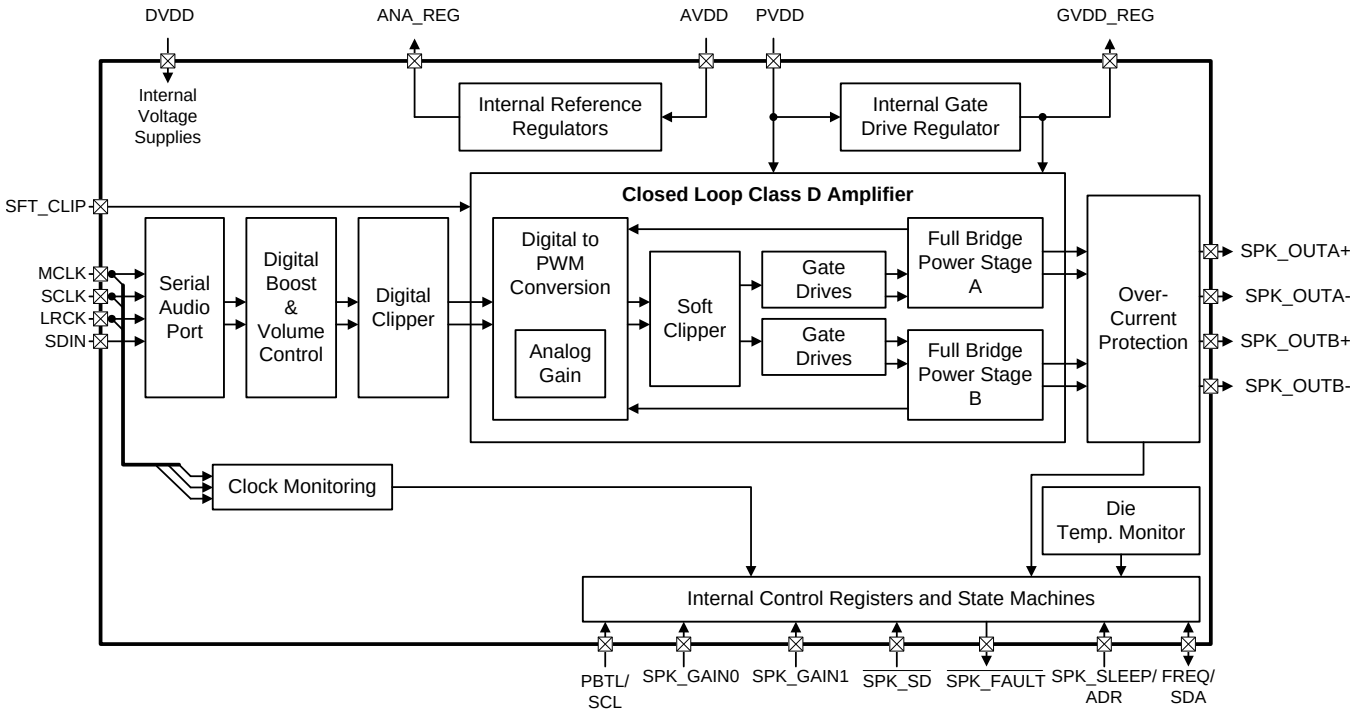


Figure 37. Efficiency vs Output Power

Theory of Operation and Detailed Description



Device Overview and Summary

The TAS5760L is a flexible and easy to use stereo Class D speaker amplifier with an I²S input serial audio port. The TAS5760L supports a variety of audio clock configurations via two speed modes. In Hardware Control mode, the device only operates in single-speed mode. When used in Software Control mode, the device can be placed into double speed mode to support higher sample rates, such as 88.2kHz and 96kHz. The outputs of the TAS5760L can be configured to drive two speakers in stereo Bridge Tied Load (BTL) mode or a single speaker in Parallel Bridge Tied Load (PBTL) mode.

Only two power supplies are required for the TAS5760L. They are a 3.3V power supply, called VDD, for the small signal analog and digital and a higher voltage power supply, called PVDD, for the output stage of the speaker amplifier. To enable use in a variety of applications, PVDD can be operated over a large range of voltages, as specified in the Recommended Operating Conditions table.

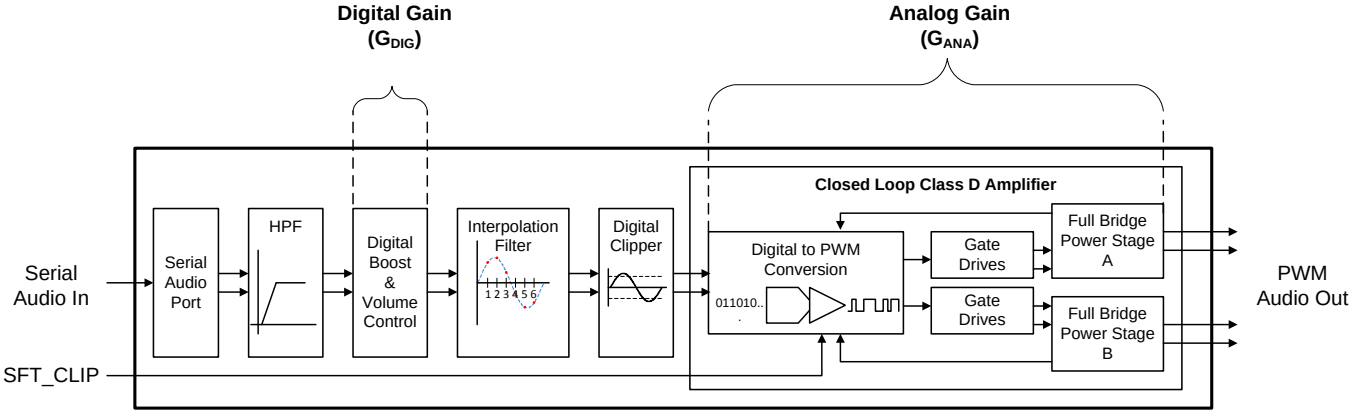
To configure and control the TAS5760L, two methods of control are available. In Hardware Control Mode, the configuration and real-time control of the device is accomplished through hardware control pins. In Software Control mode, the I²C control port is used both to configure the device and for real-time control. In Software Control Mode, several of the hardware control pins remain functional, such as the $\overline{\text{SPK\_SD}}$, $\overline{\text{SPK\_FAULT}}$, and SFT_CLIP pins.

Power Supplies

The power supply requirements for the TAS5760L consist of one 3.3V supply to power the low voltage analog and digital circuitry and one higher-voltage supply to power the output stage of the speaker amplifier. Several on-chip regulators are included on the TAS5760L to generate the voltages necessary for the internal circuitry of the audio path. It is important to note that the voltage regulators which have been integrated are sized only to provide the current necessary to power the internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs may result in reduced performance and damage to the device.

Speaker Amplifier Audio Signal Path

The block diagram for the TAS5760L's speaker amplifier is shown below. In Hardware Control mode, a limited subset of audio path controls are made available via external pins, which are pulled "HIGH" or "LOW" to configure the device. In Software Control Mode, the additional features and configurations are available. All of the available controls are discussed in this section, and the subset of controls that available in Hardware Control Mode are discussed in the respective section below.



Serial Audio Port (SAP)

The serial audio port (SAP) receives audio in either I²S, Left Justified, or Right Justified formats. In Hardware Control mode, the device operates only in 32, 48 or 64 x f_S I²S mode. In Software Control mode, additional options for left-justified and right justified audio formats are available. The supported clock rates and ratios for Hardware Control Mode and Software Control Mode are detailed in their respective sections below.

I²S Timing

I²S timing uses LRCK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCK is "LOW" for the left channel and "HIGH" for the right channel. A bit clock, called SCLK, runs at 32, 48, or 64 × f_S and is used to clock in the data. There is a delay of one bit clock from the time the LRCK signal changes state to the first bit of data on the data lines. The data is presented in 2's-complement form (MSB-first) and is valid on the rising edge of bit clock.

Left-Justified

Left-justified (LJ) timing also uses LRCK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCK is "HIGH" for the left channel and "LOW" for the right channel. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. The first bit of data appears on the data lines at the same time LRCK toggles. The data is written MSB-first and is valid on the rising edge of the bit clock. The TAS5760L can accept digital words from 16 to 24 bits wide and pads any unused trailing data-bit positions in the L/R frame with zeros before presenting the digital word to the audio signal path.

Right-Justified

Right-justified (RJ) timing also uses LRCK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCK is "HIGH" for the left channel and "LOW" for the right channel. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. The first bit of data appears on the data 8 bit-clock periods (for 24-bit data) after LRCK toggles. In RJ mode the LSB of data is always clocked by the last bit clock before LRCK transitions. The data is written MSB-first and is valid on the rising edge of bit clock. The TAS5760L pads unused leading data-bit positions in the left/right frame with zeros before presenting the digital word to the audio signal path.

DC Blocking Filter

Excessive DC content in the audio signal can damage loudspeakers and even small amounts of DC offset in the signal path cause cause audible artifacts when muting and unmuting the speaker amplifier. For these reasons, the amplifier employs two separate DC blocking methods for the speaker amplifier. The first is a high-pass filter provided at the front of the data path to remove any DC from incoming audio data before it is presented to the audio path. The -3dB corner frequencies for the filter are specified in the speaker amplifier electrical characteristics table. In Hardware Control mode, the DC blocking filter is active and cannot be disabled. In Software Control mode, the filter can be bypassed by writing a 1 to bit 7 of register 0x02. The second method is a DC detection circuit that will shutdown the power stage and issue a latching fault if DC is found to be present on the output due to some internal error of the device. This DC Error (DCE) protection is discussed in the Protection Circuitry section below.

Digital Boost and Volume Control

Following the high-pass filter, a digital boost block is included to provide additional digital gain if required for a given application as well as to set an appropriate clipping point for a given GAIN[1:0] pin configuration when in Hardware Control mode. The digital boost block defaults to +6dB when the device is in Hardware Mode. In most use cases, the digital boost block will remain unchanged when operating the device in Software Control mode, as the volume control offers sufficient digital gain for most applications. The TAS5760L's digital volume control operates from Mute to +24dB, in steps of 0.5dB. The equation below illustrates how to set the 8-bit volume control register at address 0x04:

$$\text{DVC [Hex Value]} = 0xCF + (\text{DVC [dB]} / 0.5\ \text{[dB]}) \quad (1)$$

Transitions between volume settings will occur at a rate of 0.5dB every 8 LRCK cycles to ensure no audible artifacts occur during volume changes. This volume fade feature can be disabled via Bit 7 of the Volume Control Configuration Register.

Digital Clipper

A digital clipper is integrated in the oversampled domain to provide a component-free method to set the clip point of the speaker amplifier. Via the "Digital Clipper Level x" controls in the I²C control port, the point at which the oversampled digital path clips can be set directly, which in turns sets the 10% THD+N operating point of the amplifier. This is useful for applications in which a single system is designed for use in several end applications that have different power rating specifications. Its place in the oversampled domain ensures that the digital clipper is acoustically appealing and reduces or eliminates tones which would otherwise foldback into the audio band during clipping events. The block diagram of the digital clipper is shown below:

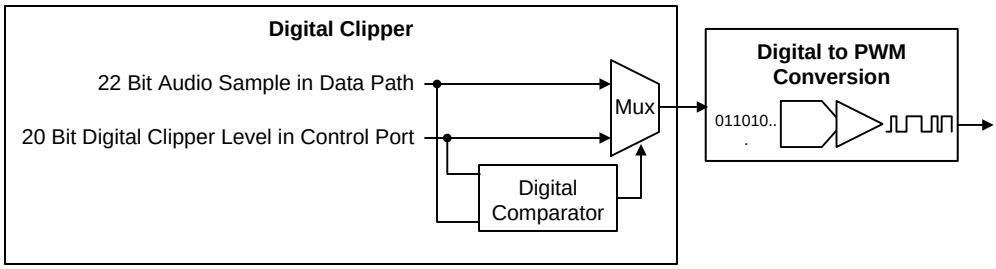


Figure 38. Digital Clipper Simplified Block Diagram

As mentioned previously, the audio signature of the amplifier when the digital clipper is active is very smooth, owing to its place in the signal chain. The typical behavior of the clipping events are shown in the screen shot below.

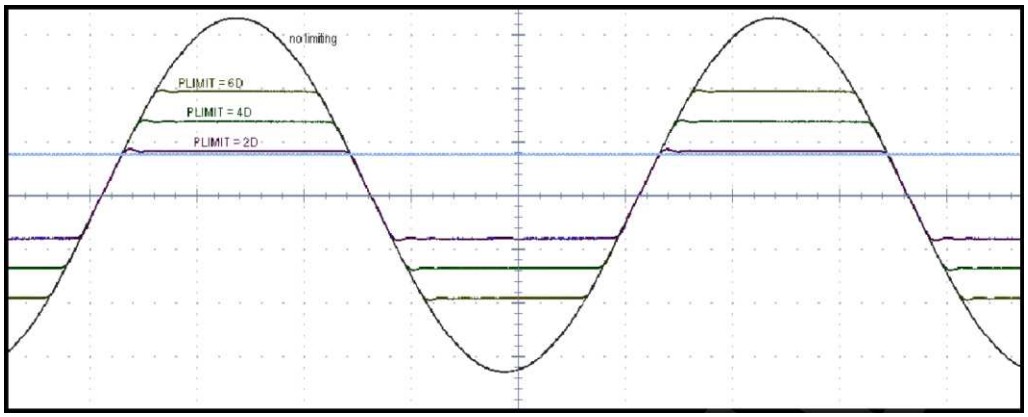


Figure 39. Digital Clipper Example Waveform for various settings of Digital Clip Level [19:0]

It is important to note that the actual signal developed across the speaker will be determined not only by the digital clipper, but also the analog gain of the amplifier. Depending on the analog gain settings and the PVDD level applied, clipping could occur as a result of the voltage swing that is determined by the gain being larger than the available PVDD supply rail. The gain structures are discussed in detail below for both Hardware Control Mode and Software Control Mode.

Closed Loop Class-D Amplifier

Following the digital clipper, the interpolated audio data is next sent to the Closed Loop Class-D amplifier, whose first stage is Digital to PWM Conversion (DPC) block. In this block, the stereo audio data is translated into two pairs of complimentary pulse width modulated (PWM) signals which are used to drive the outputs of the speaker amplifer. Feedback loops around the DPC ensure constant gain across supply voltages, reduce distortion, and increase immunity to power supply injected noise and distortion. The analog gain is also applied in the Class-D amplifier section of the device. The gain structures are discussed in detail below for both Hardware Control Mode and Software Control Mode.

The switching rate of the amplifier is configurable in both Hardware Control Mode and Software Control Mode. In both cases, the PWM switching frequency is a multiple of the sample rate. This behavior is described in the respective Hardware Control Mode and Software Control Mode sections below.

Speaker Amplifier Protection Suite

The speaker amplifier in the TAS5760L includes a robust suite of error handling and protection features. It is protected against Over-Current, Under-Voltage, Over-Voltage, Over-Temperature, DC, and Clock Errors. The status of these errors is reported via the $\overline{\text{SPK\_FAULT}}$ pin and the appropriate error status register in the I²C Control Port. The error or handling behavior of the device is characterized as being either "Latching" or "Non-Latching" depending on what is required to clear the fault and resume normal operation (that is playback of audio).

For latching errors, the $\overline{\text{SPK\_SD}}$ pin or the $\overline{\text{SPK\_SD}}$ bit in the control port must be toggled in order to clear the error and resume normal operation. If the error is still present when the $\overline{\text{SPK\_SD}}$ pin or bit transitions from "LOW" back to "HIGH", the device will again detect the error and enter into a fault state resulting in the error status bit being set in the control port and the $\overline{\text{SPK\_FAULT}}$ line being pulled "LOW". If the error has been cleared (for example, the temperature of the device has decreased below the error threshold) the device will attempt to resume normal operation after the $\overline{\text{SPK\_SD}}$ pin or bit is toggled and the required fault time out period ($T_{\overline{\text{SPK\_FAULT}}}$) has passed. If the error is still present, the device will once again enter a fault state and must be placed into and brought back out of shutdown in order to attempt to clear the error.

For non-latching errors, the device will automatically resume normal operation (that is playback) once the error has been cleared. The non-latching errors, with the exception of clock errors will not cause the $\overline{\text{SPK\_FAULT}}$ line to be pulled "LOW". It is not necessary to toggle the $\overline{\text{SPK\_SD}}$ pin or bit in order to clear the error and resume normal operation for non-latching errors. Table 1 details the types of errors protected by the TAS5760L's Protection Suite and how each are handled.

Speaker Amplifier Fault Notification ($\overline{\text{SPK\_FAULT}}$ Pin)

In both hardware and Software Control mode, the $\overline{\text{SPK\_FAULT}}$ pin of the TAS5760L serves as a fault indicator to notify the system that a fault has occurred with the speaker amplifier by being actively pulled "LOW". This pin is an open drain output pin and, unless one is provided internal to the receiver, requires an external pull-up to set the net to a known value. The behavior of this pin varies based upon the type of error which has occurred.

In the case of a latching error, the fault line will remain "LOW" until such time that the TAS5760L has resumed normal operation (that is the $\overline{\text{SPK\_SD}}$ pin has been toggled and $T_{\overline{\text{SPK\_FAULT}}}$ has passed).

With the exception of clock errors, non-latching errors will not cause the $\overline{\text{SPK\_FAULT}}$ pin to be pulled "LOW". Once a non-latching error has been cleared, normal operation will resume. For clocking errors, the SPK_FAULT line will be pulled "LOW", but upon clearing of the clock error normal operation will resume automatically, i.e. with no $T_{\overline{\text{SPK\_FAULT}}}$ delay.

One method which can be used to convert a latching error into an auto-recovered, non-latching error is to connect the $\overline{\text{SPK\_FAULT}}$ pin to the $\overline{\text{SPK\_SD}}$ pin. In this way, a fault condition will automatically toggle the $\overline{\text{SPK\_SD}}$ pin when the $\overline{\text{SPK\_FAULT}}$ pin goes "LOW" and returns "HIGH" after the $T_{\overline{\text{SPK\_FAULT}}}$ period has passed.

Table 1. Protection Suite Error Handling Summary

Error	Cause	Fault Type	Error is cleared by:
Over Voltage Error (OVE)	PVDD level rises above that specified by OVE_{RTHRES}(PVDD)	Non-Latching ($\overline{\text{SPK\_FAULT}}$ Pin is not pulled "LOW")	PVDD level returning below $OVE_{THRES(PVDD)}$
Under Voltage Error (UVE)	PVDD voltage level drops below that specified by $UVE_{FTHRES(SPK)}$	Non-Latching ($\overline{\text{SPK\_FAULT}}$ Pin is not pulled "LOW")	PVDD level returning above $UVE_{THRES(PVDD)}$
Clock Error (CLKE)	One or more of the following errors has occured: 1. Non-Supported MCLK to LRCK and/or SCLK to LRCK Ratio 2. Non-Supported MCLK or LRCK rate 3. MCLK, SCLK, or LRCK has stopped	Non-Latching ($\overline{\text{SPK\_FAULT}}$ Pin is pulled "LOW")	Clocks returning to valid state
Over-Current Error (OCE)	Speaker Amplifier output current has increased above the level specified by OCE_{THRES}	Latching	$T_{\overline{\text{SPK\_FAULT}}}$ has passed **AND** $\overline{\text{SPK\_SD}}$ Pin or Bit Toggle
DC Detect Error (DCE)	DC offset voltage on the speaker amplifier output has increased above the level specified by the DCE_{THRES}	Latching	$T_{\overline{\text{SPK\_FAULT}}}$ has passed **AND** $\overline{\text{SPK\_SD}}$ Pin or Bit Toggle
Over-Temperature Error (OTE)	The temperature of the die has increased above the level specified by the OTE_{THRES}	Latching	$T_{\overline{\text{SPK\_FAULT}}}$ has passed **AND** $\overline{\text{SPK\_SD}}$ Pin or Bit Toggle **AND** the temperature of the device has reached a level below that which is dictated by the OTE_{HYST} specification

DC DETECT PROTECTION

The TAS5760L has circuitry which will protect the speakers from DC current which might occur due to an internal amplifier error. The device behavior in response to a DCE event is detailed in the table in the previous section.

A DCE event occurs when the output differential duty-cycle of either channel exceeds 60% for more than 420 msec at the same polarity. The table below shows some examples of the typical DCE Protection threshold for several values of the supply voltage. This feature protects the speaker from large DC currents or AC currents less than 2Hz.

The minimum output offset voltages required to trigger the DC detect are show in Table 2. The outputs must remain at or above the voltage listed in the table for more than 420 msec to trigger the DC detect.

Table 2. DC Detect Threshold

PVDD [V]	$\|V_{OS}\|$- OUTPUT OFFSET VOLTAGE [V]
4.5	0.96
6	1.30
12	2.60

Hardware Control Mode

For systems which do not require the added flexibility of the I²C control port or do not have an I²C host controller, the TAS5760L can be used in Hardware Control Mode. In this mode of operation, the device operates in its default configuration and any changes to the device are accomplished via the hardware control pins, described below. The audio performance between Hardware and Software Control mode is identical, however more features and functionality are available when the device is operated in Software Control mode. The behavior of these Hardware Control Mode pins is described in the sections below.

Several static I/O's are present on the TAS5760L which are meant to be configured during PCB design and not changed during normal operation. Some examples of these are the GAIN[1:0] and PBTL/SCL pins. These pins are often referred to as being tied or pulled "LOW" or tied or pulled "HIGH". A pin which is tied or pulled "LOW" has been connected directly to the system ground. The TAS5760L is configured such that the most popular use cases for the device (that is BTL mode, 768kHz swicthing frequency, etc.) require the static I/O lines to be tied "LOW". This ensures optimum thermal performance as well as BOM reduction.

pins that are to be tied or pulled "HIGH" are connected to DVDD. For these pins, a pull-up resistor is recommended to limit the slew rate of the voltage which is presented to the pin during power up. Depending on the output impedance of the supply, and the capacitance connected to the DVDD net on the board, slew rates of this node could be high enough to trigger the integrated ESD protection circuitry at high current levels, causing damage to the device. It is not necessary to have a separate pull-up resistor for each static digital I/O pin. Instead, a single resistor can be connected to DVDD and all static I/O lines which are to be tied "HIGH" can be connected to that pull-up resistor. This connectivity is shown in the Typical Application Circuits. These pull-up resistors are not required when the digital I/O pins are driven by a controlled driver, such as a digital control line from a systems processor, as the output buffer in the system processor will ensure a controlled slew rate.

Speaker Amplifier Shut Down ($\overline{\text{SPK\_SD}}$ Pin)

In both Hardware and Software Control mode, the $\overline{\text{SPK\_SD}}$ pin is provided to place the speaker amplifier into shutdown. Driving this pin "LOW" will place the device into shutdown, while pulling it "HIGH" (to DVDD) will bring the device out of shutdown. This is the lowest power consumption mode that the device can be placed in while the power supplies are up. If the device is placed into shutdown while in normal operation, an audible artifact may occur on the output. To avoid this, the device should first be placed into sleep mode, by pulling the SPK_SLEEP/ADR pin "HIGH" before pulling the $\overline{\text{SPK\_SD}}$ low.

Serial Audio Port in Hardware Control Mode

When used in Hardware Control Mode, the Serial Audio Port (SAP) accepts only I²S formatted data. Additionally, the device operates in Single-Speed Mode (SSM), which means that supported sample rates, MCLK rates, and SCLK rates are limited to those shown in the table below. Additional clocking options, including higher sample rates, are available when operating the device in Software Control Mode.

The tables below detail the supported SCLK rates for each of the available sample rate and MCLK rate configurations. For each f_S and MCLK rate, the supported SCLK rates are shown and are represented in multiples of the sample rate, which is written as "x f_S".

Table 3. Supported SCLK Rates in Hardware Control Mode (Single Speed Mode)

	MCLK Rate [x f_S]				
	128	192	256	384	512

Table 3. Supported SCLK Rates in Hardware Control Mode (Single Speed Mode) (continued)

Sample Rate [kHz]	**12**	N/S	N/S	N/S	N/S	32, 48, 64
	16	N/S	N/S	32, 48, 64	32, 48, 64	32, 48, 64
	24	N/S	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
	32	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
	38	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
	44.1	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
	48	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64

Soft Clipper Control (SFT_CLIP Pin)

The TAS5760L has a soft clipper that can be used to clip the output voltage level below the supply rail. When this circuit is active, the amplifier operates as if it was powered by a lower supply voltage, and thereby enters into clipping sooner than if the circuit wasn't active. The result is clipping behavior very similar to that of clipping at the PVDD rail, in contrast to the digital clipper behavior which occurs in the oversampled domain of the digital path. The point at which clipping begins is controlled by a resistor divider from GVDD_REG to ground, which sets the voltage at the SFT_CLIP pin. The precision of the threshold at which clipping occurs is dependent upon the voltage level at the SFT_CLIP pin. Because of this, increasing the precision of the resistors used to create the voltage divider, or using an external reference will increase the precision of the point at which the device enters into clipping. To ensure stability, and soften the edges of the clipping event, a capacitor should be connected from pin SFT_CLIP to ground.

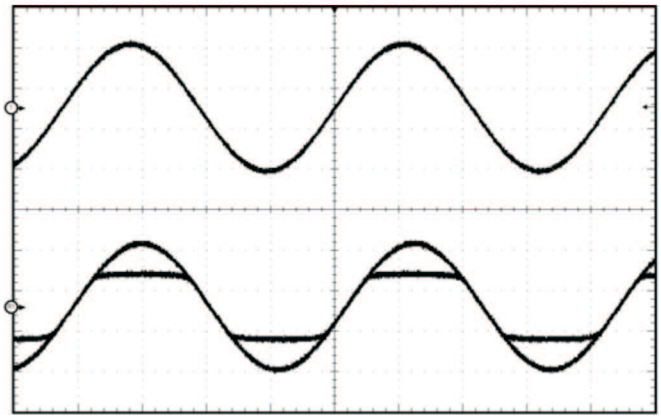


Figure 40. Soft Clipper Example Wave Form

To move the output stage into clipping, the soft clipper circuit limits the duty cycle of the output PWM pulses to a fixed maximum value. After filtering this limit applied to the duty cycle resembles a clipping event at a voltage below that of the PVDD level. The peak voltage level attainable when the soft clipper circuit is active, called V_P in the example below, is approximately 4 times the voltage at the SFT_CLIP pin, noted as V_{SFT_CLIP}. This voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance, as shown in the equation below.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{for unclipped power} \tag{2}$$

Where:

R_S is the total series resistance including $R_{DS(on)}$, and output filter resistance.
R_L is the load resistance.
V_P is the peak amplitude achievable when the soft clipper circuit is active (As mentioned previously, V_P = [4 x V_{SFT_CLIP}], provided that [4 x V_{SFT_CLIP}] < PVDD.)
P_{OUT} (10%THD) ≈ 1.25 × P_{OUT} (unclipped)

It should be noted that, if the PVDD level is below (4 x V_{SFT_CLIP}) clipping will occur due to clipping at PVDD before the clipping due to the soft clipper circuit becomes active.

Table 4. Soft Clipper Example

PVDD [V]	SFT_CLIP Pin Voltage [V]	Resistor to GND [kΩ]	Resistor to GVDD [kΩ]	Output Voltage [V_{rms}]
12	GVDD	(Open)	0	10.33
12	2.25	24	51	9.00
12	1.5	18	68	6.30

Speaker Amplifier Switching Frequency Select (FREQ/SDA Pin)

In Hardware Control mode, the PWM switching frequency of the TAS5760L is configurable via the FREQ/SDA pin. When connected to the system ground, the pin sets the output switching frequency to 16 × f_S. When connected to DVDD through a pull-up resistor, as shown in the Typical Application Circuits, the pin sets the output switching frequency to 8 × f_S. More switching frequencies are available when the TAS5760L is used in Software Control Mode.

Parallel Bridge Tied Load Mode Select (PBTL/SCL Pin)

The TAS5760L can be configured to drive a single speaker with the two output channels connected in parallel. This mode of operation is called Parallel Bridge Tied Load (PBTL) mode. This mode of operation effectively reduces the output impedance of the amplifier in half, which in turn reduces the power dissipated in the device due to conduction losses through the output FETs. Additionally, since the output channels are working in parallel, it also doubles the amount of current the speaker amplifier can source before hitting the over-current error threshold.

It should be noted that the device can be placed operated in PBTL mode in either Hardware Control Mode or in Software Control Mode, via the I²C Control Port. For instructions on placing the device in PBTL via the I²C Control Port, please see the Software Control Mode section of this document.

In order to place the TAS5760L into PBTL Mode when operating in Hardware Control Mode, the PBTL/SCL pin should be pulled "HIGH" (that is, connected to the DVDD supply through a pull-up resistor). If the device is to operate in BTL mode instead, the PBTL/SCL pin should be pulled "LOW", that is connected to the system supply ground. When operated in PBTL mode, the output pins should be connected as shown in the Typical Application Circuit Diagrams.

In PBTL mode, the amplifier selects its source signal from the left channel of the stereo signal presented on the SDIN line of the Serial Audio Port. In order to select the right channel of the stereo signal, the LRCK can be inverted in the processor that is sending the serial audio data to the TAS5760L.

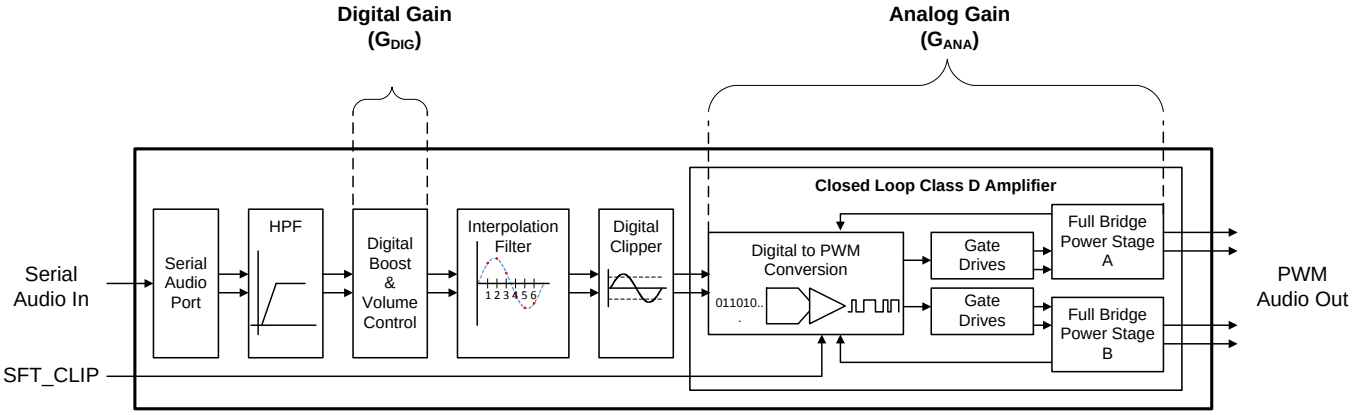
Speaker Amplifier Sleep Enable (SPK_SLEEP/ADR Pin)

In Hardware Control mode, pulling the SPK_SLEEP/ADR pin "HIGH" gracefully transitions the switching of the output devices to a non-switching state or "High-Z" state. This mode of operation is similar to mute in that no audio is present on the outputs of the device. However, unlike the 50/50 mute available in the I²C Control Port, sleep mode saves quiescent power dissipation by stopping the speaker amplifier output transitors from switching. This mode of operation saves quiescent current operation but keeps signal path blocks active so that normal operation can resume more quickly than if the device were placed into shutdown. It is recommended to place the device into sleep mode before stopping the audio signal coming in on the SDIN line or before bringing down the power supplies connected to the TAS5760L in order to avoid audible artifacts.

Speaker Amplifier Gain Select (SPK_GAIN [1:0] Pins)

In Hardware Control Mode, a combination of digital gain and analog gain is used to provide the overall gain of the speaker amplifier. The decode of the two pins "SPK_GAIN1" and "SPK_GAIN0" sets the gain of the speaker amplifier. Additionally, pulling both of the SPK_SPK_GAIN[1:0] pins "HIGH" places the device into software control mode.

As seen in the figure below, the audio path of the TAS5760L consists of a digital audio input port, a digital audio path, a digital to PWM converter (DPC), a gate driver stage, a Class D power stage, and a feedback loop which feeds the output information back into the DPC block to correct for distortion sensed on the output pins. The total amplifier gain is comprised of digital gain, shown as G_{DIG} in the digital audio path and the analog gain from the input of the analog modulator G_{ANA} to the output of the speaker amplifier power stage.



As shown above, the first gain stage for the speaker amplifier is present in the digital audio path. It consists of the volume control and the digital boost block. The volume control is set to 0dB by default and, in Hardware Control mode, it does not change. For all settings of the SPK_GAIN[1:0] pins, the digital boost block remains at +6 dB as analog gain block is transitioned through 19.2, 22.6, and 25 dBV.

The gain configurations provided in Hardware Control mode were chosen to align with popular power supply levels found in many consumer electronics and to balance the trade-off between maximum power output before clipping and noise performance. These gain settings ensure that the output signal can be driven into clipping at those popular PVDD levels. If the power level required is lower than that which is possible with the PVDD level, a lower gain setting can be used. Additionally, if clipping at a level lower than the PVDD supply is desired, the digital clipper or soft clipper can be used.

The values of G_{DIG} and G_{ANA} for each of the SPK_GAIN[1:0] settings are shown in the table below. Additionally, the recommended PVDD level for each gain setting, along with the typical unclipped peak to peak output voltage swing for a 0dBFS input signal is provided. The peak voltage levels in the table below should only be used to understand the peak target output voltage swing of the amplifier if it had not been limited by clipping at the PVDD rail.

Table 5. Gain Structure for Hardware Control Mode

PVDD Level	Recommended SPK_GAIN[1:0] Pins Setting	Digital Boost [dB]	A_GAIN [dBV]	V_{Pk} Acheivable Voltage Swing (If output is not clipped at PVDD)
12	00	6	19.2	12.90
15	01	6	22.6	19.08
This setting is not recommended for voltages supported by the TAS5760L	10	6	25	This setting is not recommended for voltages supported by the TAS5760L
-	11	(Gain is controlled via I²C Port)		

Considerations for Setting the Speaker Amplifier Gain Structure

Configuration of the gain of the amplifier is important to the overall noise and output power performance of the TAS5760L. Higher gain settings mean that more power can be driven from an amplifier before it becomes voltage limited. Moreover, when output clipping "at the rail" is desired, it becomes important that there be enough voltage gain in the signal path to drive the output signal above the PVDD level in order to "clip" the output signal at the PVDD level in the output stage. Another desirable aspect of higher gain settings is that the dynamic headroom of an amplifier is increased with higher gain settings, which increases the overall dynamic audio quality of the signal being amplified.

With these advantages in mind, it may seem that setting the gain at the highest setting available would be appropriate. However, there are some drawbacks to having a gain that is set arbitrarily high. The first drawback is that a higher gain setting results in increased amplification of any noise that is present in the signal path. If the gain is set too high, and the speaker is sensitive enough, this may result in an audible "hiss" at the speakers when no audio is playing. Another consideration is that the speakers used in the system may not be rated for operation at the power levels which would be possible for the given PVDD supply that is present in the system. For this reason, it may be necessary to limit the voltage swing of the amplifier via a lower gain setting in order to reduce the voltage presented, and therefore, the power delivered, to the speaker.

Recommendations for Setting the Speaker Amplifier Gain Structure in Hardware Control Mode

1. Determine the maximum power target and the speaker impedance which is required for the application.
2. Calculate the required output voltage swing for the given speaker impedance which will deliver the target maximum power.
3. Chose the lowest gain setting via the SPK_GAIN[1:0] pins that produces an output voltage swing higher than the required output voltage swing for the target maximum power.

NOTE

A higher gain setting can be used, provided the noise performance is acceptable and the power delivered to the speaker remains within the safe operating area (SOA) of the speaker, using the soft clipper if necessary to set the clip point within the SOA of the speaker.

4. Characterize the clipping behavior of the system at the rated power.
   - If the system does not produce the target power before clipping that is required, increase the gain setting.
   - If the system meets the power requirements, but clipping is preferred at the rated power, use the soft clipper to set the clip point
   - If the system makes more power than is required but the noise performance is too high, consider reducing the gain.
5. Repeat Step 4 above until the optimum balance of power, noise, and clipping behavior is achieved.

Software Control Mode

The TAS5760L can be used in Hardware Control Mode or Software Control Mode. In order to place the device in software control mode, the two gain pins (GAIN[1:0]) should be pulled "HIGH". When this is done, the PBTL/SCL and FREQ/SDA pins are allocated to serve as the clock and data lines for the I²C Control Port.

Speaker Amplifier Shut Down ($\overline{\text{SPK\_SD}}$ Pin)

In both hardware and Software Control mode, the $\overline{\text{SPK\_SD}}$ pin is provided to place the speaker amplifier into shutdown. Driving this pin "LOW" will place the device into shutdown, while driving it "HIGH" (DVDD) will bring the device out of shutdown. This is the lowest power consumption mode that the device can be placed in while the power supplies are up. If the device is placed into shutdown while in normal operation, an audible artifact may occur on the output. To avoid this, the device should first be placed into sleep mode, by pulling the SPK_SLEEP/ADR pin "HIGH" before pulling the $\overline{\text{SPK\_SD}}$ low.

Serial Audio Port Controls

In Software Control mode, additional digital audio data formats and clock rates are made available via the I²C control port. With these controls, the audio format can be set to left justified, right justified, or I²S formatted data.

Serial Audio Port (SAP) Clocking

When used in Software Control mode, the device can be placed into double speed mode to support higher sample rates, such as 88.2kHz and 96kHz. The tables below detail the supported SCLK rates for each of the available sample rate and MCLK rate configurations. For each f_S and MCLK Rate the support SCLK rates are shown and are represented in multiples of the sample rate, which is written as "x f_S".

Table 6. Supported SCLK Rates in Single Speed Mode

		MCLK Rate [x f_S]				
		128	**192**	**256**	**384**	**512**
Sample Rate [kHz]	**12**	N/S	N/S	N/S	N/S	32, 48, 64
	16	N/S	N/S	32, 48, 64	32, 48, 64	32, 48, 64
	24	N/S	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
	32	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
	38	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
	44.1	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
	48	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64

Table 7. Supported SCLK Rates in Double Speed Mode

		MCLK Rate [x f_S]		
		128	**192**	**256**
Sample Rate [kHz]	**88.2**	32, 48, 64	32, 48, 64	32, 48, 64
	96	32, 48, 64	32, 48, 64	32, 48, 64

Parallel Bridge Tied Load Mode via Software Control

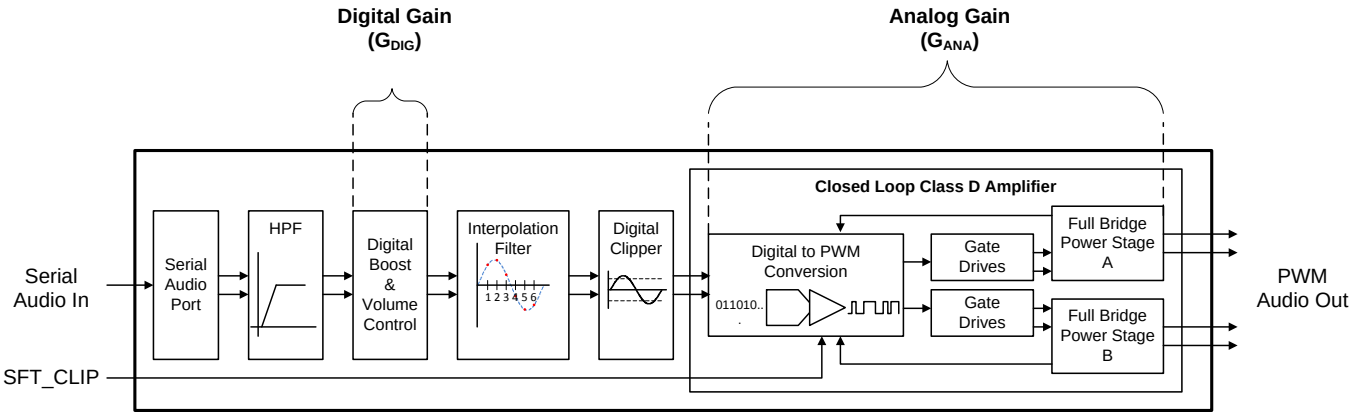
The TAS5760L can be configured to drive a single speaker with the two output channels connected in parallel. This mode of operation is called Parallel Bridge Tied Load (PBTL) mode. This mode of operation effectively reduces the on resistance of the amplifier in half, which in turn reduces the power dissipated in the device due to conduction losses through the output FETs. Additionally, since the output channels are working in parallel, it also doubles the amount of current the speaker amplifier can source before hitting the over-current error threshold.

It should be noted that the device can be placed operated in PBTL mode in either Hardware Control Mode or in Software Control Mode, via the I²C Control Port. For instructions on placing the device in PBTL via the PBTL/SCL Pin, please see the Hardware Control Mode section of this document.

In order to place the TAS5760L into PBTL Mode when operating in Software Control Mode, the Bit 7 of the Analog Control Register (0x06) should be set in the control port. This bit is cleared by default to configure the device for BTL mode operation. An additional control available in software mode control is PBTL Channel Select, which selects which of the two channels presented on the SDIN line will be used for the input signal for the amplifier. This is found at Bit 1 of the Analog Control Register (0x06). When operated in PBTL mode, the output pins should be connected as shown in the Typical Application Circuit Diagrams.

Speaker Amplifier Gain Structure

As seen below, the audio path of the TAS5760L consists of a digital audio input port, a digital audio path, a digital to analog converter, an analog modulator, a gate driver stage, a Class D power stage, and a feedback loop which feeds the output information back into the analog modulator to correct for distortion sensed on the output pins. The total amplifier gain is comprised of digital gain, shown as G_{DIG} in the digital audio path and the analog gain from the input of the analog modulator G_{ANA} to the output of the speaker amplifier power stage.



Speaker Amplifier Gain in Software Control Mode

The analog and digital gain are configured directly when operating in Software Control mode. It is important to note that the digital boost block is separate from the volume control. The digital boost block should be set before the speaker amplifier is brought out of mute and not changed during normal operation. In most cases, the digital boost can be left in its default configuration, and no further adjustment is necessary. As mentioned previously, the analog gain is directly set via the I²C control port in software control mode.

Considerations for Setting the Speaker Amplifier Gain Structure

Configuration of the gain of the amplifier is important to the overall noise and output power performance of the TAS5760L. Higher gain settings mean that more power can be driven from an amplifier before it becomes voltage limited. Moreover, when output clipping "at the rail" is desired, it becomes important that there be enough voltage gain in the signal path to drive the output signal above the PVDD level in order to "clip" the output signal at the PVDD level in the output stage. Another desirable aspect of higher gain settings is that the dynamic headroom of an amplifier is increased with higher gain settings, which increases the overall dynamic audio quality of the signal being amplified.

With these advantages in mind, it may seem that setting the gain at the highest setting available would be appropriate. However, there are some drawbacks to having a gain that is set arbitrarily high. The first drawback is that a higher gain setting results in increased amplification of any noise that is present in the signal path. If the gain is set too high, and the speaker is sensitive enough, this may result in an audible "hiss" at the speakers when no audio is playing. Another consideration is that the speakers used in the system may not be rated for operation at the power levels which would be possible for the given PVDD supply that is present in the system. For this reason it may be necessary to limit the voltage swing of the amplifier via a lower gain setting in order to reduce the voltage presented, and therefore the power delivered, to the speaker.

Recommendations for Setting the Speaker Amplifier Gain Structure in Software Control Mode

1. Determine the maximum power target and the speaker impedance which is required for the application.
2. Calculate the required output voltage swing for the given speaker impedance which will deliver the target maximum power.
3. Chose the lowest analog gain setting via the A_GAIN[3:2] bits in the control port which will produce an output voltage swing higher than the required output voltage swing for the target maximum power.

NOTE

A higher gain setting can be used, provided the noise performance is acceptable and the power delivered to the speaker remains within the safe operating area (SOA) of the speaker, using the soft clipper if necessary to set the clip point within the SOA of the speaker.

4. Characterize the clipping behavior of the system at the rated power.
   - If the system does not produce the target power before clipping that is required, increase the analog gain.
   - If the system meets the power requirements, but clipping is preferred at the rated power, use the soft clipper or the digital clipper to set the clip point
   - If the system makes more power than is required but the noise performance is too high, consider reducing the analog gain.
5. Repeat Step 4 above until the optimum balance of power, noise, and clipping behavior is achieved.

I²C Software Control Port

The TAS5760L includes an I²C control port for increased flexibility and extended feature set.

Setting the I²C Device Address

Each device on the I²C bus has a unique address that allows it to appropriately transmit and receive data to and from the I²C master controller. As part of the I²C protocol, the I²C master broadcast an 8-bit word on the bus that contains a 7-bit device address in the upper 7 bits and a read or write bit for the LSB. The TAS5760L has a configurable I²C address. The SPK_SLEEP/ADR can be used to set the device address of the TAS5760L. In Software Control mode, the seven bit I²C device address is configured as “110110x[$^{R}/_{W}$]”, where “x” corresponds to the state of the SPK_SLEEP/ADR pin at first power up sequence of the device. Upon application of the power supplies, the device latches in the value of the SPK_SLEEP/ADR pin for use in determining the I²C address of the device. If the SPK_SLEEP/ADR pin is tied "LOW" at power up (that is connected to the system ground), the device address will be set to 1101100[$^{R}/_{W}$]. If it is pulled "HIGH" (that is connected to the DVDD supply), the address will be set to 1101101[$^{R}/_{W}$] at power up.

General Operation of the I²C Control Port

The TAS5760L device has a bidirectional I²C interface that is compatible with the Inter IC (I²C) bus protocol and supports both 100-kHz and 400-kHz data transfer rates. This is a slave-only device that does not support a multimaster bus environment or wait-state insertion. The control interface is used to program the registers of the device and to read device status.

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially, one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most-significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is "HIGH" to indicate start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 41. The master generates the 7-bit slave address and the read/write (R/$\overline{W}$) bit to open communication with another device and then waits for an acknowledge condition. The TAS5760L holds SDA "LOW" during the acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence. All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pullup resistor must be used for the SDA and SCL signals to set the "HIGH" level for the bus.

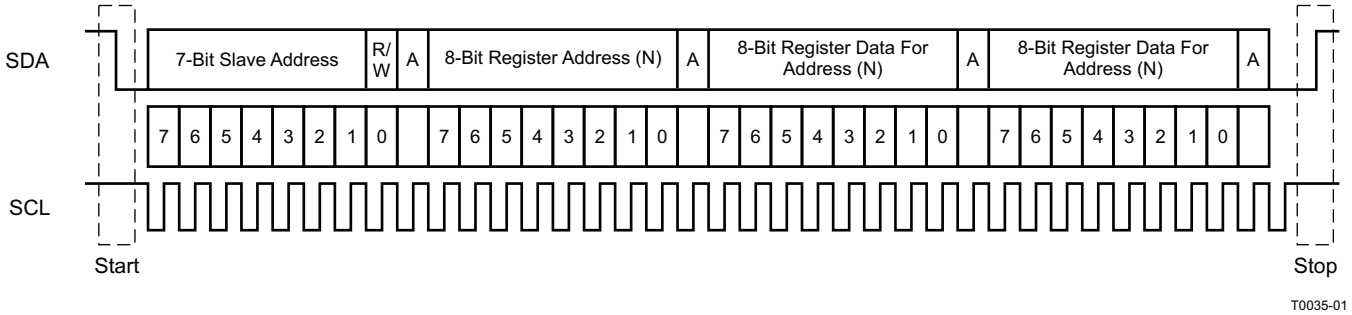


Figure 41. Typical I²C Sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 41.

Writing to the I²C Control Port

As shown in Figure 42, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C and the read/write bit. The read/write bit determines the direction of the data transfer. For a data-write transfer, the read/write bit is a 0. After receiving the correct I²C and the read/write bit, the TAS5760L responds with an acknowledge bit. Next, the master transmits the address byte corresponding to the TAS5760L register being accessed. After receiving the address byte, the TAS5760L again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5760L again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

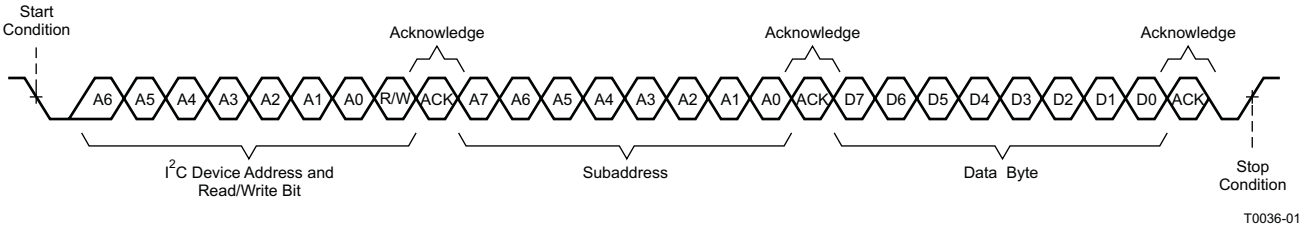


Figure 42. Write Transfer

Reading from the I²C Control Port

As shown in Figure 43, a data-read transfer begins with the master device transmitting a start condition, followed by the I²C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal register to be read. As a result, the read/write bit becomes a 0. After receiving the TAS5760L address and the read/write bit, TAS5760L responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the TAS5760L address and the read/write bit again. This time, the read/write bit becomes a 1, indicating a read transfer. After receiving the address and the read/write bit, the TAS5760L again responds with an acknowledge bit. Next, the TAS5760L transmits the data byte from the register being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the data-read transfer.

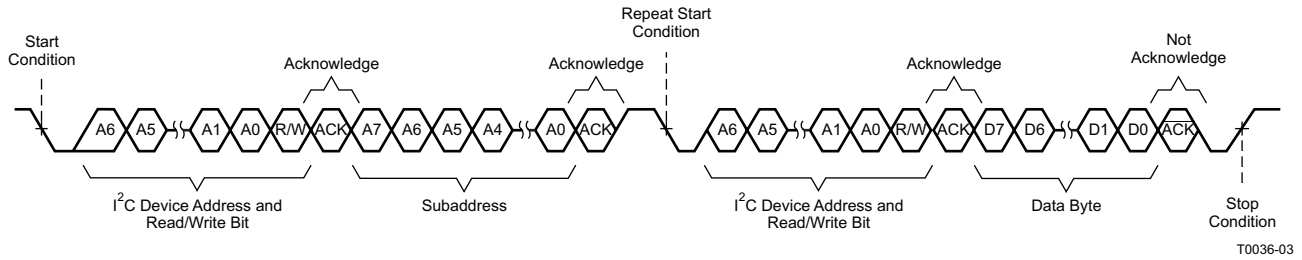


Figure 43. Read Transfer

Table 8. Control Port Quick Reference Table

Adr. (Dec)	Adr. (Hex)	Register Name	Default (Binary)								Default (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
0	0	Device Identification	Device Identification								0x00
			0	0	0	0	0	0	0	0	
1	1	Power Control	DigClipLev[19:14]						SPK_SLEEP	$\overline{\text{SPK\_SD}}$	0xFD
			1	1	1	1	1	1	0	1	
2	2	Digital Control	HPF Bypass	Reserved	Digital Boost		$\overline{\text{SS}}$/DS	Serial Audio Input Format			0x14
			0	0	0	1	0	1	0	0	
3	3	Volume Control Configuration	Fade	Reserved	Reserved	Reserved	Reserved	Reserved	Mute R	Mute L	0x80
			1	0	0	0	0	0	0	0	
4	4	Left Channel Volume Control	Volume Left								0xCF
			1	1	0	0	1	1	1	1	
5	5	Right Channel Volume Control	Volume Right								0xCF
			1	1	0	0	1	1	1	1	
6	6	Analog Control	PBTL Enable	PWM Rate Select			A_GAIN		PBTL Ch Sel	Reserved	0x51
			0	1	0	1	0	0	0	1	
7	7	Reserved	Reserved	Reserved	Reserved		Reserved	Reserved	Reserved	Reserved	0x00
			0	0	0	0	0	0	0	0	
8	8	Fault Configuration and Error Status	Reserved		OCE Thres		CLKE	OCE	DCE	OTE	0x00
			0	0	0	0	0	0	0	0	
9	9	Reserved	-	-	-	-	-	-	-	-	-
...		Reserved	-	-	-	-	-	-	-	-	-
15	F	Reserved	-	-	-	-	-	-	-	-	-
16	10	Digital Clipper 2	DigClipLev[13:6]								0xFF
			1	1	1	1	1	1	1	1	
17	11	Digital Clipper 1	DigClipLev[5:0]								0xFC
			1	1	1	1	1	1	0	0	

Control Port Detailed Register Description

Device Identification (0 / 0x00)

Device Identification [7:0] (Read Only)	0000000
TAS5760Lx	00000001

Power Control (1 / 0x01)

DigClipLev[19:14] [7:2] (R/W)	1111110 1
The digital clipper is decoded from 3 registers- DigClipLev[19:14], DigClipLev[13:6], and DigClipLev[5:0]. DigClipLev[19:14], shown here, represents the upper 6 bits of the total of 20 bits that are used to set the Digital Clipping Threshold.	(decoded)

Sleep Mode [1] (R/W)	1111111 0
Device is not in sleep mode	- - - - - - 0 -
Device is placed in sleep mode (In this mode, the power stage is disabled to reduce quiescent power consumption over a 50/50 duty cycle mute, while low-voltage blocks remain on standby. This reduces the time required to resume playback when compared with entering and exiting full shut down.)	- - - - - - 1 -

Speaker Shutdown [0] (R/W)	1111111 0
Speaker amplifier is shut down (This is the lowest power mode available when the device is connected to power supplies. In this mode, circuitry in both the DVDD and PVDD domain are powered down to minimize power consumption.)	- - - - - - - 0
Speaker amplifier is not shut down	- - - - - - - 1

Digital Control (2 / 0x02)

High-Pass Filter Bypass [7] (R/W)	0 0010100
The internal high-pass filter in the digital path is not bypassed.	0 - - - - - - -
The internal high-pass filter in the digital path is bypassed.	1 - - - - - - -

Reserved [6] (Read Only)	0 0 010100
This control is reserved and must not be changed from its default setting.	- 0 - - - - - -

Digital Boost [5:4] (R/W)	00 01 0100
+0 dB is added to the signal in the digital path	- - 0 0 - - - -
+6 dB is added to the signal in the digital path	- - 0 1 - - - -
+12 dB is added to the signal in the digital path	- - 1 0 - - - -
+18 dB is added to the signal in the digital path	- - 1 1 - - - -

Single Speed / Double Speed Mode Select	0001 0 100
Serial Audio Port will accept single speed sample rates (that is 32kHz, 44.1kHz, 48kHz)	- - - - 0 - - -
Serial Audio Port will accept double speed sample rates (that is 64kHz, 88.2kHz, 96kHz)	- - - - 1 - - -

Serial Audio Input Format	00010 100
Serial Audio Input Format is 24 Bits, Right Justified	- - - - - 0 0 0
Serial Audio Input Format is 20 Bits, Right Justified	- - - - - 0 0 1
Serial Audio Input Format is 18 Bits, Right Justified	- - - - - 0 1 0
Serial Audio Input Format is 16 Bits, Right Justified	- - - - - 0 1 1
Serial Audio Input Format is I²S	- - - - - 1 0 0
Serial Audio Input Format is 16-24 Bits, Left Justified	- - - - - 1 0 1
Settings above 101 are reserved and must not be used	> - - - - - 1 0 1

Volume Control Configuration (3 / 0x03)

Volume Fade Enable [7] (R/W)	10000000
Volume fading is disabled	0 - - - - - - -
Volume fading is enabled	1 - - - - - - -

Reserved [6:2] (Read Only)	10000000
This control is reserved and must not be changed from its default setting.	- - - - - - - -

Mute Right Channel [1] (R/W)	10000100
The right channel is not muted	- - - - - - 0 -
The right channel is muted (In software mute, most analog and digital blocks remain active and the speaker amplifier outputs transition to a 50/50 duty cycle.)	- - - - - - 1 -

Mute Left Channel [0] (R/W)	10000000
The left channel is not muted	- - - - - - - 0
The left channel is muted (In software mute, most analog and digital blocks remain active and the speaker amplifier outputs transition to a 50/50 duty cycle.)	- - - - - - - 1

Left Channel Volume Control (4 / 0x04)

Left/Right Channel Volume Control [7:0] (R/W)	11001111
Channel Volume is +24 dB	11111111
Channel Volume is +23.5 dB	11111110
Channel Volume is +23.0 dB	11111101
...	...
Channel Volume is 0 dB	11001111
...	...
Channel Volume is -100 dB	00000111
Any setting less than 00000111 places the channel in Mute	< 00000111

Right Channel Volume Control (5 / 0x05)

Left/Right Channel Volume Control [7:0] (R/W)	11001111
Channel Volume is +24 dB	11111111
Channel Volume is +23.5 dB	11111110
Channel Volume is +23.0 dB	11111101
...	...
Channel Volume is 0 dB	11001111
...	...
Channel Volume is -100 dB	00000111
Any setting less than 00000111 places the channel in Mute	< 00000111

Analog Control (6 / 0x06)

PBTL Enable [7] (R/W)	01010001
Device is placed in BTL mode	0 - - - - - - -
Device is placed in PBTL mode	1 - - - - - - -

PWM Rate Select [6:4] (R/W)	01010001
Output switching rate of the Speaker Amplifier is 6 * LRCK	- 0 0 0 - - - -
Output switching rate of the Speaker Amplifier is 8 * LRCK	- 0 0 1 - - - -
Output switching rate of the Speaker Amplifier is 10 * LRCK	- 0 1 0 - - - -
Output switching rate of the Speaker Amplifier is 12 * LRCK	- 0 1 1 - - - -
Output switching rate of the Speaker Amplifier is 14 * LRCK	- 1 0 0 - - - -
Output switching rate of the Speaker Amplifier is 16 * LRCK	- 1 0 1 - - - -
Output switching rate of the Speaker Amplifier is 20 * LRCK	- 1 1 0 - - - -
Output switching rate of the Speaker Amplifier is 24 * LRCK	- 1 1 1 - - - -
Please note that all rates listed above are valid for single speed mode. For double speed mode, switching frequency is half of that represented above.	

A_GAIN[3:2] (R/W)	01010001
Analog Gain Setting is 19.2 dBV	- - - - 0 0 - -
Analog Gain Setting is 22.6 dBV	- - - - 0 1 - -
Analog Gain Setting is 25 dBV	- - - - 1 0 - -
This setting is reserved and must not be used	- - - - 1 1 - -

Channel Selection for PBTL Mode [1] (R/W)	01010001
When placed in PBTL mode, the audio information from the Left channel of the serial audio input stream is used by the speaker amplifier	- - - - - - 0 -
When placed in PBTL mode, the audio information from the Right channel of the serial audio input stream is used by the speaker amplifier	- - - - - - 1 -

Reserved [0] (R/W)	01010001
This control is reserved and must not be changed from its default setting.	- - - - - - - -

Reserved (7 / 0x07)

Reserved [7:0] (R/W)	00000000
Reserved	- - - - - - - -

Fault Configuration and Error Status (8 / 0x08)

Reserved [7:6] (R)	00000000
This control is reserved and must not be changed from its default setting.	- - - - - - - -

OCE Threshold [5:4] (R)	00000000
Threshold is set to the default level specified in the electrical characteristics table	- - 0 0 - - - -
Threshold is reduced to 75% of the evel specified in the electrical characteristics table	- - 0 1 - - - -
Threshold is reduced to 50% of the evel specified in the electrical characteristics table	- - 1 0 - - - -
Threshold is reduced to 25% of the evel specified in the electrical characteristics table	- - 1 1 - - - -

Clock Error Status [3] (R)	10000000
Clocks are valid and no error is currently detected	- - - - 0 - - -
A clock error is occuring (This error is non-latching, so intermittent clock errors will be cleared when clocks re-enter valid state and the device will resume normal operation automatically. This bit will likewise be cleared once normal operation resumes.)	- - - - 1 - - -

Over Current Error Status[2] (R)	10000000
The output current levels of the speaker amplifier outputs are below the OCE threshold	- - - - - 0 - -
The DC offset level of the outputs has exceeded the OCE threshold, causing an error (This is a latching error and SPK_SD must be toggled after an OCE event for the device to resume normal operation. This bit will remain "HIGH" until SPK_SD is toggled.)	- - - - - 1 - -

Output DC Error Status [1] (R)	10000000
The DC offset level of the speaker amplifier outputs are below the DCE threshold	- - - - - - 0 -
The DC offset level of the speaker amplifier outputs has exceeded the DCE threshold, causing an error (This is a latching error and SPK_SD must be toggled after an DCE event for the device to resume normal operation. This bit will remain "HIGH" until SPK_SD is toggled.)	- - - - - - 1 -

Over-Temperature Error Status[1] (R)	10000000
A clock error will occur if SCLK is stopped	- - - - - - - 0
The temperature of the die has exceeded the level specified in the electrical characteristics table. (This is a latching error and SPK_SD must be toggled for the device to resume normal operation. This bit will remain "HIGH" until SPK_SD is toggled.)	- - - - - - - 1

Reserved Controls (9 / 0x09) - (15 / 0x0F)

The controls in this section of the control port are reserved and must not be used.

Digital Clipper Control 2 (16 / 0x10)

DigClipLev[13:6] [7:0] (R/W)	11111111
The digital clipper is decoded from 3 registers- DigClipLev[19:14], DigClipLev[13:6], and DigClipLev[5:0]. DigClipLev[13:6], shown here, represents the [13:6] bits of the total of 20 bits that are used to set the Digital Clipping Threshold.	(decoded)

DigClipLev[5:0] [7:2] (R/W)	11111111
The digital clipper is decoded from 3 registers- DigClipLev[19:14], DigClipLev[13:6], and DigClipLev[5:0]. DigClipLev[13:6], shown here, represents the [5:0] bits of the total of 20 bits that are used to set the Digital Clipping Threshold.	(decoded)

Reserved [1:0] (R/W)	11111100
These controls are reserved and should not be changed from there default values	- - - - - - - -

APPLICATION INFORMATION

These typical connection diagrams highlight the required external components and system level connections for proper operation of the device in several popular use cases.

Each of these configurations can be realized using the Evaluation Modules (EVMs) for the device. These flexible modules allow full evaluation of the device in all available modes of operation. Additioanlly, some of the application circuits are available as reference designs and can be found on the TI website. Also see the TAS5760L's product page for information on ordering the EVM. Note that not all configurations are available as reference designs; however, any design variation can be supported by TI through schematic and layout reviews. Visit support.ti.com for additional design assistance. Also, join the audio amplifier discussion forum at http://e2e.ti.com.

TAS5760x Typical Application Circuits

These application circuits detail the recommended component selection and board configurations for the TAS5760M or TAS5760L device. Note that in Software Control mode, the clipping point of the amplifier and thus the "rated power" of the end equipment can be set using the digital clipper if desired. Additionally, if the sonic signature of the soft clipper is preferred, it can be used in addition to or in lieu of the digital clipper. The software control application circuit detailed in this section shows the soft clipper in its bypassed state, which results in a lower BOM count than when using the soft clipper. The trade-off between the sonic characteristics of the clipping events in the amplifier and BOM minimization can be chosen based upon the design goals related to the end product.

For further information regarding component selection, please refer tothe user guide provided with the device's EVM.

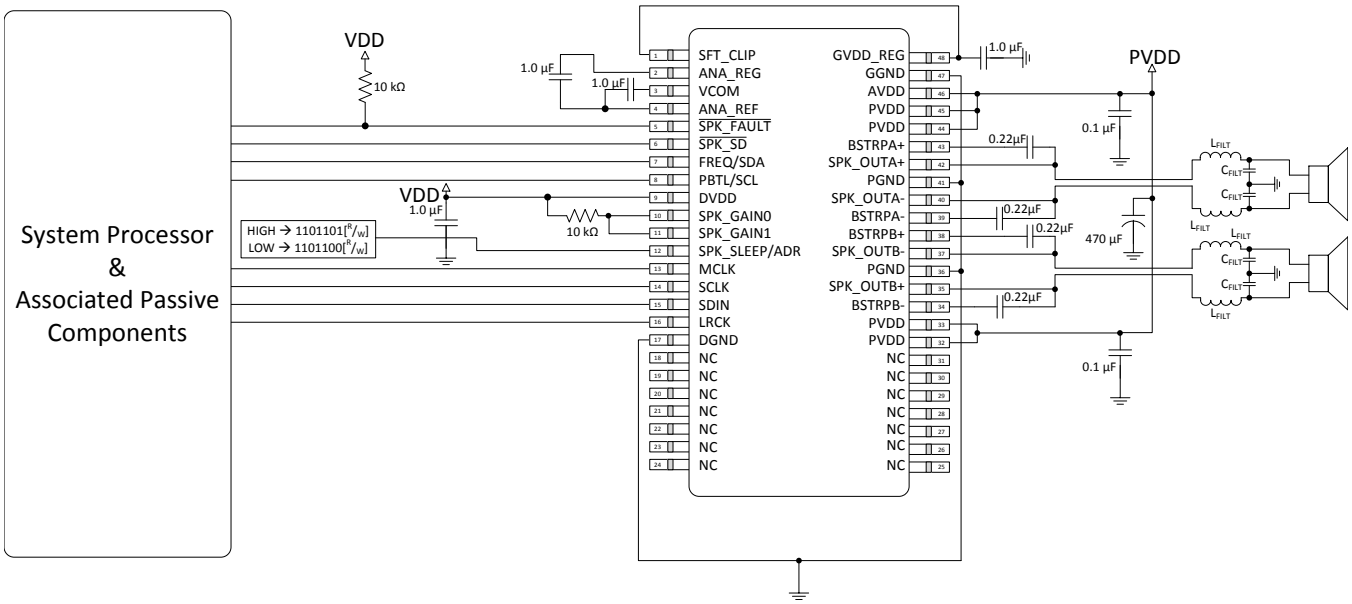


Figure 44. Stereo BTL using Software Control, 48 Pin DCA Package Option

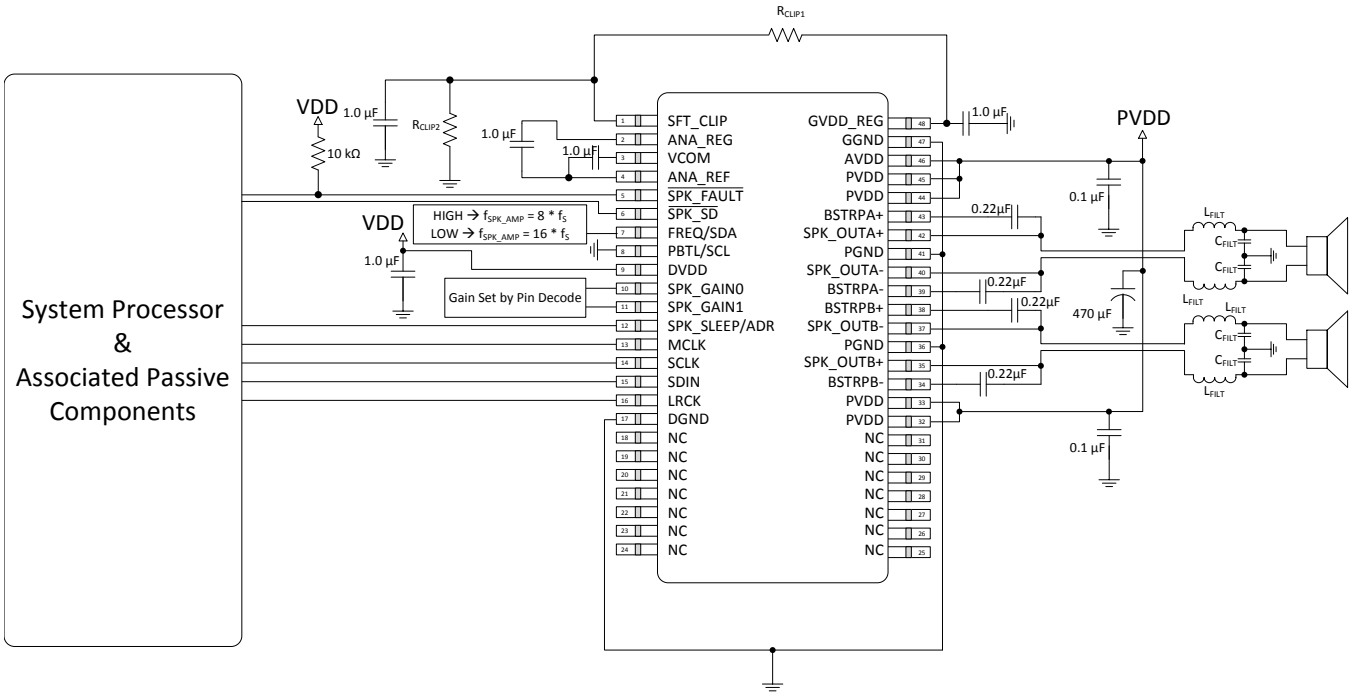


Figure 45. Stereo BTL using Hardware Control, 48 Pin DCA Package Option

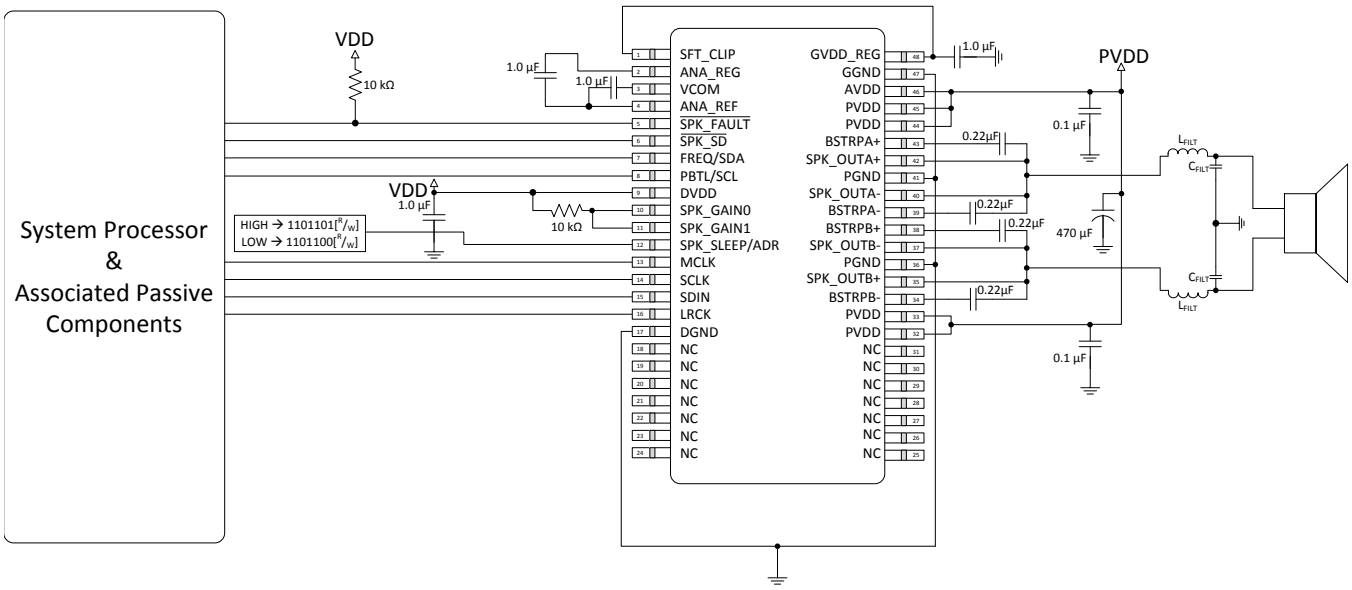


Figure 46. Mono PBTL using Software Control, 48 Pin DCA Package Option

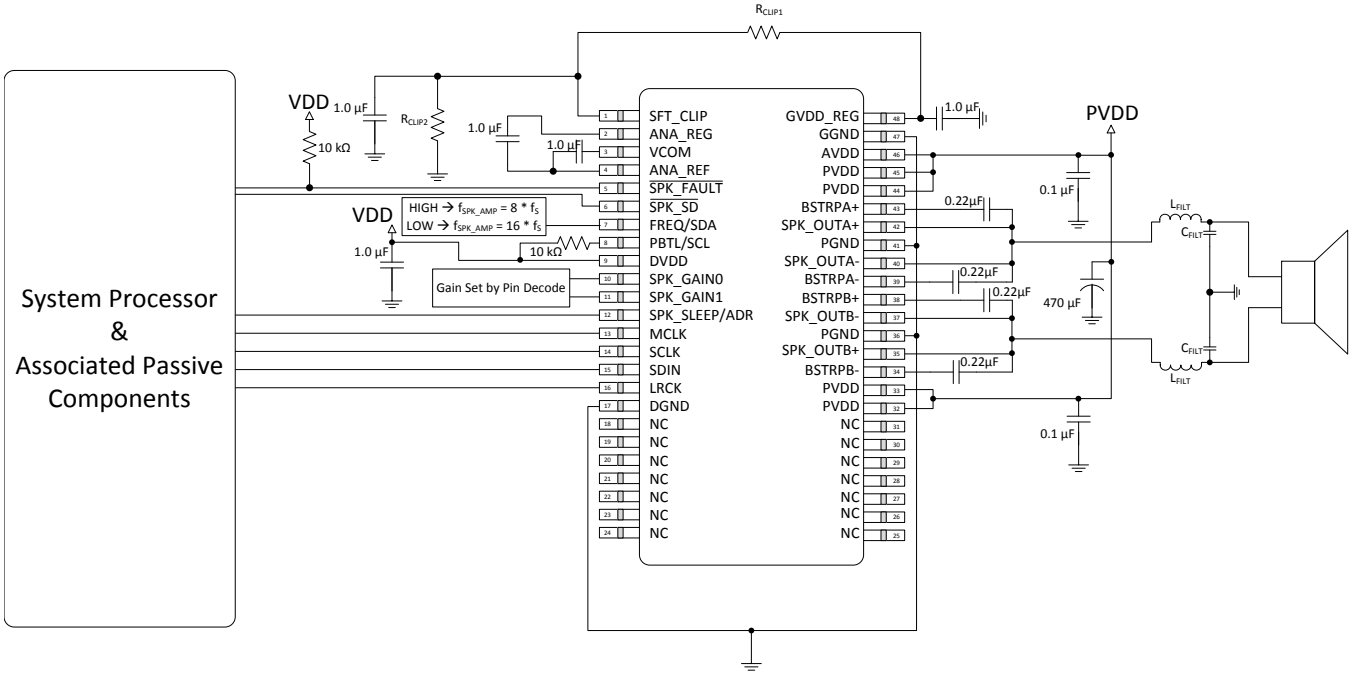


Figure 47. Mono PBTL using Hardware Control, 48 Pin DCA Package Option

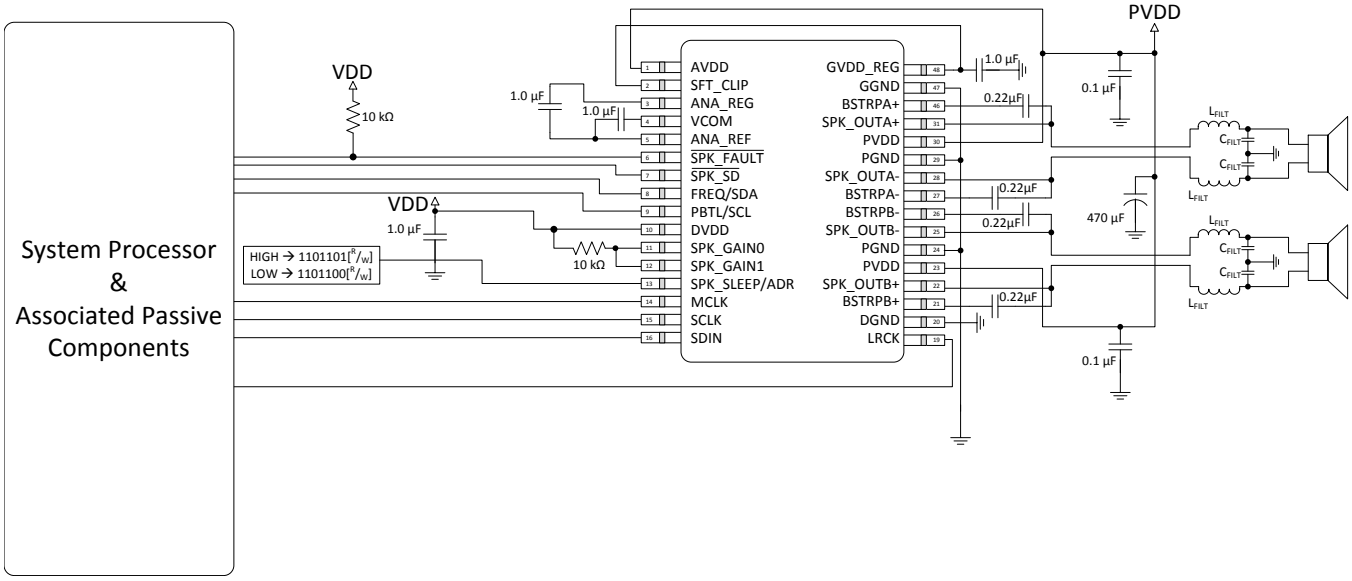


Figure 48. Stereo BTL using Software Control, 32 Pin DAP Package Option

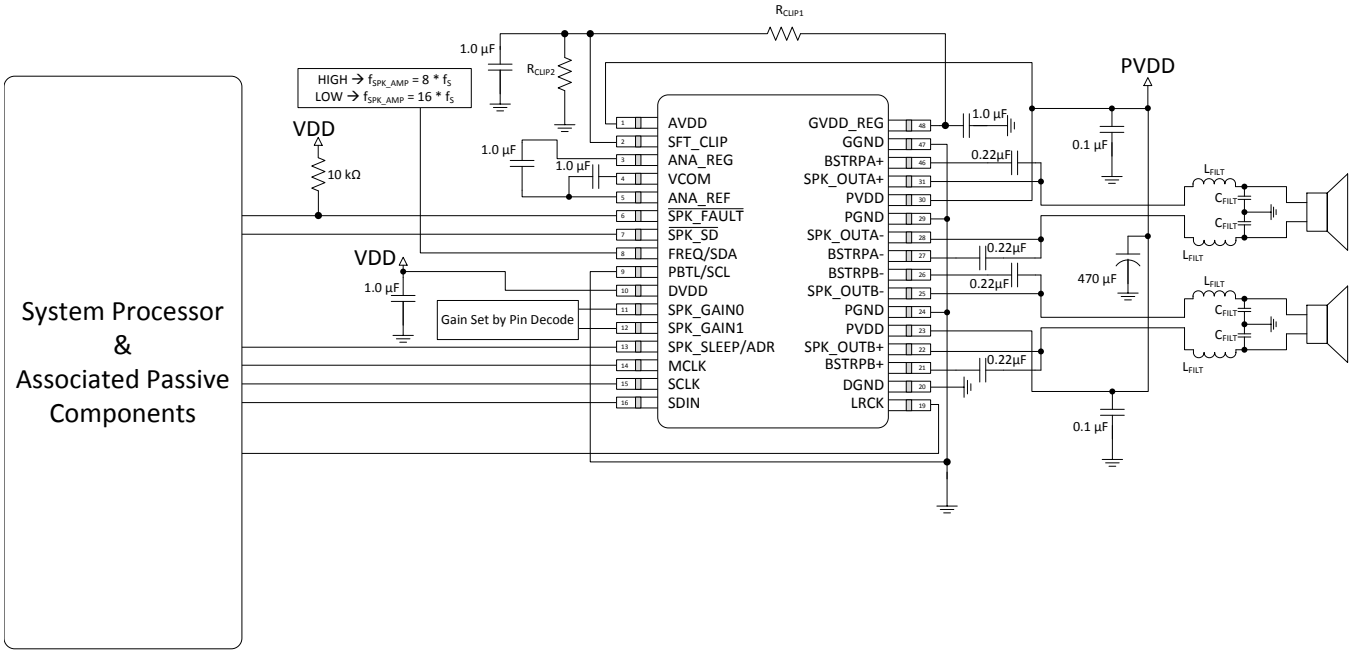


Figure 49. Stereo BTL using Hardware Control, 32 Pin DAP Package Option

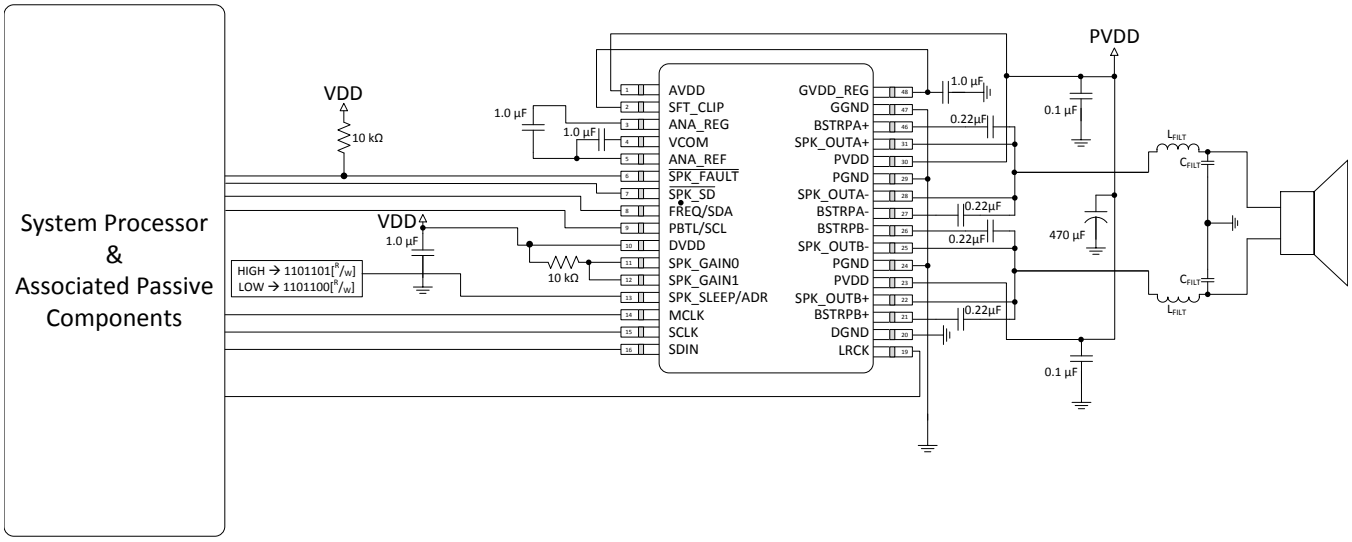


Figure 50. Mono PBTL using Software Control, 32 Pin DAP Package Option

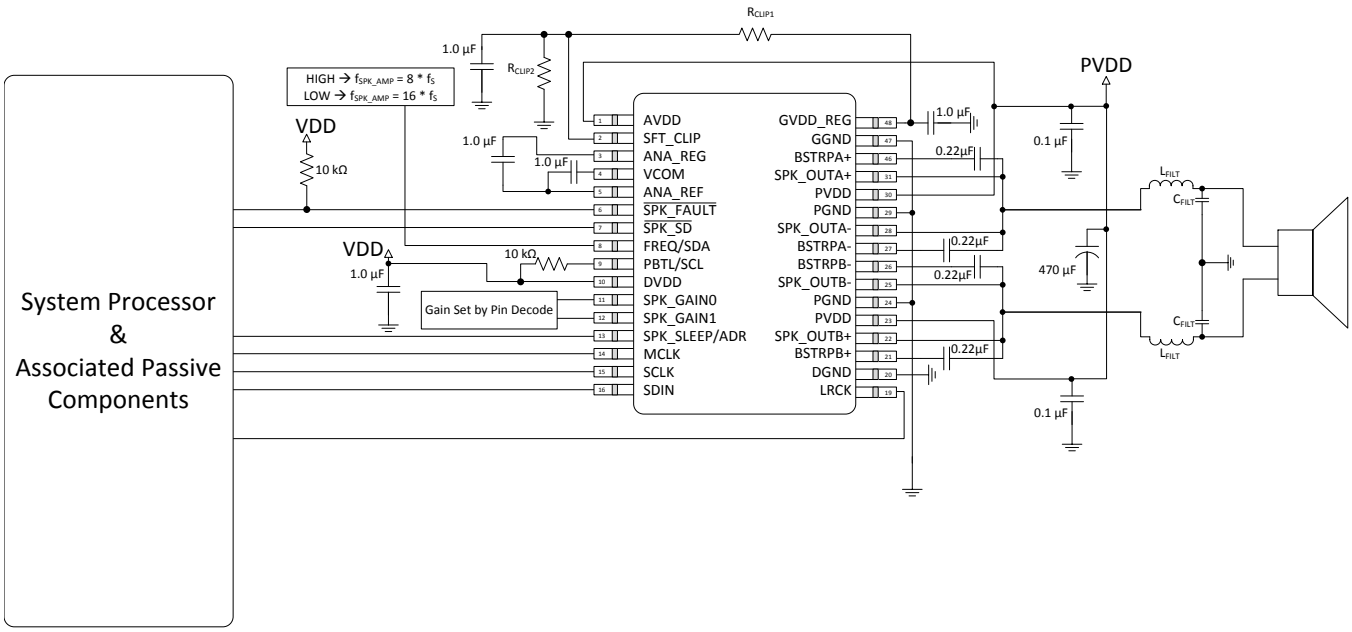


Figure 51. Mono PBTL using Hardware Control, 32 Pin DAP Package Option

Component Selection and Hardware Connections

The Typical Application Circuits shown above detail the typical connections required for proper operation of the device. It is with this list of components that the device was simulated, tested, and characterized. Deviation from this typical application circuit unless recommended by this document may produce unwanted results, which could range from degradation of audio performance to destructive failure of the device.

I²C Pull-Up Resistors

It is important to note that when the device is operated in Software Control Mode, the customary pull-up resistors are required on the SCL and SDA signal lines. They are not shown in the Typical Application Circuits, since they are shared by all of the devices on the I²C bus and are considered to be part of the associated passive components for the System Processor. These resistor values should be chosen per the guidance provided in the I²C Specification.

Digital I/O Connectivity

The digital I/O lines of the TAS5760L are described in previous sections. As discussed, whenever a static digital pin (that is a pin that is hardwired to be "HIGH" or "LOW") is required to be pulled "HIGH", it should be connected to DVDD through a pull-up resistor in order to control the slew rate of the voltage presented to the digital I/O pins. It is not, however, necessary to have a separate pull-up resistor for each static digital I/O line. Instead, a single resistor can be used to tie all static I/O lines "HIGH" to reduce BOM count. For instance, if Software Control Mode is desired both the GAIN[1:0] and the PBTL/SCL pins can both be pulled "HIGH" through a single pull-up resistor.

Recommended Startup and Shutdown Procedures

The start up and shutdown procedures for both Hardware Control Mode and Software Control Mode are shown below.

Startup Procedures- Hardware Control Mode

1. Configure all hardware pins as required by the application using PCB connections (that is PBTL, FREQ, GAIN, etc.)
2. Start with $\overline{\text{SPK\_SD}}$ pin pulled "LOW" and SPK_SLEEP/ADR pin pulled "HIGH"
3. Bring up power supplies (it does not matter if PVDD/AVDD or DVDD comes up first, provided the device is

held in shutdown.)

4. Once power supplies are stable, start MCLK, SCLK, LRCK
5. Once power supplies and clocks are stable and all hardware control pins have been configured, bring $\overline{\text{SPK\_SD}}$ "HIGH"
6. Once the device is out of shutdown mode, bring SPK_SLEEP/ADR "LOW"
7. The device is now in normal operation

Shutdown Procedures- Hardware Control Mode

1. The device is in normal operation
2. Pull SPK_SLEEP/ADR "HIGH"
3. Pull $\overline{\text{SPK\_SD}}$ "LOW"
4. The clocks can now be stopped and the power supplies brought down
5. The device is now fully shutdown and powered off

Startup Procedures- Software Control Mode

1. Configure all digital I/O pins as required by the application using PCB connections (that is SPK_GAIN[1:0] = 11, ADR, etc.)
2. Start with $\overline{\text{SPK\_SD}}$ Pin = "LOW"
3. Bring up power supplies (it does not matter if PVDD/AVDD or DVDD comes up first, provided the device is held in shutdown.)
4. Once power supplies are stable, start MCLK, SCLK, LRCK
5. Configure the device via the control port in the manner required by the use case, making sure to mute the device via the control port
6. Once power supplies and clocks are stable and the control port has been programmed, bring $\overline{\text{SPK\_SD}}$ "HIGH"
7. Unmute the device via the control port
8. The device is now in normal operation

It is important to note that control port register changes should only occur when the device is placed into shutdown. This can be accomplished either by pulling the $\overline{\text{SPK\_SD}}$ pin "LOW" or clearing the $\overline{\text{SPK\_SD}}$ bit in the control port.

Shutdown Procedures- Software Control Mode

1. The device is in normal operation
2. Mute via the control port
3. Pull $\overline{\text{SPK\_SD}}$ "LOW"
4. The clocks can now be stopped and the power supplies brought down
5. The device is now fully shutdown and powered off

It is important to note that any control port register changes excluding volume control changes should only occur when the device is placed into shutdown. This can be accomplished either by pulling the $\overline{\text{SPK\_SD}}$ pin "LOW" or clearing the $\overline{\text{SPK\_SD}}$ bit in the control port.

REVISION HISTORY

Changes from Original (July 2013) to Revision A **Page**

- Changed Figure 50 44
- Changed Figure 51 45

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5760LDAP	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	TAS5760L	Samples
TAS5760LDAPR	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	TAS5760L	Samples
TAS5760LDCA	ACTIVE	HTSSOP	DCA	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	TAS5760L	Samples
TAS5760LDCAR	ACTIVE	HTSSOP	DCA	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	TAS5760L	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

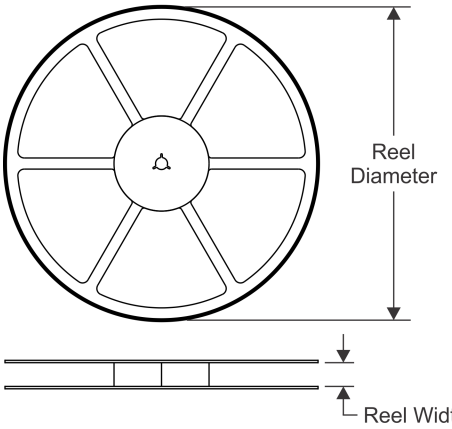
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

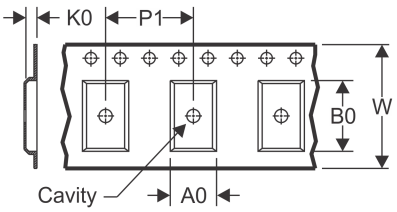
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

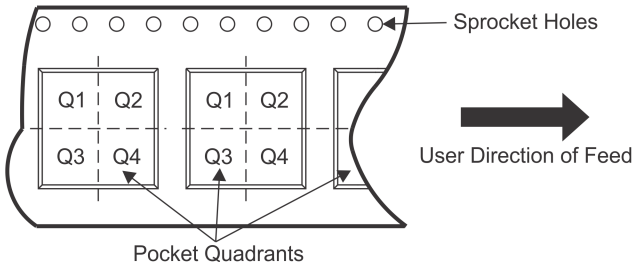


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

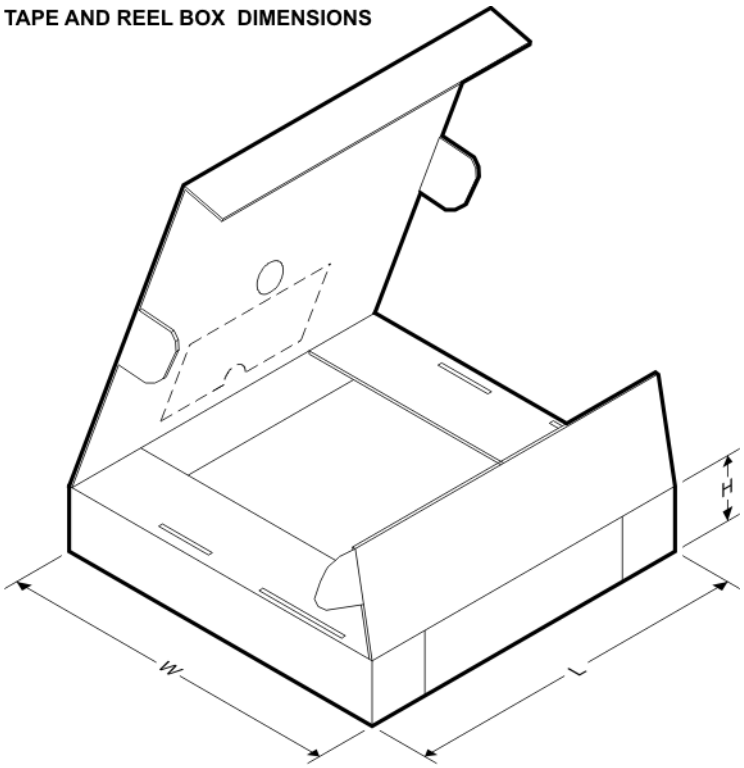
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5760LDAPR	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1
TAS5760LDCAR	HTSSOP	DCA	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1

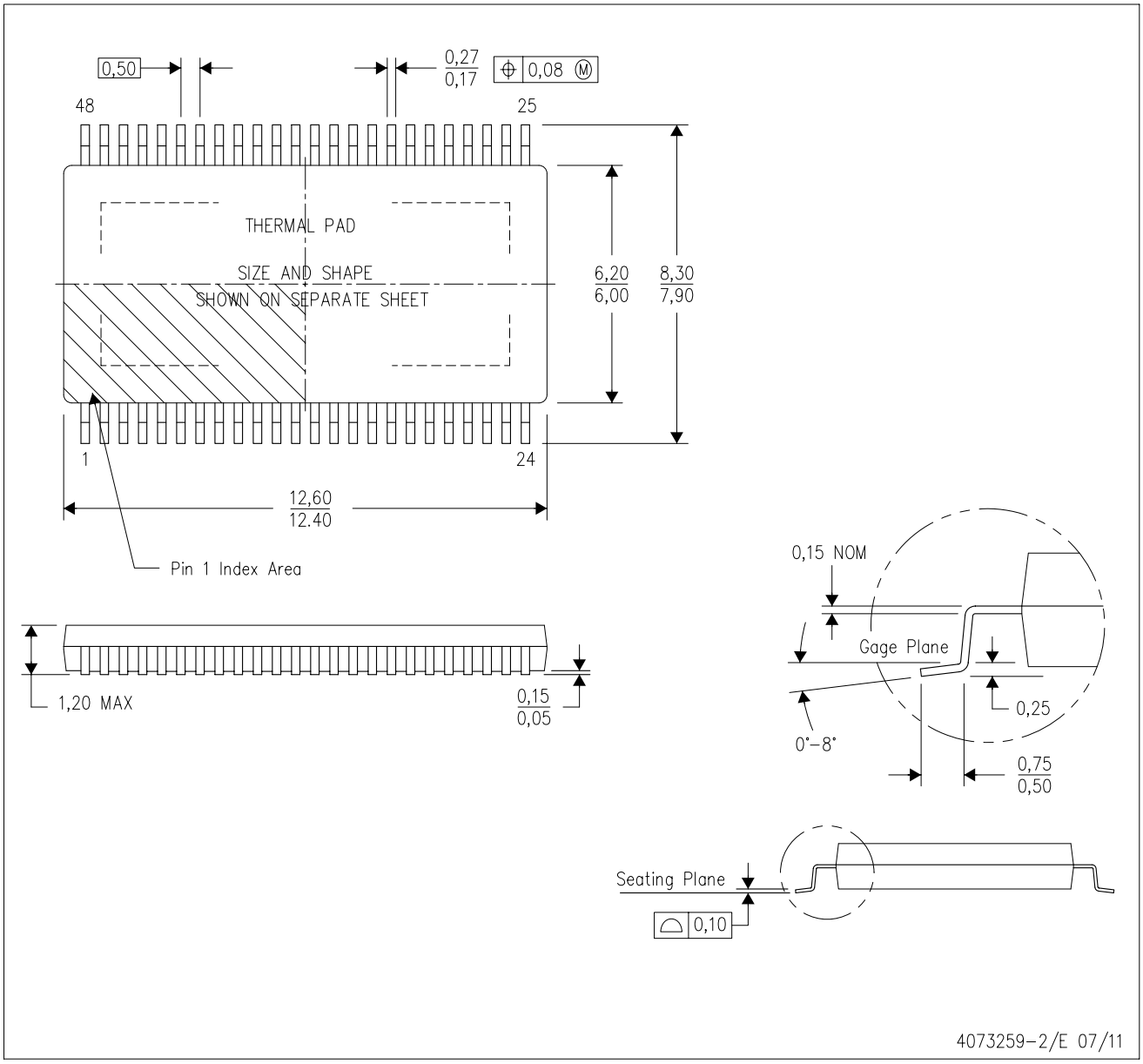
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5760LDAPR	HTSSOP	DAP	32	2000	367.0	367.0	45.0
TAS5760LDCAR	HTSSOP	DCA	48	2000	367.0	367.0	45.0

DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

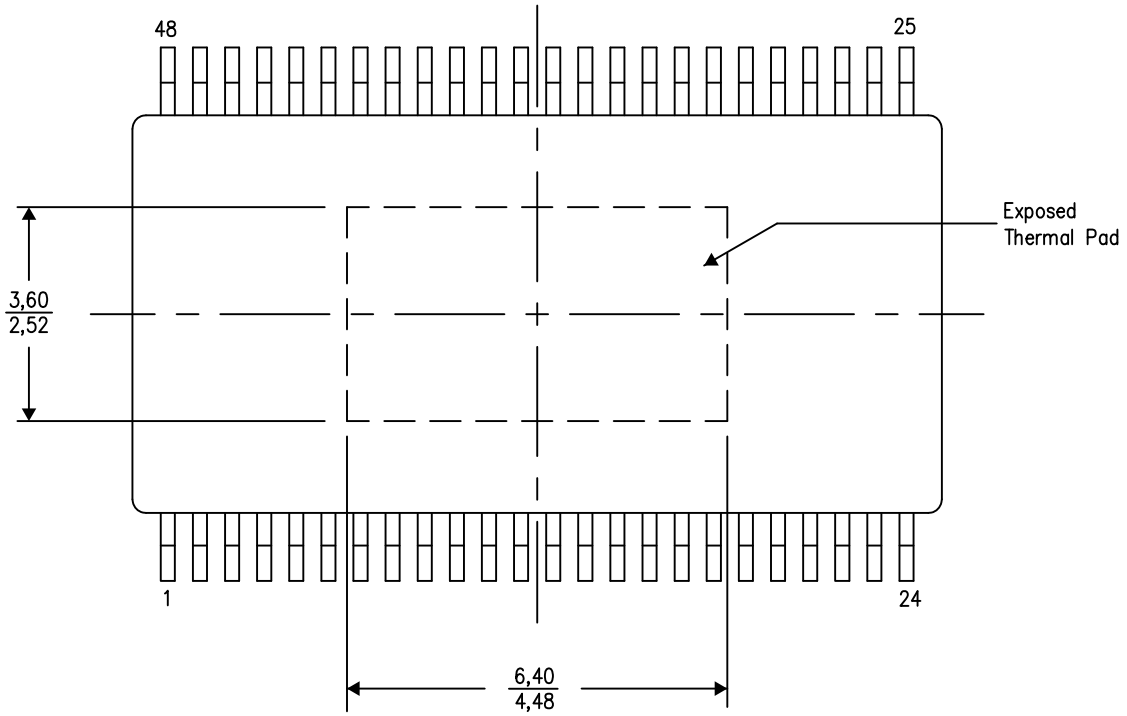
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

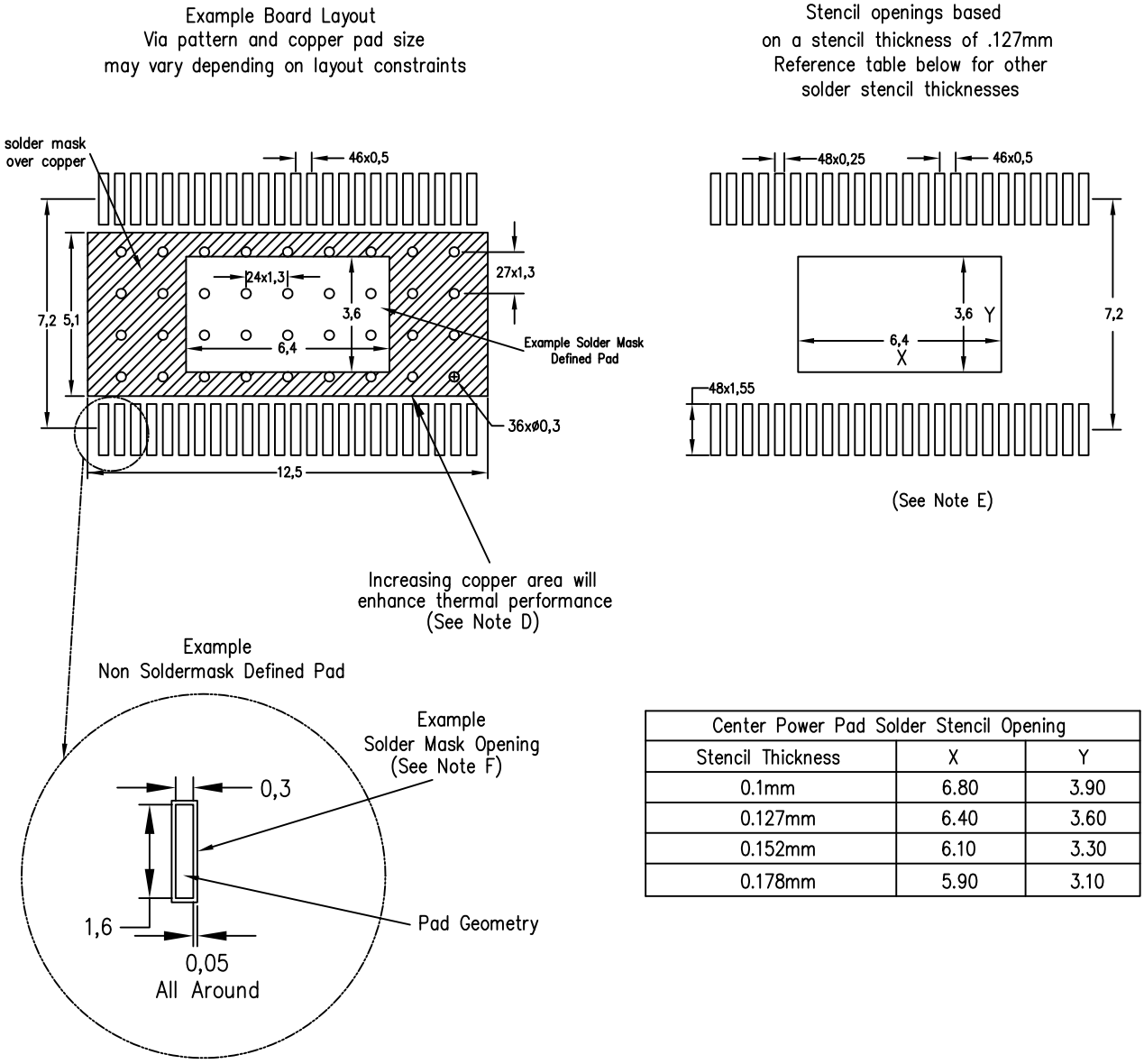
Exposed Thermal Pad Dimensions

4206320–4/R 03/13

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE

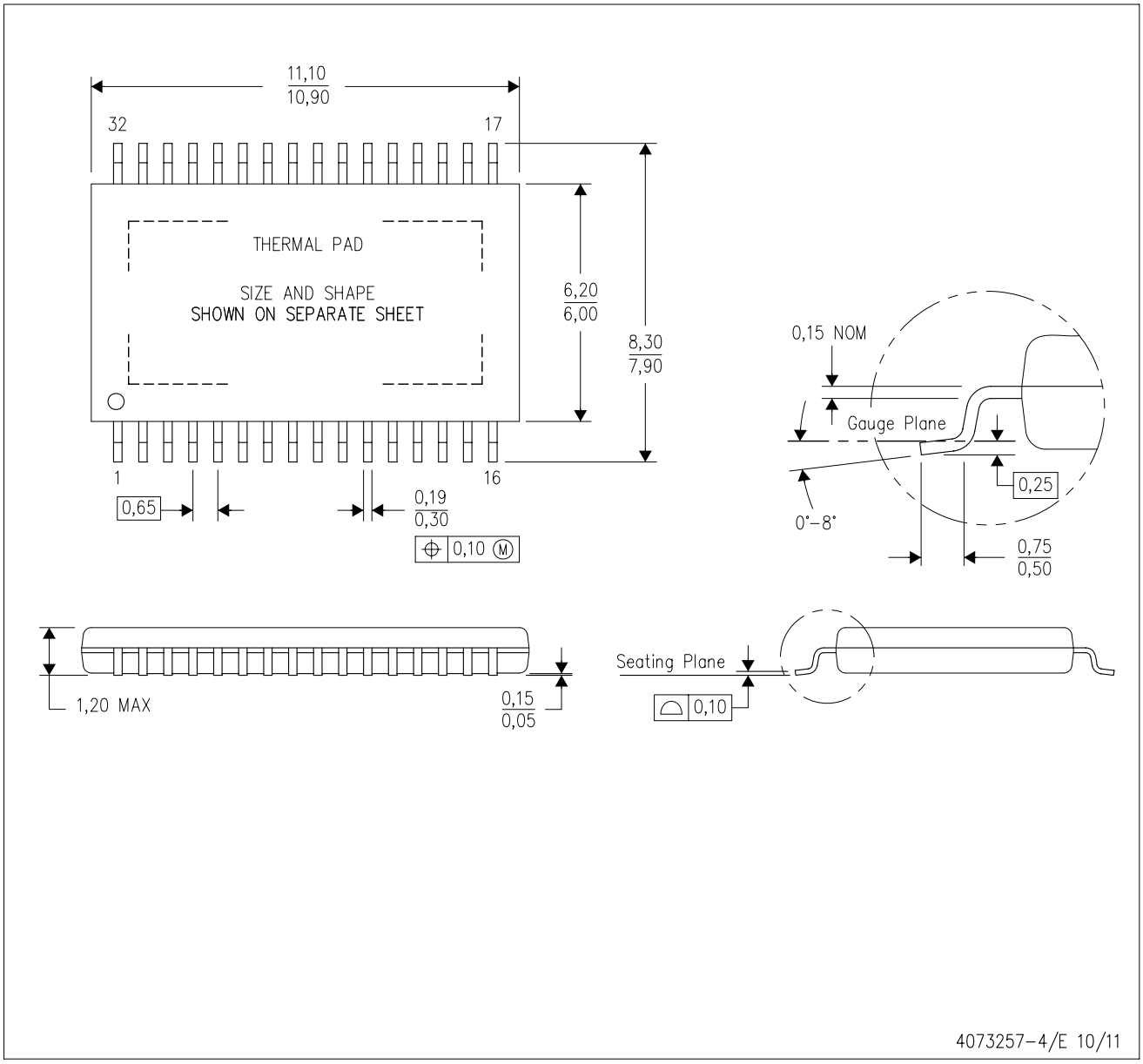


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.80	3.90
0.127mm	6.40	3.60
0.152mm	6.10	3.30
0.178mm	5.90	3.10

4208546–3/G 12/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
F. Falls within JEDEC MO–153 Variation DCT.

PowerPAD is a trademark of Texas Instruments.

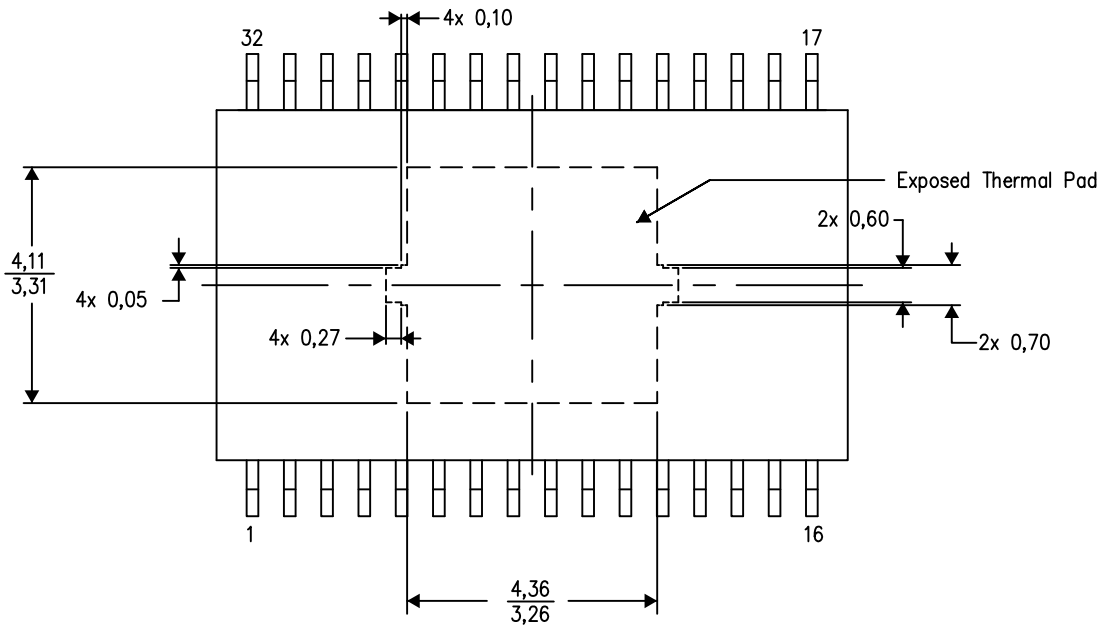
DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

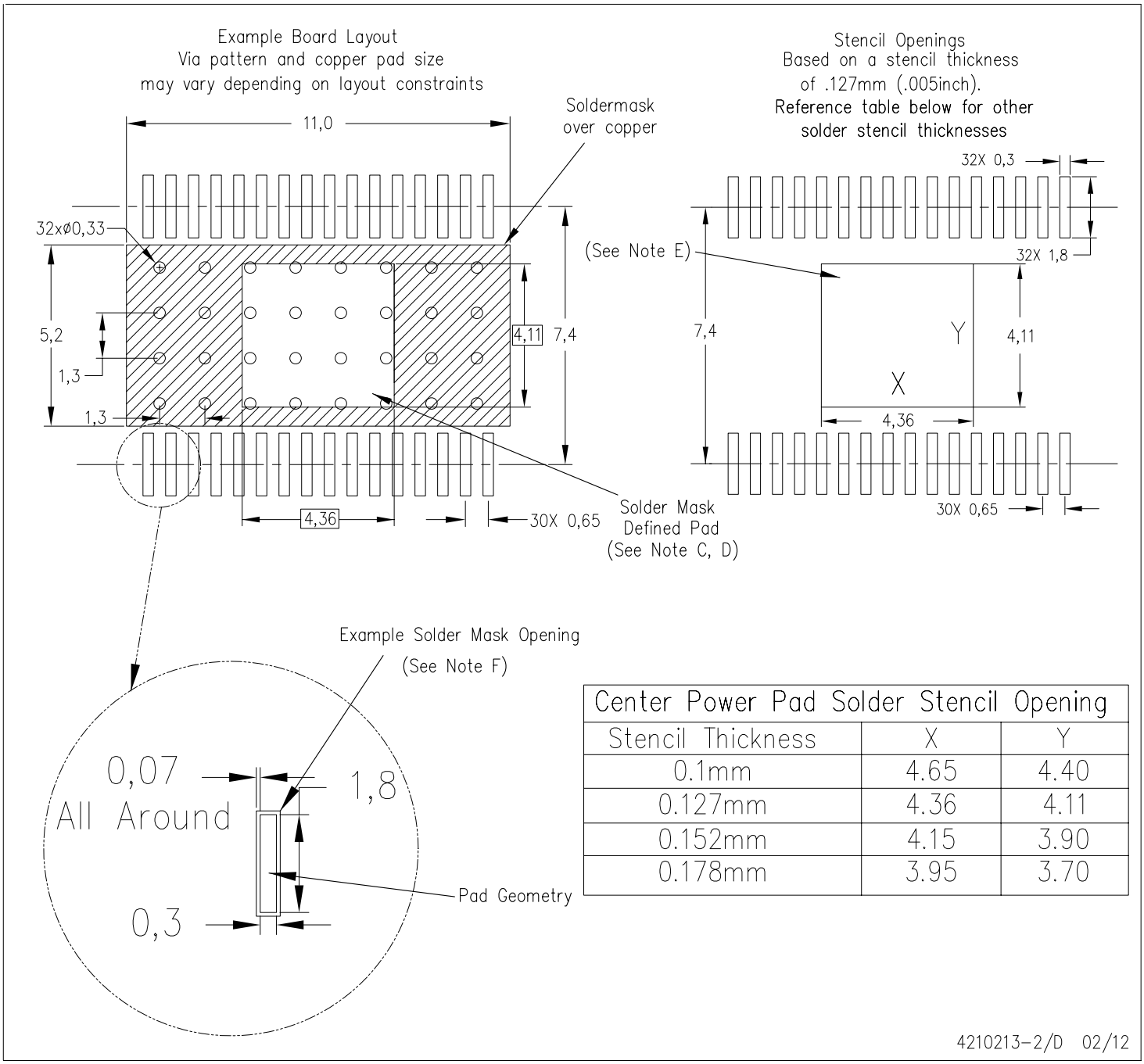
Exposed Thermal Pad Dimensions

4206319–3/M 09/13

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.65	4.40
0.127mm	4.36	4.11
0.152mm	4.15	3.90
0.178mm	3.95	3.70

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Contact the board fabrication site for recommended soldermask tolerances.

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