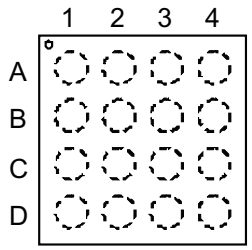
Low-Voltage 8-Bit I²C and SMBus I/O Expander with Interrupt Output, RESET, I/O Direction Registers, and Programmable Pull-up/Pull-down

Check for Samples: TCA7408

FEATURES

- **Operating Power-Supply Voltage Range of 1.65V to 3.6V**
- **Allows Bidirectional Voltage-Level Translation and GPIO Expansion Between:**
  - **1.8V SCL/SDA and 1.8V, 2.5V, 3.3V GPIO port**
  - **2.5V SCL/SDA and 1.8V, 2.5V, 3.3V GPIO port**
  - **3.3V SCL/SDA and 1.8V, 2.5V, 3.3V GPIO port**
  - **5V SCL/SDA and 1.8V, 2.5V, 3.3V GPIO port**
- **Standby Current Consumption of <2 µA at 1.8V**
- **Active Current Consumption of:**
  - **<2 µA at 1.8V 100 kHz clock**
  - **<5 µA at 1.8V 400 kHz clock**
- **100-kHz, 400-kHz Fast Mode**
- **Internal Power-On-Reset and Watchdog Timer**
- **Fail safe I²C, $\overline{\text{INT}}$, and $\overline{\text{RESET}}$ lines**
- **Noise Filter on SCL/SDA and Inputs**
- **Schmitt-Trigger Action Allows Slow Input Transition and Better Switching Noise Immunity at the SCL and SDA Inputs**
  - **V_{hys} = 0.18V Typ at 1.8V**
  - **V_{hys} = 0.25V Typ at 2.5V**
  - **V_{hys} = 0.33V Typ at 3.3V**
- **Active-Low Reset ($\overline{\text{RESET}}$) Input**
- **Open-Drain Active-Low Interrupt ($\overline{\text{INT}}$) Output**
- **Automatic power save mode**
- **Programmable Pull-up/Pull-down Resistors for GPIO Inputs**
- **Programmable Edge Detection for Generating Interrupts**
- **Interrupt Latching**
- **Software Reset**
- **Input/Output Direction Register**
- **Power Up With All Channels Configured as Inputs**
- **No Glitch On Power Up**
- **Latched Outputs With High-Current Drive Maximum Capability for Directly Driving LEDs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **1000-V Charged-Device Model (C101)**

ZSZ PACKAGE
(TOP THROUGH VIEW)



	1	2	3	4
A	GND	GPIO7	GPIO6	GPIO5
B	V_{CCI}	V_{CCP}	ADDR	GPIO4
C	SDA	$\overline{\text{INT}}$	$\overline{\text{RESET}}$	GPIO3
D	SCL	GPIO0	GPIO1	GPIO2

DESCRIPTION

This 8-bit I/O expander for the two-line bidirectional bus (I²C) is designed to provide general-purpose remote I/O expansion via the I²C interface [serial clock (SCL) and serial data (SDA)].

The major benefit of this device is its wide V_{CC} range. It can operate from 1.65V to 3.6V on the GPIO-port side and 1.65V to 5.5V on the SDA/SCL side. This allows the TCA7408 to interface with next-generation microprocessors and microcontrollers on the SDA/SCL side, where supply levels are dropping down to conserve power.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The bidirectional voltage-level translation in the TCA7408 is provided through V_{CCI}. V_{CCI} should be connected to the V_{CC} of the external SCL/SDA lines. This indicates the V_{CC} level of the I^2C bus to the TCA7408. The voltage level on the GPIO-port of the TCA7408 is determined by V_{CCP}.

At power on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O direction bits. The data for each input or output is kept in the corresponding Input or Output Register. All registers can be read by the system master.

The system master can reset the TCA7408 in the event of a timeout or other improper operation by asserting a low in the $\overline{\text{RESET}}$ input. The power-on reset (POR) puts the registers in their default state and initializes the I^2C/SMBus state machine. The $\overline{\text{RESET}}$ pin causes the same reset/initialization to occur without depowering the part. The system master can also execute a software reset by asserting B0 in register 01h. The POR, and hardware reset events will reset the state machine and the registers to the default state. A software reset will only reset the registers to the default state and will not reset the state machine. In addition the watch dog timer only resets the state machine

The TCA7408 open-drain interrupt ($\overline{\text{INT}}$) output is activated when any GPIO set as an input has a transition to the state opposite of that in the Input Default State (09h) register and the corresponding bit in the Interrupt Mask Register (11h) is set to 0. It is used to indicate to the system master that an input has changed to a pre-determined state. $\overline{\text{INT}}$ is also activated after either a hardware reset or software reset. Watch dog timer does not activate the $\overline{\text{INT}}$ pin.

$\overline{\text{INT}}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^2C bus. Thus, the TCA7408 can remain a simple slave device.

One hardware pin (ADDR) can be used to program the I^2C address and allow up to two devices to share the same I^2C bus or SMBus.

The integrated watchdog timer will reset the I^2C state machine in the event the SDA is internally held low, after 200 ms (nominal). This reset does not reset the registers as they retain their previous value.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	µCSP – ZSZ package	Tape and reel	TCA7408ZSZR	ZUQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

DEVICE INFORMATION

TOP THROUGH VIEW

	1	2	3	4
A	GND	GPIO7	GPIO6	GPIO5
B	V_{CCI}	V_{CCP}	ADDR	GPIO4
C	SDA	$\overline{INT}$	$\overline{RESET}$	GPIO3
D	SCL	GPIO0	GPIO1	GPIO2

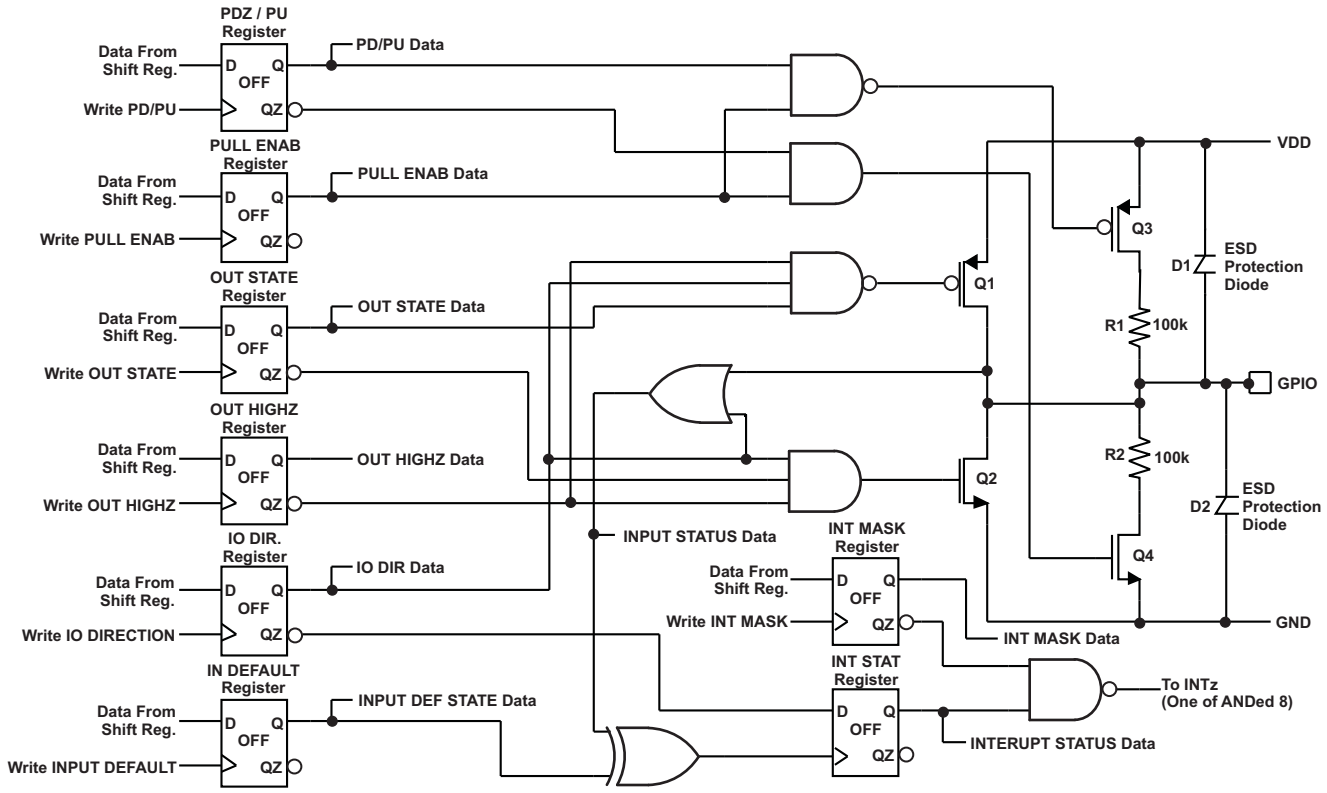
PIN FUNCTIONS

μCSP (ZSZ)		DESCRIPTION
PIN NO.	NAME	
B1	VCCI	Supply voltage of I^2C bus. Connect directly to the VCCI of the external I^2C master. Provides voltage level translation.
B3	ADDR	Address input. Connect directly to V_{CCI} or ground.
C3	$\overline{RESET}$	Active-low reset input. Connect to V_{CCI} through a pull-up resistor, if no active connection is used.
D2	GPIO0	GPIO-port input/output (push-pull design structure). At power on, GPIO0 is configured as an input.
D3	GPIO1	GPIO-port input/output (push-pull design structure). At power on, GPIO1 is configured as an input.
D4	GPIO2	GPIO-port input/output (push-pull design structure). At power on, GPIO2 is configured as an input.
C4	GPIO3	GPIO-port input/output (push-pull design structure). At power on, GPIO3 is configured as an input.
A1	GND	Ground
B4	GPIO4	GPIO-port input/output (push-pull design structure). At power on, GPIO4 is configured as an input.
A4	GPIO5	GPIO-port input/output (push-pull design structure). At power on, GPIO5 is configured as an input.
A3	GPIO6	GPIO-port input/output (push-pull design structure). At power on, GPIO6 is configured as an input.
A2	GPIO7	GPIO-port input/output (push-pull design structure). At power on, GPIO7 is configured as an input.
C2	$\overline{INT}$	Active-low interrupt output. Connect to V_{CCI} through a pull-up resistor.
D1	SCL	Serial clock bus. Connect to V_{CCI} through a pull-up resistor.
C1	SDA	Serial data bus. Connect to V_{CCI} through a pull-up resistor.
B2	VCCP	Supply voltage of TCA7408 for GPIO-port

VOLTAGE TRANSLATION

V_{CCI} (SCL AND SDA OF I^2C MASTER) (V)	V_{CCP} (GPIO-PORT) (V)
1.8	1.8
1.8	2.5
1.8	3.3
2.5	1.8
2.5	2.5
2.5	3.3
3.3	1.8
3.3	2.5
3.3	3.3
5	1.8
5	2.5
5	3.3

SIMPLIFIED LOGIC DIAGRAM (POSITIVE LOGIC)



On power up or reset, all registers return to default values.

I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input.

If the I/O is configured as an output, Q1 or Q2 is enabled depending on the state of the Output Port Register. In this case, there are low impedance paths between the I/O pin and either V_{CCP} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

Q4 is turned on at power-on to enable the pull down resistor. Q3 and Q4 are enabled accordingly to the Pull-up/-down Select Register and the Pull-up/-down Enable Register.

When the GPIO-port is set as an output the input buffers are disabled such that the bus is allowed to float.

I^2C INTERFACE

The bidirectional I^2C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to V_{CCI} through a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I^2C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output, while the SCL input is high. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address (ADDR) input of the slave device must not be changed between the Start and the Stop conditions.

On the I^2C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master.

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

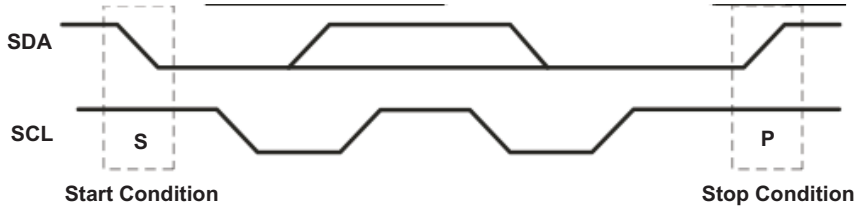


Figure 1. Definition of Start and Stop Conditions

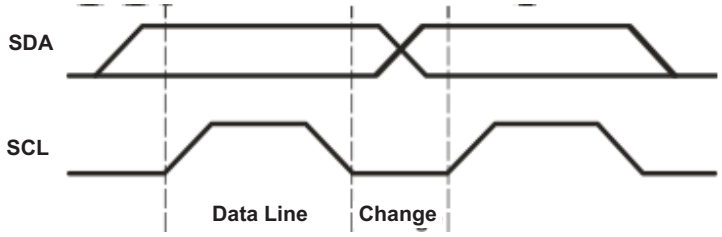


Figure 2. Bit Transfer

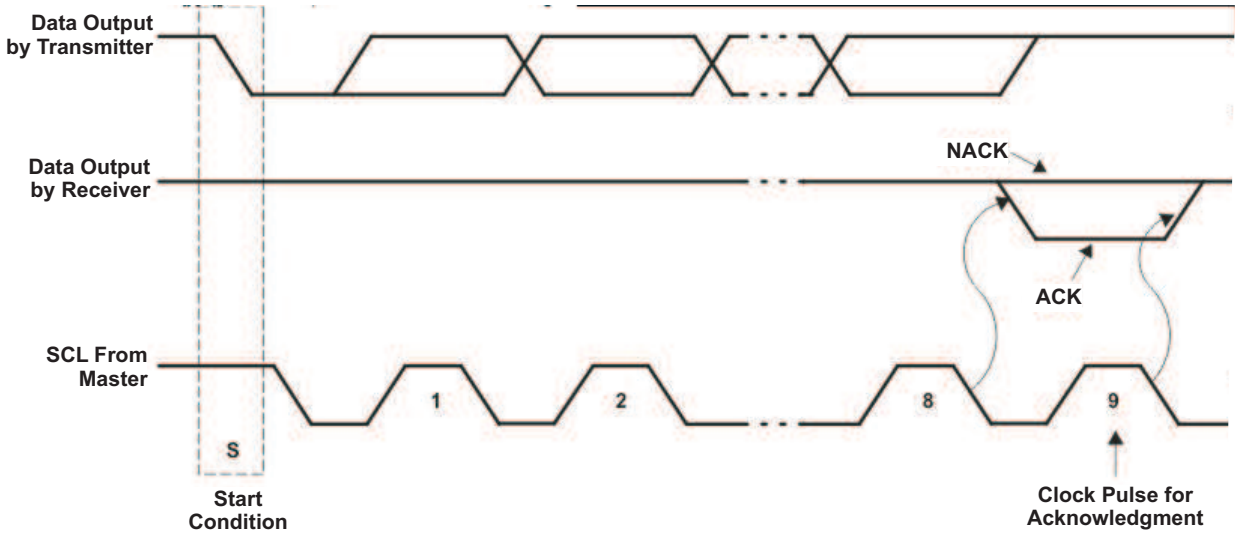


Figure 3. Acknowledgment on I^2C Bus

DEVICE ADDRESS

The address of the device is shown below

ADDRESS REFERENCE

ADDR	SLAVE ADDRESS								I^2C BUS SLAVE ADDRESS
	B7	B6	B5	B4	B3	B2	B1	B0	
0	1	0	0	0	0	1	1	0 (W)	134 (decimal), 86(h)
0	1	0	0	0	0	1	1	1 (R)	135 (decimal), 87(h)
1	1	0	0	0	1	0	0	0 (W)	136 (decimal), 88(h)
1	1	0	0	0	1	0	0	1 (R)	137 (decimal), 89(h)

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

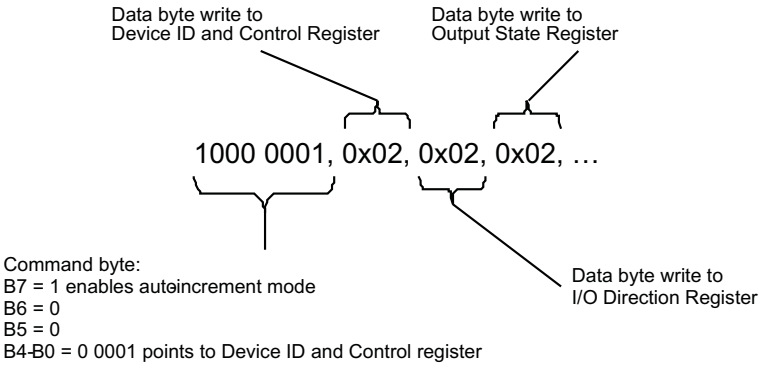
CONTROL REGISTER AND COMMAND BYTE

Following the successful acknowledgement of the address byte, the bus master sends a command byte, which is stored in the Control Register in the TCA7408. Five bits of this data byte state the operation (read or write) and the internal registers that will be affected. This register can be written or read through the I^2C bus. The command byte is sent only during a write transmission.

AUTO INCREMENT MODE

An automatic increment feature as been added to the control register for block writes. The master can write to all 10 registers with 1 command byte being sent initially. In auto-increment mode the last five bits of the command byte are automatically incremented after the byte is written and the next data byte is stored in the corresponding register. Registers are written in the order shown in the register map shown below. Writes attempted to read only registers do not change the value in the register.

If B7=0, all the data bytes are written to or read from the register defined by B4 through B0 in a non-incremented fashion. B6 and B5 should always be 0.



REGISTER MAP

CONTROL REGISTER BITS								COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B7	B6	B5	B4	B3	B2	B1	B0				
AI	0	0	0	0	0	0	1	01h	Device ID and Control	Read (B7-B1) Write (B0)	0100 0010
AI	0	0	0	0	0	1	1	03h	I/O Direction	Read/write byte	0000 0000
AI	0	0	0	0	1	0	1	05h	Output State	Read/write byte	0000 0000
AI	0	0	0	0	1	1	1	07h	Output High-Impedance	Read/write byte	1111 1111
AI	0	0	0	1	0	0	1	09h	Input Default State	Read/write byte	0000 0000
AI	0	0	0	1	0	1	1	0Bh	Pull-up/down Enable	Read/write byte	1111 1111
AI	0	0	0	1	1	0	1	0Dh	Pull-up/down Select	Read/write byte	0000 0000
AI	0	0	0	1	1	1	1	0Fh	Input Status	Read byte	xxxx xxxx
AI	0	0	1	0	0	0	1	11h	Interrupt Mask	Read/write byte	0000 0000
AI	0	0	1	0	0	1	1	13h	Interrupt Status	Read byte	0000 0000

REGISTER DESCRIPTIONS

Register 01h – Device ID and Control

The Device ID and Control register contains the manufacturer ID and firmware revision. The Control register indicates whether the device has been reset and the default values have been set.

- The Reset Interrupt is set B1=1 when the device is either reset by the $\overline{\text{RESET}}$ pin, a power on reset, or software reset.
- Reset Interrupt is then cleared after being read by the master.
- Writing to B7–B1 has no effect on these bits in the register.
- A software reset is issued when the master writes B0=1.
- When reading from B0, the value read will always be 0.

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	Manufacturer ID			Firmware Revision			Reset Interrupt	Software Reset
DEFAULT	0	1	0	0	0	0	1	0

Register 03h – I/O Direction

The I/O Direction Register configures the direction of the I/O pins.

- If a bit in this register is set to 0, the corresponding port pin is enabled as an input
- If a bit in this register is set to 1, the corresponding port pin is enabled as an output.
- When the port is set as an output the input buffers are disabled such that the bus can float.

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
DEFAULT	0	0	0	0	0	0	0	0

Register 05h – Output Port Register

The Output Port Register sets the outgoing logic levels of the pins defined as outputs.

- When Bx is set to 0, GPIOx = L
- When Bx is set to 1, GPIOx = H
- Bit values in this register have no effect on pins defined as inputs
- Reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
DEFAULT	0	0	0	0	0	0	0	0

Register 07h – Output High-Impedance

The Output High-Impedance Register determines whether pins set as output are enabled or high-impedance

- When a bit in this register is set to 0, the corresponding GPIO-port output state follows register the output port register (05h).
- When a bit in this register is set to 1, the corresponding GPIO-port output is set to high-impedance.
- Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
DEFAULT	1	1	1	1	1	1	1	1

Register 09h – Input Default State

The Input Default State Register sets the default state of the GPIO-port input for generating interrupts.

- When a bit in this register is set to 0, the default for the corresponding input is set to LOW
- When a bit in this register is set to 1, the default for the corresponding input is set to HIGH
- Bit values in this register have no effect on pins defined as outputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the default state, not the actual pin value.

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
DEFAULT	1	1	1	1	1	1	1	1

Register 0Bh – Pull-up/-down Enable

The Pull-up/-down Enable Register enables or disables the pull-up/down resistor on the GPIO-port as defined in the Pull-up/down Select Register (0Dh).

- When a bit in this register is set to 0, the pull-up/down on the corresponding GPIO is disabled.
- When a bit in this register is set to 1, the pull-up/down on the corresponding GPIO is enabled.

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
DEFAULT	1	1	1	1	1	1	1	1

Register 0Dh – Pull-up/-down Select

The Pull-up/down Select Register allows the user to select either a pull-up or pull-down on the GPIO-port. This register only selects the pull-up/down resistor on the GPIO-port, while the enabling/disabling is controlled by the Pull-up/down Enable Register (0Bh).

- When a bit in this register is set to 0, the pull-down on the corresponding GPIO is selected.
- When a bit in this register is set to 1, the pull-up on the corresponding GPIO is selected.

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
DEFAULT	0	0	0	0	0	0	0	0

Register 0Fh – Input Status Register

The Input Status Register reflects the incoming logic levels of the GPIOs set as inputs.

- The default value, X, is determined by the externally applied logic level.
- It only acts on read operation. Attempted writes to this register have no effect.
- For GPIOs set as outputs this register will read HIGH.

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
DEFAULT	X	X	X	X	X	X	X	X

Register 11h – Interrupt Mask Register

The Interrupt Mask Register controls the generation of an interrupt to the $\overline{INT}$ pin when the GPIO-port input state changes state.

- When a bit in this register is set to 0, an interrupt generated by the interrupt status register causes the $\overline{INT}$ pin to be asserted LOW.
- When a bit in this register is set to 1, the interrupt for the corresponding GPIO is disabled. The corresponding bit in the Interrupt Status Register (13h) will still be asserted.
- $\overline{INT}$ is not affected when GPIO-port is defined as outputs.

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
DEFAULT	0	0	0	0	0	0	0	0

Register 13h – Interrupt Status Register

The Interrupt Status Register bit is asserted when the bit changes to a value opposite to the default value defined in the Input Default State Register (09h).

- This bit is cleared and the $\overline{INT}$ pin is de-asserted upon read of this register.
- The input must be asserted back to the default state before this bit is set again.
- If the GPIO-port pin is defined as an output, this bit is never set.
- Attempted writes to this register, have no effect.

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
DEFAULT	0	0	0	0	0	0	0	0

POWER-ON RESET

When power (from 0V) is applied to V_{CCP}, an internal power-on reset holds the TCA7408 in a reset condition until V_{CCP} has reached V_{POR}. At that time, the reset condition is released, and the TCA7408 registers and I^2C/SMBus state machine initialize to their default states. After that, V_{CCP} must be lowered to below V_{PORF} and back up to the operating voltage for a power-reset cycle.

- During power up, if V_{CCI} ramps before V_{CCP}, a power on reset event occurs and the I^2C registers are reset.
- If V_{CCP} ramps up before V_{CCI}, then the device with reset as if $\overline{RESET}$ = 0
- The device is reset regardless of which V_{CCx} ramps first.

RESET ($\overline{RESET}$) INPUT

The $\overline{RESET}$ input can be asserted to initialize the system while keeping V_{CCP} at its operating level. A reset can be accomplished by holding the $\overline{RESET}$ pin low for a minimum of t_W. The TCA7408 registers and I^2C/SMBus state machine are changed to their default state once $\overline{RESET}$ is low (0). Only when $\overline{RESET}$ is high (1), GPIO registers can be accessed by the I^2C pin. This input requires a pull-up resistor to V_{CCI}, if no active connection is used.

INTERRUPT ($\overline{INT}$) OUTPUT

An interrupt is generated by a rising or falling edge of the port inputs in the input mode. After time t_{iv}, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved by reading the Interrupt Status Register. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$. The values in the interrupt status register are sampled on the rising edge of SCL during the read address acknowledge. If an interrupt occurs before this event, it will be reflected in this register in the next read cycle. If an interrupt occurs very close to this event, it may be reflected in both the current and the next read cycle. At no point is a valid interrupt ever missed.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Default State Register.

The $\overline{INT}$ output has an open-drain structure and requires a pullup resistor to V_{CCP} or V_{CCI} depending on the application. $\overline{INT}$ should be connected to the voltage source of the device that requires the interrupt information.

BUS TRANSACTIONS

Data is exchanged between the master and TCA7408 through write and read commands.

Writes

Data is transmitted to the TCA7408 by sending the device address and setting the least significant bit (LSB) to a logic 0. The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission.

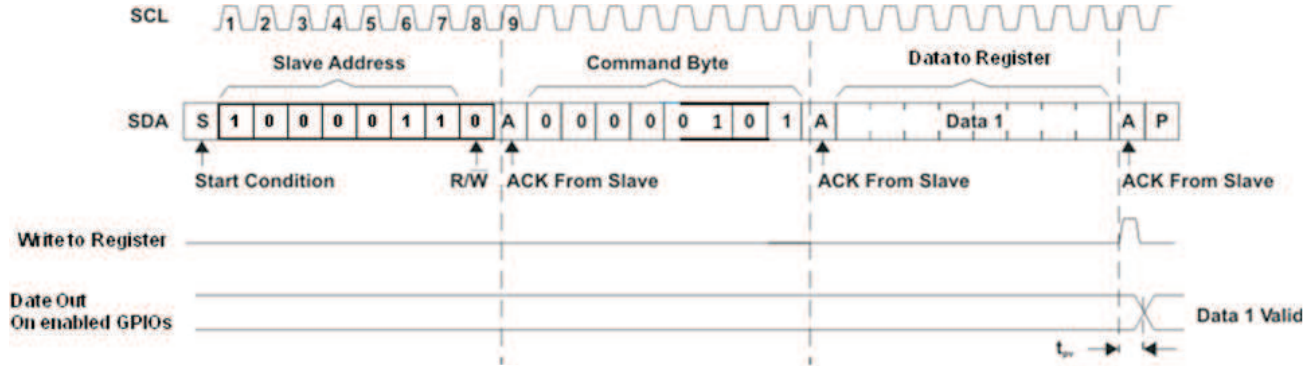


Figure 4. Write to Output state Register (Note: ADDR = 0)

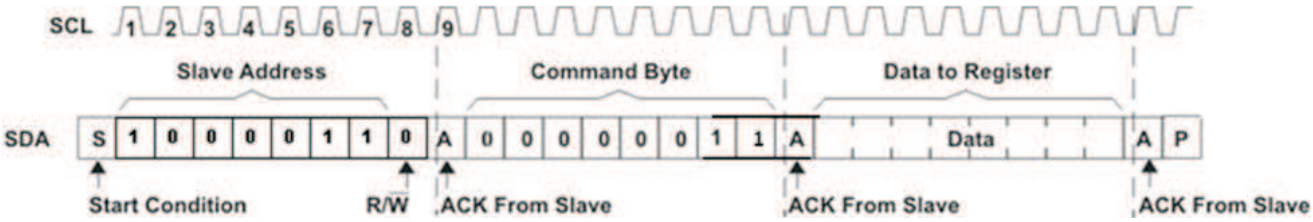


Figure 5. Write to I/O Direction Register (Note: ADDR = 0)

Reads

The bus master first must send the TCA7408 address with the LSB set to a logic 0. The command byte is sent after the address and determines which register is accessed.

After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the TCA7408.

Data is clocked into the register on the rising edge of the ACK clock pulse.

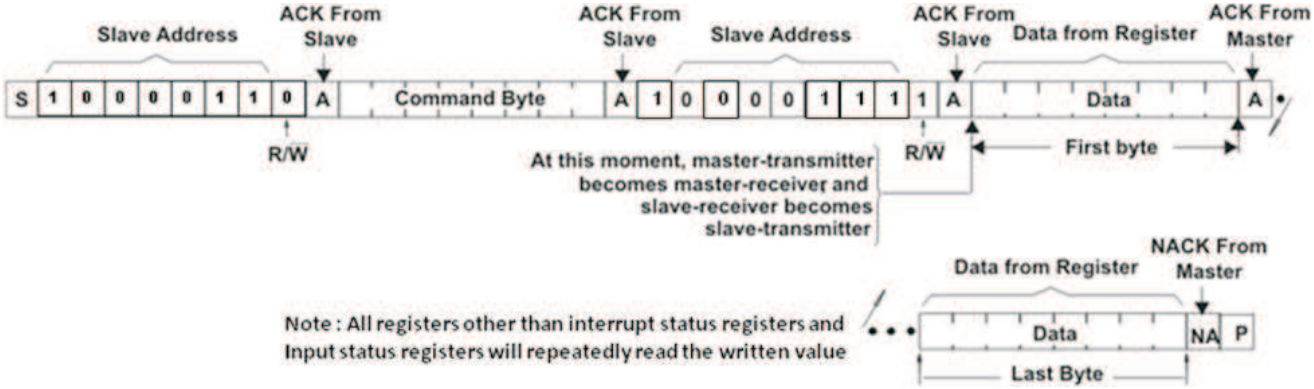
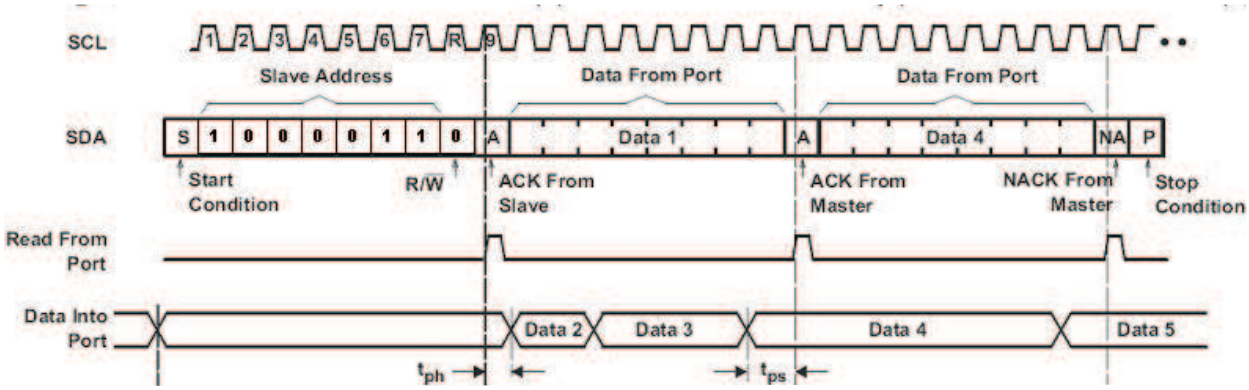


Figure 6. Read From Register



NOTE: ADDR = 0

Figure 7. Read From Input Status Register

Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 0Fh (read Input Status Register). This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from GPIO.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

				MIN	MAX	UNIT
V_{CCI}	Supply voltage range			–0.3	6	V
V_{CCP}				–0.3	4	
V_I	Input voltage range			–0.3	6	V
V_O	Output voltage range			–0.3	6	V
I_{IK}	Input clamp current	ADDR, $\overline{RESET}$, SCL	$V_I < 0$		±20	mA
I_{OK}	Output clamp current	INT	$V_O < 0$		±20	mA
I_{IOK}	Input/output clamp current	GPIO port	$V_O < 0$ or $V_O > V_{CCP}$		±20	mA
		SDA	$V_O < 0$ or $V_O > V_{CCI}$		±20	
I_{OL}	Continuous output low current	GPIO port	$V_O = 0$ to V_{CCP}		10	mA
		SDA, $\overline{INT}$	$V_O = 0$ to V_{CCI}		10	
I_{OH}	Continuous output high current	GPIO port	$V_O = 0$ to V_{CCP}		10	mA
I_{CC}	Continuous current through GND				200	mA
	Continuous current through V_{CCP}				160	
	Continuous current through V_{CCI}				10	
θ_{JA}	Package thermal impedance	ZSZ package		TBD		°C/W
T_{stg}	Storage temperature range			–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CCI}	Supply voltage		1.65	5.5	V
V_{CCP}			1.65	3.6	
V_{IH}	High-level input voltage	SCL, SDA	0.7 × V_{CCI}	5.5	V
		$\overline{RESET}$, ADDR	0.65 × V_{CCI}	5.5	
		GPIO7–GPIO0	0.65 × V_{CCP}	3.6	
V_{IL}	Low-level input voltage	SCL, SDA	–0.3	0.3 × V_{CCI}	V
		$\overline{RESET}$, ADDR	–0.3	0.35 x V_{CCI}	
		GPIO7–GPIO0	–0.3	0.35 × V_{CCP}	
I_{OH}	High-level output current	GPIO7–GPIO0		10	mA
I_{OL}	Low-level output current	GPIO7–GPIO0		10	mA
T_A	Operating free-air temperature		–40	85	°C

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	V_{CCI}	V_{CCP}	MIN	TYP	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA	1.65 V to 5.5 V	1.65 V to 3.6 V	–1.2			V
V_{POR}	Power-on reset voltage(1)	V_I = V_{CCP} or GND, I_O = 0	1.65 V to 3.6 V	1.65 V to 3.6 V		1	1.4	V
V_{OH}	GPIO-port high-level output voltage	I_{OH} = –6 mA	1.65 V	1.65 V	1.2			V
			2.3 V	2.3 V	1.8			
			3 V	3 V	2.6			
		I_{OH} = –10 mA	1.65 V	1.65 V	1.1			V
			2.3 V	2.3 V	1.7			
			3 V	3 V	2.5			
V_{OL}	GPIO-port low-level output voltage	I_{OL} = 6 mA	1.65 V	1.65 V			0.45	V
			2.3 V	2.3 V			0.25	
			3 V	3 V			0.25	
		I_{OL} = 10 mA	1.65 V	1.65 V			0.6	V
			2.3 V	2.3 V			0.3	
			3 V	3 V			0.25	
I_{OL}	SDA(2)	V_{OL} = 0.4 V	1.65 V to 5.5 V	1.65 V to 3.6 V	10			mA
			2.3 to 5.5 V	2.3 to 3.6 V	20			
	$\overline{INT}$		1.65 V to 5.5 V	1.65 V to 3.6 V	3			
I_I	SCL, SDA, $\overline{RESET}$, ADDR	V_I = V_{CCI} or GND	1.65 V to 5.5 V	1.65 V to 3.6 V			±0.1	µA
		V_I = V_{CCP} or GND					±0.1	
I_{IH}	GPIO port	V_I = V_{CCP}	1.65 V to 5.5 V	1.65 V to 3.6 V			1	µA
I_{IL}		V_I = GND					1	

(1) When power (from 0 V) is applied to V_{CCP}, an internal power-on reset holds the TCA7408 in a reset condition until V_{CCP} has reached V_{POR}. At that time, the reset condition is released, and the TCA7408 registers and I^2C/SMBus state machine initialize to their default states. After that, V_{CCP} must be lowered to below 0.2 V and back up to the operating voltage for a power-reset cycle.
(2) I_{OL} for SDA is specified for standard mode, fast mode, and fast mode plus capability (at 2.3 V).

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER			TEST CONDITIONS	VCCI	VCCP	MIN	TYP(1)	MAX	UNIT
I_{CC} (I_{CCI} + I_{CCP})	Fast Mode Operating mode	SDA, GPIO port, ADDR, $\overline{RESET}$	V_I on SDA, ADDR, and $_{RESET}$= V_{CCI} or GND, V_I on GPIO port = V_{CCP} or GND, I_O = 0, I/O = inputs, f_{SCL} = 400 kHz	3.6 V to 5.5 V	3.6 V		4	9	µA
				2.3 V to 3.6 V	2.3 V to 3.6 V		6.5	15	
				1.65 V to 2.3 V	1.65 V to 2.3 V		10	20	
	Standby mode	SCL, SDA, GPIO port, ADDR, $\overline{RESET}$	V_I on SCL, SDA and $\overline{RESET}$ = V_{CCI} or GND, V_I on GPIO port and ADDR = V_{CCI} or GND, I_O = 0, I/O = inputs, f_{SCL} = 0	3.6 V to 5.5 V	3.6 V		1.5	7	µA
				2.3 V to 3.6 V	2.3 V to 3.6 V		1	3.2	
				1.65 V to 2.3 V	1.65 V to 2.3 V		0.5	1.7	
ΔI_{CCI}	Additional current in standby mode	SCL, SDA, $\overline{RESET}$	One input at V_{CCI} – 0.6 V, Other inputs at V_{CCI} or GND	1.65 V to 5.5 V	1.65 V to 3.6 V			25	µA
ΔI_{CCP}		GPIO port, ADDR	One input at V_{CCP} – 0.6 V, Other inputs at V_{CCP} or GND	1.65 V to 5.5 V	1.65 V to 3.6 V			80	µA
C_i	SCL		V_I = V_{CCI} or GND	1.65 V to 5.5 V	1.65 V to 3.6 V		6		pF
C_{io}	SDA		V_{IO} = V_{CCI} or GND	1.65 V to 5.5 V	1.65 V to 3.6 V		7		pF
	GPIO port		V_{IO} = V_{CCP} or GND				7.5		
R_{PU}	Pull up resistor		V_I = GND	1.65 V to 5.5 V	1.65 V to 3.6 V		100		kΩ
R_{PD}	Pull down resistor		V_I = V_{CCP}	1.65 V to 5.5 V	1.65 V to 3.6 V		100		kΩ

(1) All typical values are at nominal supply voltage (1.8V, 2.5V, 3.3V, or 5V VCC) and T_A = 25°C.

I2C INTERFACE TIMING REQUIREMENTS

PARAMETER		STANDARD MODE I^2C BUS		FAST MODE I^2C BUS		UNIT
		MIN	MAX	MIN	MAX	
f_{scl}	I^2C clock frequency	0	100	0	400	kHz
t_{sch}	I^2C clock high time	4		0.6		µs
t_{scl}	I^2C clock low time	4.7		1.3		µs
t_{sp}	I^2C spike time		50		50	ns

I2C INTERFACE TIMING REQUIREMENTS (continued)

PARAMETER		STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
		MIN	MAX	MIN	MAX	
t_{sds}	I²C serial data setup time	250		100		ns
t_{sdh}	I²C serial data hold time	0		0		ns
t_{icr}	I²C input rise time		1000	$20 + 0.1C_b$	300	ns
t_{icf}	I²C input fall time		300	$20 + 0.1C_b$	300	ns
t_{ocf}	I²C output fall time; 10 pF to 400 pF bus		300	$20 + 0.1C_b$	300	µs
t_{buf}	I²C bus free time between Stop and Start	4.7		1.3		µs
t_{sts}	I²C Start or repeater Start condition setup time	4.7		0.6		µs
t_{sth}	I²C Start or repeater Start condition hold time	4		0.6		µs
t_{sps}	I²C Stop condition setup time	4		0.6		µs
$t_{vd(data)}$	Valid data time; SCL low to SDA output valid		1	0.3	0.9	µs
$t_{vd(ack)}$	Valid data time of ACK condition; ACK signal from SCL low to SDA (out) low		1	0.3	0.9	µs

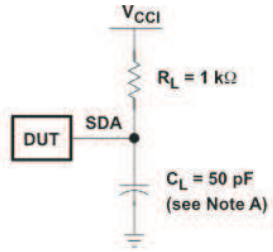
RESET TIMING REQUIREMENTS

PARAMETER		STANDARD MODE, FAST MODE, I²C BUS		UNIT
		MIN	MAX	
t_W	Reset pulse duration	250		ns
t_{REC}	Reset recovery time	250		ns
t_{RESET}	Time to reset	250		ns

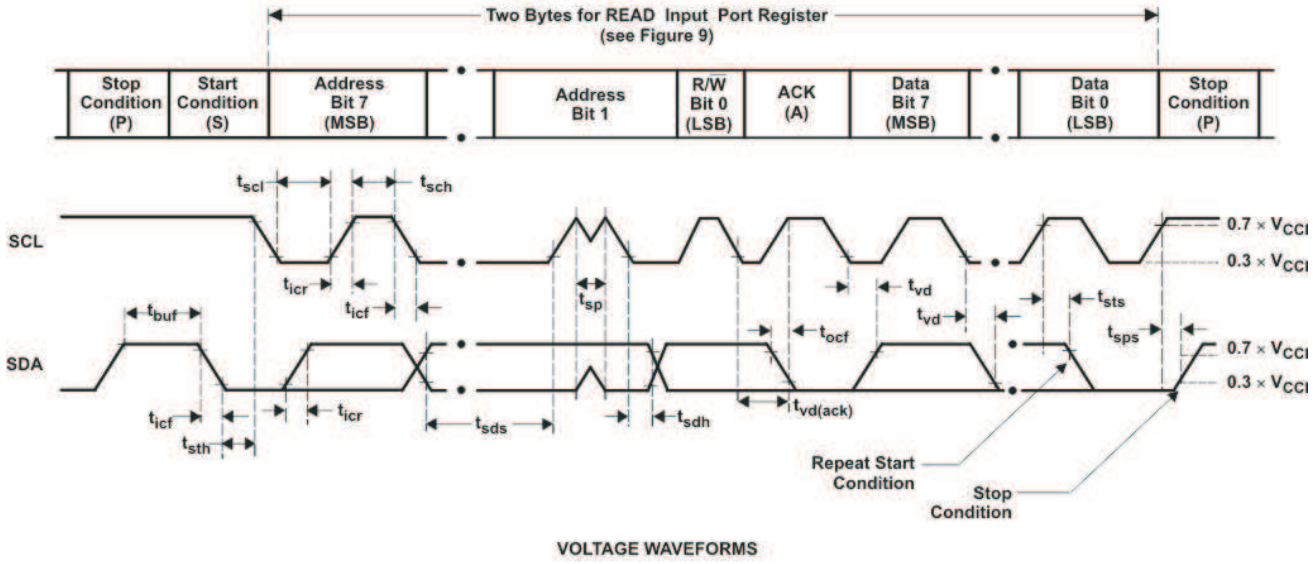
SWITCHING CHARACTERISTICS

PARAMETER		FROM (INPUT)	TO (OUTPUT)	STANDARD MODE, FAST MODE, I²C BUS		UNIT
				MIN	MAX	
t_{iv}	Interrupt valid time	GPIO port	INT		20	ns
t_{ir}	Interrupt reset delay time	SCL	INT		250	ns
t_{pv}	Output data valid	SCL	GPIO7–GPIO0		250	ns
t_{ps}	Input data setup time	GPIO port	SCL	0		ns
t_{ph}	Input data hold time	GPIO port	SCL	300		ns

PARAMETER MEASUREMENT INFORMATION



SDA LOAD CONFIGURATION



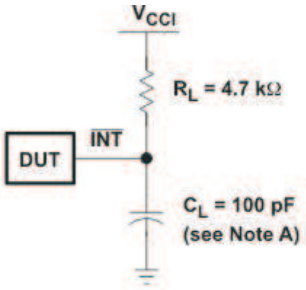
VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2	Input register port data

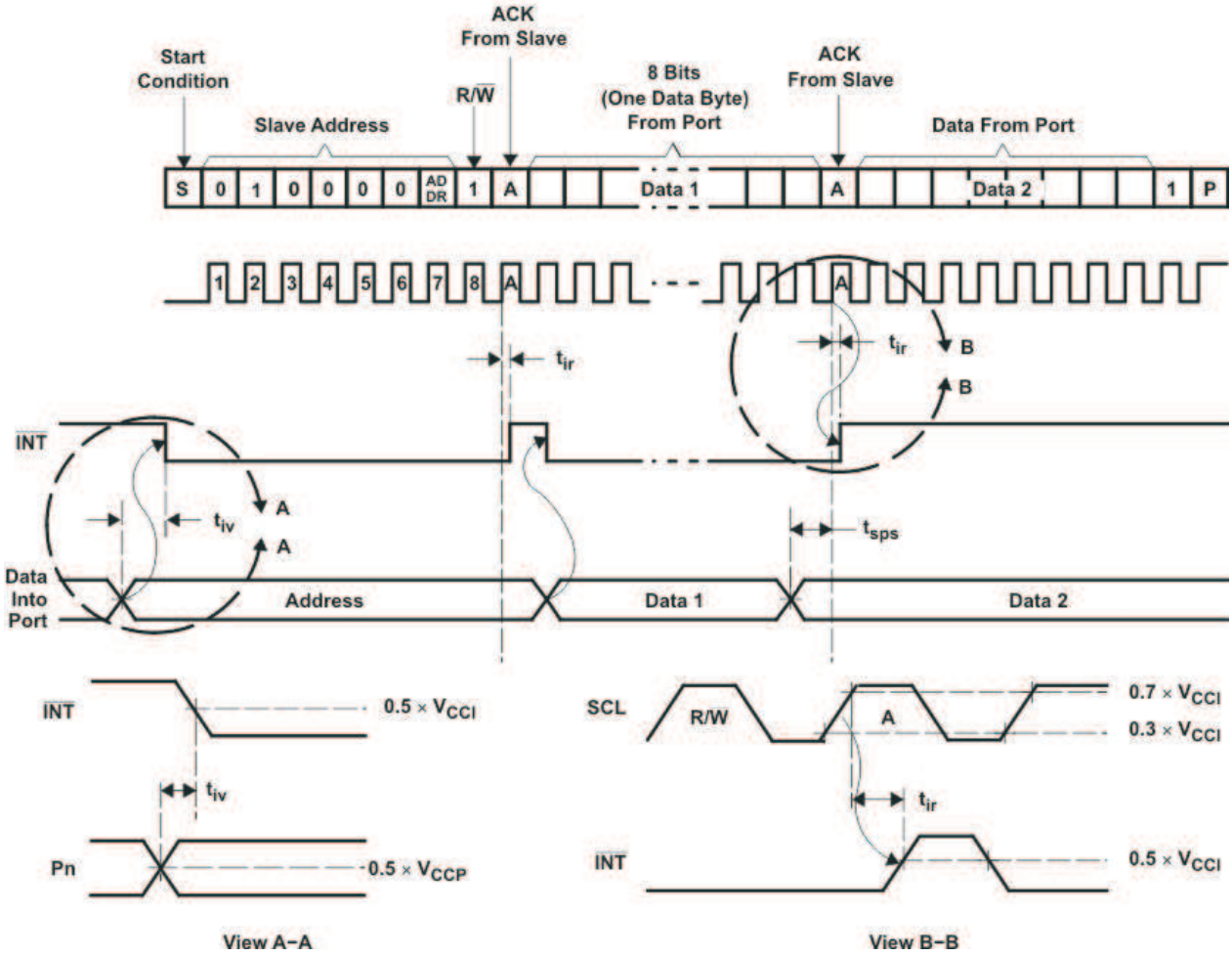
NOTE: C_L includes probe and jig capacitance. t_{ocf} is measured with C_L of 10 pF or 400 pF. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns. All parameters and waveforms are not applicable to all devices.

Figure 8. I^2C Interface Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



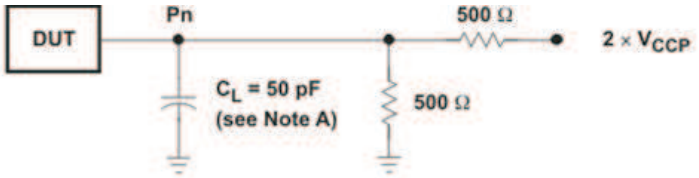
INTERRUPT LOAD CONFIGURATION



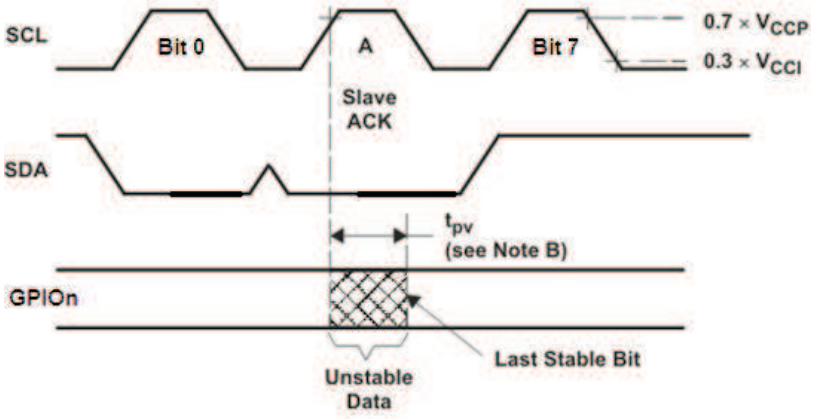
NOTE: C_L includes probe and jig capacitance. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns. All parameters and waveforms are not applicable to all devices.

Figure 9. Interrupt Load Circuit and Voltage Waveforms

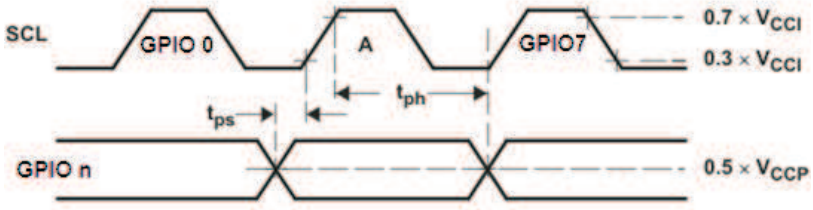
PARAMETER MEASUREMENT INFORMATION (continued)



GPIO-PORT LOAD CONFIGURATION



WRITE MODE (R/$\overline{W}$ = 0)

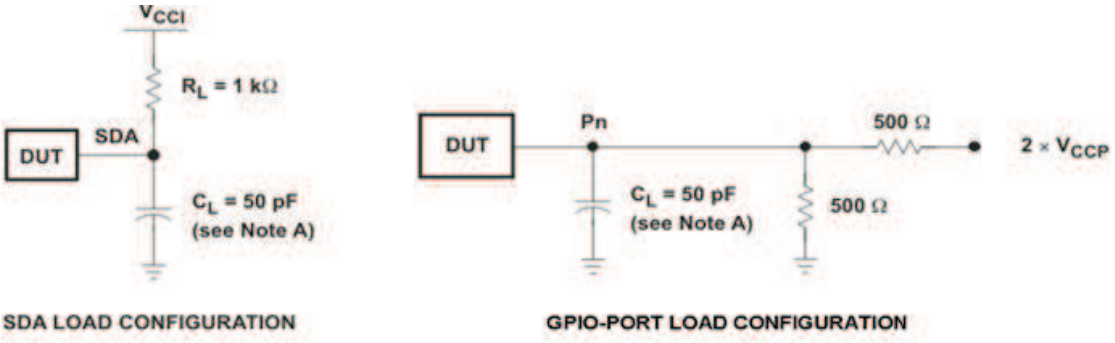


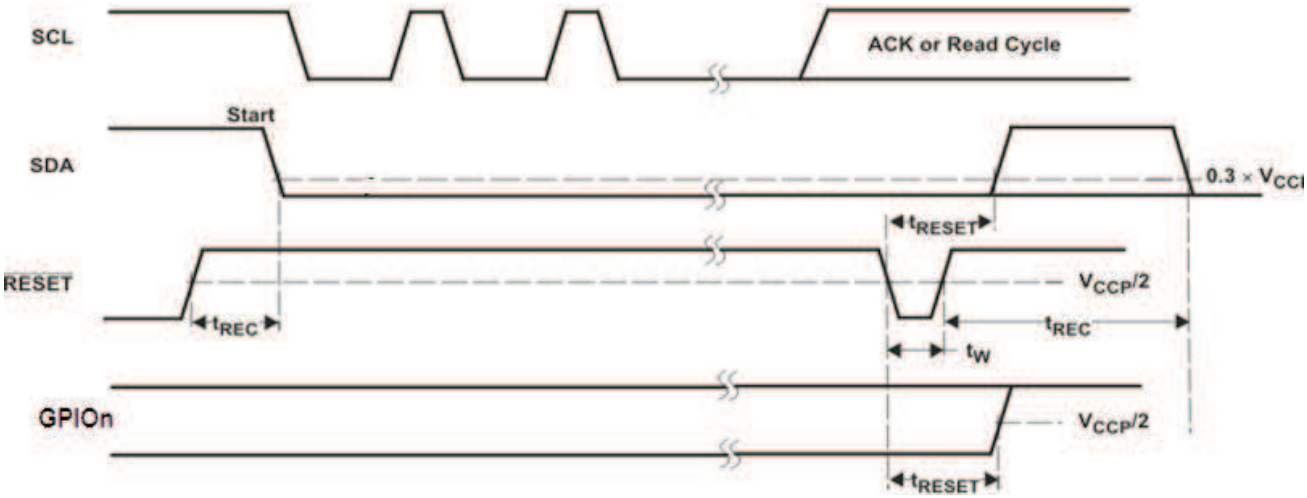
READ MODE (R/$\overline{W}$ = 1)

NOTE: C_L includes probe and jig capacitance. tpv is measured from 0.7 × V_{CC} on SCL to 50% I/O (Pn) output. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns. The outputs are measured one at a time, with one transition per measurement. All parameters and waveforms are not applicable to all devices.

Figure 10. GPIO-port Load Circuit and Timing Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)





NOTE: C_L includes probe and jig capacitance. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns. The outputs are measured one at a time, with one transition per measurement. I/Os are configured as inputs. All parameters and waveforms are not applicable to all devices.

Figure 11. Reset Load Circuits and Voltage Waveforms

APPLICATION INFORMATION

POWER-ON RESET REQUIREMENTS

In the event of a glitch or data corruption, TCA7408 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in the figures below:

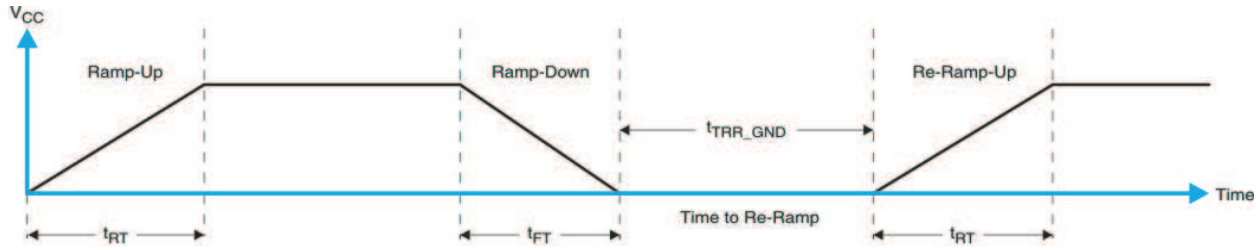


Figure 12. V_{CC} is Lowered Below 0.2 V or 0 V and Then Ramped Up to V_{CC}

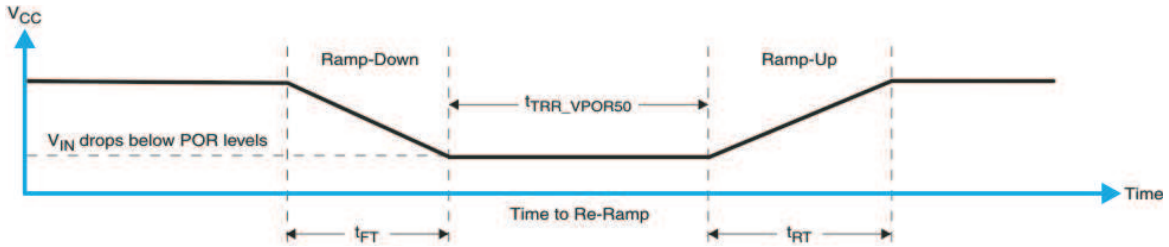


Figure 13. V_{CC} is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CC}

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (t_{GW}) and height (t_{GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 14 provides more information on how to measure these specifications.

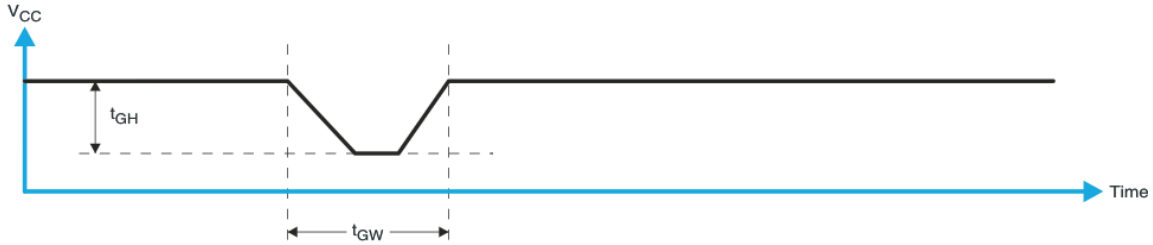


Figure 14. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Figure 15 provides more details on this specification.

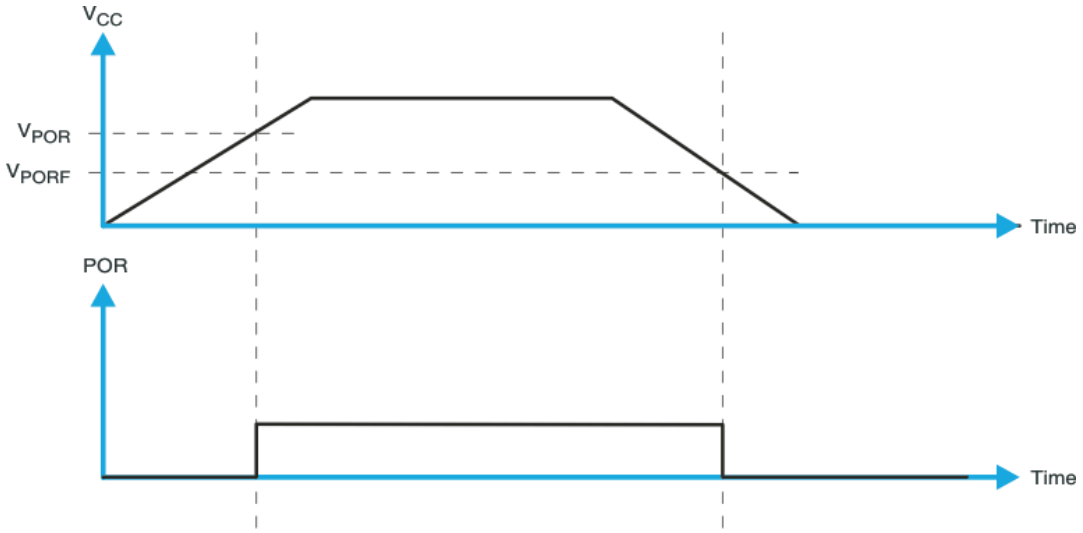


Figure 15. VPOR

The table below specifies the performance of the power-on reset feature for TCA7408 for both types of power-on reset.

RECOMMENDED SUPPLY SEQUENCING AND RAMP RATES AT T_A = 25°C(1)

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{FT}	Fall rate	1		100	ms
t_{RT}	Rise rate	0.1		100	ms
t_{RR_GND}	Time to re-ramp (when V_{CC} drops to GND)	40			µs
t_{RR_POR50}	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV)	40			µs
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CCX_GW} = 1 µs			1.2	V
t_{GW}	Glitch width that will not cause a functional disruption when V_{CCX_GH} = 0.5 × V_{CCx}			10	µs
V_{PORF}	Voltage trip point of POR on falling V_{CC}	0.86		1.22	V
V_{PORR}	Voltage trip point of POR on rising V_{CC}	1.1		1.34	V

(1) Not tested. Specified by design.

REVISION HISTORY

Changes from Revision A (November 2012) to Revision B	Page
• Reverted document back to previous version.	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA7408ZSZR	ACTIVE	uCSP	ZSZ	16	2500	Green (RoHS & no Sb/Br)	0.5NI | 0.2AU	Level-2-260C-1 YEAR	-40 to 85	ZUQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

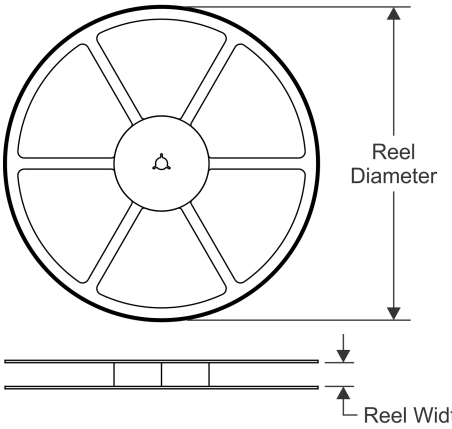
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

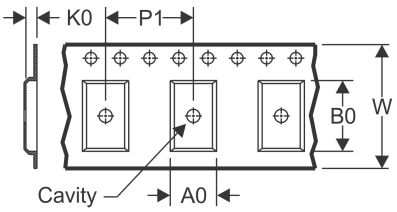
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

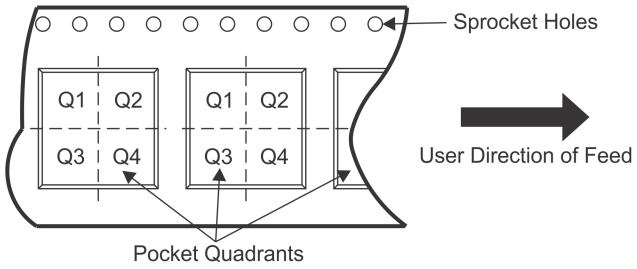


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

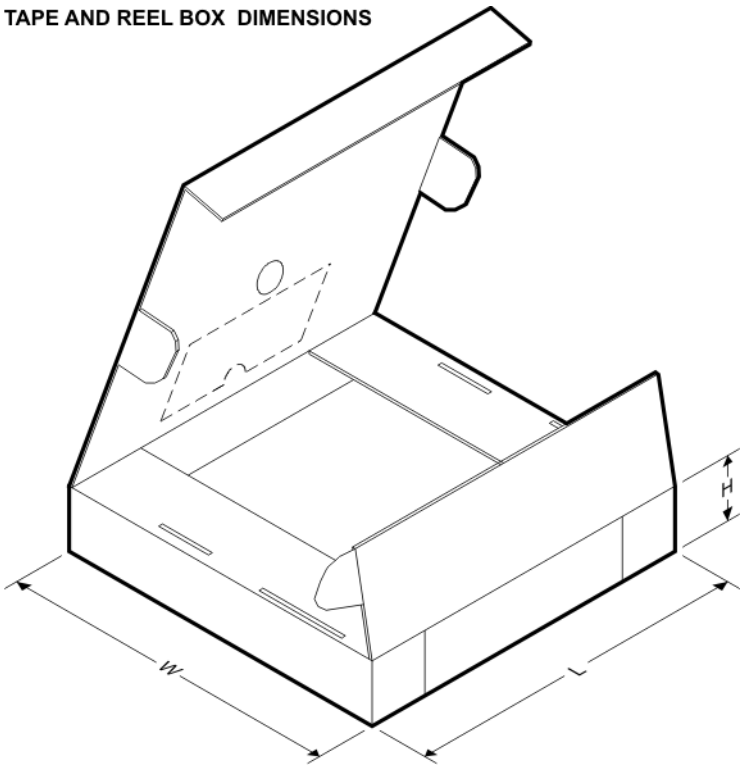
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA7408ZSZR	uCSP	ZSZ	16	2500	330.0	8.4	2.18	2.18	0.7	4.0	8.0	Q1

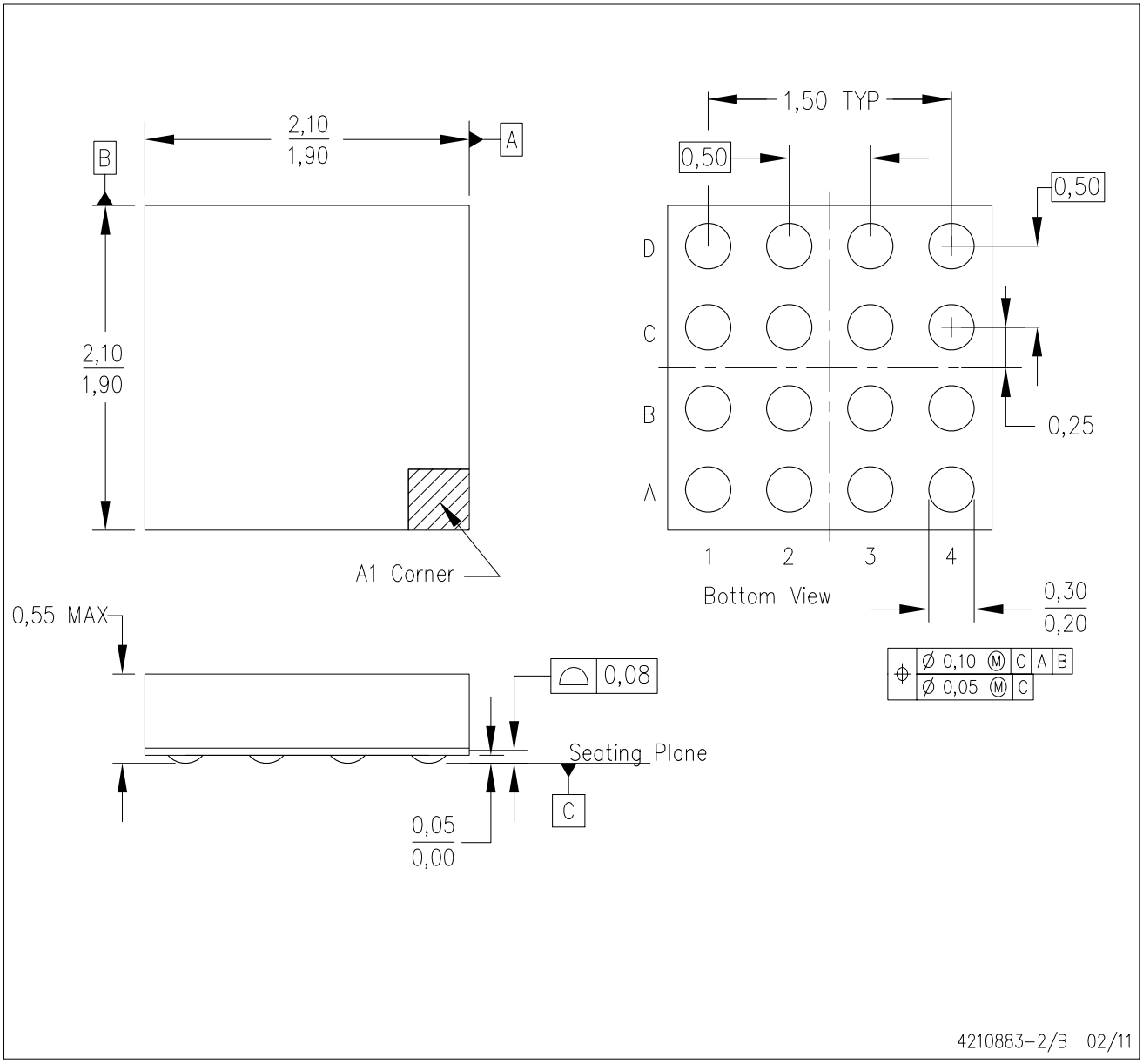
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA7408ZSZR	uCSP	ZSZ	16	2500	338.1	338.1	20.6

ZSZ (S–uCSP–N16) MicrostarCSP™



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. MicrostarCSP™ configuration.
D. This is a PB–free solder ball design.

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