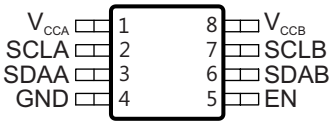
LEVEL-TRANSLATING FM+ I²C BUS REPEATER

Check for Samples: TCA9617A

FEATURES

- **Two-Channel Bidirectional Buffer**
- **Operating Supply Voltage Range of 0.8 V to 5.5 V on A Side**
- **Operating Supply Voltage Range of 2.2 V to 5.5 V on B Side**
- **Voltage-Level Translation From 0.8 V to 5.5 V and 2.2 V to 5.5 V**
- **Footprint and Function Replacement for TCA9517**
- **Active-High Repeater-Enable Input**
- **Open-Drain I²C I/O**
- **5.5-V Tolerant I²C and Enable Input Support**
- **Mixed-Mode Signal Operation**
- **Lockup-Free Operation**
- **Accommodates Standard Mode and Fast Mode I²C Devices and Multiple Masters**
- **Powered-Off High-Impedance I²C Pins**
- **1 Mhz FastMode+ I²C Bus**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **4000-V Human-Body Model (A114-A)**
  - **1500-V Charged-Device Model (C101)**

DGK PACKAGE
(TOP VIEW)



DESCRIPTION

This dual bidirectional I²C™ buffer is operational at 2.2 V to 5.5 V.

The TCA9617A is a BiCMOS integrated circuit intended for I²C bus and SMBus systems. It can provide bidirectional voltage-level translation (up-translation and down-translation) between low voltages (down to 0.8 V) and higher voltages (2.2 V to 5.5 V) in mixed-mode applications. This device enables I²C and similar bus systems to be extended, without degradation of performance even during level shifting.

The TCA9617A buffers both the serial data (SDA) and the serial clock (SCL) signals on the I²C bus, thus allowing two buses of 400-pF bus capacitance to be connected in an I²C application. This device can also be used to isolate two halves of a bus for voltage and capacitance.

ORDERING INFORMATION

For package and ordering information, see the Package Option Addendum at the end of this document.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

The B-side drivers operate from 2.2 V to 5.5 V. The output low level for this internal buffer is approximately 0.5 V, but the input voltage must be 70 mV or more below the output low level when the output is externally driven low. The higher-voltage low signal is called a buffered low. When the B-side I/O is driven low internally, the low is not recognized as a low by the input. This feature prevents a lockup condition from occurring when the input low condition is released.

This type of design on the B side prevents it from being used in series with another TCA9617A B side or other buffers that incorporate a static- or dynamic- offset voltage. This is because these devices do not recognize buffered low signals as a valid low and do not propagate it as a buffered low again.

The A-side drivers operate from 0.8 V to 5.5 V and drive more current. They do not require the buffered low feature (or the static offset voltage). This means that a low signal on the B side translates to a nearly 0-V low on the A side, which accommodates smaller voltage swings of low-voltage logic. The output pulldown on the A side drives a hard low, and the input level is set to 0.3 V_{CCA} to accommodate the need for a lower low level in systems where the low-voltage-side supply voltage is as low as 0.9 V.

The A side of two or more TCA9617As can be connected together to allow a start topography, with the A side on the common bus. Also, the A side can be connected directly to any other buffer with static- or dynamic-offset voltage. Multiple TCA9617As can be connected in series, A side to B side, with no buildup in offset voltage with only time-of-flight delays to consider.

The TCA9617A has an active-high enable (EN) input with an internal pullup to V_{CCB}, which allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up reset. It should never change state during an I^2C operation, because disabling during a bus operation may hang the bus, and enabling part way through the bus cycles could confuse the I^2C parts being enabled. The EN input should change state only when the global bus and repeater port are in the idle state, to prevent system failures.

The TCA9617A includes a power-up circuit that keeps the output drivers turned off until V_{CCB} is above 2.5 V and V_{CCA} is above 0.7 V. V_{CCA} is only used to provide references for the A-side input comparators and the power-good-detect circuit. The TCA9617A internal circuitry and all I/Os are powered by the V_{CCB} pin. V_{CCB} and V_{CCA} can be applied in any sequence at power up. However, due to ESD protection requirements on the SCLA and SDAA, it is recommended to power-up V_{CCB} prior to V_{CCA}.

After power up and with the EN high, the A side falling below 0.7 V_{CCA} turns on the corresponding B-side driver (either SDA or SCL) and drives the B-side down momentarily to 0V before settling to approximately 0.5 V. When the A-side rises above 0.3 V_{CCA}, the B-side pulldown driver is turned off and the external pullup resistor pulls the pin high. If the B side falls first and goes below 0.7 V_{CCB}, the A-side driver is turned on and drives the A-side to 0 V. When the B-side rises above 0.45 V, the A-side pulldown driver is turned off and the external pullup resistor pulls the pin high.

As with the standard I^2C system, pullup resistors are required to provide the logic-high levels on the buffered bus. The TCA9617A has standard open-collector configuration of the I^2C bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with Standard mode, Fast mode and Fast Mode+ I^2C devices.

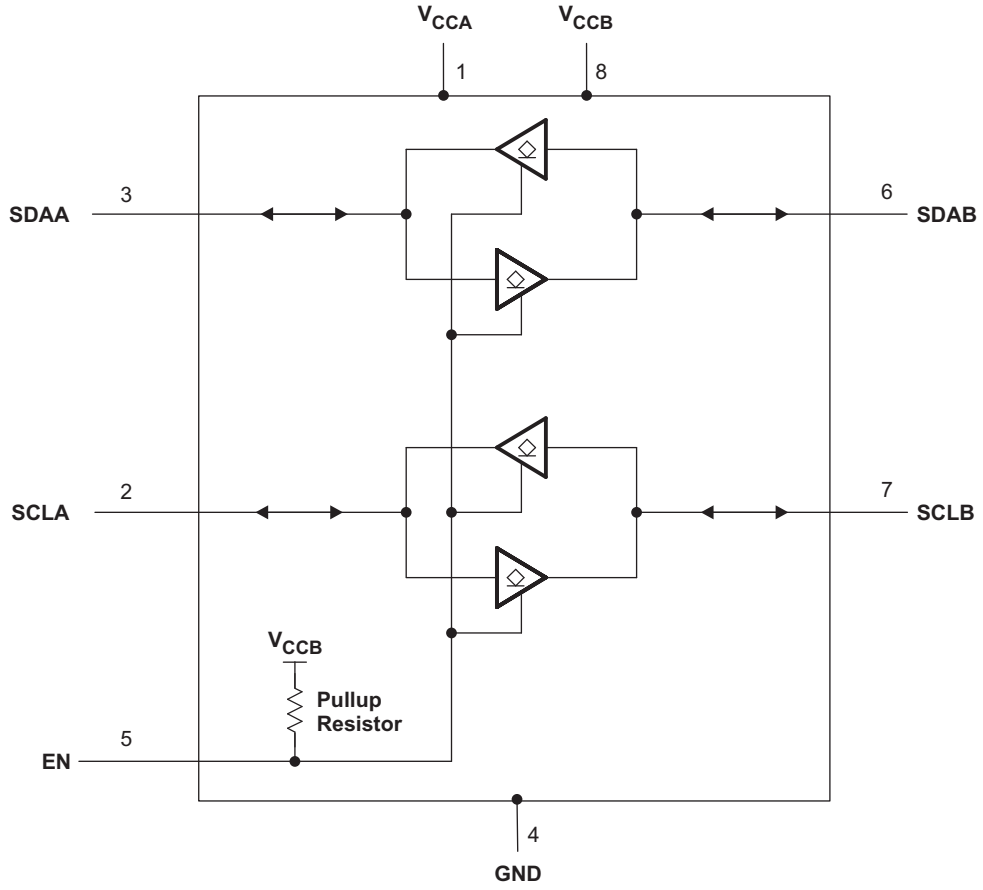
PIN FUNCTIONS

NO.	NAME	DESCRIPTION
1	V_{CCA}	A-side supply voltage (0.8 V to 5.5 V)
2	SCLA	Serial clock bus, A side. Connect to V_{CCA} through a pullup resistor.
3	SDAA	Serial data bus, A side. Connect to V_{CCA} through a pullup resistor.
4	GND	Supply ground
5	EN	Active-high repeater enable input
6	SDAB	Serial data bus, B side. Connect to V_{CCB} through a pullup resistor.
7	SCLB	Serial clock bus, B side. Connect to V_{CCB} through a pullup resistor.
8	V_{CCB}	B-side and device supply voltage (2.2 V to 5.5 V)

Table 1. FUNCTION TABLE

INPUT EN	FUNCTION
L	Outputs disabled
H	SDAA = SDAB SCLA = SCLB

Figure 1. FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCB}	Supply voltage range		–0.5	7	V
V_{CCA}	Supply voltage range		–0.5	7	V
V_I	Enable input voltage range(2)		–0.5	7	V
$V_{I/O}$	I^2C bus voltage range(2)		–0.5	7	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

THERMAL IMPEDANCE

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
θ_{JA}	Package thermal impedance(1)	DGK package		172	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CCA}	Supply voltage, A-side bus		0.8(1)	V_{CCB}	V
V_{CCB}	Supply voltage, B-side bus		2.2	5.5	V
V_{IH}	High-level input voltage	SDAA, SCLA	0.7 × V_{CCA}	V_{CCB}	V
		SDAB, SCLB	0.7 × V_{CCB}	V_{CCB}	
		EN	0.7 × V_{CCB}	5.5	
V_{IL}	Low-level input voltage	SDAA, SCLA		0.3 × V_{CCA}	V
		SDAB, SCLB		0.4	
		EN		0.3 × V_{CCB}	
I_{OLA}	Low-level output current			30	mA
I_{OLB}	Low-level output current		100 µA	30 mA	
T_A	Operating free-air temperature		–40	85	°C

(1) Low-level supply voltage

ELECTRICAL CHARACTERISTICS

V_{CCB} = 2.2 V to 5.5 V, GND = 0 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CCB}	MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = –18 mA	2.2 V to 5.5 V			–1.2	V
V_{OL}	Low-level output voltage	SDAB, SCLB	I_{OL} =100uA or 30mA, V_{ILA} = 0 V	2.2 V to 5.5 V	0.48	0.53	0.58	V
		SDAA, SCLA	I_{OL} = 30mA			0.1	0.2	
I_{CCA}	Quiescent supply current for V_{CCA}		Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open, or SDAA = SCLA = open and SDAB = SCLB = GND				13	µA
I_{CCB}	Quiescent supply current		Both Channels low, SDAA = SCLA = V_{CCA} B-side with pullup resistors IOLB = 100 uA	5.5 V		+4.5	+7	mA
			Both channels low, SDAA = SCLA = GND, ILB=100uA			+5.7	+8.1	
I_I	Input leakage current	SDAB, SCLB	V_I = V_{CCB}	2.2 V to 5.5 V	–1		+1	µA
			V_I = 0.2 V, EN = 0 (1)		–10		+10	
			V_I = V_{CCB} – 0.2 V		–1		+1	
		SDAA, SCLA	V_I = V_{CCA}		–1		+1	
			V_I = 0.2 V		–10		+10	
			V_I = V_{CCA} – 0.2 V		–1		+1	
		EN	V_I = V_{CCB}		–1		+1	
			V_I = 0.2 V		–25			
C_I	Input capacitance	EN	V_I = 3 V or 0 V	3.3 V			7	pF
		SCLA, SCLB	V_I = 3 V or 0 V	3.3 V			9	
				0 V			9	
C_I	Input/output capacitance	SDAA, SDAB	V_I = 3 V or 0 V	3.3 V			14	pF
				0 V			14	

(1) EN taken low to prevent A to B path from impacting input leakage measurement

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
t_{su}	Setup time, EN high before Start condition (1)	100		ns

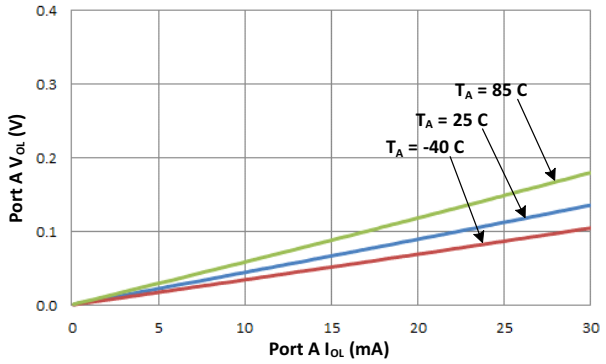
(1) EN should change state only when the global bus and the repeater port are in an idle state.

TIMING REQUIREMENTS

V_{CCA} = 0.8 V to 5.5 V, V_{CCB} = 2.2 V to 5.5 V, GND = 0V, TA = -40°C to 85° (unless otherwise noted)(1)(2)

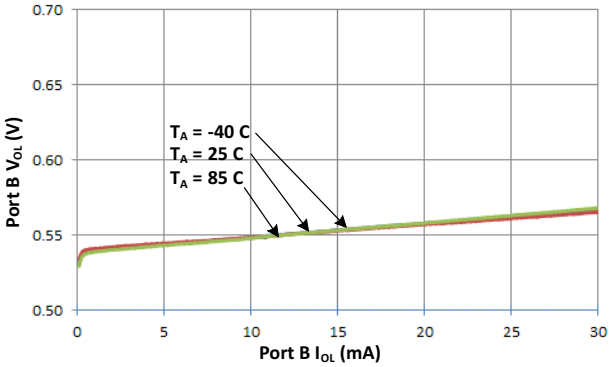
PARAMETER			FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP(3)	MAX	UNIT
t_{PLH}	Propagation delay		SDAB, SCLB	SDAA, SCLA		42	55	90	ns
			SDAA, SCLA	SDAB, SCLB	$V_{CCB} \le 3$ V	61	88	137	
					$V_{CCB} > 3$ V	61	94	250	
t_{PHL}	Propagation delay		SDAB, SCLB	SDAA, SCLA		69	93	144	ns
			SDAA, SCLA	SDAB, SCLB		68	90	140	
t_{TLH}(4)	Transition time	B side	30%	70%			88		ns
		A side	30%	70%			37		ns
t_{THL}	Transition time	B side	70%	30%		5.40	6.41	13.8	ns
		A side				1.40	4.71	11.3	

(1) Times are specified with loads of 240 Ω ±1% and 400 pF ±10% on B-side and 240 Ω ±1% and 200 pF ±10% on A-side. Different load resistance and capacitance alter the RC time constant, thereby changing the propagation delay and transition times.
(2) Pullup voltages are V_{CCA} on the A side and V_{CCB} on the B side.
(3) Typical values were measured with V_{CCA} = 0.9 and V_{CCB} = 2.5V at T_A = 25°C, unless otherwise noted.
(4) T_{TLH} is determined by the pull-up resistance and load capacitance.



Measured with VCCA = 0.9 V and VCCB = 2.2 V

Figure 2. Port A V_{OL} vs I_{OL}



Measured with VCCA = 0.9 V and VCCB = 2.2 V

Figure 3. Port B V_{OL} vs I_{OL}

APPLICATION INFORMATION

A typical application is shown in Figure 4. In this example, the system master is running on a 0.9-V I2C bus, and the slave is connected to a 2.5-V bus. Both buses are running at 400 kHz. Decoupling capacitors are required but are not shown in Figure 2 for simplicity.

The TCA9617A is 5 V tolerant so no additional circuits is required to translate between 0.8-V to 5.5-V bus voltages and 2.7-V to 5.5-V bus voltages.

When the A side of the TCA9617A is pulled low by a driver on the I2C bus, a comparator detects the falling edge when it goes below 0.7 V_{CCA} and cause the internal driver on the B side to turn on. The B-side will first pull-down to 0-V and then settle to 0.5-V. When the B side of the TCA9617A falls below 0.45 V, the TCA9617A will detect the falling edge, turn on the internal driver on the A side and pull the A-side pin down to ground. In order to illustrate what would be seen for an A to B transition refer to Figure 6, and for a B to A transition see Figure 5.

On the B-side bus of the TCA9617A, the clock and data lines will have a positive offset from ground equal to the VOL of the TCA9617A. After the eighth clock pulse, the data line is pulled to the VOL of the slave device, which is close to ground in this example. At the end of the acknowledge, the level rises only to the low level set by the driver of the TCA9617A for a short delay (approximately 0.5-V), while the A-side bus rises above 0.3 V_{CCA} and then continues high.

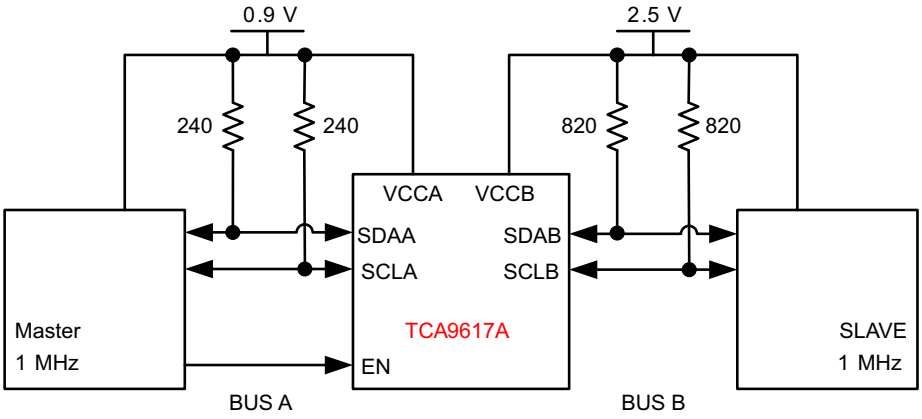


Figure 4. Typical Application Diagrams

Pull-up Resistor Sizing

For the TCA9617A to function correctly, all devices on the B-side must be able to pull the B-side below the voltage input low contention level (0.45-V). This means that the V_{OL} of any device on the B-side must be below 0.4-V to ensure proper operation.

The VOL of a device can be adjusted by changing the IOL through the device which is set by the pull-up resistor value. The pull-up resistor on the B-side must be carefully selected to ensure that logic levels will be transferred correctly to the A-side.

The B-side pullup resistor sizing must also ensure that the RC is greater than 20 ns. Shorter RCs will increase the pedestal overshoot discussed in the next section. Note that the B-side RC should also be less than 1 µs to conform with the I^2C standard mode specification.

B-side Pedestal

Figure 5 depicts the pedestal on the B side of the device. At point 1 in Figure 5 the slave device is driving the B-side low. As the slave releases and the B-side rises, it will only be allowed to rise to 0.5 V until the A-side rises above $0.3V_{CCA}$. This effect is called the pedestal. Once this threshold is crossed the B-side will continue to rise to V_{CCB}.

Due to nature of the B-side pedestal and the static offset voltage, there will be a slight overshoot (point 2) as the B-side rises from the V_{OL} of the B-side driver to the 0.5 V offset. The TCA9617A is designed to control this behavior provided the system is designed with RCs greater than 20 ns. Note that care should be taken to limit the pull-up strength when devices with rise time accelerators are present on the B side. Excessive overshoot on the B-side pedestal may cause devices with rise time accelerators to trip prematurely if the accelerator thresholds are below 0.3 V_{CCB}.

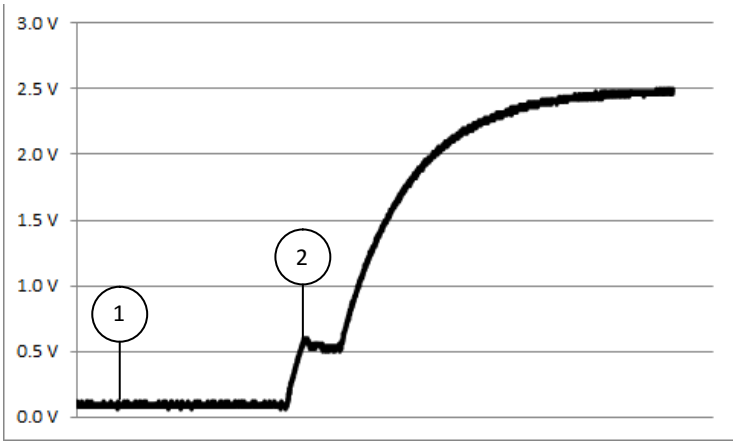


Figure 5. B-side Pedestal

B-side Inverted Pedestal

To decrease the propagation delay of the TCA9617A, an inverted pedestal (Figure 6) is used on the B side of the device. When the A side of the Bus drives to 0.7 V_{CCA} the B side driver will turn on. This will drive the B-side to 0 V for a short period (point 1) and then the B-side will rise to the static offset voltage of 0.5 V (point 2). This design allows the B-side to drive to logic low much faster than simply driving to the static offset as driving to the static offset voltage requires that the fall time be slowed to prevent ringing.

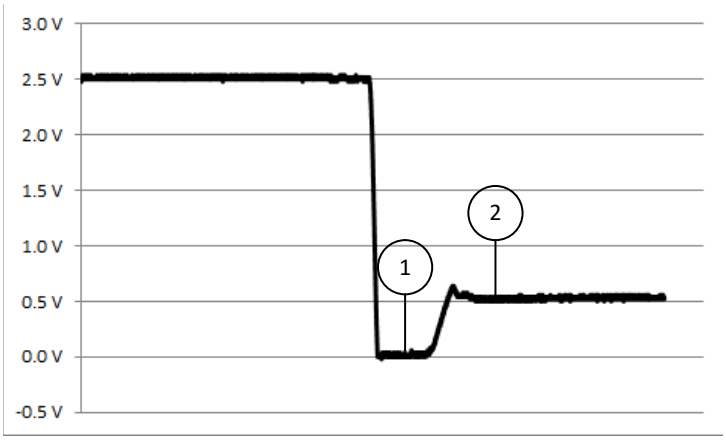


Figure 6. B-side Inverted Pedestal

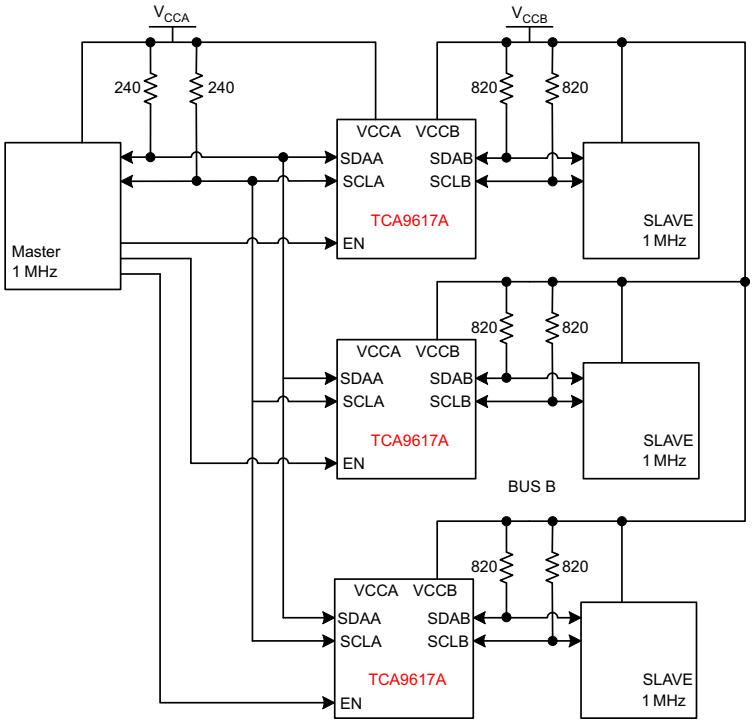


Figure 7. Typical Star Application

Multiple TCA9617A A sides can be connected in a star configuration, allowing all nodes to communicate with each other.

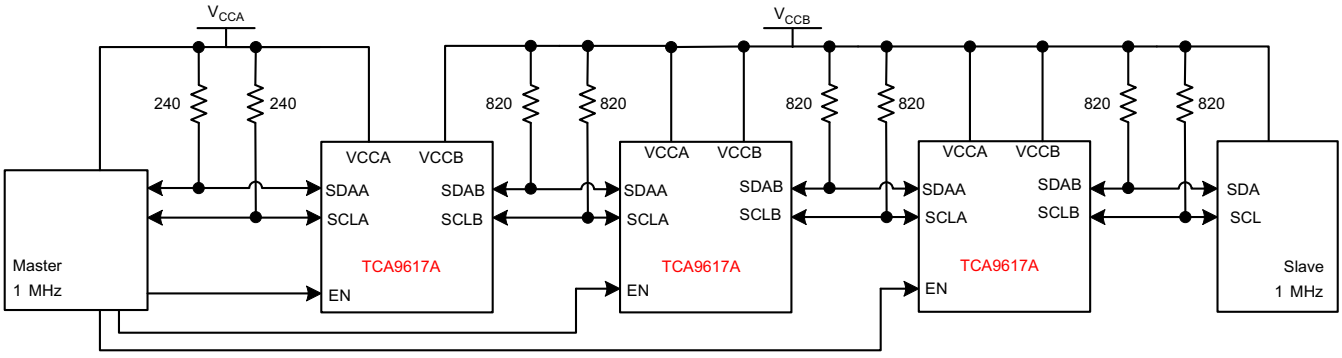


Figure 8. Typical Series Application

Multiple TCA9617As can be connected in series as long as the A side is connected to the B side. I2C bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

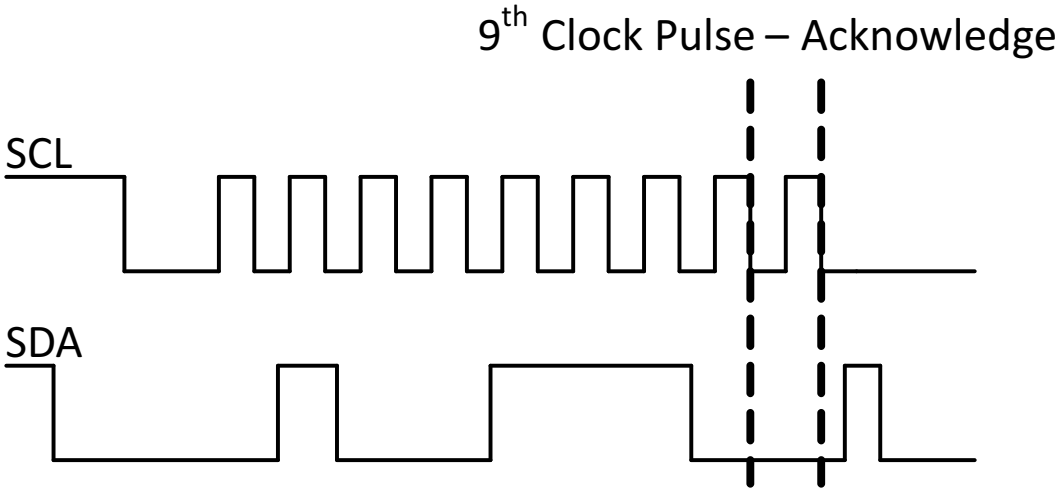


Figure 9. Bus A (0.8 V to 5.5 V Bus) Waveform

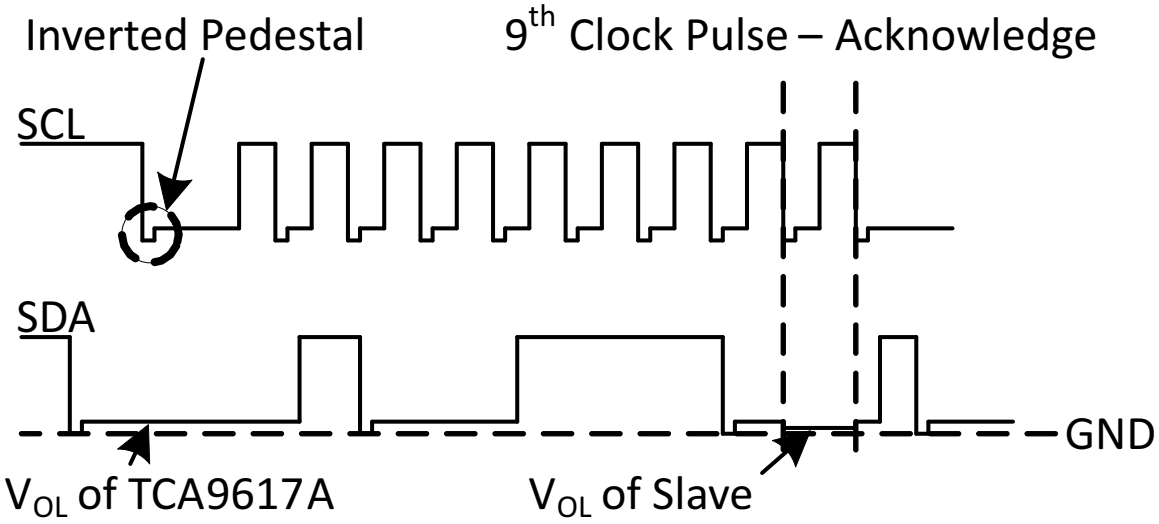


Figure 10. Bus B (2.2 V to 5.5 V Bus) Waveform

PARAMETER MEASUREMENT INFORMATION

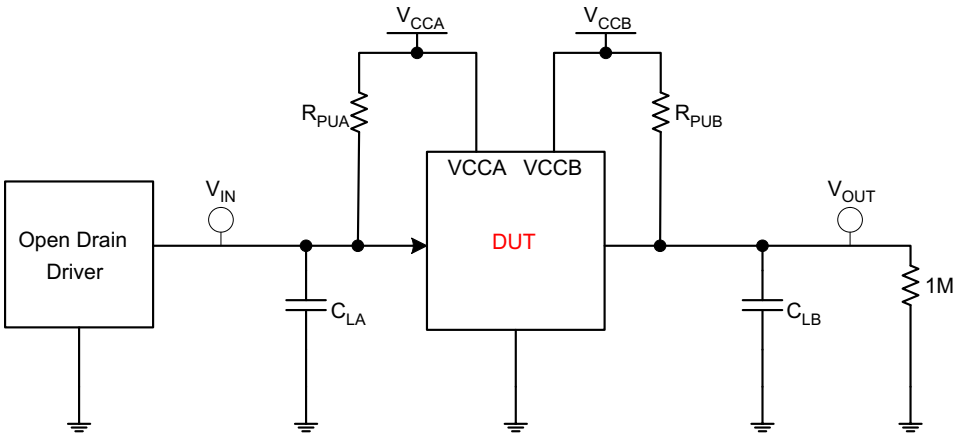
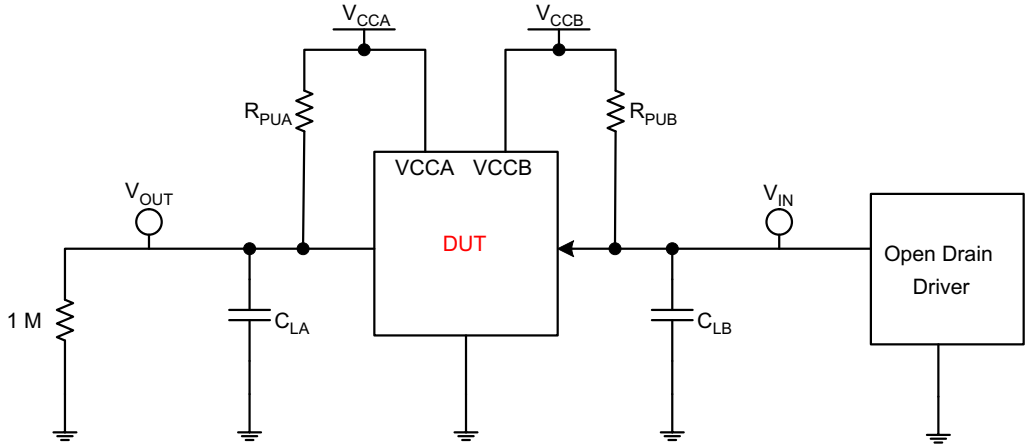


Figure 11. Test Circuit for Open Drain Output from A to B



A. V_{CCA} = 0.9 V

B. V_{CCB} = 2.5 V

C. R_L = 240 Ω on the A-side and the B-side

D. C_L = 200 pF on A-side and 400 pF on B-side includes probe and jig capacitance

E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns

F. The outputs are measured one at a time, with one transition per measurement.

Figure 12. Test Circuit for Open Drain Output from B to A

PARAMETER MEASUREMENT INFORMATION (continued)

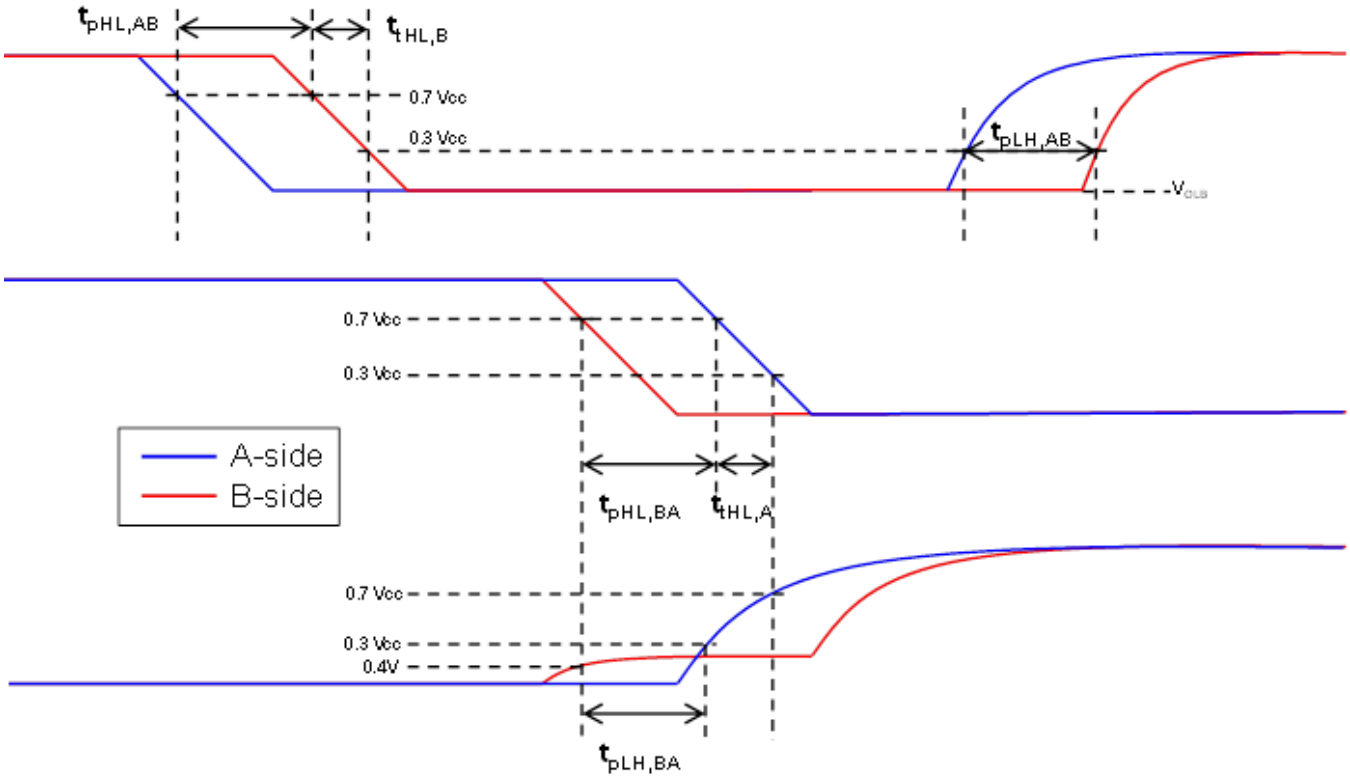


Figure 13. Propagation Delay and Transition Times

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9617ADGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	DWK	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

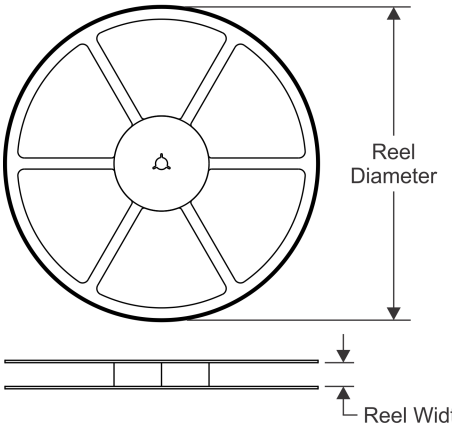
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

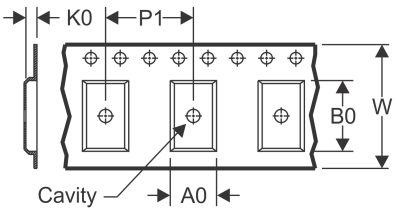
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

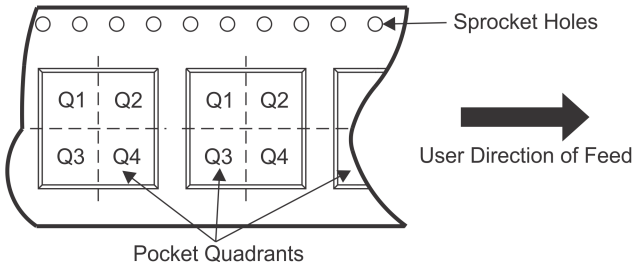


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

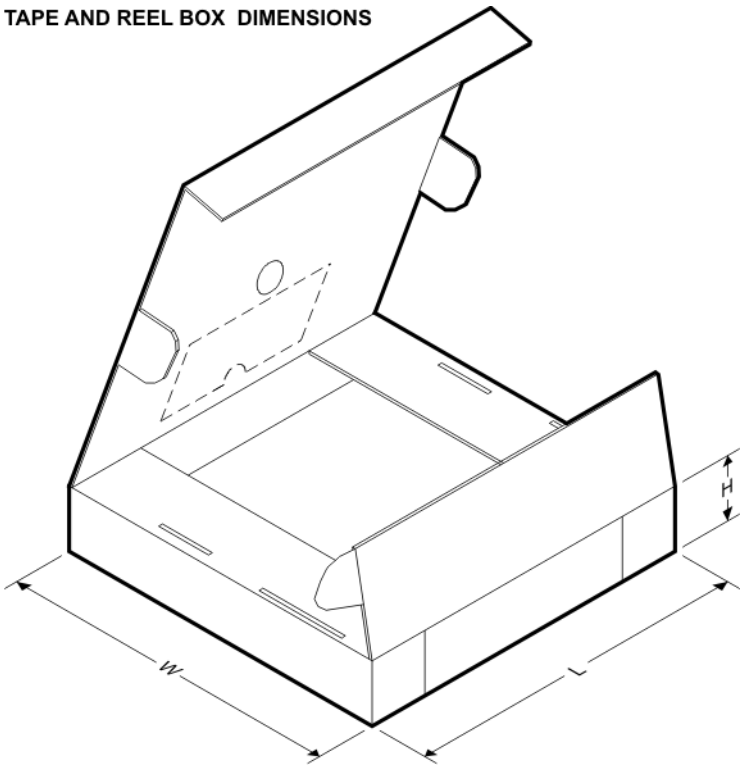
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9617ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

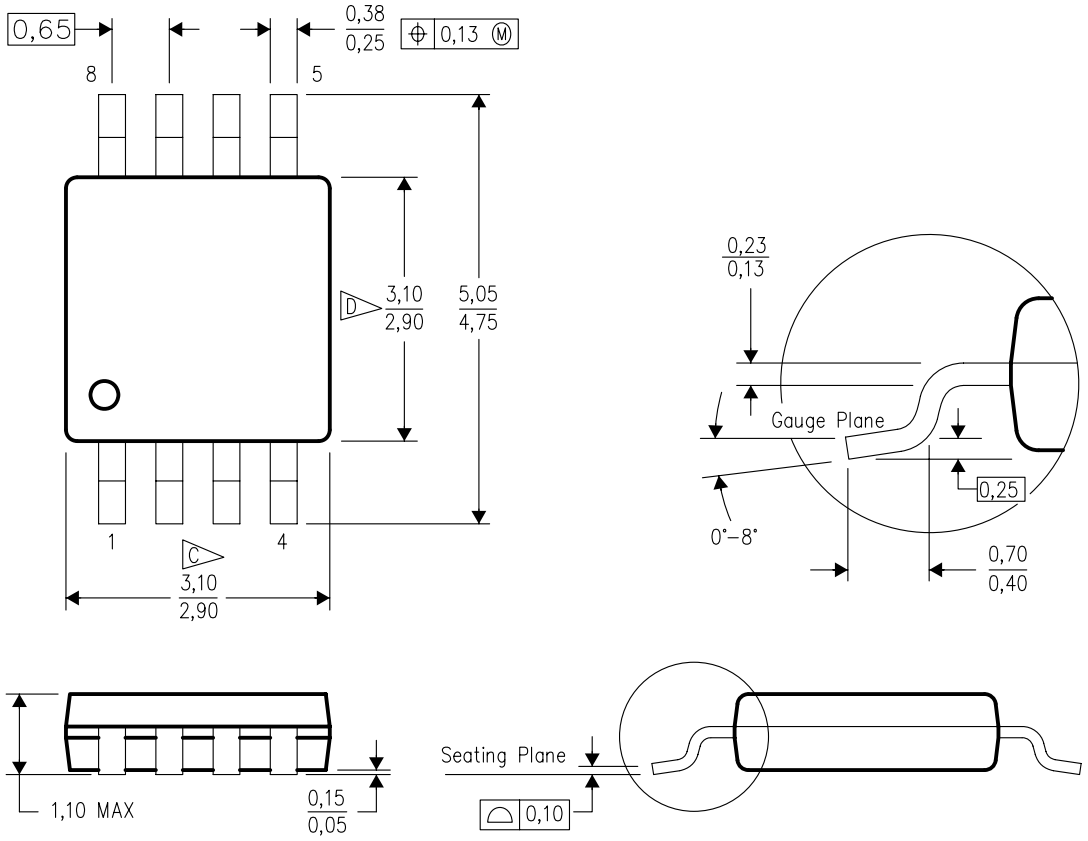
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9617ADGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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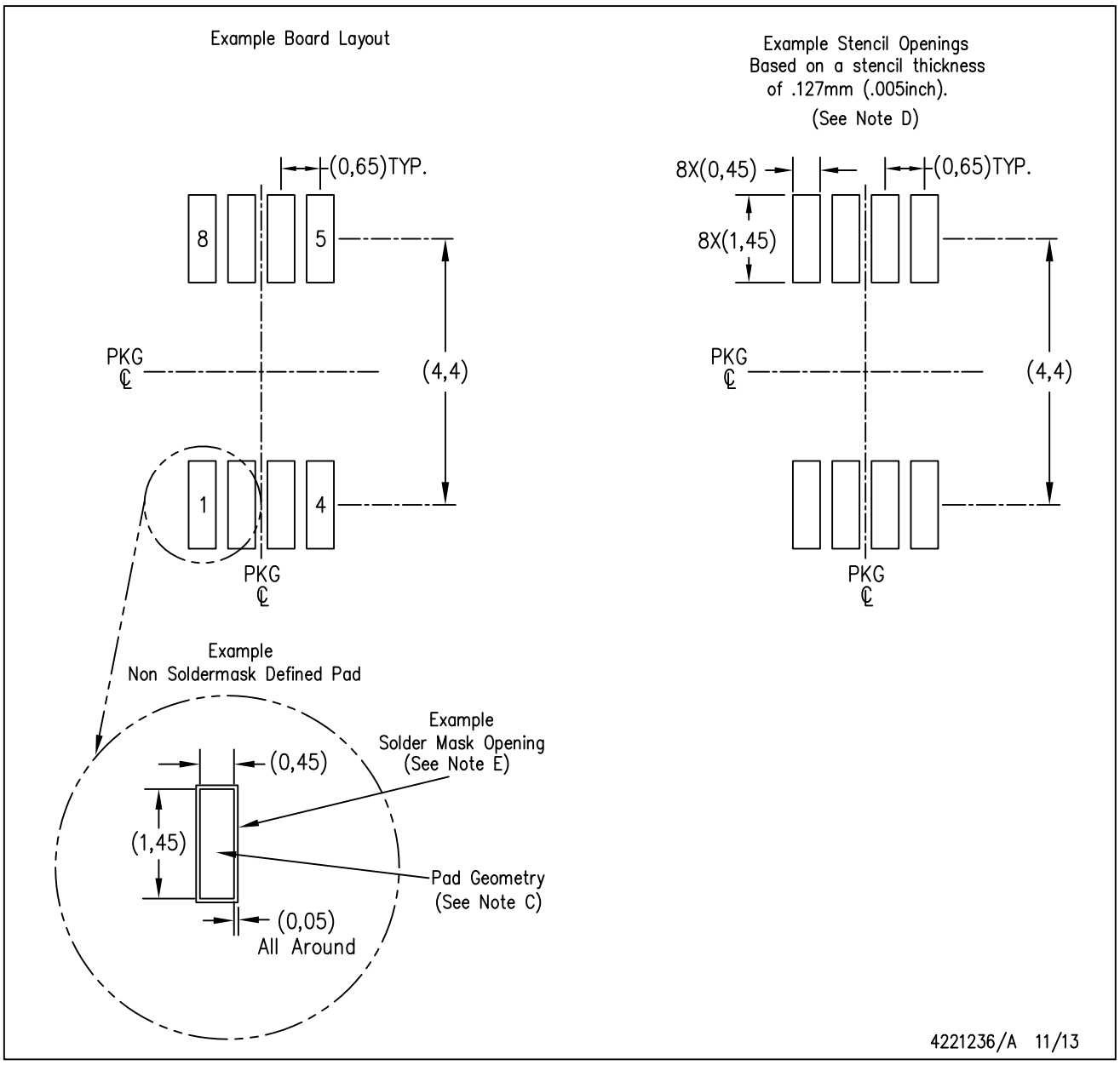
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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