- **Supports Pixel Rates Up to 165MHz (Including 1080p and WUXGA at 60 Hz)**
- **Digital Visual Interface (DVI 1.0) Specification Compliant[1]**
- **Pin-for-Pin Compatible With TFP501 for Simple Upgrade Path to HDCP[2]**
- **True-Color, 24 Bit/Pixel, 16.7M Colors at 1 or 2-Pixels per Clock**
- **Laser Trimmed (50 Ω) Input Stage for Optimum Fixed Impedance Matching**
- **Skew Tolerant up to One Pixel Clock Cycle (High Clock and Data Jitter Tolerance)**
- **4x Over-Sampling for Reduced Bit-Error Rates and Better Performance Over Longer Cables**
- **Reduced Power Consumption—1.8-V Core Operation With 3.3 V I/Os and Supplies[3]**
- **Reduced Ground Bounce Using Time Staggered Pixel Outputs**
- **Lowest Noise and Best Power Dissipation Using PowerPAD™ Packaging**
- **Advanced Technology Using TI 0.18-μm EPIC-5™ CMOS Process**
- **Supports Hot Plug Detection**

description

The Texas Instruments TFP403 is a *PanelBus*™ flat panel display products, part of a comprehensive family of end-to-end DVI 1.0 compliant solutions. Targeted primarily at desktop LCD monitors and digital projectors, the TFP403 finds applications in any design requiring high-speed digital interface.

The TFP403 supports display resolutions up to 1080p and WUXGA in 24-bit true color pixel format. The TFP403 offers design flexibility to drive one or two pixels per clock, supports TFT or DSTN panels, and provides an option for time staggered pixel outputs for reduced ground bounce.

PowerPAD advanced packaging technology results in best of class power dissipation, footprint, and ultralow ground inductance.

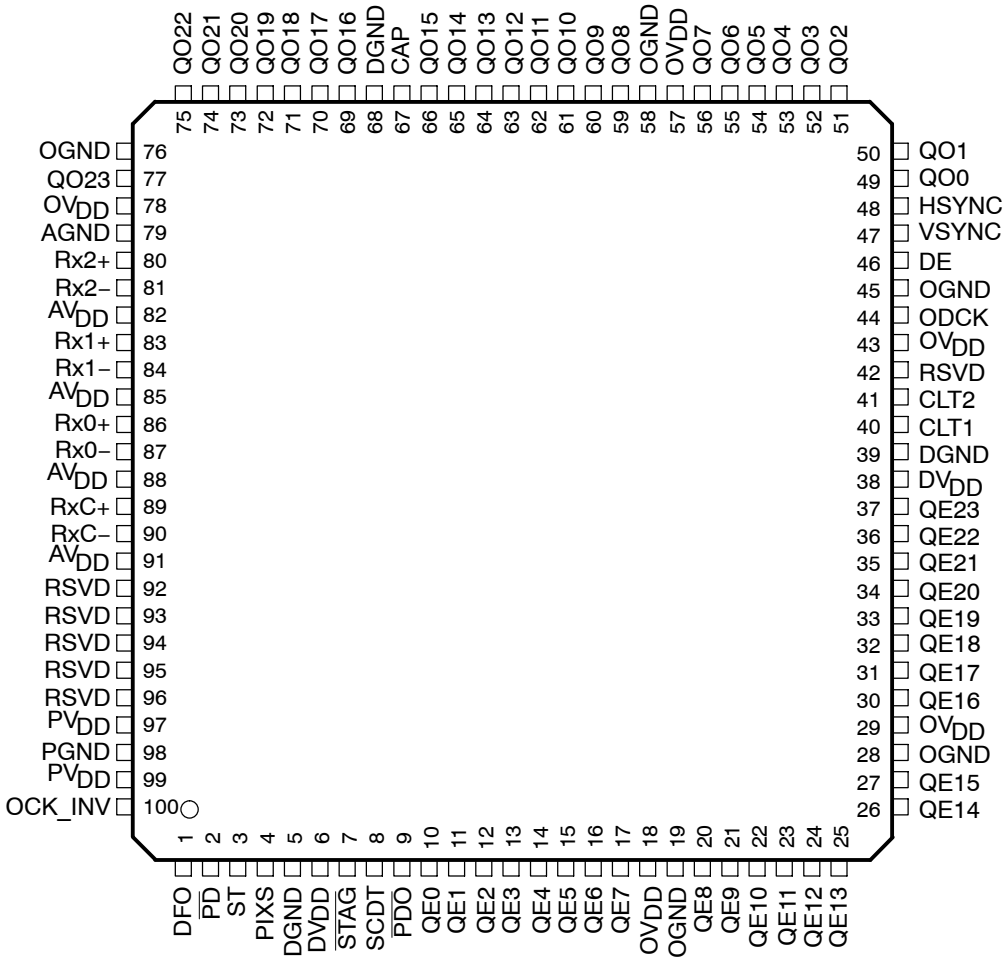
The TFP403 combines *PanelBus*™ circuit innovation with TIs advanced 0.18-μm EPIC-5™ CMOS process technology, along with PowerPAD™ package technology to achieve a reliable, low-powered, low-noise, high-speed digital interface solution.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

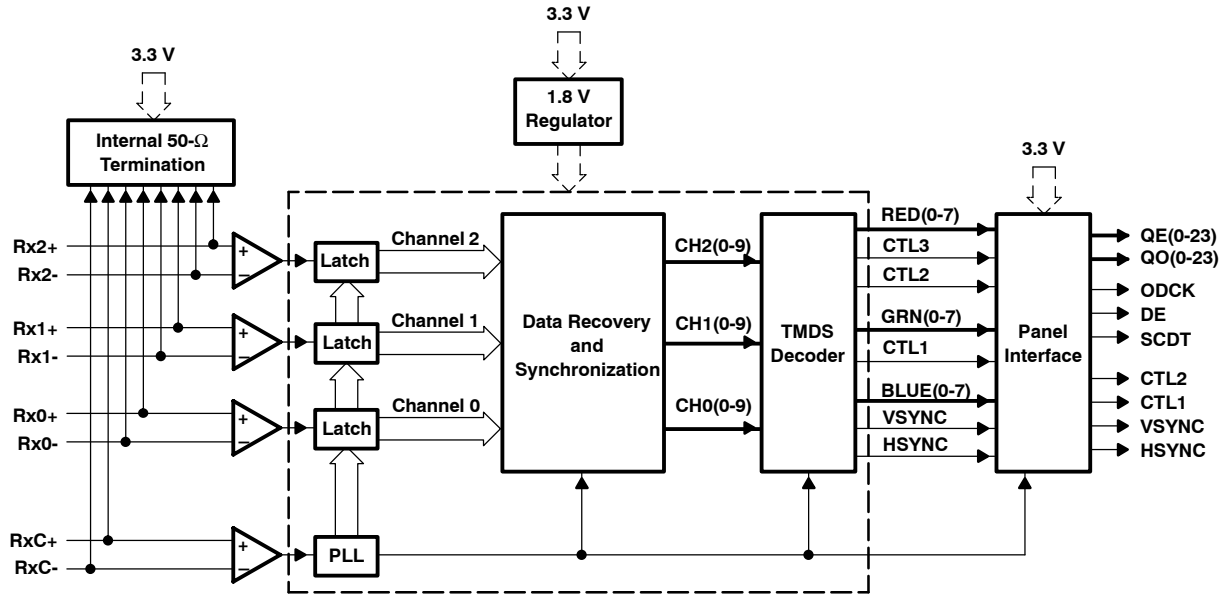
1. The Digital Visual Interface Specification (DVI) is an industry standard developed by the Digital Display Working Group (DDWG) for high-speed digital connection to digital displays. The TFP403 is compliant with the DVI Specification Rev. 1.0.
2. High-bandwidth digital content protection (HDCP) is the system used for protecting DVI outputs from being copied. The TFP501 is TI's DVI receiver with HDCP functionality.
3. The TFP403 has an internal voltage regulator that provides the 1.8-V core power supply from the externally supplied 3.3-V supplies.

PanelBus, PowerPAD, and EPIC-5 are trademarks of Texas Instruments.

PZP PACKAGE
(TOP VIEW)



functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	79	GND	Analog ground—Ground reference and current return for analog circuitry
AV_{DD}	82,85,88, 91	V_{DD}	Analog V_{DD}—Power supply for analog circuitry. Nominally 3.3 V
CAP	67	V_{DD}	Bypass capacitor—4.7 μF tantalum and 0.01 μF ceramic connected to ground. This capacitor is optional for the TFP403, but is required for the TFP501.
CTL[2:1]	41,40	DO	General-purpose control signals—Used for user defined control. In normal mode CTL1 is not powered down via $\overline{PDO}$.
DE	46	DO	Output data enable—Used to indicate time of active video display versus nonactive display or blank time. During blank, only HSYNC, VSYNC, and CTL1-2 are transmitted. During times of active display, or nonblank, only pixel data, QE[23:0] and QO[23:0], is transmitted. High : Active display time Low: Blank time
DFO	1	DI	Output clock data format—Controls the output clock (ODCK) format for either TFT or DSTN panel support. For TFT support ODCK clock runs continuously. For DSTN support ODCK only clocks when DE is high; otherwise ODCK is held low when DE is low. High : DSTN support/ODCK held low when DE = low Low: TFT support/ODCK runs continuously.
DGND	5,39,68	GND	Digital ground—Ground reference and current return for digital core
DV_{DD}	6,38	V_{DD}	Digital V_{DD}—Power supply for digital core. Nominally 3.3 V
HSYNC	48	DO	Horizontal sync output
OCK_INV	100	DI	ODCK polarity—Selects ODCK edge on which pixel data (QE[23:0] and QO[23:0]) and control signals (HSYNC, VSYNC, DE, CTL1-2) are latched Normal mode: High : Latches output data on rising ODCK edge Low : Latches output data on falling ODCK edge

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ODCK	44	DO	Output data clock—Pixel clock. All pixel outputs QE[23:0] and QO[23:0] (if in 2-pixel/clock mode) along with DE, HSYNC, VSYNC, and CTL[2:1] are synchronized to this clock.
OGND	19,28,45, 58,76	GND	Output driver ground—Ground reference and current return for digital output drivers
OV_{DD}	18,29,43, 57,78	V_{DD}	Output driver V_{DD}—Power supply for output drivers. Nominally 3.3 V
$\overline{PD}$	2	DI	Power down—An active low signal that controls the TFP403 power-down state. During power down all output buffers are switched to a high impedance state. All analog circuits are powered down and all inputs are disabled, except for $\overline{PD}$. If $\overline{PD}$ is left unconnected an internal pullup will default the TFP403 to normal operation. High : Normal operation Low: Power down
$\overline{PDO}$	9	DI	Output drive power down—An active low signal that controls the power-down state of the output drivers. During output drive powerdown, the output drivers (except SCDT and CTL1) are driven to a high impedance state. A weak pulldown will slowly pull these outputs to a low level. When $\overline{PDO}$ is left unconnected, an internal pullup defaults the TFP403 to normal operation. High : Normal operation/output drivers on Low: Output drive power down.
PGND	98	GND	PLL GND—Ground reference and current return for internal PLL
PIXS	4	DI	Pixel select—Selects between one or two pixels per clock output modes. During the 2-pixel/clock mode, both even pixels, QE[23:0], and odd pixels, QO[23:0], are output in tandem on a given clock cycle. During 1-pixel/clock, even and odd pixels are output sequentially, one at a time, with the even pixel first, on the even pixel bus, QE[23:0]. (The first pixel per line is pixel-0, the even pixel. The second pixel per line is pixel-1, the odd pixel.) High : 2-pixel/clock Low: 1-pixel/clock
PV_{DD}	97	V_{DD}	PLL V_{DD}—Power supply for internal PLL. Nominally 3.3 V
QE[0:7]	10-17	DO	Even blue pixel output—Output for even and odd blue pixels when in 1-pixel/clock mode. Output for even only blue pixel when in 2-pixel per clock mode. Output data is synchronized to the output data clock, ODCK. LSB: QE0/pin 10 MSB: QE7/pin 17
QE[8:15]	20-27	DO	Even green pixel output—Output for even and odd green pixels when in 1-pixel/clock mode. Output for even only green pixel when in 2-pixel/clock mode. Output data is synchronized to the output data clock, ODCK. LSB: QE8/pin 20 MSB: QE15/pin 27
QE[16:23]	30-37	DO	Even red pixel output—Output for even and odd red pixels when in 1-pixel/clock mode. Output for even only red pixel when in 2-pixel/clock mode. Output data is synchronized to the output data clock, ODCK. LSB: QE16/pin 30 MSB: QE23/pin 37
QO[0:7]	49-56	DO	Odd blue pixel output—Output for odd only blue pixel when in 2-pixel/clock mode. Not used, and held low, when in 1-pixel/clock mode. Output data is synchronized to the output data clock, ODCK. LSB: QO0/pin 49 MSB: QO7/pin 56
QO[8:15]	59-66	DO	Odd green pixel output—Output for odd only green pixel when in 2-pixel/clock mode. Not used, and held low, when in 1-pixel/clock mode. Output data is synchronized to the output data clock, ODCK. LSB: QO8/pin 59 MSB: QO15/pin 66
QO[16:23]	69-75,77	DO	Odd red pixel output—Output for odd only red pixel when in 2-pixel/clock mode. Not used, and held low, when in 1-pixel/clock mode. Output data is synchronized to the output data clock, ODCK. LSB: QO16/pin 69 MSB: QO23/pin 77

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
RSVD	42	DO	Reserved. Must be tied high for normal operation
	92–96	AI	Reserved. See TFP501 data sheet for intended future use.
RxC+	89	AI	Clock positive receiver input—Positive side of reference clock. TMDS low voltage signal differential input pair
RxC–	90	AI	Clock negative receiver input—Negative side of reference clock. TMDS low voltage signal differential input pair
Rx0+	86	AI	Channel-0 positive receiver input—Positive side of channel-0. TMDS low voltage signal differential input pair. Channel-0 receives blue pixel data in active display and HSYNC, VSYNC control signals in blank.
Rx0–	87	AI	Channel-0 negative receiver input—Negative side of channel-0. TMDS low voltage signal differential input pair.
Rx1+	83	AI	Channel-1 positive receiver input—Positive side of channel-1 TMDS low voltage signal differential input pair. Channel-1 receives green pixel data in active display and CTL1 control signals in blank.
Rx1–	84	AI	Channel-1 negative receiver input—Negative side of channel-1 TMDS low voltage signal differential input pair
Rx2+	80	AI	Channel-2 positive receiver input—Positive side of channel-2 TMDS low voltage signal differential input pair. Channel-2 receives red pixel data in active display and CTL2 control signals in blank.
Rx2–	81	AI	Channel-2 negative receiver input—Negative side of channel-2 TMDS low voltage signal differential input pair.
SCDT	8	DO	Sync detect—Output to signal when the link is active or inactive. The link is considered to be active when DE is actively switching. The TFP403 monitors the state DE to determine link activity. SCDT can be tied externally to $\overline{PDO}$ to power down the output drivers when the link is inactive. High: Active link Low: Inactive link
ST	3	DI	Output drive strength select—Selects output drive strength for high or low current drive. (See dc specifications for I_{OH} and I_{OL} vs ST state.) High : High drive strength Low : Low drive strength
$\overline{STAG}$	7	DI	Staggered pixel select—An active low signal used in the 2-pixel/clock pixel mode (PIXS = high). Time staggers the even and odd pixel outputs to reduce ground bounce. Normal operation outputs the odd and even pixels simultaneously. High : Normal simultaneous even/odd pixel output Low: Time staggered even/odd pixel output
VSYNC	47	DO	Vertical sync output

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, DV_{DD}, AV_{DD}, OV_{DD}, PV_{DD} . . . . . –0.3 V to 4 V
Input voltage range, logic/analog signals . . . . . –0.3 V to 4 V
Operating ambient temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C
Case temperature for 10 seconds . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Package power dissipation/PowerPAD: Soldered (see Note 1) . . . . . 4.3 W
Not soldered (see Note 2) . . . . . 2.7 W
ESD Protection, all pins . . . . . 2.5 KV Human Body Model
JEDEC latch up (EIA/JESD78) . . . . . 100 mA

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Specified with PowerPAD bond pad on the backside of the package soldered to a 2 oz. Cu plate PCB thermal plane. Specified at maximum allowed operating temperature, 70°C.
2. PowerPAD bond pad on the backside of the package is not soldered to a thermal plane. Specified at maximum allowed operating temperature, 70°C.

recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply voltage, V_{DD} (DV_{DD}, AV_{DD}, PV_{DD}, OV_{DD})	3	3.3	3.6	V
Pixel time, t_{pix}‡	6.06		40	ns
Single ended analog input termination resistance, R_t	45	50	55	Ω
Operating free-air temperature, T_A	0	25	70	°C

‡ t_{pix} is the pixel time defined as the period of the RxC clock input. The period of the output clock, ODCK is equal to t_{pix} when in 1-pixel/clock mode and $2t_{pix}$ when in 2-pixel/clock mode.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

dc digital I/O specifications

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High level digital input voltage†			2		DV_{DD}	V
V_{IL}	Low level digital input voltage†			0		0.8	V
I_{OH}	High level output drive current‡	ST = High,	V_{OH} = 2.4 V	5	10	18	mA
		ST = Low,	V_{OH} = 2.4 V	3	6	12	
I_{OL}	Low level output drive current‡	ST = High,	V_{OL} = 0.8 V	10	13	19	mA
		ST = Low,	V_{OL} = 0.8 V	5	7	11	
I_{OZ}	Hi-Z output leakage current	$\overline{PD}$ = Low or $\overline{PDO}$ = Low		–1		1	μA

† Digital inputs are labeled DI in I/O column of Terminal Functions Table.
‡ Digital outputs are labeled DO in I/O column of Terminal Functions Table.

dc specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ID}	Analog input differential voltage (see Note 3)		75		1200	mv
V_{IC}	Analog input common mode voltage (see Note 3)		AV_{DD}-300		AV_{DD}-37	mv
$V_{I(OC)}$	Open circuit analog input voltage		AV_{DD}-10		AV_{DD}+10	mv
$I_{DD(2PIX)}$	Normal 2-pix/clock power supply current (see Note 4)	PIXEL RATE = 82.5 MHz 2-pix/clock			400	mA
$I_{(PD)}$	Power down current (see Note 5)	$\overline{PD}$ = Low			10	mA
$I_{(PDO)}$	Output drive power down current (see Note 5)	$\overline{PDO}$ = Low			45	mA

NOTES: 3. Specified as dc characteristic with no overshoot or undershoot.
4. Alternating 2-pixel black/2-pixel white pattern. ST = high, $\overline{STAG}$ = high, QE[23:0] and QO[23:0] C_L = 10 pF.
5. Analog inputs are open circuit (transmitter is disconnected from TFP403).

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

ac specifications

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ID(2)}$	Differential input sensitivity†			150		1560	mV_{p-p}
t_{ps}	Analog input intra-pair (+ to -) differential skew (see Note 6)					0.4	t_{bit}‡
$t_{(ccs)}$	Analog Input inter-pair or channel-to-channel skew (see Note 6) Analog Input inter-pair or channel-to-channel skew (see Note 6)					1	t_{pix}§
$t_{(ijit)}$	Worse case differential input clock jitter tolerance¶ (see Note 6) Worse case differential input clock jitter tolerance¶ (see Note 6)			50			ps
$t_{f(1)}$	Fall time of data and control signals#, ‖		ST = Low, C_L = 5 pF ST = High, C_L = 10 pF			2.4 1.9	ns
$t_{r(1)}$	Rise time of data and control signals#, ‖		ST = Low, C_L = 5 pF ST = High, C_L = 10 pF			2.4 1.9	ns
$t_{r(2)}$	Rise time of ODCK clock#		ST = Low, C_L = 5 pF ST = High, C_L = 10 pF			2.4 1.9	ns
$t_{f(2)}$	Fall time of ODCK clock#		ST = Low, C_L = 5 pF ST = High, C_L = 10 pF			2.4 1.9	ns
$t_{su(1)}$	Setup time, data, and control signal to falling edge of ODCK	1 pixel, OCK_INV = low‖, PIXS = low	ST = Low, C_L = 5 pF ST = High, C_L = 10 pF	1.0			ns
$t_{h(1)}$	Hold time, data, and control signal to falling edge of ODCK	1 pixel, OCK_INV = low‖, PIXS = low	ST = Low, C_L = 5 pF ST = High, C_L = 10 pF	1.0			ns
$t_{su(2)}$	Setup time, data, and control signal to rising edge of ODCK	1 pixel, OCK_INV = high‖, PIXS = low	ST = Low, C_L = 5 pF ST = High, C_L = 10 pF	1.0			ns
$t_{h(2)}$	Hold time, data, and control signal to rising edge of ODCK	2 pixel and STAG OCK_INV = high‖ PIXS = high	ST = Low, C_L = 5 pF ST = High, C_L = 10 pF	0.5			ns
$f_{(ODCK)}$	ODCK frequency		PIX = Low (1-PIX/CLK)	25		165	MHz
			PIX = High (2-PIX/CLK)	12.5		82.5	
	ODCK duty-cycle			40%	50%	60%	
$t_{pd(PDL)}$	Propagation delay time from $\overline{PD}$ low to Hi-Z outputs					9	ns
$t_{pd(PDOL)}$	Propagation delay time from $\overline{PDO}$ low to Hi-Z outputs					9	ns
$t_{t(HSC)}$	Transition time between DE transition to SCDT low☆				1e6		t_{pix}
$t_{t(FSC)}$	Transition time between DE transition to SCDT high☆				1600		t_{pix}
t_d	Delay time, ODCK latching edge to QE[23:0] data output		$\overline{STAG}$ = Low Pixs = High		0.5		t_{pix}

† Specified as ac parameter to include sensitivity to overshoot, undershoot, and reflection.
‡ t_{bit} is 1/10 the pixel time, tpix
§ t_{pix} is the pixel time defined as the period of the RxC input clock. The period of ODCK is equal to t_{pix} in 1-pixel/clock mode or $2t_{pix}$ when in 2-pixel/clock mode.
¶ Measured differentially at 50% crossing using ODCK output clock as trigger.
# Rise and fall times measured as time between 20% and 80% of signal amplitude.
‖ Data and control signals are : QE[23:0], QO[23:0], DE, HSYNC, VSYNC and CTL[2:1]
☆Link active or inactive is determined by amount of time detected between DE transitions. SCDT indicates link activity.
NOTE 6: By characterization

PARAMETER MEASUREMENT INFORMATION

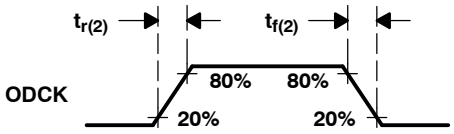


Figure 1. Rise and Fall Time of ODCK

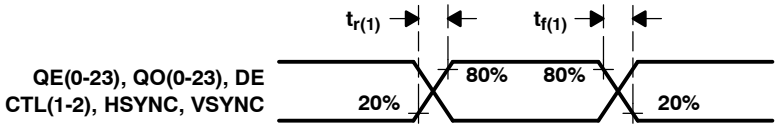


Figure 2. Rise and Fall Time of Data and Control Signals

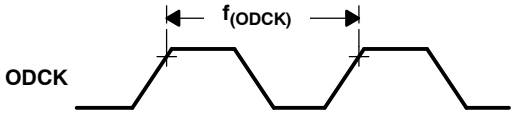


Figure 3. ODCK Frequency

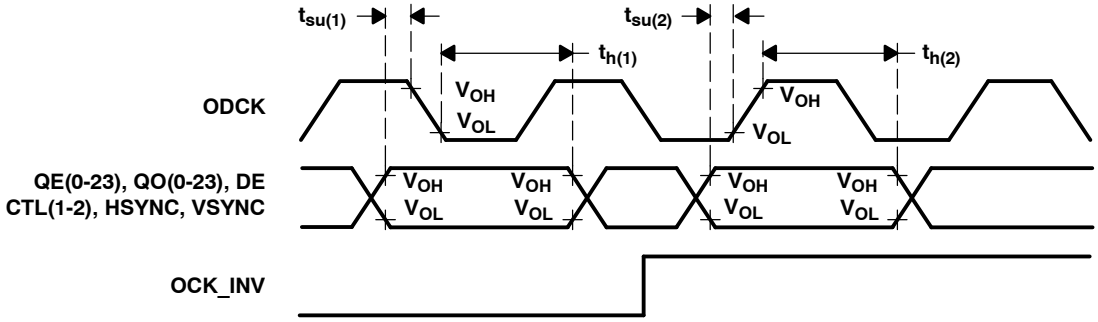


Figure 4. Data Setup and Hold Time to Rising and Falling Edge of ODCK

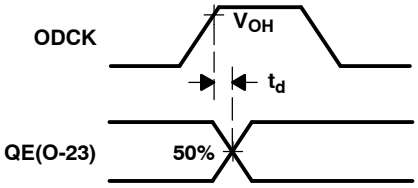


Figure 5. ODCK High to QE[23:0] Staggered Data Output

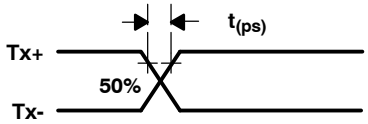


Figure 6. Analog Input Intra-Pair Differential Skew

PARAMETER MEASUREMENT INFORMATION

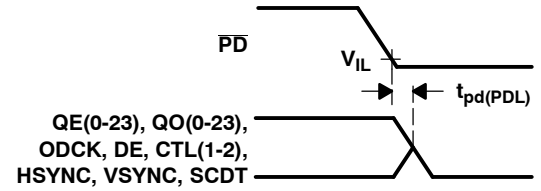


Figure 7. Delay From $\overline{PD}$ Low to Hi-Z Outputs

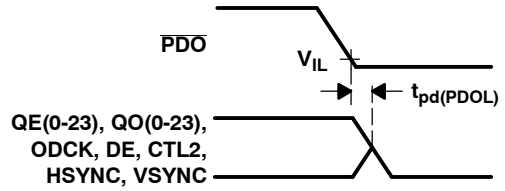


Figure 8. Delay From $\overline{PDO}$ Low to Hi-Z Outputs

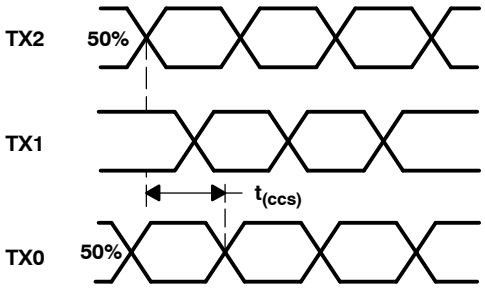


Figure 9. Analog Input Channel-to-Channel Skew

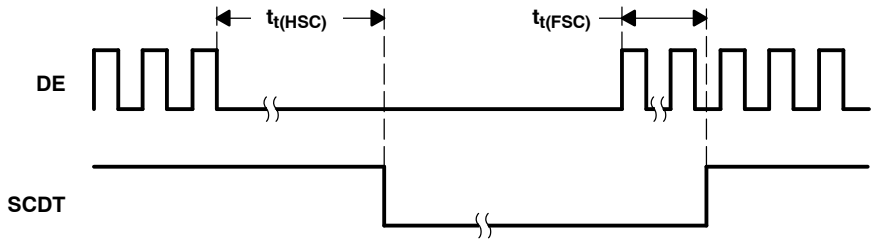


Figure 10. Time Between DE Transitions to SCDT Low and SCDT High

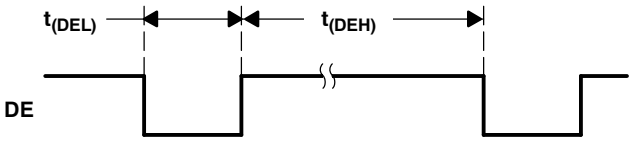


Figure 11. Minimum DE Low and Maximum DE High

detailed description

fundamental operation

The TFP403 is a digital visual interface (DVI) compliant TMDS digital receiver that is used in digital flat panel display systems to receive and decode TMDS encoded RGB pixel data streams. In a digital display system a host, usually a PC or workstation, contains a DVI compatible transmitter that receives 24 bit pixel data along with appropriate control signals. The transmitter encodes them into a high-speed low-voltage differential serial bit stream optimized for transmission over a twisted-pair cable to a display device. The display device, usually a flat-panel monitor, will require a DVI compatible receiver like the TI TFP403 to decode the serial bit stream back to the same 24 bit pixel data and control signals that originated at the host. This decoded data can then be applied directly to the flat panel drive circuitry to produce an image on the display. Since the host and display can be separated by distances up to 5 meters or more, serial transmission of the pixel data is preferred. To support modern display resolutions up to UXGA a high bandwidth receiver with good jitter and skew tolerance is required.

TMDS pixel data and control signal encoding

TMDS stands for transition minimized differential signaling. Only one of two possible TMDS characters for a given pixel will be transmitted at a given time. The transmitter keeps a running count of the number of ones and zeros previously sent and transmits the character that will minimize the number of transitions and approximate a dc balance of the transmission line.

Three TMDS channels are used to receive RGB pixel data during active display time, DE = high. The same three channels also receive control signals, HSYNC, VSYNC, and user defined control signals CTL[2:1]. These control signals are received during inactive display or blanking-time. Blanking-time is when DE = low. The following table maps the received input data to appropriate TMDS input channel in a DVI compliant system.

RECEIVED PIXEL DATA ACTIVE DISPLAY DE = HIGH	INPUT CHANNEL	OUTPUT PINS (VALID FOR DE = HIGH)
Red[7:0]	Channel – 2 (Rx2 ±)	QE[23:16] QO[23:16]
Green[7:0]	Channel – 1 (Rx1 ±)	QE[15:8] QO[15:8]
Blue[7:0]	Channel – 0 (Rx0 ±)	QE[7:0] QO[7:0]
RECEIVED CONTROL DATA BLANKING DE = LOW	**INPUT CHANNEL**	**OUTPUT PINS (VALID FOR DE = LOW)**
CTL[3:2] (see Note 7)	Channel – 2 (Rx2 ±)	CTL2
CTL[1: 0] (see Note 7)	Channel – 1 (Rx1 ±)	CTL1
HSYNC, VSYNC	Channel – 0 (Rx0 ±)	HSYNC, VSYNC

NOTE 7: Some TMDS transmitters transmit a CTL0 signal. The TFP403 decodes and transfers CTL[2:1] and ignores CTL0 characters. CTL3 is used internally to enable HDCP decryption. CTL3 and CTL0 are not available as TFP501 outputs.

The TFP403 discriminates between valid pixel TMDS characters and control TMDS characters to determine the state of active display versus blanking, i.e., state of DE.

detailed description (continued)

TFP403 clocking and data synchronization

The TFP403 receives a clock reference from the DVI transmitter that has a period equal to the pixel time, Tpix. The frequency of this clock is also referred to as the pixel rate. Since the TMDS encoded data on Rx[2:0] contains 10 bits per 8 bit pixel it follows that the Rx[2:0] serial bit rate is 10 times the pixel rate. For example, the required pixel rate to support an UXGA resolution with 60 Hz refresh rate is 165 MHz. The TMDS serial bit rate is 10x the pixel rate or 1.65 Gb/s. Due to the transmission of this high-speed digital bit stream, on three separate channels (or twisted-pair wires) of long distances (3-5 meters), phase synchronization between the data steams and the input reference clock is not guaranteed. In addition, skew between the three data channels is common. The TFP403 uses a 4x oversampling scheme of the input data streams to achieve reliable synchronization with up to 1-Tpix channel-to-channel skew tolerance. Accumulated jitter on the clock and data lines due to reflections and external noise sources is also typical of high speed serial data transmission, hence the TFP403s design for high jitter tolerance.

The input clock to the TFP403 is conditioned by a phase-locked-loop (PLL) to remove high frequency jitter from the clock. The PLL provides four 10x clock outputs of different phase to locate and sync the TMDS data streams (4x oversampling). During active display the pixel data is encoded to be transition minimized, whereas in blank, the control data is encoded to be transition maximized. A DVI compliant transmitter is required to transmit in blank for a minimum period of time, 128-Tpix, to ensure sufficient time for data synchronization when the receiver sees a transition maximized code. Synchronization during blank, when the data is transition maximized, ensures reliable data bit boundary detection. Phase synchronization to the data streams is unique for each of the three input channels and is maintained as long as the link remains active.

TFP403 TMDS input levels and input impedance matching

The TMDS inputs to the TFP403 receiver have a fixed single-ended termination to AV_{DD} The TFP403 is internally optimized using a laser trim process to precisely fix the impedance at 50 Ω. The device will function normally with or without a resistor on the EXT_RES pin, so it remains drop-in compatible with current sockets. The fixed impedance eliminates the need for an external resistor while providing optimum impedance matching to standard 50-Ω DVI cables.

Figure 12 shows a conceptual schematic of a DVI transmitter and TFP403 receiver connection. A transmitter drives the twisted pair cable via a current source, usually achieved with an open drain type output driver. The internal resistor, which is matched to the cable impedance, at the TFP403 input provides a pullup to AV_{DD}. Naturally, when the transmitter is disconnected and the TFP403 DVI inputs are left unconnected, the TFP403 receiver inputs pullup to AV_{DD}. The single ended differential signal and full differential signal is shown in Figure 13. The TFP403 is designed to respond to differential signal swings ranging from 150 mV to 1.56 V with common mode voltages ranging from (AV_{DD}-300 mV) to (AV_{DD}-37 mV).

TFP403 TMDS input levels and input impedance matching (continued)

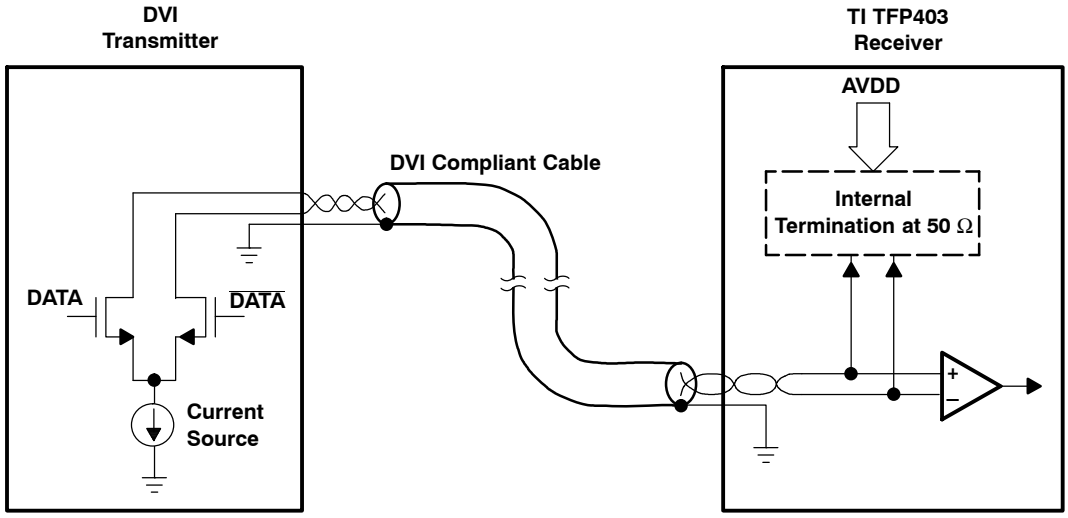


Figure 12. TMDS Differential Input and Transmitter Connection

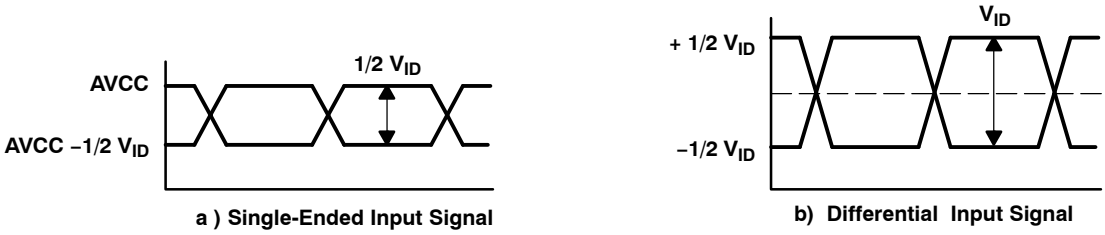


Figure 13. TMDS Inputs

TFP403 modes of operation

The TFP403 provides systems design flexibility and value by providing the system designer with configurable options or modes of operation to support varying system architectures. The following table outlines the various panel modes that can be supported along with appropriate external control pin settings.

PANEL	PIXEL RATE	ODCK LATCH EDGE	ODCK	DFO	PIXS	OCK_INV
TFT or 16-bit DSTN	1 pix/clock	Falling	Free run	0	0	0
TFT or 16-bit DSTN	1 pix/clock	Rising	Free run	0	0	1
TFT	2 pix/clock	Falling	Free run	0	1	0
TFT	2 pix/clock	Rising	Free run	0	1	1
24-bit DSTN	1 pix/clock	Falling	Gated low	1	0	0
NONE	1 pix/clock	Rising	Gated low	1	0	1
24-bit DSTN	2 pix/clock	Falling	Gated low	1	1	0
24-bit DSTN	2 pix/clock	Rising	Gated low	1	1	1

detailed description (continued)

TFP403 output driver configurations

The TFP403 provides flexibility by offering various output driver features that can be used to optimize power consumption, ground-bounce, and power-supply noise. The following sections outline the output driver features and their effects.

Output driver power down ($\overline{PDO}$ = low), Pulling $\overline{PDO}$ low will place all the output drivers, except CTL1 and SCDT, into a high-impedance state. The SCDT output which indicates link-disabled or link-inactive can be tied directly to the $\overline{PDO}$ input to disable the output drivers when the link is inactive or when the cable is disconnected. An internal pullup on the $\overline{PDO}$ pin will default the TFP403 to the normal nonpower down output drive mode if left unconnected.

Drive Strength (ST = high for high drive strength, ST=low for low drive strength.) The TFP403 allows for selectable output drive strength on the data, control and ODCK outputs. See the dc specifications table for the values of I_{OH} and I_{OL} current drives for a given ST state. The high output strength offers approximately two times the drive as the low output drive strength.

Time Staggered Pixel Output. This option works only in conjunction with the 2-pixel/clock mode (PIXS = high). Setting $\overline{STAG}$ = low will time stagger the even and odd pixel output so as to reduce the amount of instantaneous current surge from the power supply. Depending on the PCB layout and design this can help reduce the amount of system ground bounce and power supply noise. The time stagger is such that in 2-pixel/clock mode the even pixel is delayed from the latching edge of ODCK by 0.25 Tcip. (Tcip is the period of ODCK. The ODCK period is 2Tpix when in 2-pixel/clock mode.)

Depending on system constraints of output load, pixel rate, panel input architecture and board cost the TFP403 drive strength and staggered pixel options allow flexibility to reduce system power-supply noise, ground bounce and EMI.

Power Management. The TFP403 offers several system power management features.

The output driver power down ($\overline{PDO}$ = low) is an intermediate mode which offers several uses. During this mode, all output drivers except SCDT and CTL1 are driven to a high impedance state while the rest of the device circuitry remains active

The TFP403 power down ($\overline{PD}$ = low) is a complete power down in that it powers down the digital core, the analog circuitry, and output drivers. All output drivers are placed into a Hi-Z state. All inputs are disabled except for the $\overline{PD}$ input. The TFP403 will not respond to any digital or analog inputs until $\overline{PD}$ is pulled high.

Both $\overline{PDO}$ and $\overline{PD}$ have internal pullup so if left unconnected they will default the TFP403 to normal operating modes.

Sync Detect. The TFP403 offers an output, SCDT to indicate link activity. The TFP403 monitors activity on DE to determine if the link is active. When 1 million (1e6) pixel clock periods pass without a transition on DE, the TFP403 considers the link inactive and SCDT is driven low. The SCDT goes high immediately after the first transition on DE. The SCDT again becomes low when no more transitions are seen after 2^{18} ocillator clocks.

SCDT can be used to signal a system power management circuit to initiate a system power down when the link is considered inactive. The SCDT can also be tied directly to the TFP403 $\overline{PDO}$ input to power down the output drivers when the link is inactive. It is not recommended to use the SCDT to drive the $\overline{PD}$ input since, once in complete power down, the analog inputs are ignored and the SCDT state does not change. An external system power management circuit to drive $\overline{PD}$ is preferred.

detailed description (continued)

PowerPAD 100-TQFP package

The TFP403 is packaged in TI's thermally enhanced PowerPAD 100TQFP packaging. The PowerPAD package is a 14 mm × 14 mm × 1 mm TQFP outline with 0.5 mm lead-pitch. The PowerPAD package has a specially designed die mount pad that offers improved thermal capability over typical TQFP packages of the same outline. The TI 100-TQFP PowerPAD package offers a back-side solder plane that connects directly to the die mount pad for enhanced thermal conduction. Soldering the back side of the TFP403 to the application board is not required thermally, as the device power dissipation is well within the package capability when not soldered.

Soldering the back side of the device to the PCB ground plane is recommended for electrical considerations. Since the die pad is electrically connected to the chip substrate and hence chip ground, connection of the PowerPAD back side to a PCB ground plane will help to improve EMI, ground bounce, and power supply noise performance.

Table 1 outlines the thermal properties of the TI 100-TQFP PowerPAD package. The 100-TQFP non-PowerPAD package is included only for reference.

Table 1. TI 100-TQFP (14 × 14 × 1 mm)/0.5 mm Lead Pitch

PARAMETER	WITHOUT PowerPAD	PowerPAD NOT CONNECTED TO PCB THERMAL PLANE	PowerPAD CONNECTED TO PCB THERMAL PLANE†
Theta-JA†,‡	45°C/W	27.3°C/W	17.3°C/W
Theta-JC†,‡	3.11°C/W	0.12°C/W	0.12°C/W
Maximum power dissipation†,‡,§	1.6 W	2.7 W	4.3 W

† Specified with 2 oz. Cu PCB plating.
‡ Airflow is at 0 LFM (no airflow)
§ Measured at ambient temperature, T_A = 70°C.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TFP403PZP	ACTIVE	HTQFP	PZP	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	TFP403PZP	Samples
TFP403PZPG4	ACTIVE	HTQFP	PZP	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	TFP403PZP	Samples

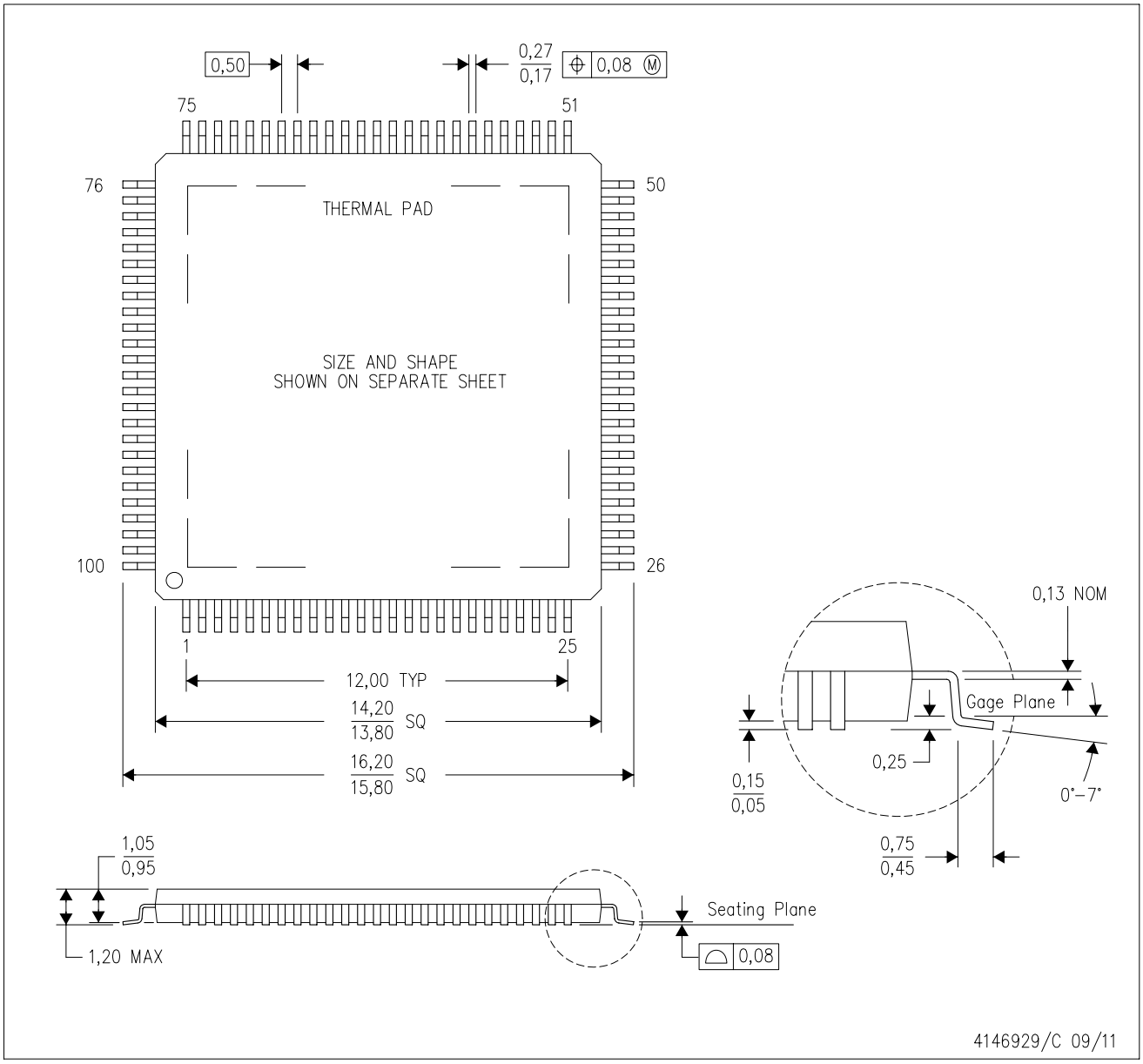
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

PZP (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

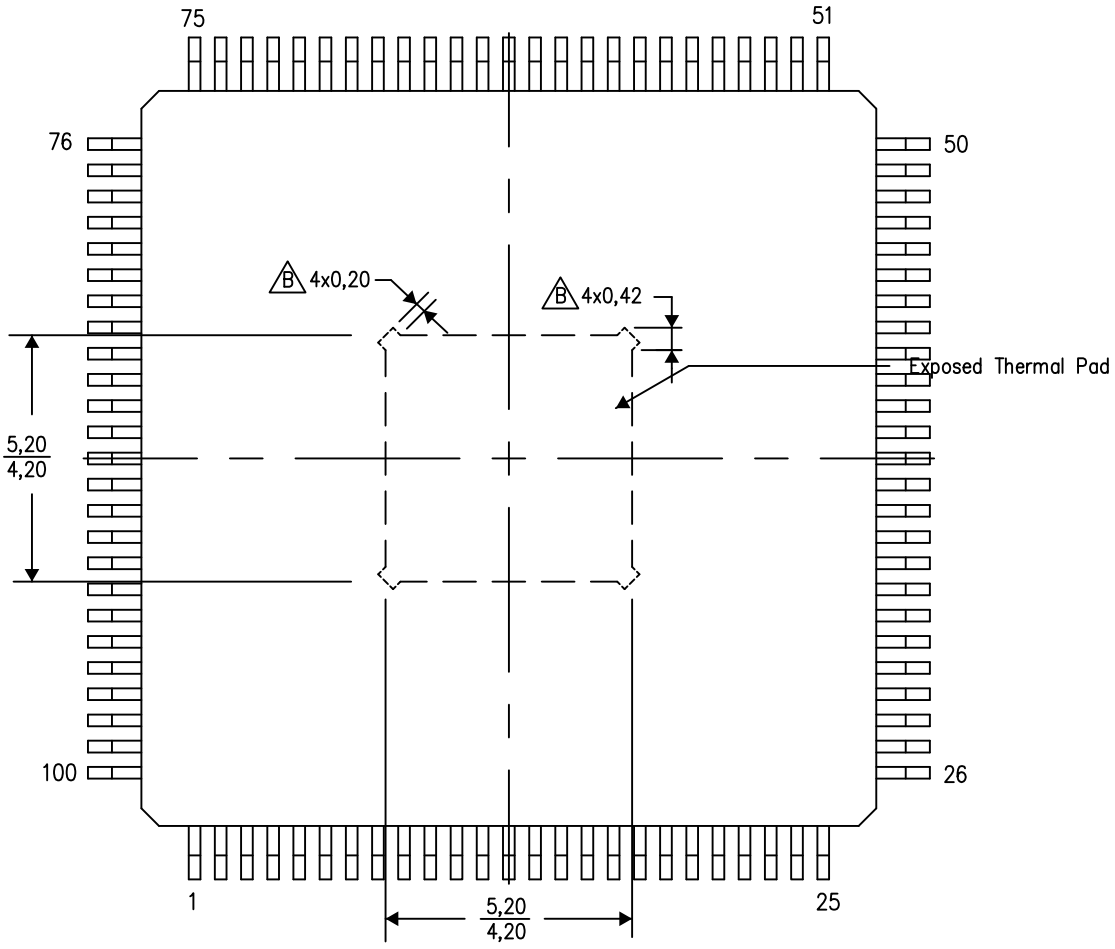
PZP (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

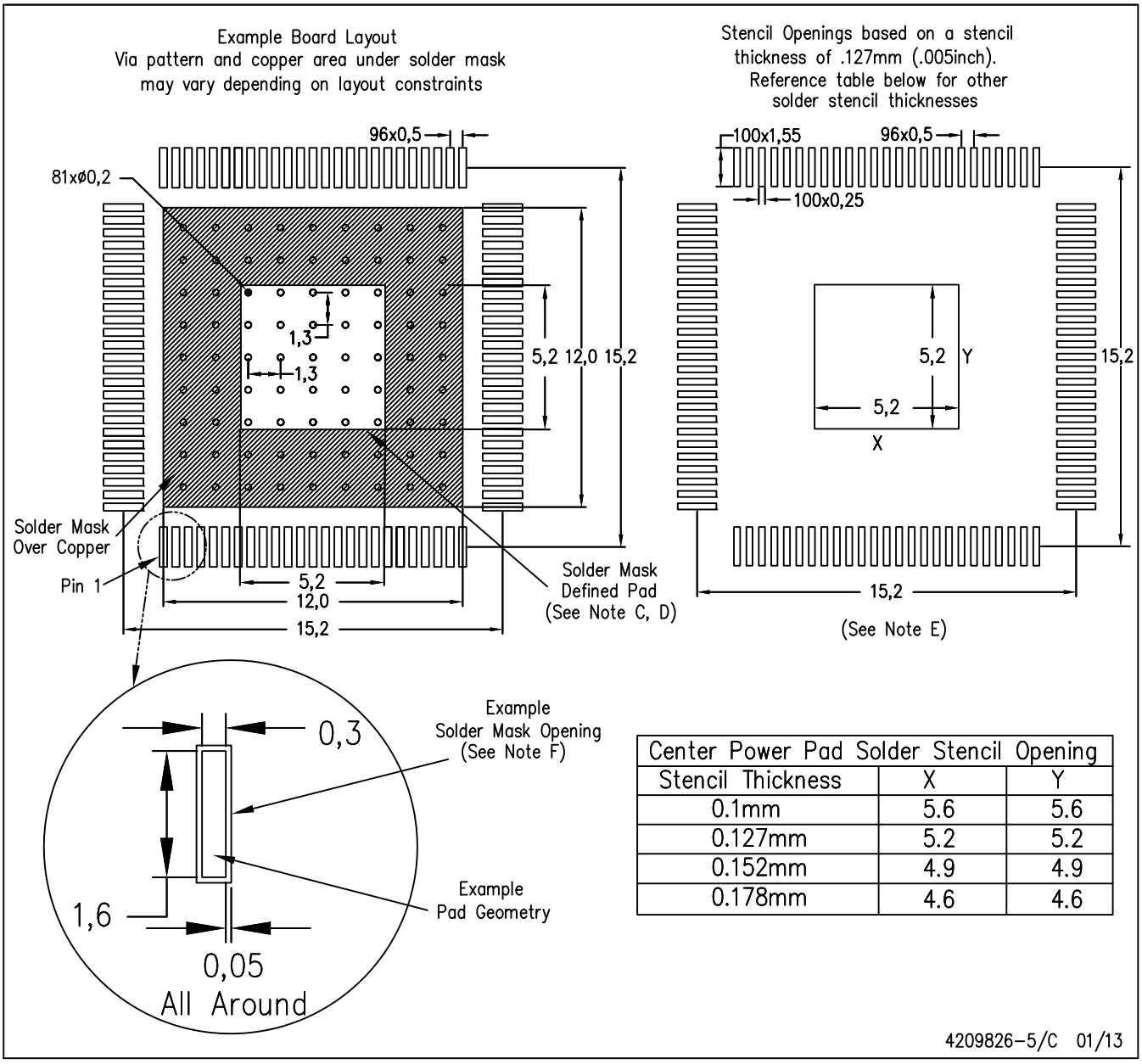
Exposed Thermal Pad Dimensions

4206333–2/I 12/12

NOTE: A. All linear dimensions are in millimeters

B Tie strap features may not be present.

PZP (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.6	5.6
0.127mm	5.2	5.2
0.152mm	4.9	4.9
0.178mm	4.6	4.6

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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