

TIBPAL16L8-25C, TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C TIBPAL16L8-30M, TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M LOW-POWER HIGH-PERFORMANCE **IMPACT™** PAL® CIRCUITS

SRPS059A – FEBRUARY 1984 – REVISED DECEMBER 2010

- **High-Performance Operation:**
Propagation Delay
C Suffix . . . 25 ns Max
M Suffix . . . 30 ns Max
- **Functionally Equivalent, but Faster Than**
PAL16L8A, PAL16R4A, PAL16R6A, and
PAL16R8A
- **Power-Up Clear on Registered Devices (All**
Register Outputs Are Set High, but Voltage
Levels at the Output Pins Go Low)
- **Package Options Include Both Plastic and**
Ceramic Chip Carriers in Addition to Plastic
and Ceramic DIPs
- **Dependable Texas Instruments Quality and**
Reliability

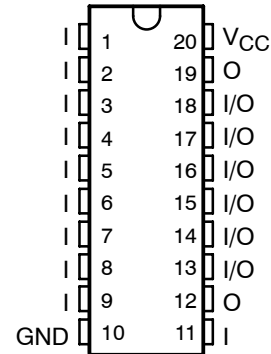
DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state buffers)	4
PAL16R6	8	0	6 (3-state buffers)	2
PAL16R8	8	0	8 (3-state buffers)	0

description

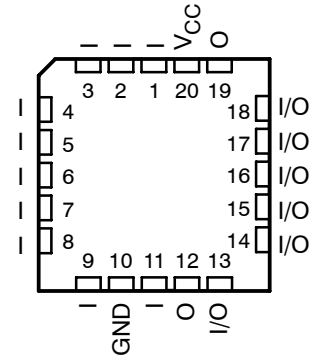
These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These **IMPACT™** circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

The TIBPAL16' C series is characterized from 0°C to 75°C. The TIBPAL16' M series is characterized for operation over the full military temperature range of –55°C to 125°C.

TIBPAL16L8'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J OR W PACKAGE
(TOP VIEW)



TIBPAL16L8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

IMPACT is a trademark of Texas Instruments.
PAL is a registered trademark of Advanced Micro Devices Inc.

PRODUCTION DATA information is current as of publication date.
Products conform to specifications per the terms of Texas Instruments
standard warranty. Production processing does not necessarily include
testing of all parameters.



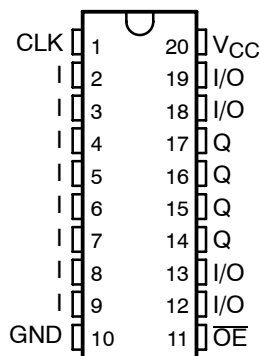
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2010, Texas Instruments Incorporated

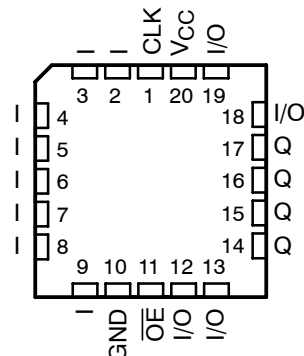
TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ PAL® CIRCUITS

SRPS059A FEBRUARY 1984 – REVISED DECEMBER 2010

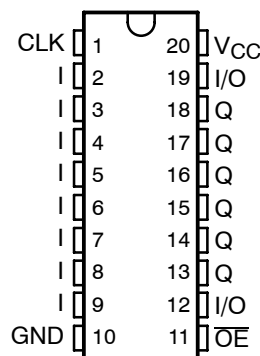
TIBPAL16R4'
C SUFFIX ... J OR N PACKAGE
M SUFFIX ... J OR W PACKAGE
(TOP VIEW)



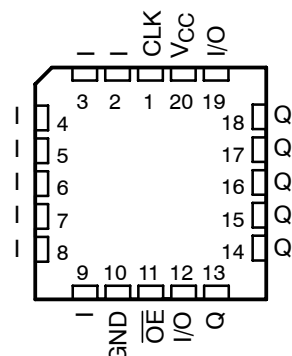
TIBPAL16R4'
C SUFFIX ... FN PACKAGE
M SUFFIX ... FK PACKAGE
(TOP VIEW)



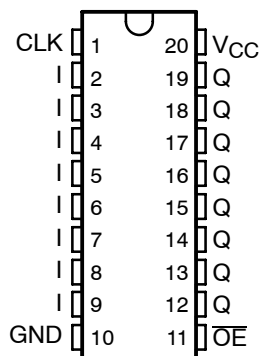
TIBPAL16R6'
C SUFFIX ... J OR N PACKAGE
M SUFFIX ... J OR W PACKAGE
(TOP VIEW)



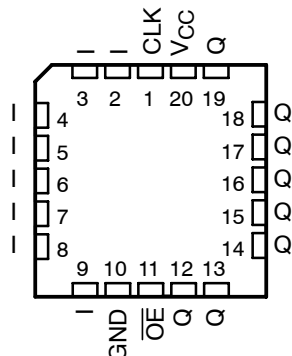
TIBPAL16R6'
C SUFFIX ... FN PACKAGE
M SUFFIX ... FK PACKAGE
(TOP VIEW)



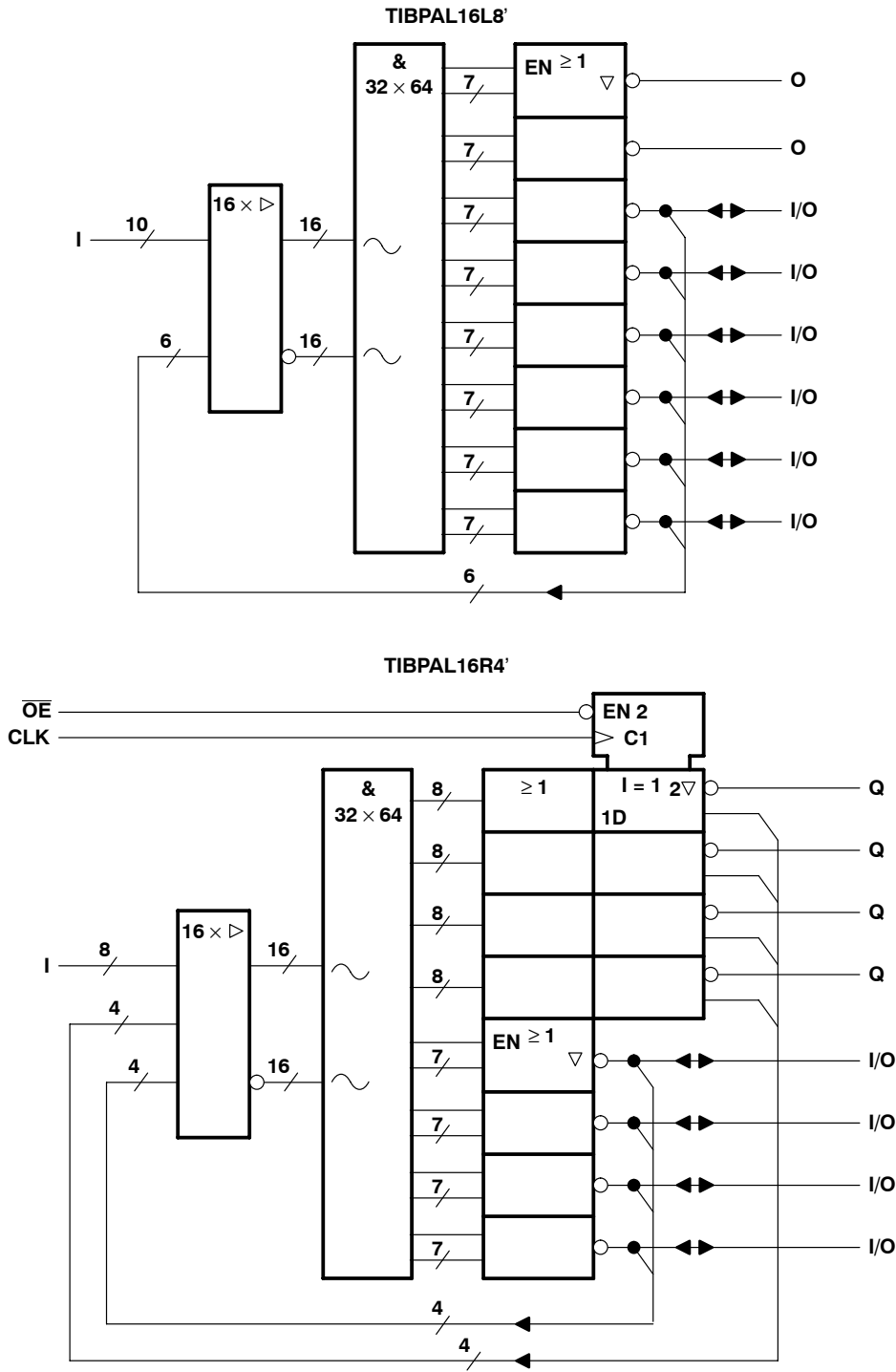
TIBPAL16R8'
C SUFFIX ... J OR N PACKAGE
M SUFFIX ... J OR W PACKAGE
(TOP VIEW)



TIBPAL16R8'
C SUFFIX ... FN PACKAGE
M SUFFIX ... FK PACKAGE
(TOP VIEW)



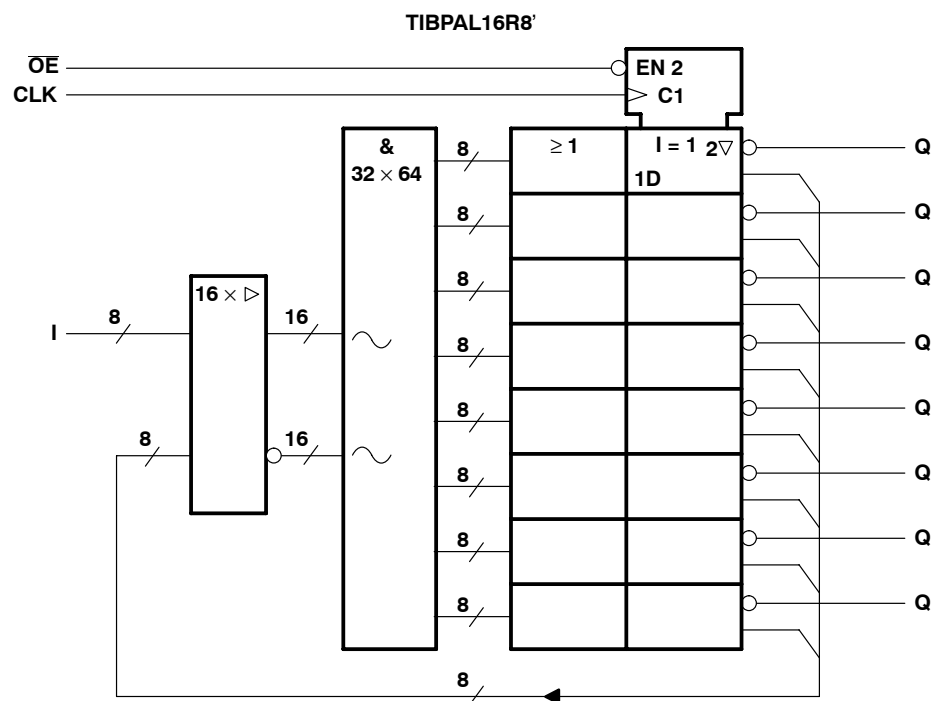
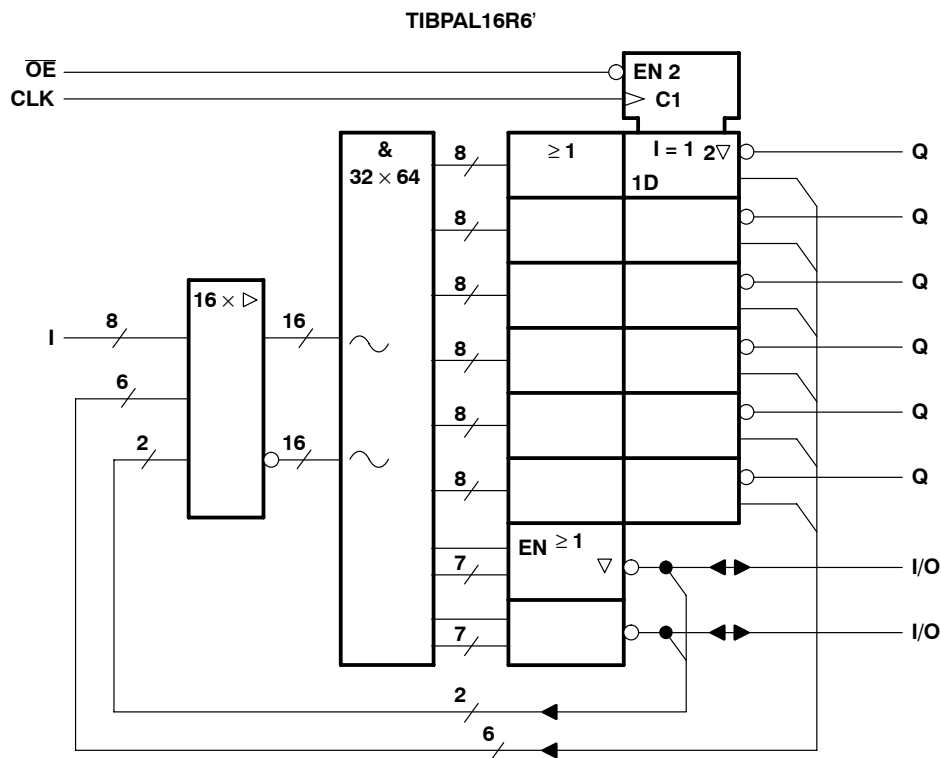
functional block diagrams (positive logic)



TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ PAL® CIRCUITS

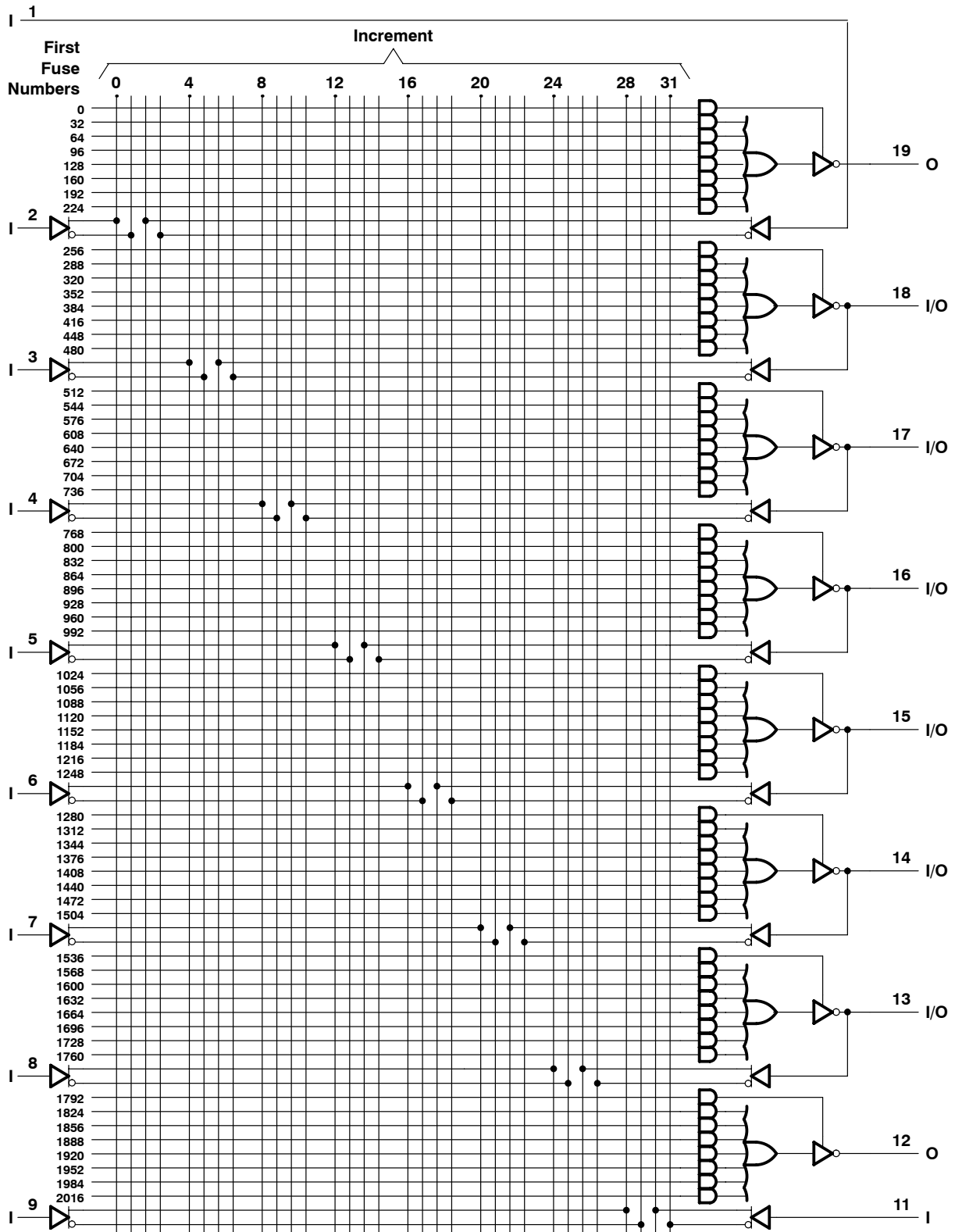
SRPS059A FEBRUARY 1984 – REVISED DECEMBER 2010

functional block diagrams (positive logic)



⋯ denotes fused inputs

logic diagram (positive logic)

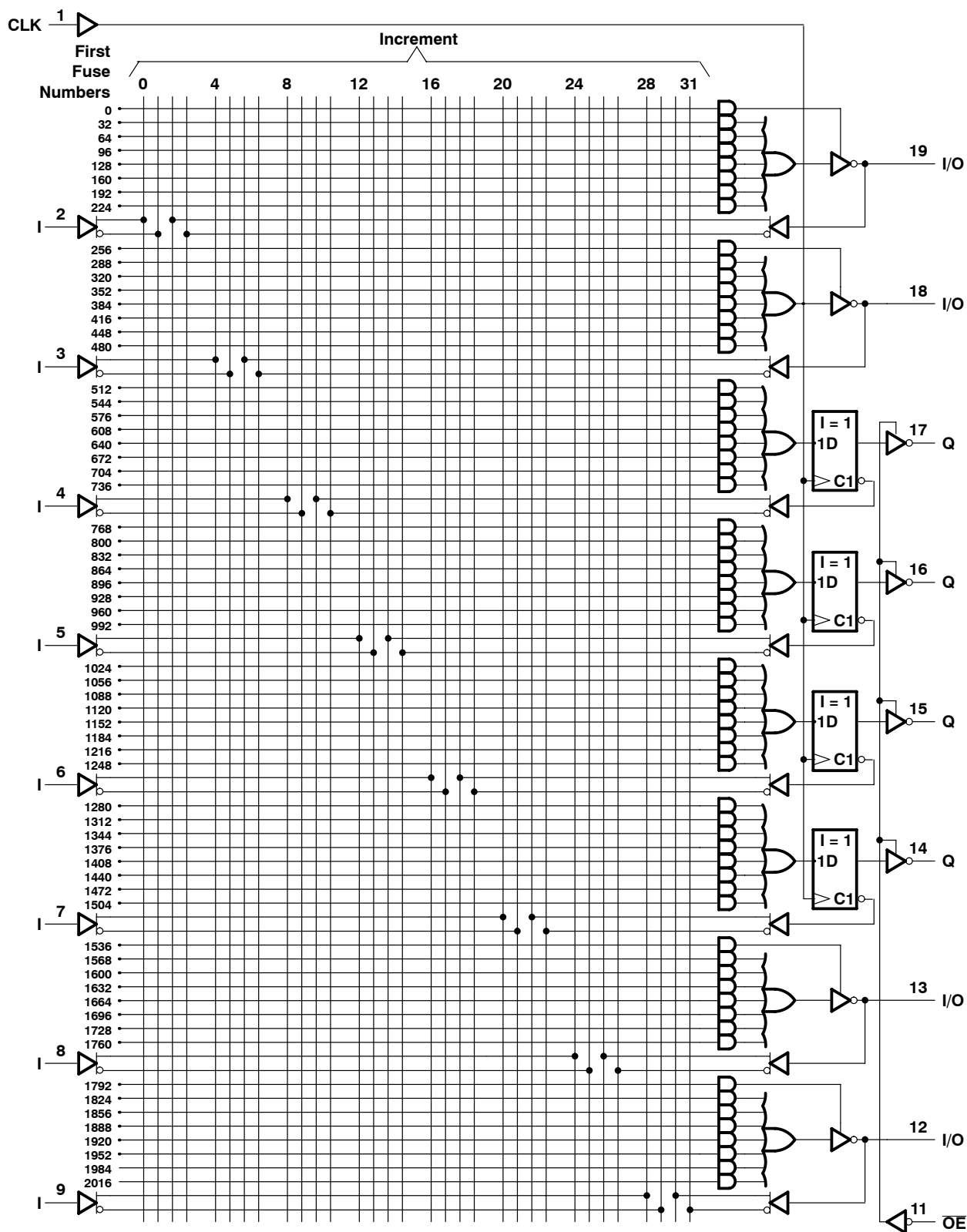


Fuse number = First fuse number + Increment

TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ PAL® CIRCUITS

SRPS059A FEBRUARY 1984 – REVISED DECEMBER 2010

logic diagram (positive logic)

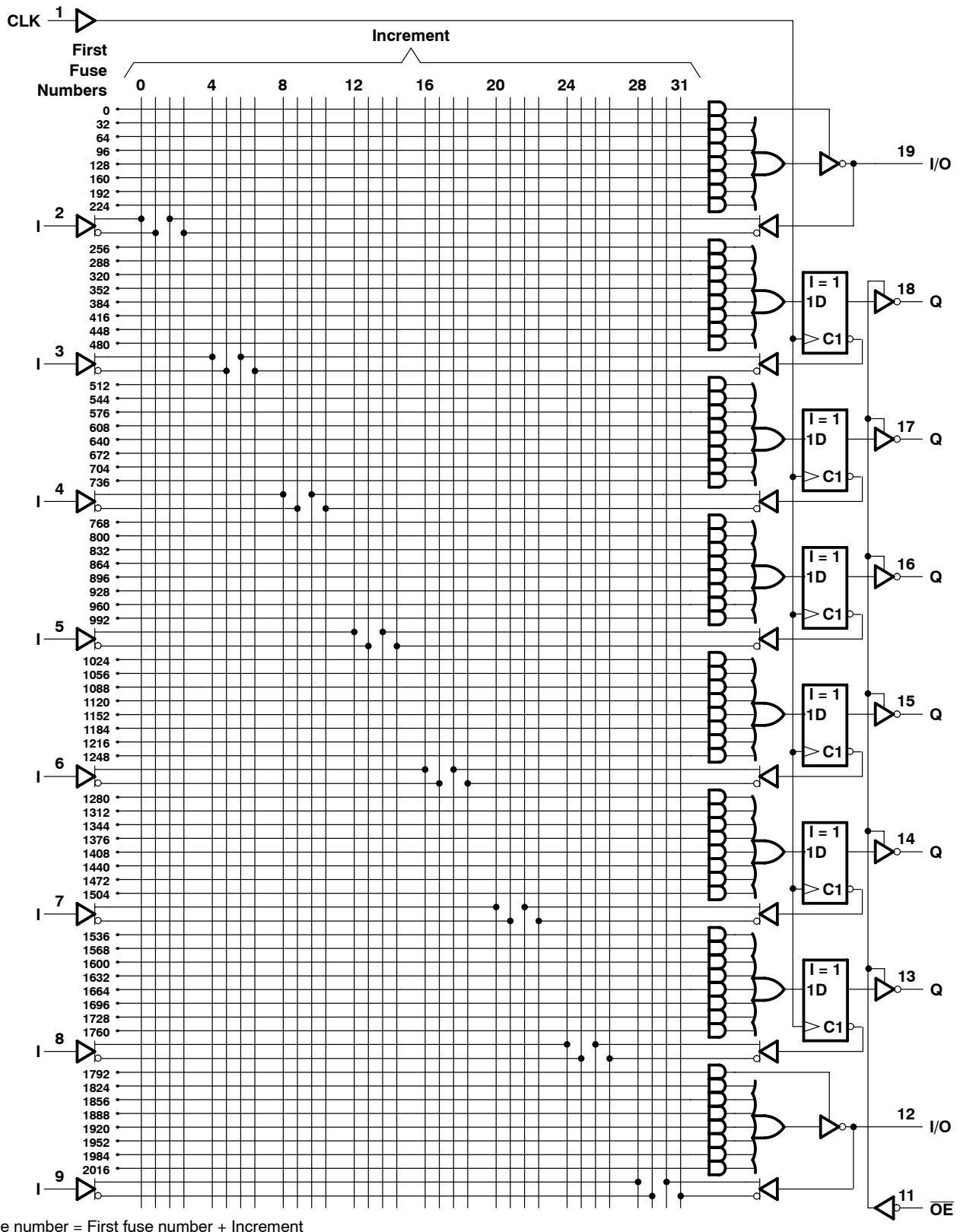


Fuse number = First fuse number + Increment



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

logic diagram (positive logic)

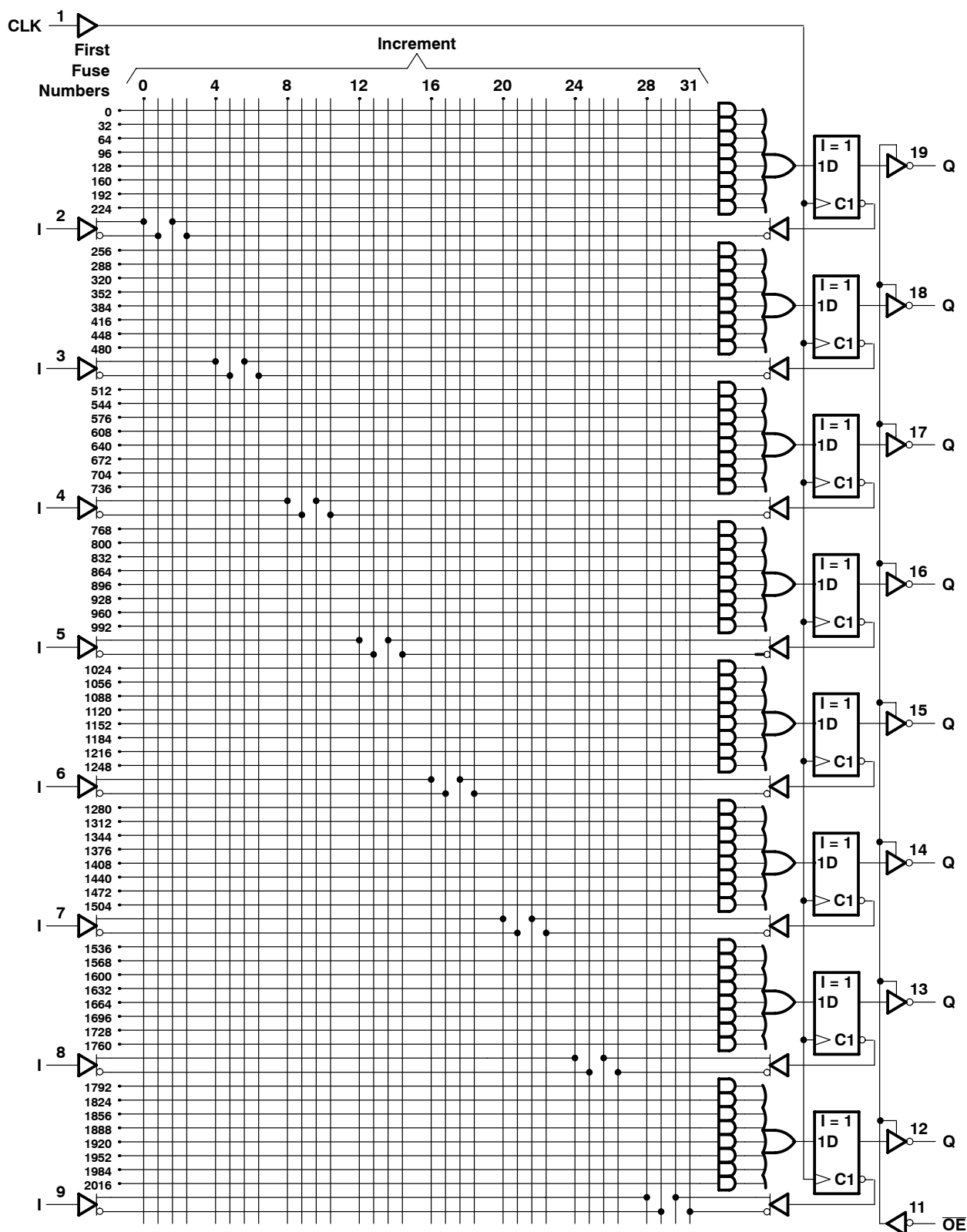


Fuse number = First fuse number + Increment

TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ PAL® CIRCUITS

SRPS059A FEBRUARY 1984 – REVISED DECEMBER 2010

logic diagram (positive logic)



Fuse number = First fuse number + Increment



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS
SRPS059A FEBRUARY 1984 – REVISED DECEMBER 2010

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range, T_{stg}	–65°C to 150°C

NOTE 1: These ratings apply, except for programming pins, during a programming cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–3.2	mA
I_{OL}	Low-level output current			24	mA
f_{clock}	Clock frequency	0		30	MHz
t_w	Pulse duration, clock (see Note 2)	High	10		ns
		Low	15		
t_{su}	Setup time, input or feedback before clock↑	20			ns
t_h	Hold time, input or feedback after clock↑	0			ns
T_A	Operating free-air temperature	0	25	75	°C

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock} . The minimum pulse durations specified are for clock high or low only, but not for both simultaneously.



TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

SRPS059A FEBRUARY 1984 – REVISED DECEMBER 2010

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.75\text{ V}$,	$I_I = -18\text{ mA}$			-1.5	V
V_{OH}		$V_{CC} = 4.75\text{ V}$,	$I_{OH} = -3.2\text{ mA}$	2.4	3.3		V
V_{OL}		$V_{CC} = 4.75\text{ V}$,	$I_{OL} = 24\text{ mA}$		0.35	0.5	V
I_{OZH}	Outputs	$V_{CC} = 5.25\text{ V}$,	$V_O = 2.7\text{ V}$			20	μA
	I/O ports					100	
I_{OZL}	Outputs	$V_{CC} = 5.25\text{ V}$,	$V_O = 0.4\text{ V}$			-20	μA
	I/O ports					-250	
I_I		$V_{CC} = 5.25\text{ V}$,	$V_I = 5.5\text{ V}$			0.1	mA
I_{IH}		$V_{CC} = 5.25\text{ V}$,	$V_I = 2.7\text{ V}$			20	μA
I_{IL}		$V_{CC} = 5.25\text{ V}$,	$V_I = 0.4\text{ V}$			-0.25	mA
$I_O^\ddagger$		$V_{CC} = 5.25\text{ V}$,	$V_O = 2.25\text{ V}$	-30		-125	mA
I_{CC}		$V_{CC} = 5.25\text{ V}$,	$V_I = 0$, Outputs open		75	100	mA

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one-half of the short-circuit output current, I_{OS} .

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$f_{\max}$			R1 = 500 Ω , R2 = 500 Ω , See Figure 3	30			MHz
t_{pd}	I, I/O	O, I/O			15	25	ns
t_{pd}	CLK↑	Q			10	15	ns
t_{en}	OE↓	Q			15	20	ns
t_{dis}	OE↑	Q			10	20	ns
t_{en}	I, I/O	O, I/O			14	25	ns
t_{dis}	I, I/O	O, I/O			13	25	ns

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS
SRPS059A FEBRUARY 1984 – REVISED DECEMBER 2010

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	–55°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C

NOTE 1: These ratings apply, except for programming pins, during a programming cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–2	mA
I_{OL}	Low-level output current			12	mA
f_{clock}	Clock frequency	0		25	MHz
t_w	Pulse duration, clock (see Note 2)	High	15		ns
		Low	20		
t_{su}	Setup time, input or feedback before clock↑	25			ns
t_h	Hold time, input or feedback after clock↑	0			ns
T_A	Operating free-air temperature	–55	25	125	°C

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock} . The minimum pulse durations specified are for clock high or low only, but not for both simultaneously.



TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

SRPS059A FEBRUARY 1984 – REVISED DECEMBER 2010

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.5	V
V_{OH}		$V_{CC} = 4.5\text{ V}$,	$I_{OH} = -2\text{ mA}$	2.4	3.2		V
V_{OL}		$V_{CC} = 4.5\text{ V}$,	$I_{OL} = 12\text{ mA}$		0.25	0.4	V
I_{OZH}	Outputs	$V_{CC} = 5.5\text{ V}$	$V_O = 2.7\text{ V}$			20	μA
	I/O ports					100	
I_{OZL}	Outputs	$V_{CC} = 5.5\text{ V}$,	$V_O = 0.4\text{ V}$			-20	μA
	I/O ports					-250	
I_I	Pin 1, 11	$V_{CC} = 5.5\text{ V}$,	$V_I = 5.5\text{ V}$			0.2	mA
	All others					0.1	
I_{IH}	Pin 1, 11	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$			50	μA
	I/O ports					100	
	All others					20	
I_{IL}	I/O ports	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.4\text{ V}$			-0.25	mA
	All others					-0.2	
$I_{OS}^\ddagger$		$V_{CC} = 5.5\text{ V}$,	$V_O = 0.5\text{ V}$	-30		-250	mA
I_{CC}		$V_{CC} = 5.5\text{ V}$,	$V_I = 0$, Outputs open		75	105	mA

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test-equipment degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$f_{\max}$			R1 = 390 Ω , R2 = 750 Ω , See Figure 4	25			MHz
t_{pd}	I, I/O	O, I/O			15	30	ns
t_{pd}	CLK↑	Q			10	20	ns
t_{en}	OE↓	Q			15	25	ns
t_{dis}	OE↑	Q			10	25	ns
t_{en}	I, I/O	O, I/O			14	30	ns
t_{dis}	I, I/O	O, I/O			13	30	ns

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.



programming information

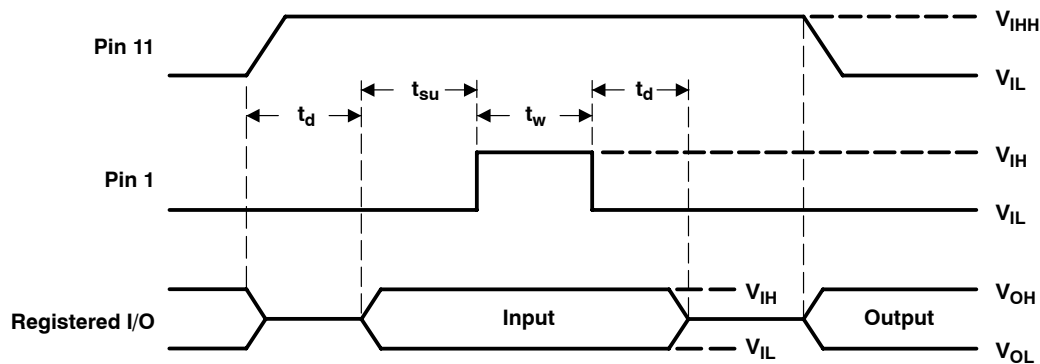
Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic also is available, upon request, from the nearest TI field sales office or local authorized TI distributor, by calling Texas Instruments at +1 (972) 644-5580, or by visiting the TI Semiconductor Home Page at www.ti.com/sc.

preload procedure for registered outputs (see Figure 1 and Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

- Step 1. With V_{CC} at 5 V and Pin 1 at V_{IL} , raise Pin 11 to V_{IHH} .
- Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
- Step 3. Pulse Pin 1, clocking in preload data.
- Step 4. Remove output voltage, then lower Pin 11 to V_{IL} . Preload can be verified by observing the voltage level at the output pin.



NOTE 3: $t_d = t_{su} = t_h = 100 \text{ ns to } 1000 \text{ ns}$ $V_{IHH} = 10.25 \text{ V to } 10.75 \text{ V}$

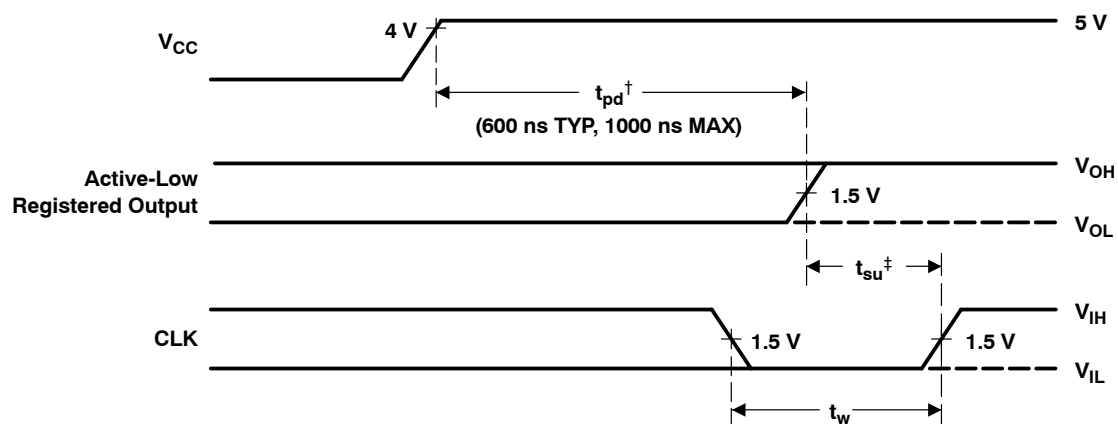
Figure 1. Preload Waveforms

TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ PAL® CIRCUITS

SRPS059A FEBRUARY 1984 – REVISED DECEMBER 2010

power-up reset (see Figure 2)

Following power up, all registers are set high. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.

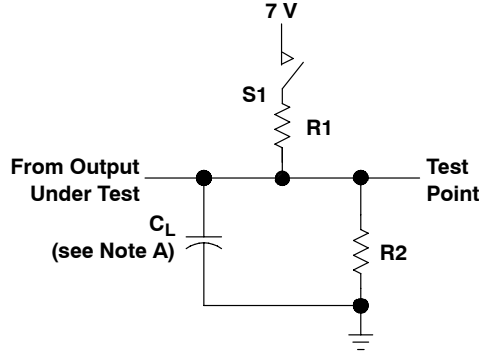


[†] This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.

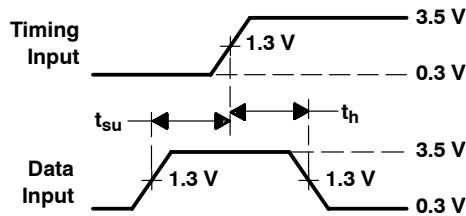
[‡] This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms

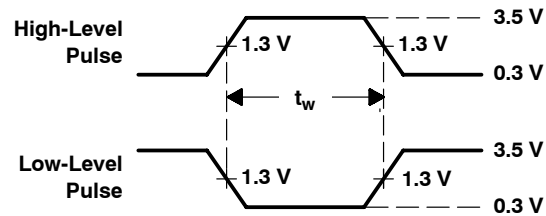
PARAMETER MEASUREMENT INFORMATION



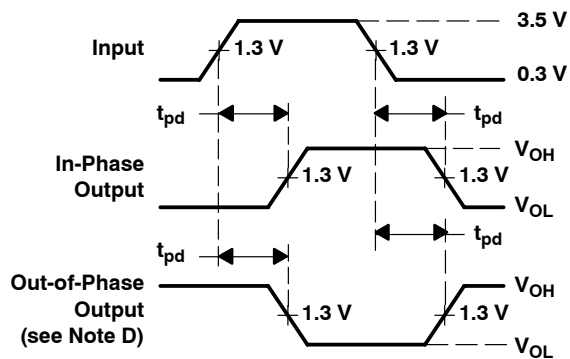
LOAD CIRCUIT FOR 3-STATE OUTPUTS



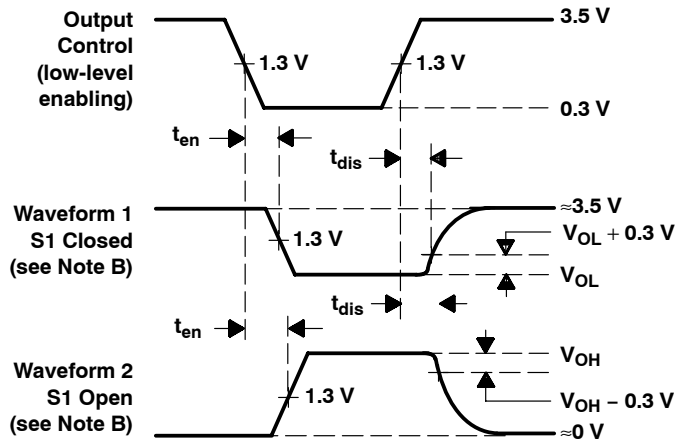
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATIONS**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

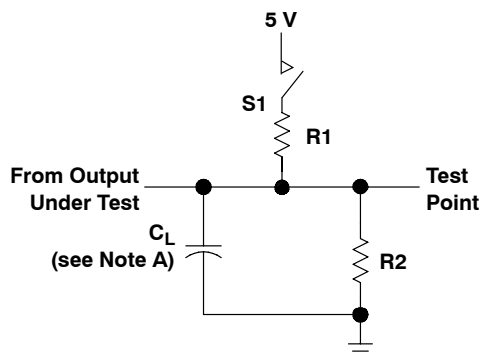


**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

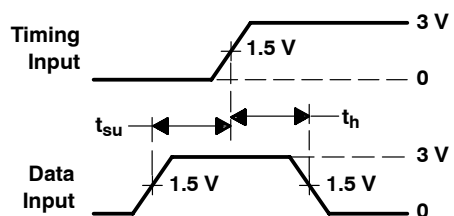
- NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en} , 5 pF for t_{dis} .
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%.
- D. When measuring propagation delay times of 3-state outputs from low to high, switch S1 is closed. When measuring propagation delay times of 3-state outputs from high to low, switch S1 is open.
- E. Equivalent loads may be used for testing.

Figure 3. Load Circuit and Voltage Waveforms

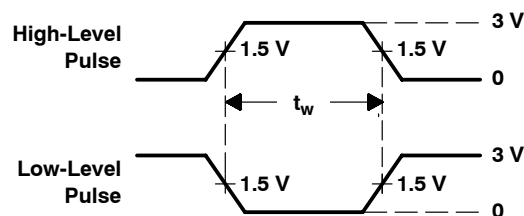
PARAMETER MEASUREMENT INFORMATION



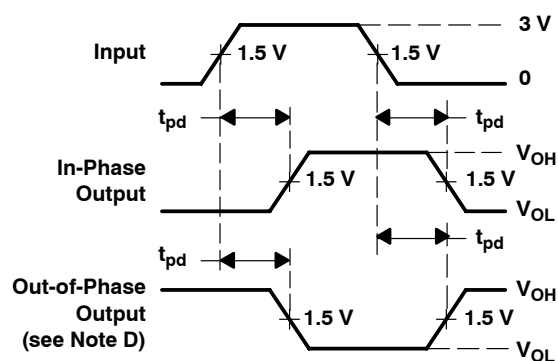
LOAD CIRCUIT FOR 3-STATE OUTPUTS



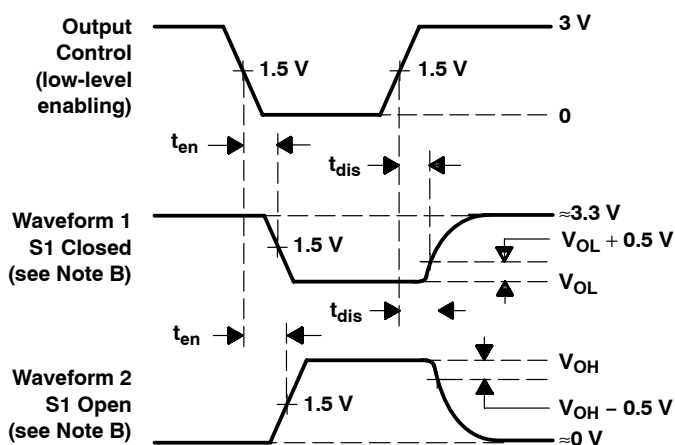
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en} , 5 pF for t_{dis} .
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses have the following characteristics: $PRR \leq 10$ MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%
 D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
 E. Equivalent loads may be used for testing.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-85155052A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 85155052A TIBPAL16 L8-30MFKB	Samples
5962-8515505RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515505RA TIBPAL16L8-30M JB	Samples
5962-8515505SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8515505SA TIBPAL16L8-30M WB	Samples
5962-85155062A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 85155062A TIBPAL16 R8-30MFKB	Samples
5962-8515506RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515506RA TIBPAL16R8-30M JB	Samples
5962-8515506SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8515506SA TIBPAL16R8-30M WB	Samples
5962-85155072A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 85155072A TIBPAL16 R6-30MFKB	Samples
5962-8515507RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515507RA TIBPAL16R6-30M JB	Samples
5962-8515507SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8515507SA TIBPAL16R6-30M WB	Samples
5962-85155082A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 85155082A TIBPAL16 R4-30MFKB	Samples
5962-8515508RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515508RA TIBPAL16R4-30M JB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8515508SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8515508SA TIBPAL16R4-30M WB	Samples
JM38510/50605BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 50605BRA	Samples
JM38510/50606BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 50606BRA	Samples
JM38510/50607BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 50607BRA	Samples
JM38510/50608BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 50608BRA	Samples
M38510/50605BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 50605BRA	Samples
M38510/50606BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 50606BRA	Samples
M38510/50607BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 50607BRA	Samples
M38510/50608BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 50608BRA	Samples
TIBPAL16L8-25CFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	0 to 75	16L8-25	Samples
TIBPAL16L8-25CJ	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI			
TIBPAL16L8-25CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 75	TIBPAL16L8-25C N	Samples
TIBPAL16L8-30MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 85155052A TIBPAL16 L8-30MFKB	Samples
TIBPAL16L8-30MJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	TIBPAL16L8-30M J	Samples
TIBPAL16L8-30MJB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515505RA TIBPAL16L8-30M JB	Samples
TIBPAL16L8-30MWB	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8515505SA TIBPAL16L8-30M WB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TIBPAL16R4-25CFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	0 to 75	16R4-25	Samples
TIBPAL16R4-25CJ	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI			
TIBPAL16R4-25CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 75	TIBPAL16R4-25C N	Samples
TIBPAL16R4-30MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 85155082A TIBPAL16 R4-30MFKB	Samples
TIBPAL16R4-30MJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	TIBPAL16R4-30M J	Samples
TIBPAL16R4-30MJB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515508RA TIBPAL16R4-30M JB	Samples
TIBPAL16R4-30MWB	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8515508SA TIBPAL16R4-30M WB	Samples
TIBPAL16R6-25CFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	0 to 75	16R6-25	Samples
TIBPAL16R6-25CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 75	TIBPAL16R6-25C N	Samples
TIBPAL16R6-30MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 85155072A TIBPAL16 R6-30MFKB	Samples
TIBPAL16R6-30MJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	TIBPAL16R6-30M J	Samples
TIBPAL16R6-30MJB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515507RA TIBPAL16R6-30M JB	Samples
TIBPAL16R6-30MWB	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8515507SA TIBPAL16R6-30M WB	Samples
TIBPAL16R8-25CFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	0 to 75	16R8-25	Samples
TIBPAL16R8-25CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 75	TIBPAL16R8-25C N	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TIBPAL16R8-30MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-85155062A TIBPAL16 R8-30MFKB	Samples
TIBPAL16R8-30MJB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515506RA TIBPAL16R8-30M JB	Samples
TIBPAL16R8-30MWB	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8515506SA TIBPAL16R8-30M WB	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

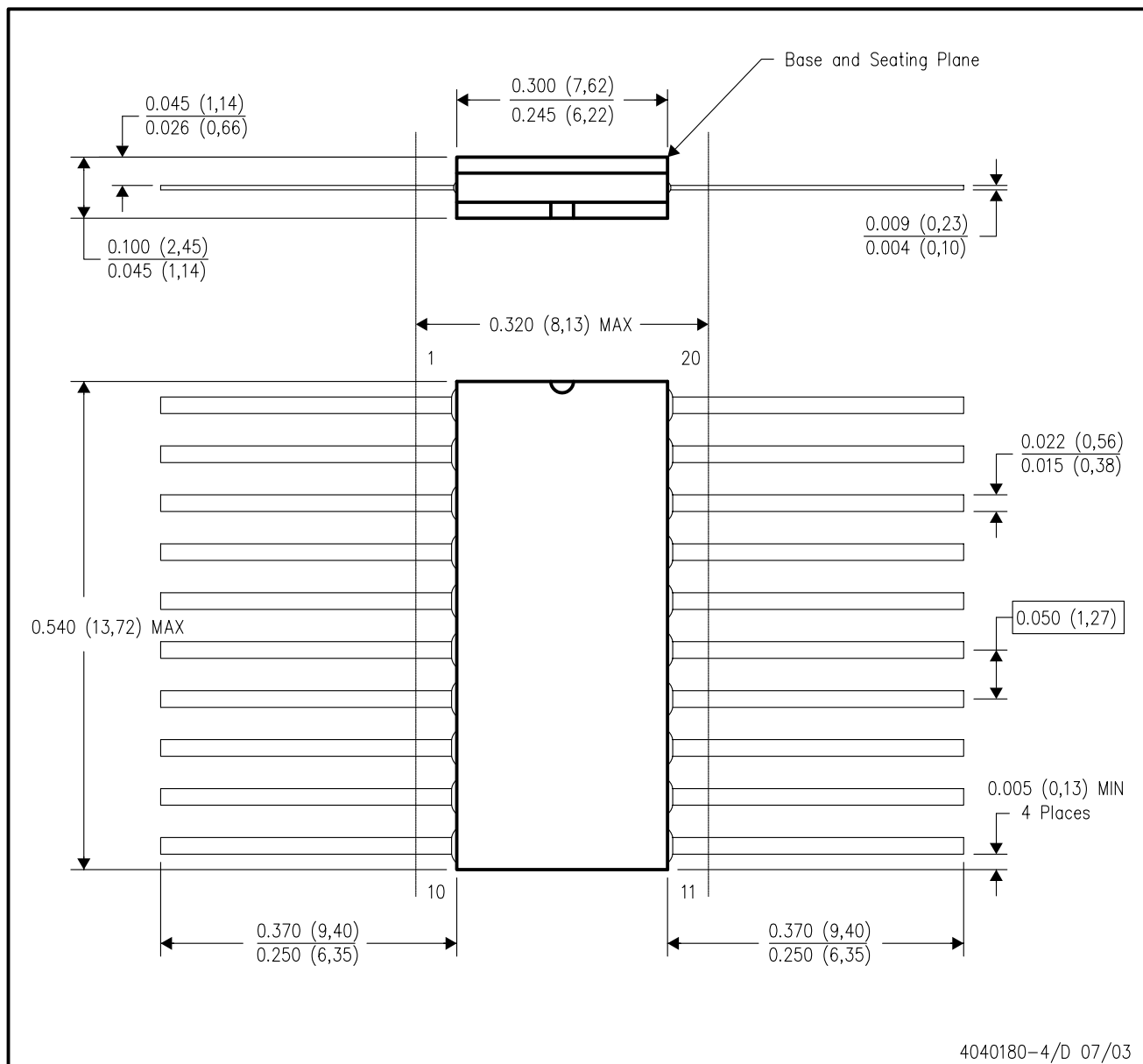


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



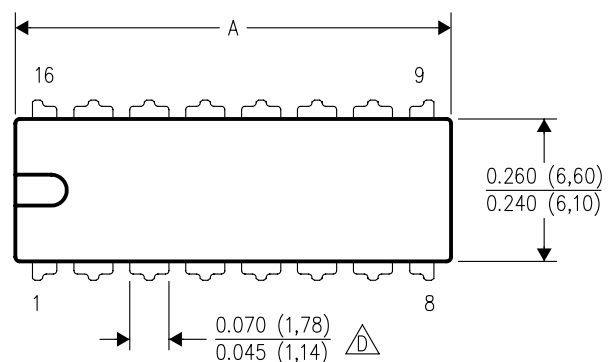
4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

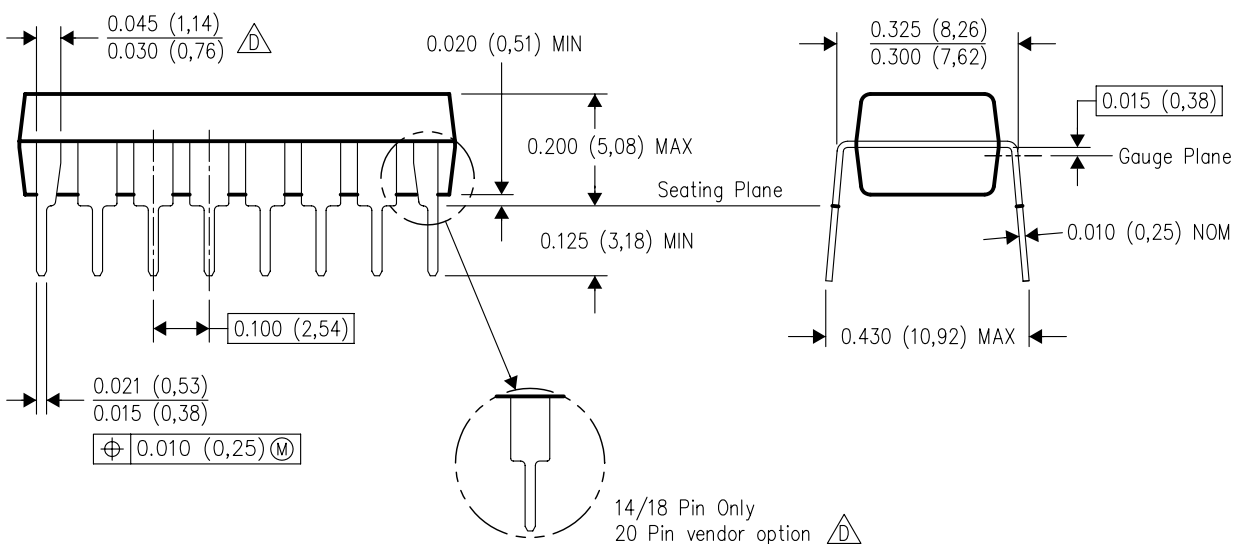
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



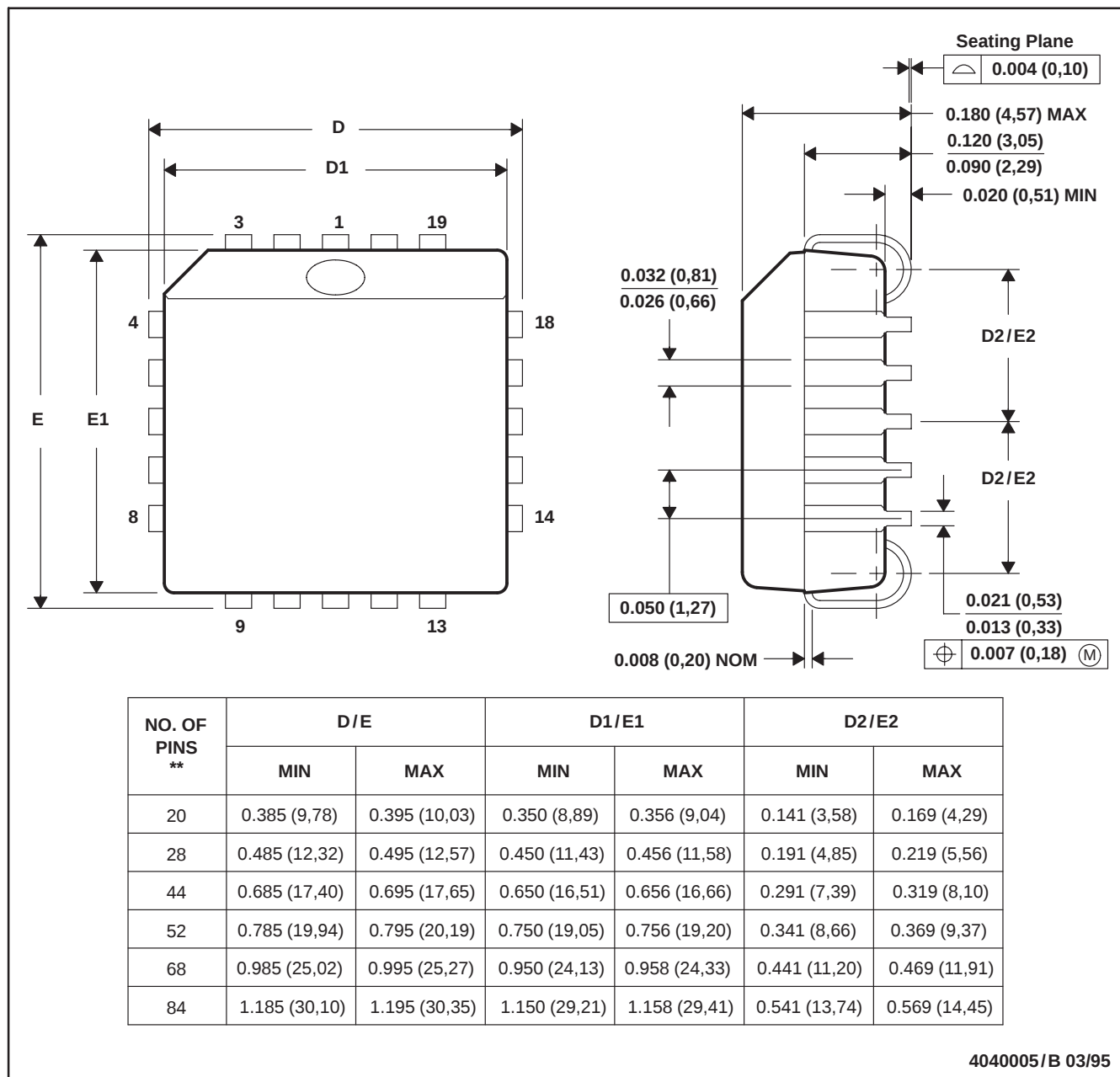
4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-018

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com