- **Qualified for Automotive Applications**
- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Precision Voltage Sensor**
- **Temperature-Compensated Voltage Reference**
- **Programmable Delay Time by External Capacitor**
- **Supply Voltage Range . . . 2 V to 6 V**
- **Defined $\overline{\text{RESET}}$ Output from $V_{DD} \geq 1$ V**
- **Power-Down Control Support for Static RAM With Battery Backup**
- **Maximum Supply Current of 16 μA**
- **Power Saving Totem-Pole Outputs**

PW PACKAGE
(TOP VIEW)

CONTROL	1	8	V_{DD}
$\overline{\text{RESIN}}$	2	7	SENSE
CT	3	6	RESET
GND	4	5	$\overline{\text{RESET}}$
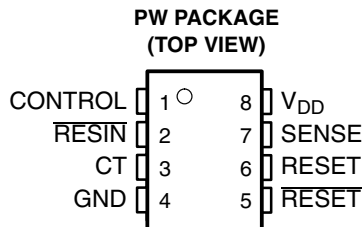
description

The TLC77xx family of micropower supply voltage supervisors provide reset control, primarily in microcomputer and microprocessor systems.

During power-on, $\overline{\text{RESET}}$ is asserted when V_{DD} reaches 1 V. After minimum V_{DD} ($\geq$ 2 V) is established, the circuit monitors SENSE voltage and keeps the reset outputs active as long as SENSE voltage ($V_{I(SENSE)}$) remains below the threshold voltage. An internal timer delays return of the output to the inactive state to ensure proper system reset. The delay time, t_d, is determined by an external capacitor:

$$t_d = 2.1 \times 10^4 \times C_T$$

Where

   C_T is in farads

   t_d is in seconds

Except for the TLC7701, which can be customized with two external resistors, each supervisor has a fixed SENSE threshold voltage set by an internal voltage divider. When SENSE voltage drops below the threshold voltage, the outputs become active and stay in that state until SENSE voltage returns above threshold voltage and the delay time, t_d, has expired.

In addition to the power-on-reset and undervoltage-supervisor function, the TLC77xx adds power-down control support for static RAM. When CONTROL is tied to GND, RESET will act as active high. The voltage monitor contains additional logic intended for control of static memories with battery backup during power failure. By driving the chip select ($\overline{\text{CS}}$) of the memory circuit with the RESET output of the TLC77xx and with the CONTROL driven by the memory bank select signal ($\overline{\text{CSH1}}$) of the microprocessor (see Figure 10), the memory circuit is automatically disabled during a power loss. (In this application the TLC77xx power has to be supplied by the battery.)

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ORDERING INFORMATION[†‡]

T$_A$	PACKAGE[§]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 125°C	TSSOP – PW	Tape and reel	TLC7701QPWRQ1	7701Q1
	TSSOP – PW	Tape and reel	TLC7705QPWRQ1	7705Q1
	TSSOP – PW	Tape and reel	TLC7733QPWRQ1	7733Q1

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

[‡] Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.
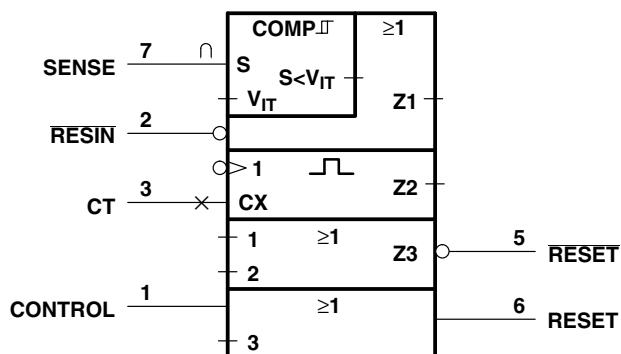
[§] The PW package is only available left-end taped and reeled (indicated by the R suffix on the device type; e.g., TLC7701QPWREP).

FUNCTION TABLE

CONTROL	$\overline{\text{RESIN}}$	V$_{I(SENSE)}$>V$_{IT+}$	RESET	$\overline{\text{RESET}}$
L	L	False	H	L
L	L	True	H	L
L	H	False	H	L
L	H	True	L[§]	H[§]
H	L	False	H	L
H	L	True	H	L
H	H	False	H	L
H	H	True	H	H[§]

[§] RESET and $\overline{\text{RESET}}$ states shown are valid for t > t$_d$.

logic symbol[¶]

[¶] This symbol is in accordance with ANSI/IEEE Std 91−1984 and IEC Publication 617-12.

functional block diagram
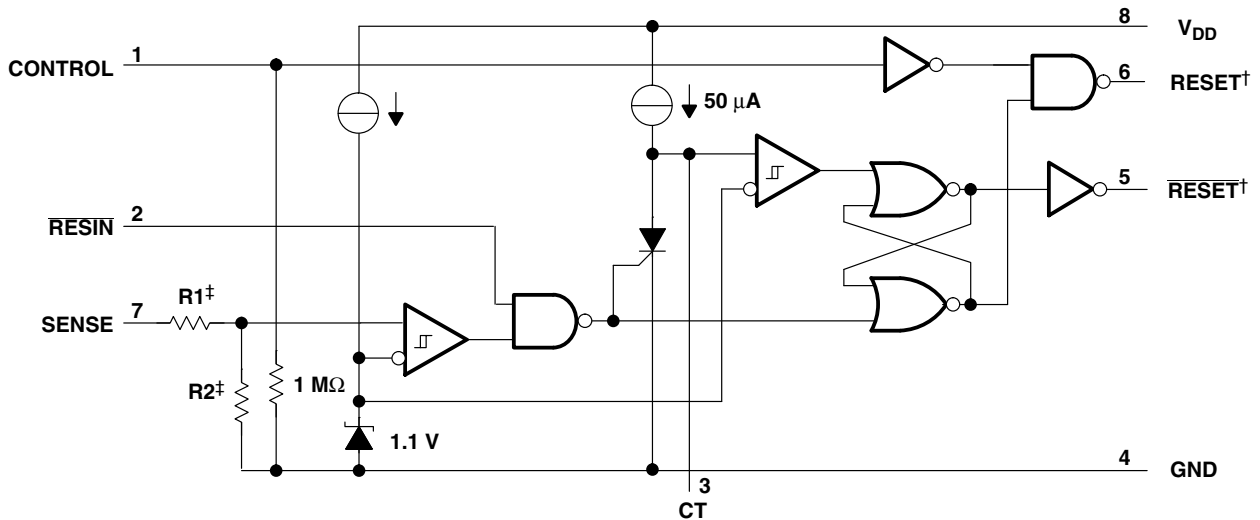
† Outputs are totem-pole configuration. External pullup or pulldown resistors are not required.
‡ Nominal values:

	R1 (Typ)	R2 (Typ)
TLC7701	0	∞
TLC7705	910 kΩ	290 kΩ
TLC7733	750 kΩ	450 kΩ

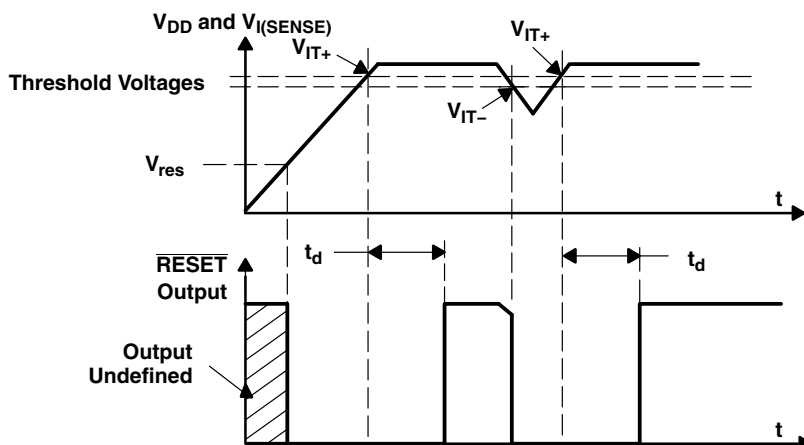## timing diagram

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage, V_{DD} (see Note 1)	7 V
Input voltage range, CONTROL, $\overline{RESIN}$, SENSE (see Note 1)	−0.3 V to 7 V
Maximum low output current, I_{OL}	10 mA
Maximum high output current, I_{OH}	−10 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	±10 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	±10 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: TL77xxQ	−40°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
PW	525 mW	4.2 mW/°C	273 mW	105 mW

recommended operating conditions at specified temperature range

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	6	V
Input voltage, V_I		0	V_{DD}	V
High-level input voltage at $\overline{RESIN}$ and CONTROL[‡], V_{IH}		$0.7 \times V_{DD}$		V
Low-level input voltage at $\overline{RESIN}$ and CONTROL[‡], V_{IL}			$0.2 \times V_{DD}$	V
High-level output current, I_{OH}	$V_{DD} \geq 2.7$ V		−2	mA
Low-level output current, I_{OL}			2	mA
Input transition rise and fall rate at $\overline{RESIN}$ and CONTROL, $\Delta t/\Delta V$			100	ns/V
Operating free-air temperature range, T_A		−40	125	°C

[‡] To ensure a low supply current, V_{IL} should be kept < 0.3 V and $V_{IH} > V_{DD} - 0.3$ V.

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electrical characteristics over recommended operating conditions (see Note 2) (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TLC77xx			UNIT
				MIN	TYP†	MAX	
V_{OH}	High-level output voltage	$I_{OH} = -20 \mu A$	$V_{DD} = 2 V$	1.8			V
			$V_{DD} = 2.7 V$	2.5			
			$V_{DD} = 4.5 V$	4.3			
		$I_{OH} = -2 mA$	$V_{DD} = 4.5 V$	3.7			
V_{OL}	Low-level output voltage	$I_{OL} = 20 \mu A$	$V_{DD} = 2 V$			0.2	V
			$V_{DD} = 2.7 V$			0.2	
			$V_{DD} = 4.5 V$			0.2	
		$I_{OL} = 2 mA$	$V_{DD} = 4.5 V$			0.5	
V_{IT-}	Negative-going input threshold voltage, SENSE (see Note 3)	TLC7701	$V_{DD} = 2 V$ to $6 V$	1.04	1.1	1.16	V
		TLC7705		4.43	4.5	4.63	
		TLC7733		2.855	2.93	3.03	
V_{hys}	Hysteresis voltage, SENSE	TLC7701	$V_{DD} = 2 V$ to $6 V$		30		mV
		TLC7705			70		
		TLC7733					
V_{res}	Power-up reset voltage‡		$I_{OL} = 20 \mu A$			1	V
I_I	Input current	$\overline{RESIN}$	$V_I = 0 V$ to V_{DD}			2	μA
		CONTROL	$V_I = V_{DD}$		7	15	
		SENSE	$V_I = 5 V$		5	10	
		SENSE, TLC7701 only	$V_I = 5 V$			2	
I_{DD}	Supply current		$\overline{RESIN} = V_{DD}$, SENSE = $V_{DD} \geq V_{IT}$max + 0.2 V CONTROL = 0 V, Outputs open		9	16	μA
$I_{DD(d)}$	Supply current during t_d		$V_{DD} = 5 V$, $V_{CT} = 0$, $\overline{RESIN} = V_{DD}$, SENSE = V_{DD}, CONTROL = 0 V, Outputs open		120	150	μA
C_I	Input capacitance, SENSE		$V_I = 0 V$ to V_{DD}		50		pF

† Typical values apply at $T_A = 25°C$.
‡ The lowest supply voltage at which $\overline{RESET}$ becomes active. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology. Rise time of $V_{DD} \geq 15 \mu s/V$.
NOTES: 2. All characteristics are measured with $C_T = 0.1 \mu F$.
     3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be connected near the supply terminals.

switching characteristics at V_{DD} = 5 V, R_L = 2 kΩ, C_L = 50 pF, T_A = Full Range (unless otherwise noted)

| PARAMETER | | MEASURED | | TEST CONDITIONS | TLC77xx | | | UNIT |
		FROM (INPUT)	TO (OUTPUT)		MIN	TYP	MAX	
t_d	Delay time	$V_{I(SENSE)} \geq V_{IT+}$	RESET and $\overline{\text{RESET}}$	$\overline{\text{RESIN}}$ = 0.7 × V_{DD}, CONTROL = 0.2 × V_{DD}, C_T = 100 nF, T_A = Full range, See timing diagram	1.1	2.1	4.2	ms
t_{PLH}	Propagation delay time, low-to-high-level output	SENSE	$\overline{\text{RESET}}$	V_{IH} = V_{IT+}max + 0.2 V, V_{IL} = V_{IT-}min – 0.2 V, $\overline{\text{RESIN}}$ = 0.7 × V_{DD}, CONTROL = 0.2 × V_{DD}, CT = NC[†]			20	µs
t_{PHL}	Propagation delay time, high-to-low-level output	SENSE	$\overline{\text{RESET}}$				5	µs
t_{PLH}	Propagation delay time, low-to-high-level output	SENSE	RESET				5	µs
t_{PHL}	Propagation delay time, high-to-low-level output	SENSE	RESET				20	µs
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$	V_{IH} = 0.7 × V_{DD}, V_{IL} = 0.2 × V_{DD}, SENSE = V_{IT+}max + 0.2 V, CONTROL = 0.2 × V_{DD}, CT = NC[†]			20	µs
t_{PHL}	Propagation delay time, high-to-low-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$				60	ns
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{\text{RESIN}}$	RESET				65	ns
t_{PHL}	Propagation delay time, high-to-low-level output	$\overline{\text{RESIN}}$	RESET				20	µs
t_{PLH}	Propagation delay time, low-to-high-level output	CONTROL	RESET	V_{IH} = 0.7 × V_{DD}, V_{IL} = 0.2 × V_{DD}, SENSE = V_{IT+}max + 0.2 V, $\overline{\text{RESIN}}$ = 0.7 × V_{DD}, CT = NC[†]			58	ns
t_{PHL}	Propagation delay time, high-to-low-level output	CONTROL	RESET				58	ns
	Low-level minimum pulse duration to switch RESET and $\overline{\text{RESET}}$	SENSE		V_{IH} = V_{IT+}max + 0.2 V, V_{IL} = V_{IT-}min – 0.2 V,	3			µs
		$\overline{\text{RESIN}}$		V_{IL} = 0.2 × V_{DD}, V_{IH} = 0.7 × V_{DD}	1			µs
t_r	Rise time		RESET and $\overline{\text{RESET}}$	10% to 90%		8		ns/V
t_f	Fall time			90% to 10%		4		ns/V

[†] NC = No capacitor, and includes up to 100-pF probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION
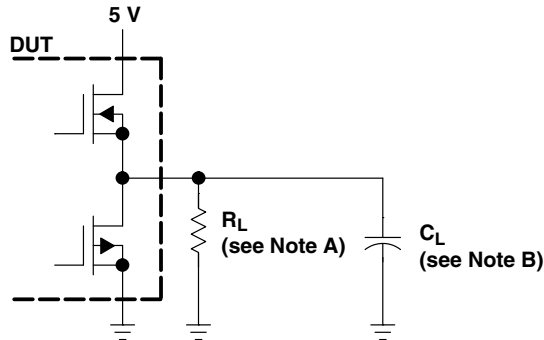
NOTES: A. For switching characteristics, R_L = 2 kΩ.
           B. C_L = 50 pF includes jig and probe capacitance.

Figure 1. RESET AND $\overline{\text{RESET}}$ Output Configurations
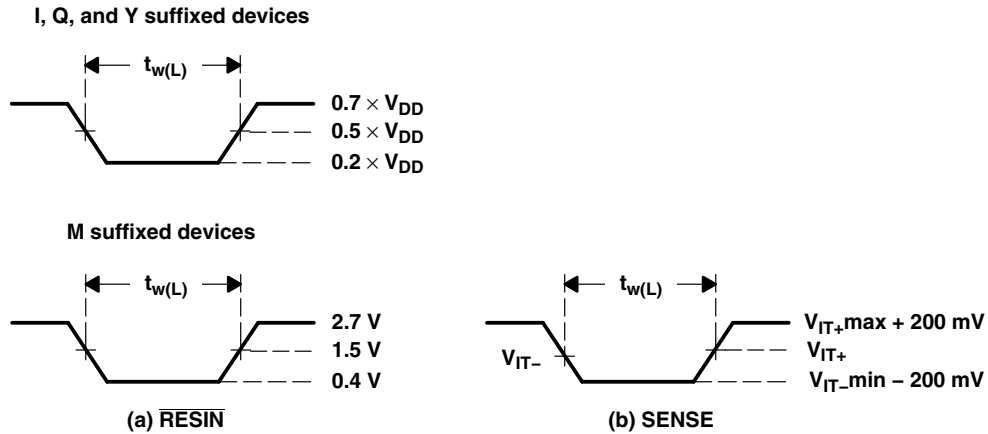
I, Q, and Y suffixed devices

M suffixed devices

(a) $\overline{\text{RESIN}}$ (b) SENSE

Figure 2. Input Pulse Definition Waveforms

TYPICAL CHARACTERISTICS

NORMALIZED INPUT THRESHOLD VOLTAGE
vs
TEMPERATURE

Figure 3

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

Figure 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 5

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT
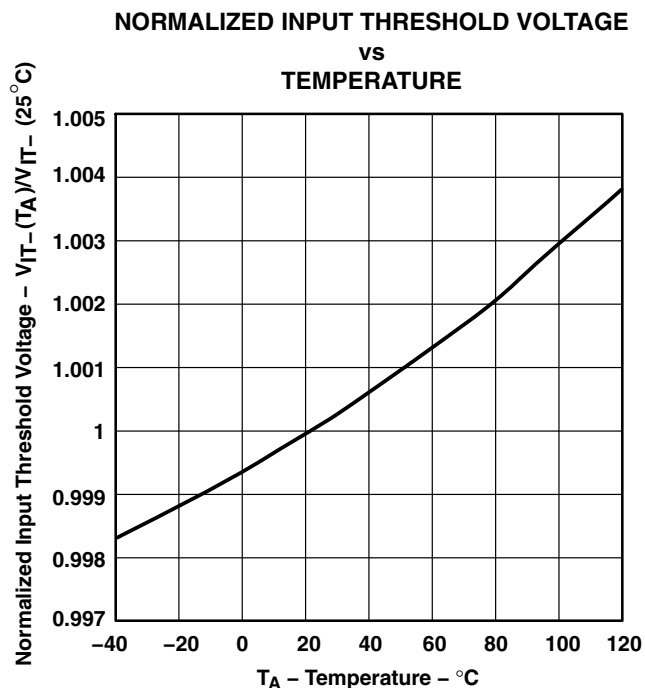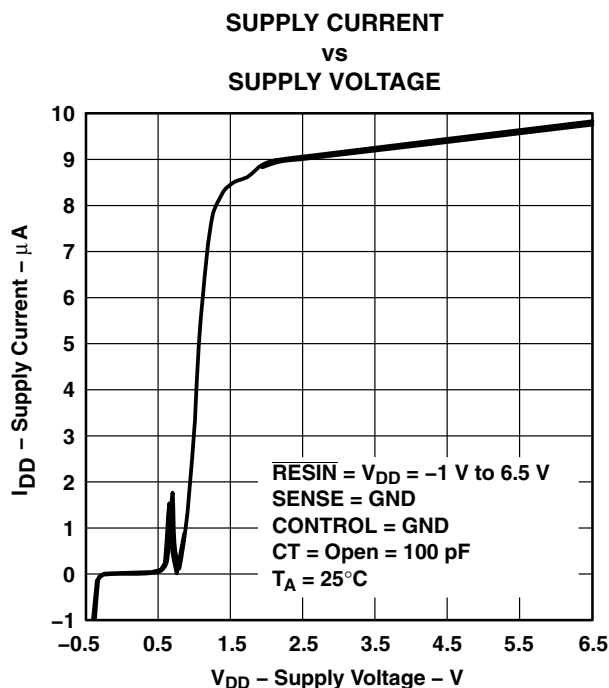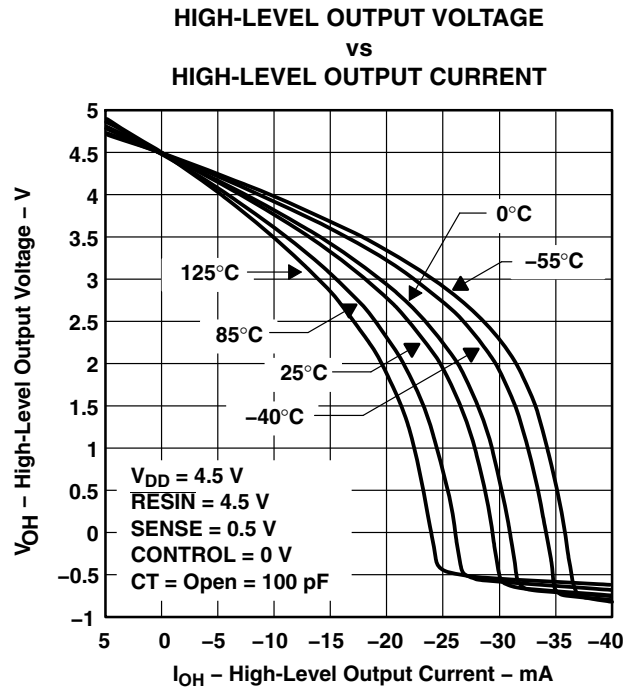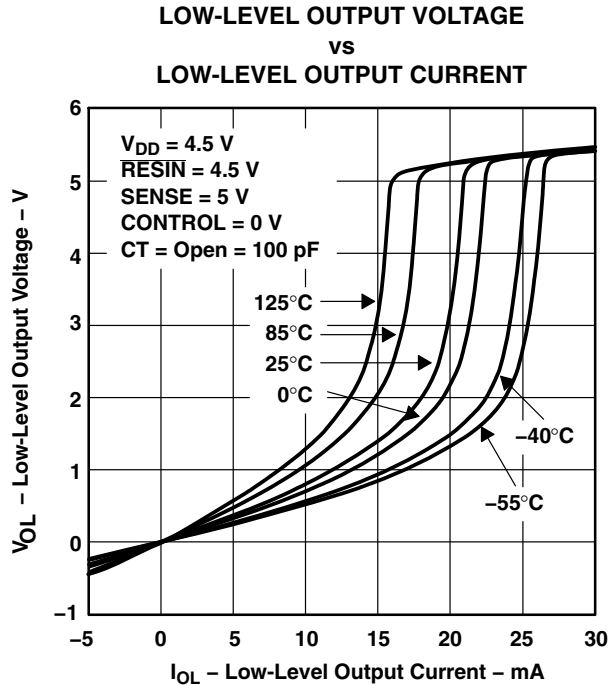
Figure 6

TYPICAL CHARACTERISTICS
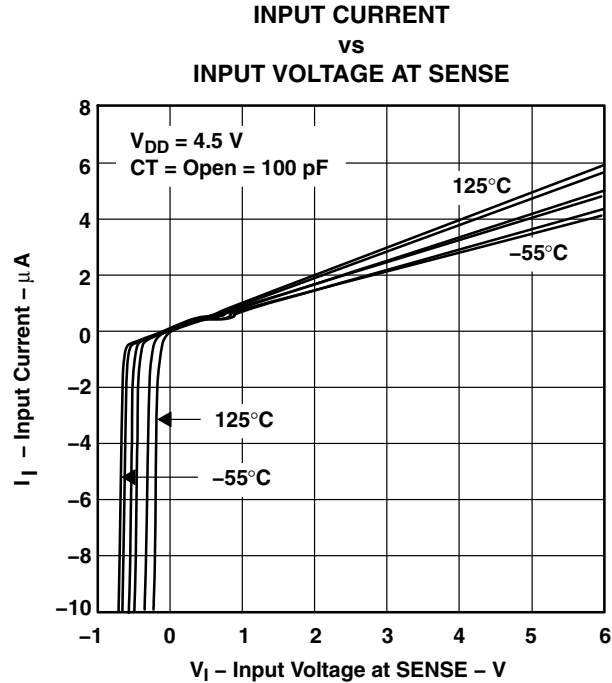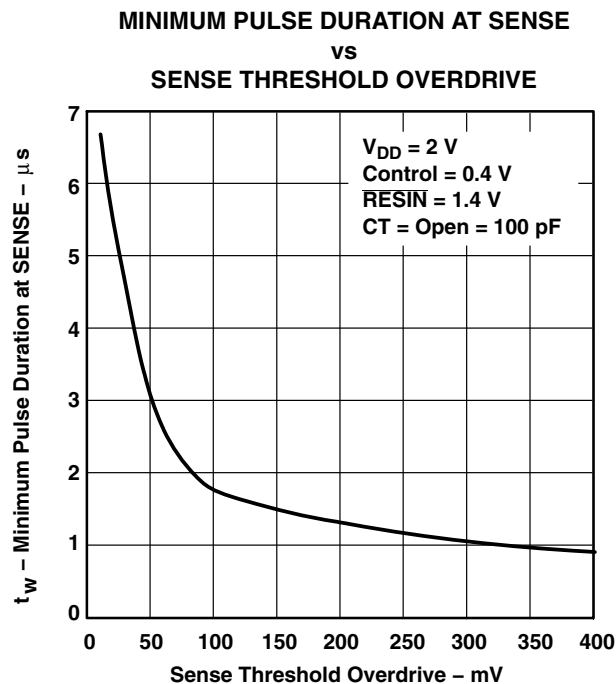
INPUT CURRENT
vs
INPUT VOLTAGE AT SENSE

Figure 7

MINIMUM PULSE DURATION AT SENSE
vs
SENSE THRESHOLD OVERDRIVE

Figure 8

APPLICATION INFORMATION

Figure 9. Reset Controller in a Microcomputer System
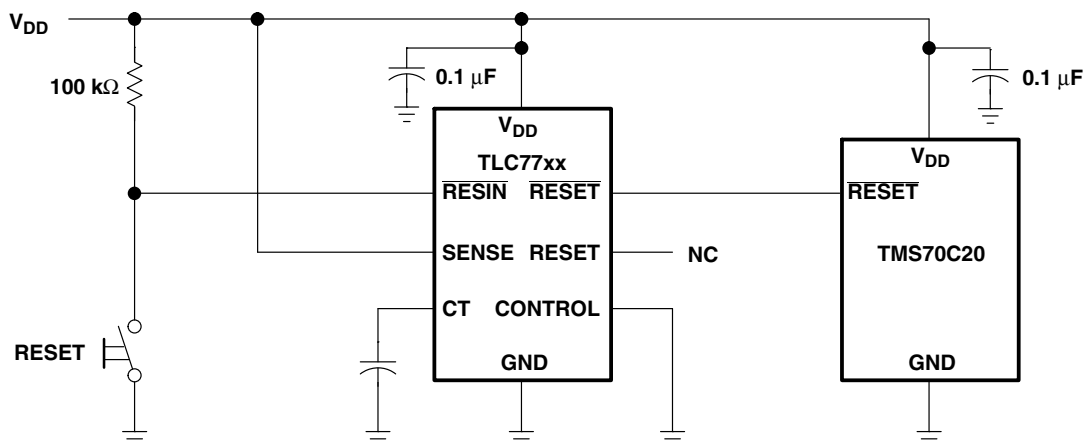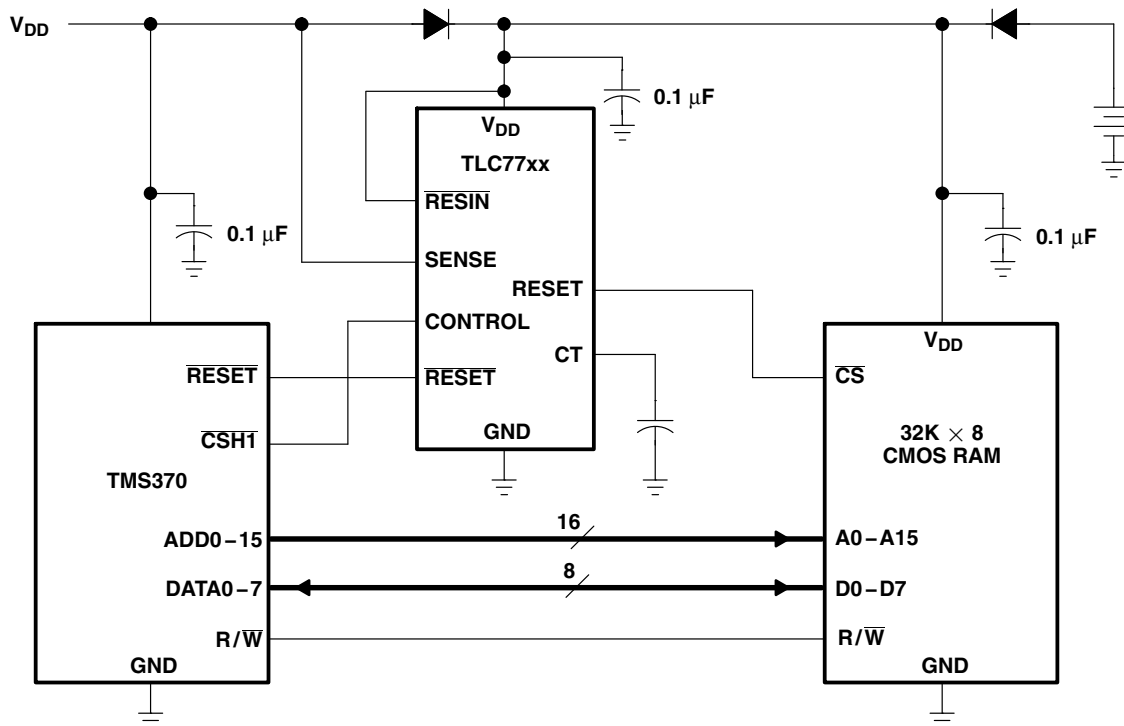

Figure 10. Data Retention During Power Down Using Static CMOS RAMs

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC7701QPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7701Q1	Samples
TLC7701QPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7701Q1	Samples
TLC7705QPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705Q1	Samples
TLC7733QPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7733Q1	Samples
TLC7733QPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7733Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

![Texas Instruments logo]

OTHER QUALIFIED VERSIONS OF TLC7701-Q1, TLC7705-Q1, TLC7733-Q1 :

- Catalog: TLC7701, TLC7705, TLC7733

- Enhanced Product: TLC7701-EP, TLC7705-EP, TLC7733-EP

- Military: TLC7705M, TLC7733M

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
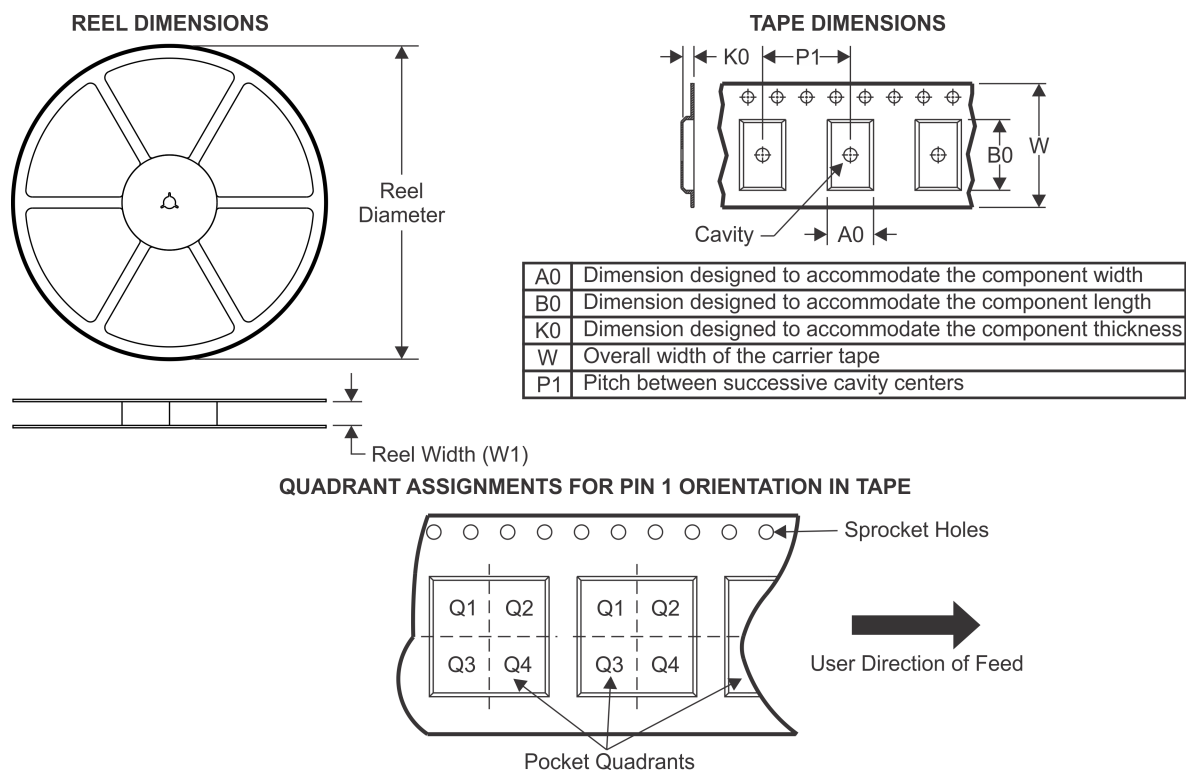
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC7733QPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC7733QPWRG4Q1	TSSOP	PW	8	2000	367.0	367.0	35.0

PW (R−PDSO−G8)   PLASTIC SMALL OUTLINE
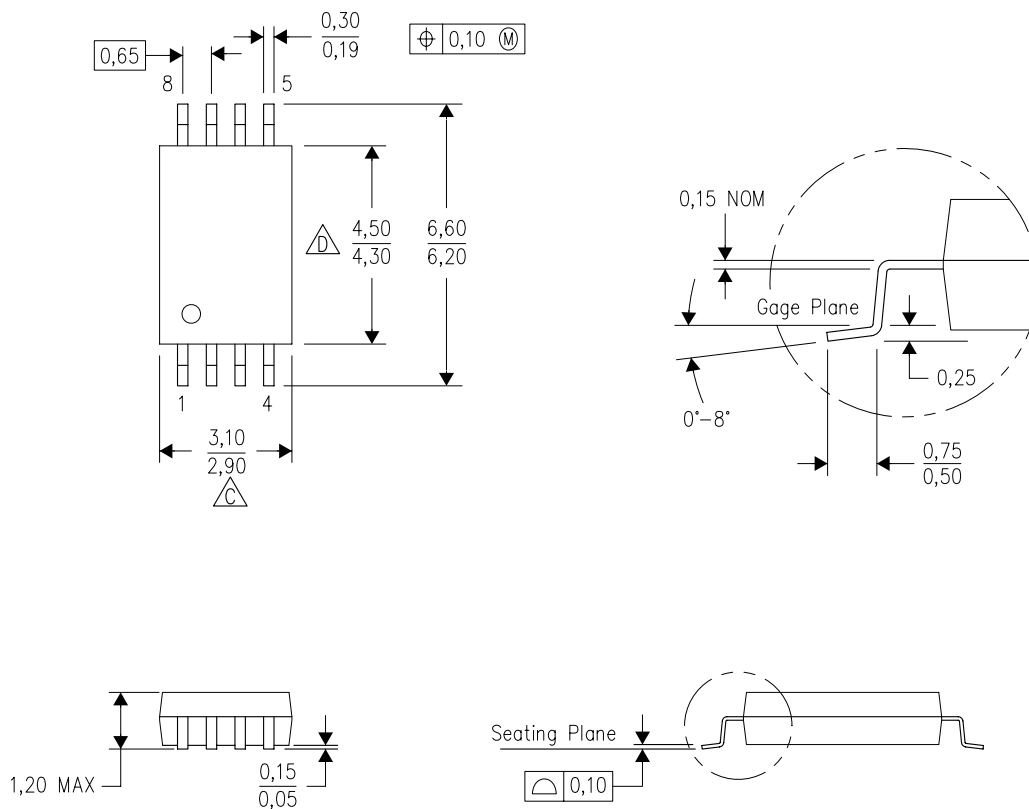
4040064−2/G 02/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
         D.   Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
         E.   Falls within JEDEC MO−153

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DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
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OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		