TLK3134
4-Channel Multi-Rate Transceiver

Data Manual

Literature Number: SLLS838F
May 2007–Revised December 2009

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4-Channel Multi-Rate Transceiver

Check for Samples: TLK3134

1 Introduction

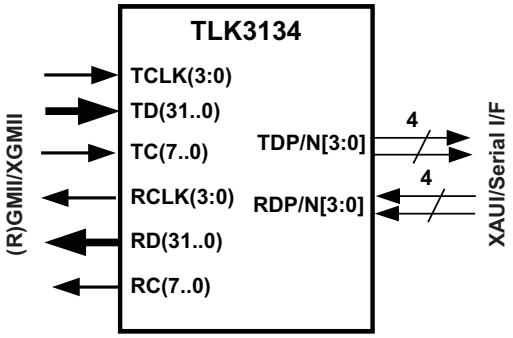
1.1 Features

- Four-Channel 600Mbps to 3.75Gbps Multi-Rate Transceiver
- Supports 10GbE (XAUI), 1X/2X/10X Fibre Channel (FC), CPRI (x1/x2/x4), OBSAI (x1/x2/x4), and 1GbE (1000Base-X) Data Rates
- Complete IEEE Compliant 10 GbE XGXS (XAUI) Compliant Core and 1000Base-X PCS Support
- Supports Independent Channel SERDES Operation Modes in 8/10 Bit Data Modes (TBI and 8 Bit + Control)
- Serial Side Transmit De-Emphasis and Receive Adaptive Equalization to Allow Extended Backplane Reach
- Low Jitter LC Oscillator Jitter-Cleaner Allows use of Poor Quality REFCLK
- Full Datapath Loopback Capability (Serial/Parallel Side)
- Support PRBS 2^7-1 and 2^{23} - 1 Gen/Verify. Support standard defined CJPAT, CRPAT, High and Low Frequency, and Mixed Freq Testing.
- XGMII/GMII/RGMII: HSTL Class 1 I/O With On-Chip 50Ω Termination on Inputs/Outputs (1.5/1.8 V Power Supply)
- XGMII/GMII/RGMII: Source And Data Centered I/O Timing Modes
- Supports Jumbo Packet (9600 byte maximum) Operation.
- XAUI Align Character Skew Support of 30 Bit Times at Chip Pins
- MDIO: IEEE 802.3ae Clause 22 and Clause 45 Compliant Management Data Input / Output Interface Modes (Either 1.2 V or 2.5 V MDIO I/O)
- 1.2 V Core, 1.5 V/1.8 V HSTL I/O Supply, and 2.5 V LVCMOS I/O Supply
- JTAG: IEEE 1149.1/1149.6 Test Interface
- ±200 ppm Clock Tolerance in XAUI TX and 1000Base-X/XAUI RX Datapaths
- 90 nm Advanced CMOS Technology
- Package: PBGA, 19×19mm, 289 Ball, 1mm Pitch
- 1.3W Maximum Power Dissipation (1.5 V HSTL XAUI Mode, Input HSTL Termination Disabled)
- Asymmetric RX/TX Rates Supported in Independent Channel Modes
- Industrial Ambient Operating Temperature (–40°C to 85°C) at Full Rate

1.2 Applications

- Gigabit Ethernet links
- CPRI/OBSAI Links
- Point-to-Point High-Speed Backplane Links

1.3 Pin Out



1.4 Description

The TLK3134 is a flexible four-channel independently configurable serial transceiver. It can be configured to be compliant with the 10Gbps Ethernet XAUI specification. It can also be configured to be compliant with the 1000Base-X 1Gbps Ethernet Specification (Auto-Negotiation not supported). The TLK3134 provides high-speed bidirectional point-to-point data transmissions with up to 30 Gbps of raw data transmission capacity. The primary application of this device is in backplanes and front panel connections requiring 10Gbps connections over controlled impedance media of approximately 50Ω. The transmission media can be printed circuit board (PCB) traces, copper cables or fiber-optical media. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling into the lines.

The TLK3134 performs the parallel-to-serial, serial-to-parallel conversion, and clock extraction functions for a physical layer interface. The TLK3134 provides a complete XGXS/PCS function defined in Clause 47/48 of the IEEE 802.3ae 10Gbps Ethernet standard. The TLK3134 also provides 1000Base-X (PCS) layer functionality described in Clause 36 of 802.3-2002. The serial transmitter is implemented using differential Current Mode Logic (CML) with integrated termination resistors.

The TLK3134 can be optionally configured as a XAUI or 10GFC transceiver. TLK3134 supports a 32-bit data path, 4-bit control, 10 Gigabit Media Independent Interface (XGMII) to the protocol device. Figure 1-1 shows an example system block diagram for TLK3134 used to provide the 10Gbps Ethernet Physical Coding Sublayer to Coarse Wave-length Division Multiplexed optical transceiver or parallel optics.

Many common applications may be enabled by way of externally available control pins. Detailed control of the TLK3134 on a per channel basis is available by way of accessing a register space of control bits available through a two-wire access port called the Management Data Input/Output (MDIO) interface.

The PCS (Physical Coding Sublayer) functions such as the CTC FIFO are designed to be compliant for an IEEE 802.3 XAUI or 1000Base-X PCS link. However, each of the PCS functions may be disabled or bypassed until the TLK3134 is operating at its most basic state, that of a simple four channel 10-bit SERDES suitable for a wide range of applications such as CPRI or OBSAI wireless infrastructure links.

The differential output swing for the TLK3134 is suitable for compliance with IEEE 802.3 XAUI links, which is also suitable for CPRI LV serial links. The TLK3134 provides for setting larger output signal swing suitable for CPRI HV links by setting an appropriate register bit available though MDIO.

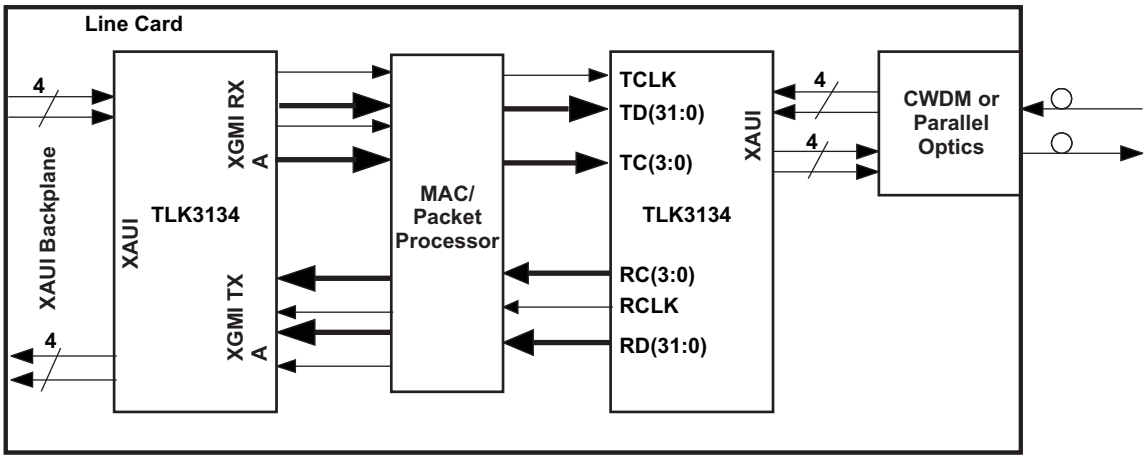


Figure 1-1. System Block Diagram – XAUI

Figure 1-2 shows an example system block diagram for TLK3134 used to provide the system backplane interconnect.

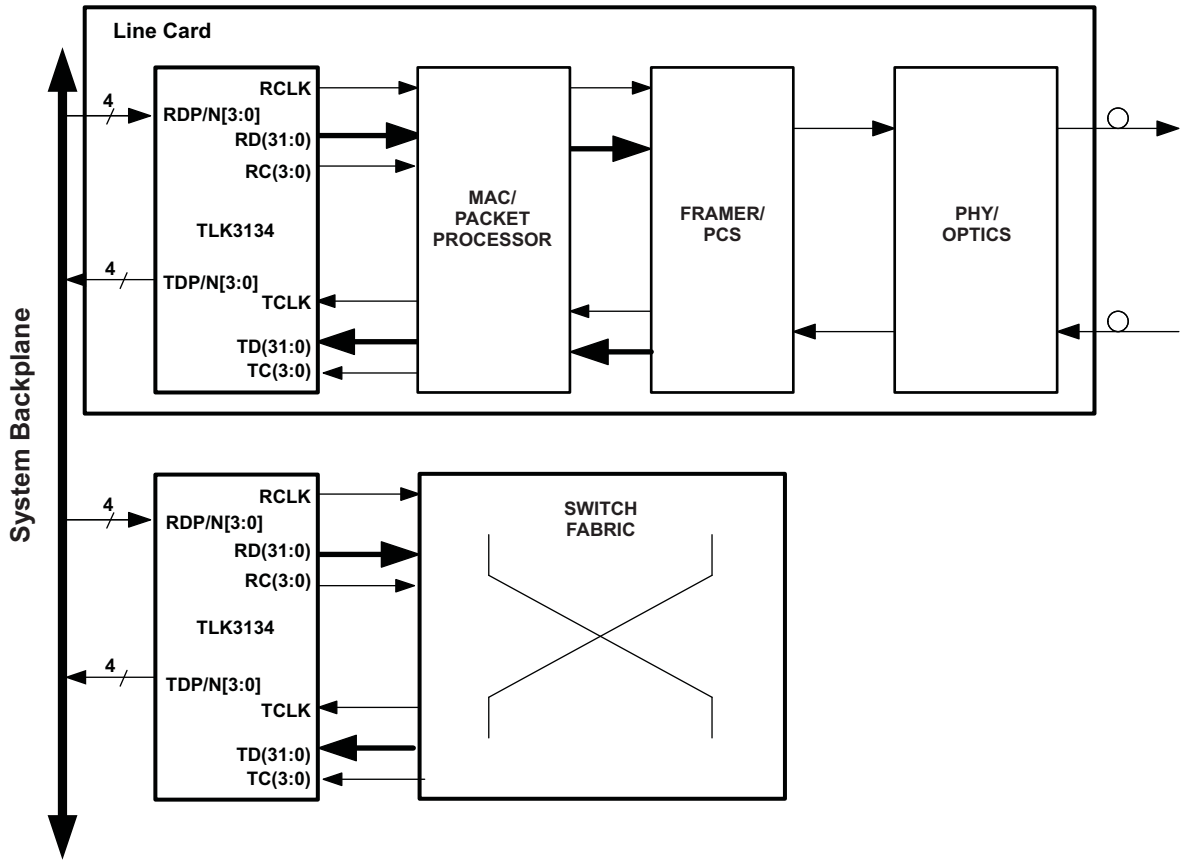


Figure 1-2. System Block Diagram – XAUI Backplane

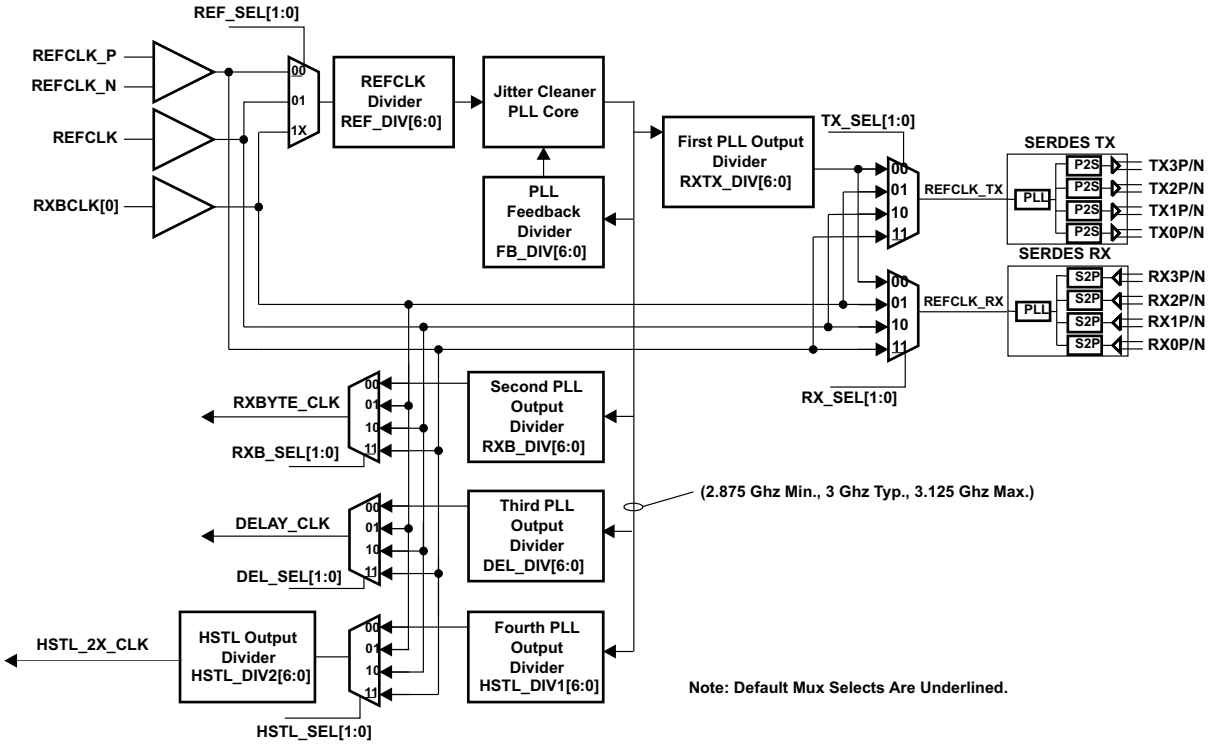


Figure 1-3. Block Diagram – TLK3134 Clocking Architecture

2 Detailed Description

2.1 Clocking Modes

The TLK3134 contains an internal low-bandwidth, low-jitter high quality LC oscillator that may be configured as a jitter cleaner. The jitter cleaner oscillator has a high frequency narrow band of operation that may be used to generate all common reference clock frequencies by way of programmable pre-scaler and post-scaler registers. In this manner a poor quality input reference clock can be input to the jitter cleaner which will lock to the reference clock and provide a clean reference to the internal SERDES PLLs. Appendix A defines in detail the clocking possibilities, and device settings.

Alternatively, the jitter cleaner may be used to lock to a recovered byte clock from RX channel 0 and remove jitter that may have transferred through the clock/data recovery circuit from the serial data stream to the recovered byte clock (including parallel output data timing). In this way the recovered byte clock may be extracted from the serial data stream yet be suitable for use in applications that require a clean clock source derived from the serial data stream. The TLK3134 jitter cleaner may only be used on the recovered byte clock from Channel 0. If the jitter cleaner is used to clean the recovered byte clock, it may not be used to clean the input reference clock, and the PLL at the center of the deserializer core must have a clean low-jitter reference clock from an external clock source, preferably a low-jitter crystal based oscillator. Note that the Transmit SERDES macro can run from the cleaned recovered RX channel 0 byte clock which allows for the outgoing TX serial data rate for all channels to exactly match the incoming data rate of RX Channel 0.

The TLK3134 clocking architecture allows for bypass of the Jitter cleaner PLL in cases where power or application board area is critical.

See Figure 1-3 Clocking Architecture for a representation of the use of the jitter cleaner in the TLK3134.

2.2 Operating Frequency Range

The TLK3134 is optimized for operation at a serial data rate of 600 Mbit/s through 3.75 Gbit/s. The external differential (optionally single-ended) reference clock has a large operating frequency range allowing support for many different applications. The reference clock frequency must be within ±200 PPM of the incoming serial data rate, and have less than 40ps of jitter. Table 2-1 shows a summary of frequency ranges supported. For more details, see Appendix A. In all applications except XAUI/10GFC, the transmit parallel clock must be frequency locked (0 ppm) to the supplied REFCLK frequency (XAUI/10GFC allows ±200 ppm).

Table 2-1. Supported Protocol Rates and REFCLK Values

PROTOCOL	Refclk (MHz)	LINE RATE (Gbps)
XAUI – 10G Ethernet	78.125/156.25/312.5	3.125
10 Gigabit Fibre Channel	79.6875/159.375/ 318.75	3.1875
1G Ethernet	62.5/125/250	1.25
1X/2X Fibre Channel	53.125/106.25/212.5	2.125 1.0625
OBSAI	76.8/153.6/307.2	3.072 1.536 0.768
CPRI	61.44/122.88/245.76	2.4576 1.2288 0.6144
Generic TBI	50 → 375 MHz	0.600 → 3.75
Generic RTBI	50 → 375 MHz	0.600 → 1.6
Generic NBID/TBID	50 → 375 MHz	0.600 → 3.2

2.3 CPRI Latency Support

The TLK3134 has a round trip latency measurement capability to support its use in CPRI applications. When enabled, the TLK3134 will measure the elapsed time from the transmission of a K28.5 code in a CPRI frame until the reception of a K28.5 code in the receive path. This measurement result may be read through an MDIO readable register. The measurement has an accuracy of ±4 ns with the Jitter Cleaner PLL enabled, and an accuracy of ±2 parallel byte clock periods if the Jitter Cleaner PLL is disabled.

2.4 Powerdown Mode

The TLK3134 (through the ENABLE pin and through register control) is capable of going into a low power quiescent state. In this state, all analog and digital circuitry is disabled.

2.5 Application Examples

TLK3134 supports many different application modes. Detailed register settings per application mode are shown in Table 2-2. The following application diagrams do not show all possible applications, and are intended only to illustrate the flexibility of the device.

Figure 2-1 shows the TLK3134 in a Quad independent channel SERDES Application. The 1000Base-X PCS layer can be enabled or disabled. Note that in independent channel mode, the 8B/10B encoder/decoder functions can either be turned on or turned off. When turned off, either 5 or 10 bits (DDR/SDR) of data is accepted from and presented to the parallel side. When the 8B/10B encoder/decoder functions are enabled, 1 bit of control and 8 bits of data are accepted from and presented to the parallel side using the standardized (R)GMII control characters.

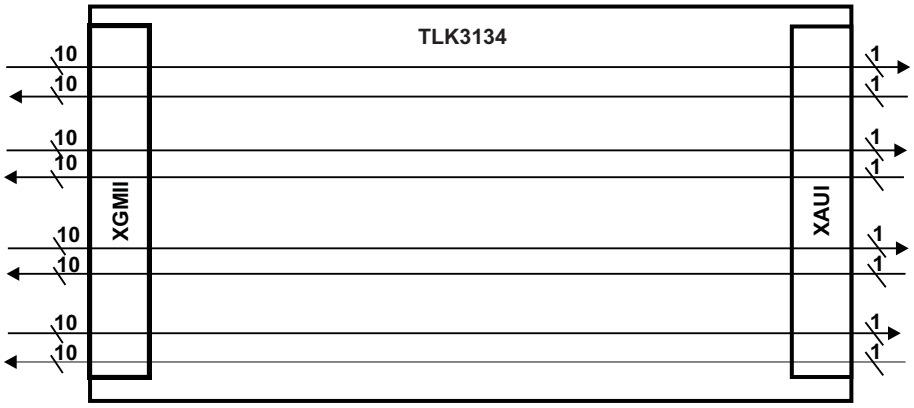


Figure 2-1. Quad 10-Bit SERDES Application

Figure 2-2 shows the TLK3134 in a XAUI Loopback Application. It is possible to configure XAUI side loopback in SERDES mode for all 4 channels on an individual basis.

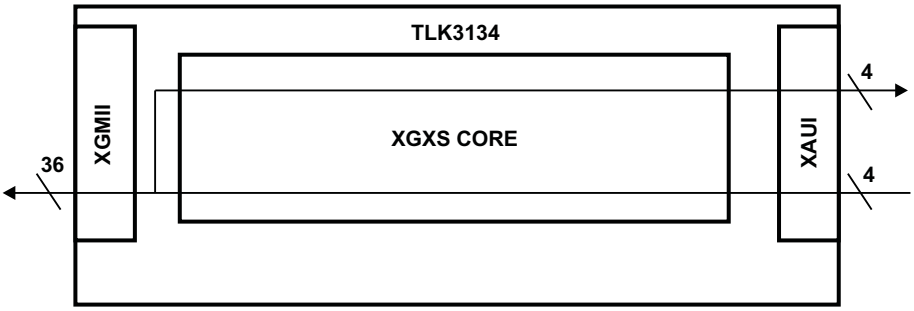


Figure 2-2. XAUI Mode – XAUI (Serial) Loopback Application

Figure 2-3 shows the TLK3134 in a XGMII Loopback Application. It is possible to configure XGMII side loopback in SERDES mode for all 4 channels on an individual basis.

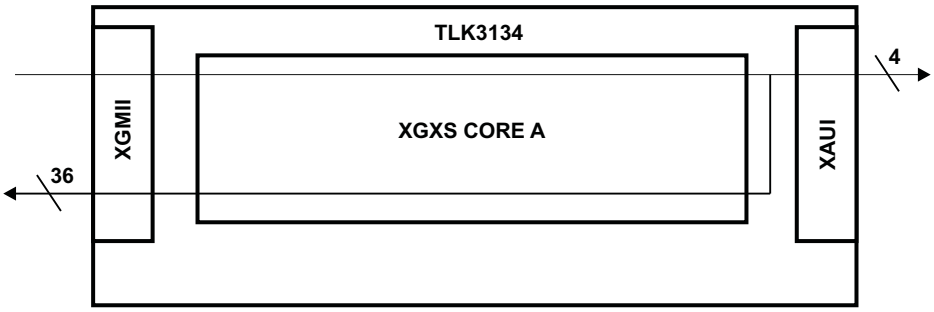


Figure 2-3. XAUI Mode - XGMII (Parallel) Loopback Application

Figure 2-4 shows the TLK3134 in a custom application example with mixed modes per Channel.

- Channel 1 in Parallel independent loopback mode
- Channel 3 in Serial independent loopback mode
- Channel 0 & 2 in independent channel transceiver mode

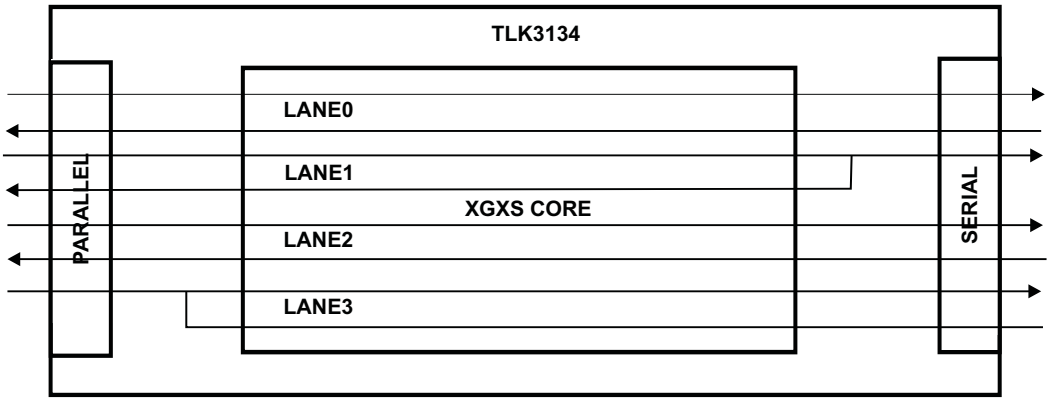


Figure 2-4. Custom Independent Configuration Application

The TLK3134 supports the IEEE 802.3 defined Management Data Input/Output (MDIO) Interface to allow ease in configuration and status monitoring of the link. The bi-directional data pin (MDIO) **must** be externally pulled up to 1.2 V or 2.5 V (VDDM) per the standard for MDIO.

The TLK3134 supports the IEEE 1149.1/1149.6 defined JTAG test port for ease in board manufacturing test. It also supports a comprehensive series of built-in tests for self-test purposes including PRBS generation and verification, CRPAT, CJPAT, Mixed/High/Low Frequency testing.

The TLK3134 operates with a 1.2 V core voltage supply, a 1.5/1.8 V HSTL I/O voltage supply and a 2.5 V LVCMOS/bias supply.

The TLK3134 is packaged in a 19×19mm, 289-ball, 1mm ball pitch Plastic Ball Grid Array (PBGA) package and is characterized for operation from –40°C to 85°C Ambient, 105°C Junction, and 5% power supply variation at the balls of the device unless noted otherwise.

The following block diagram provides a high level description of the TLK3134.

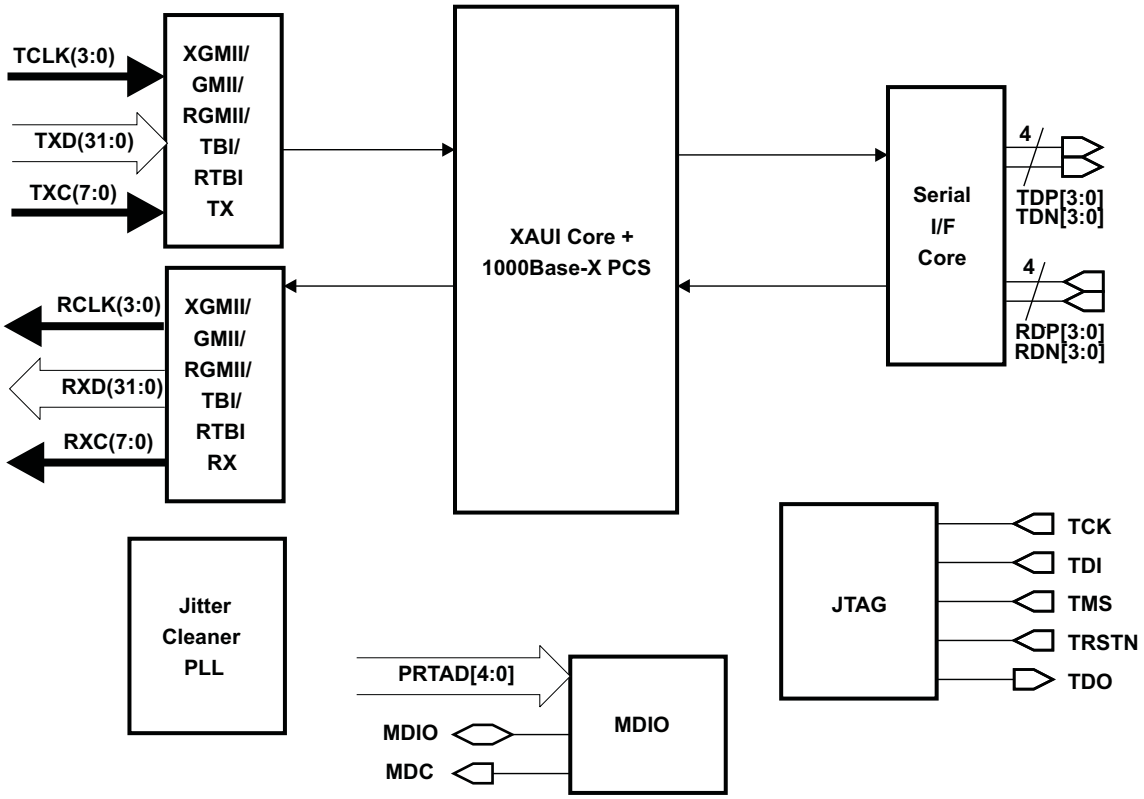


Figure 2-5. TLK3134 Block Diagram

Following is a more detailed block diagram description of the XAUI core.

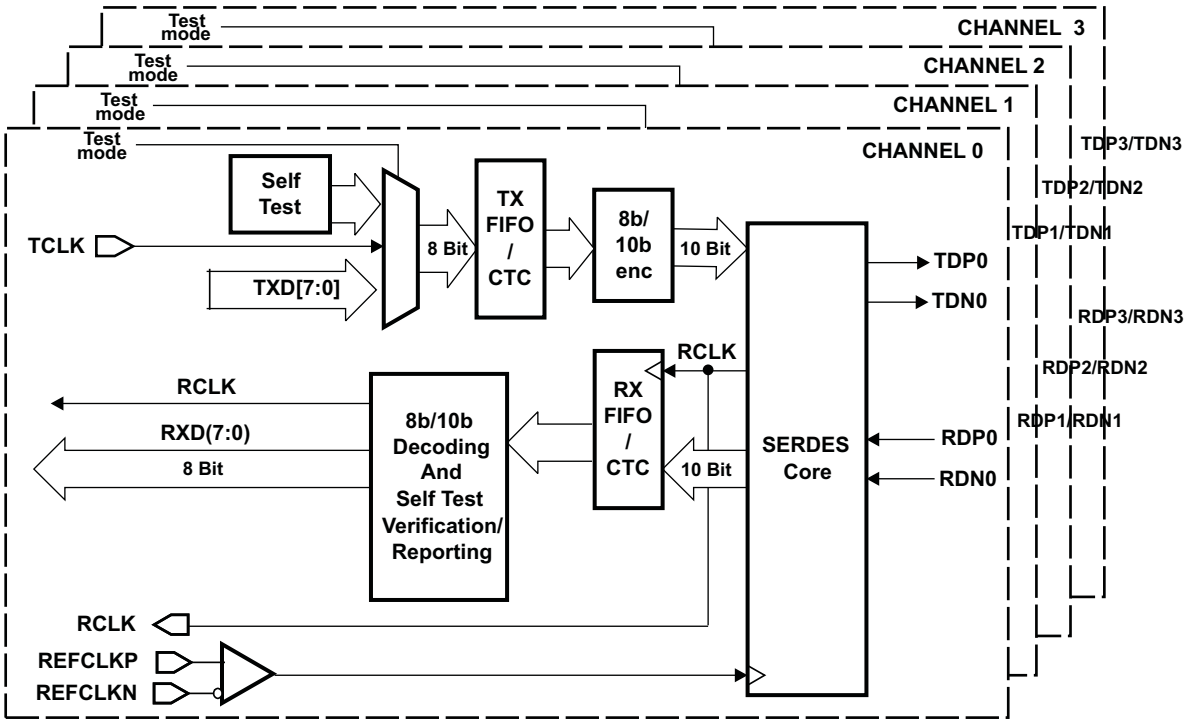


Figure 2-6. Detailed XAUI/1000Base-X Core Block Diagram

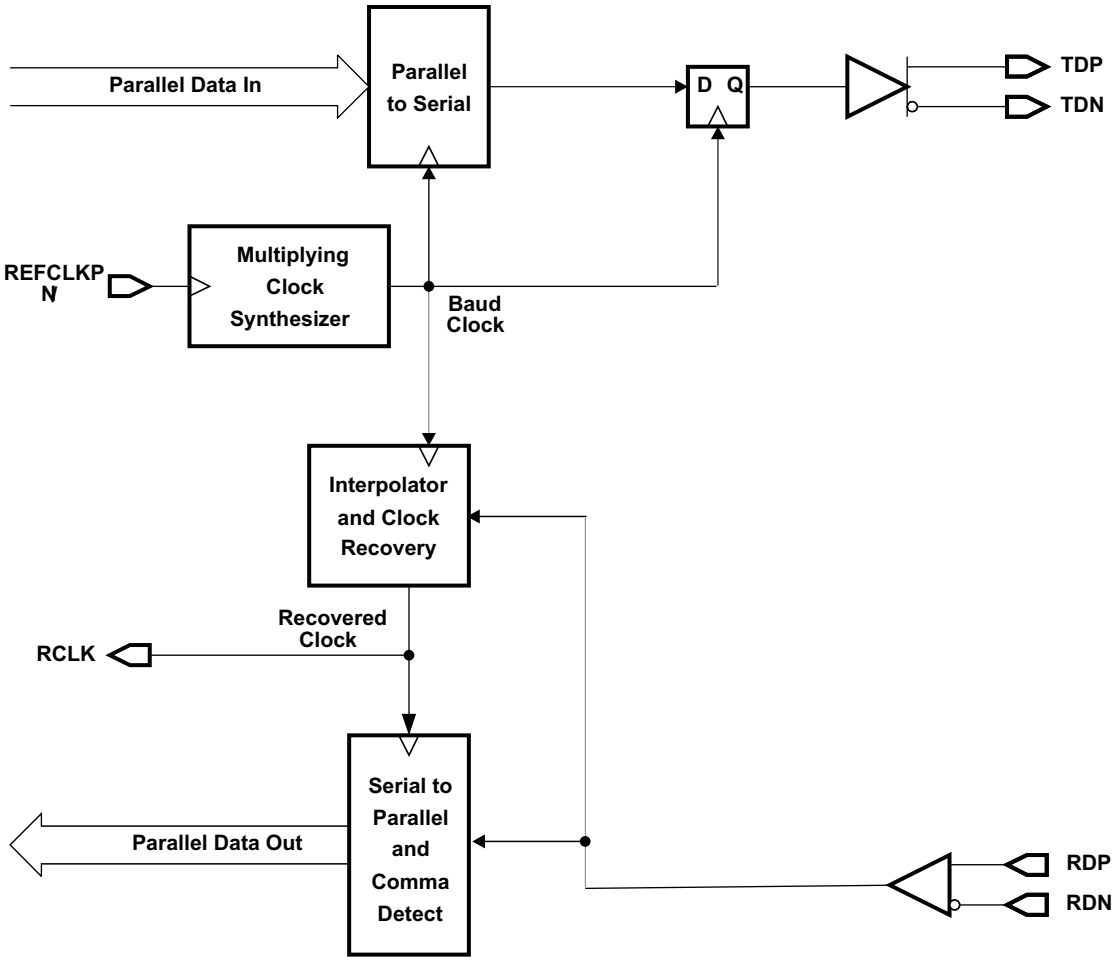


Figure 2-7. Block Diagram of SERDES Core

2.6 Device Operation Modes

Table 2-2. Device Operation Modes

DEVICE MODE	XAUI[1] (DDR)	10GFC[2] (DDR)	RGMII (DDR)	GMII (SDR)	RTBI (DDR)	TBI (SDR)	REBI (DDR)	EBI (SDR)	RNBI (DDR)	NBI (SDR)	TBID (DDR)	NBID (DDR)
ST Primary Chip Input	0		1									
MDIO Access Method	Clause 45		Clause 22[3]									
XAUI_ORDER 32809.15 Logical Or w/CODE pin	1	0	X									
XAUI_TX_EDGE_ALIGN 32808.15	0/1											
XAUI_RX_EDGE_ALIGN 32808.11												
DDR_SDR 17.5	X		1	0	1	0	1	0	1	0	X	
NIBBLE_ORDER 17.4			0/1	X	0/1	X	0/1	X	0/1	X		
TX_EDGE_MODE 17.1			0/1									
RX_EDGE_MODE 17.0												
FC_ENC_MODE 17.6			0						0/1		0	0/1
COMMA_DET_EN 17.7			1		0/1		0		1		0/1	1
PCS_EN 17.3 Logical OR w/CODE pin					0							
ENC_DEC_EN 17.2					0				1		0	1
BUSWIDTH 36864.7			0				1		0			
FULL_DDR 17.9			0								1	
Legend : (X = Don't Care) — (0 = Must Be Zero) — (1 = Must Be One) — (0/1 = Can Be Either Zero-or-One)												

(1) Default Mode if ST Primary Chip Input Pin "0", CODE Primary Chip Input Pin "1".
(2) Default Mode if ST Primary Chip Input Pin "0", CODE Primary Chip Input Pin "0".
(3) All Clause 22 Registers are Per Device Channel.

2.7 Parallel Interface Modes - Detailed Description

The TLK3134 has several parallel interface modes. The major parallel interface modes of operation are presented below:

2.7.1 XAUI/10GFC Mode

Table 2-3. XAUI – Lane To Functional Pin Mapping (XAUI_ORDER = 1)

XAUI LANE	TRANSMIT CONTROL BIT (INPUT)	TRANSMIT DATA BYTE (INPUT)	RECEIVE CONTROL BIT (OUTPUT)	RECEIVE CONTROL BYTE (OUTPUT)	TRANSMIT CLOCK (INPUT)	RECEIVE CLOCK (OUTPUT)
Lane 3	TXC_[3]	TXD_[31:24]	RXC_[3]	RXD_[31:24]	TXCLK_[1]	RXCLK_[1]
Lane 2	TXC_[2]	TXD_[23:16]	RXC_[2]	RXD_[23:16]	TXCLK_[1]	RXCLK_[1]
Lane 1	TXC_[1]	TXD_[15:8]	RXC_[1]	RXD_[15:8]	TXCLK_[1]	RXCLK_[1]
Lane 0	TXC_[0]	TXD_[7:0]	RXC_[0]	RXD_[7:0]	TXCLK_[1]	RXCLK_[1]

Table 2-4. 10GFC – Lane To Functional Pin Mapping (XAUI_ORDER = 0)

10GFC LANE	TRANSMIT CONTROL BIT (INPUT)	TRANSMIT DATA BYTE (INPUT)	RECEIVE CONTROL BIT (OUTPUT)	RECEIVE CONTROL BYTE (OUTPUT)	TRANSMIT CLOCK (INPUT)	RECEIVE CLOCK (OUTPUT)
Lane 0	TXC_[3]	TXD_[31:24]	RXC_[3]	RXD_[31:24]	TXCLK_[1]	RXCLK_[1]
Lane 1	TXC_[2]	TXD_[23:16]	RXC_[2]	RXD_[23:16]	TXCLK_[1]	RXCLK_[1]
Lane 2	TXC_[1]	TXD_[15:8]	RXC_[1]	RXD_[15:8]	TXCLK_[1]	RXCLK_[1]
Lane 3	TXC_[0]	TXD_[7:0]	RXC_[0]	RXD_[7:0]	TXCLK_[1]	RXCLK_[1]

2.7.2 RGMII Mode (Reduced Gigabit Media Independent Interface)

Table 2-5. RGMII – Lane To Functional Pin Mapping

DATA CHANNEL NUMBER	TX_EN/TX_ER CONTROL BIT (INPUT)	TRANSMIT DATA NIBBLE (INPUT)	RX_DV/RX_ER CONTROL BIT (OUTPUT)	RECEIVE CONTROL NIBBLE (OUTPUT)	TRANSMIT CLOCK (INPUT)	RECEIVE CLOCK (OUTPUT)
Channel 0	TXD_[4]	TXD_[3:0]	RXD_[4]	RXD_[3:0]	TXCLK_[0]	RXCLK_[0]
Channel 1	TXD_[12]	TXD_[11:8]	RXD_[12]	RXD_[11:8]	TXCLK_[1]	RXCLK_[1]
Channel 2	TXD_[20]	TXD_[19:16]	RXD_[20]	RXD_[19:16]	TXCLK_[2]	RXCLK_[2]
Channel 3	TXD_[28]	TXD_[27:24]	RXD_[28]	RXD_[27:24]	TXCLK_[3]	RXCLK_[3]

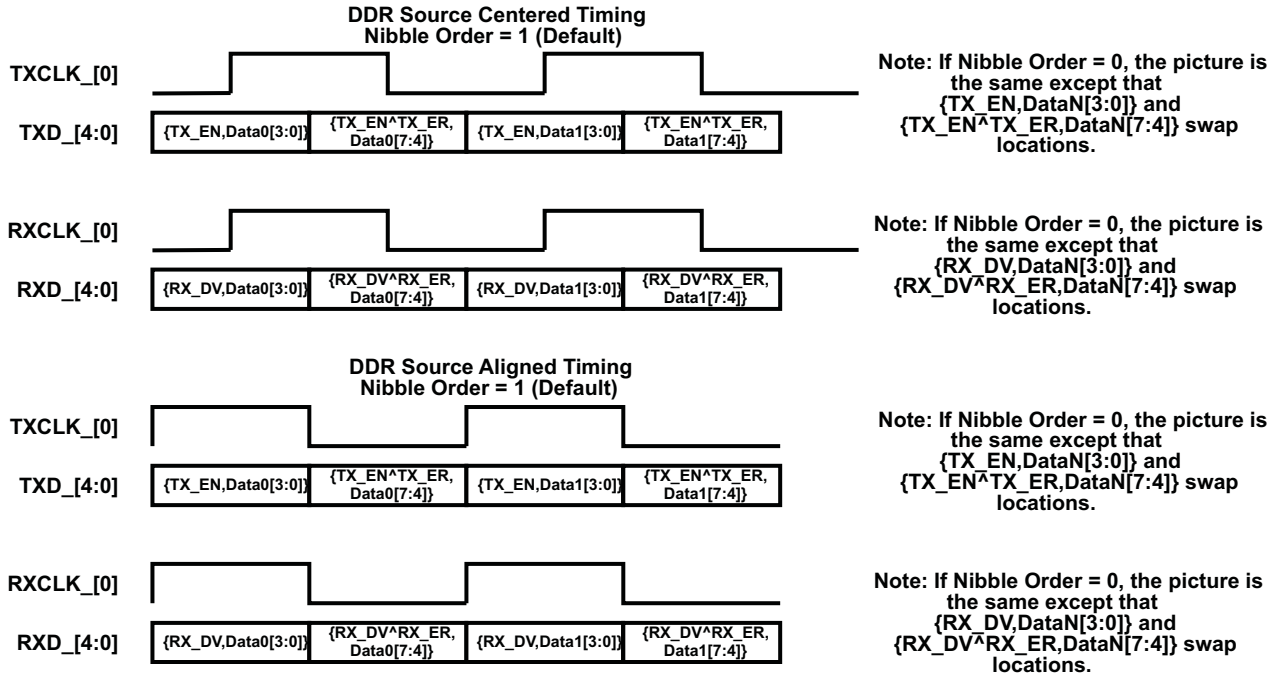


Figure 2-8. RGMII – Individual Channel Byte Ordering – Channel 0 Example

2.7.3 RTBI Mode (Reduced Ten Bit Interface)

Table 2-6. RTBI – Lane To Functional Pin Mapping

DATA CHANNEL NUMBER	TRANSMIT DATA 5 BITS (INPUT)	RECEIVE DATA 5 BITS (OUTPUT)	TRANSMIT CLOCK (INPUT)	RECEIVE CLOCK (OUTPUT)
Channel 0	TXD_[4:0]	RXD_[4:0]	TXCLK_[0]	RXCLK_[0]
Channel 1	TXD_[12:8]	RXD_[12:8]	TXCLK_[1]	RXCLK_[1]
Channel 2	TXD_[20:16]	RXD_[20:16]	TXCLK_[2]	RXCLK_[2]
Channel 3	TXD_[28:24]	RXD_[28:24]	TXCLK_[3]	RXCLK_[3]

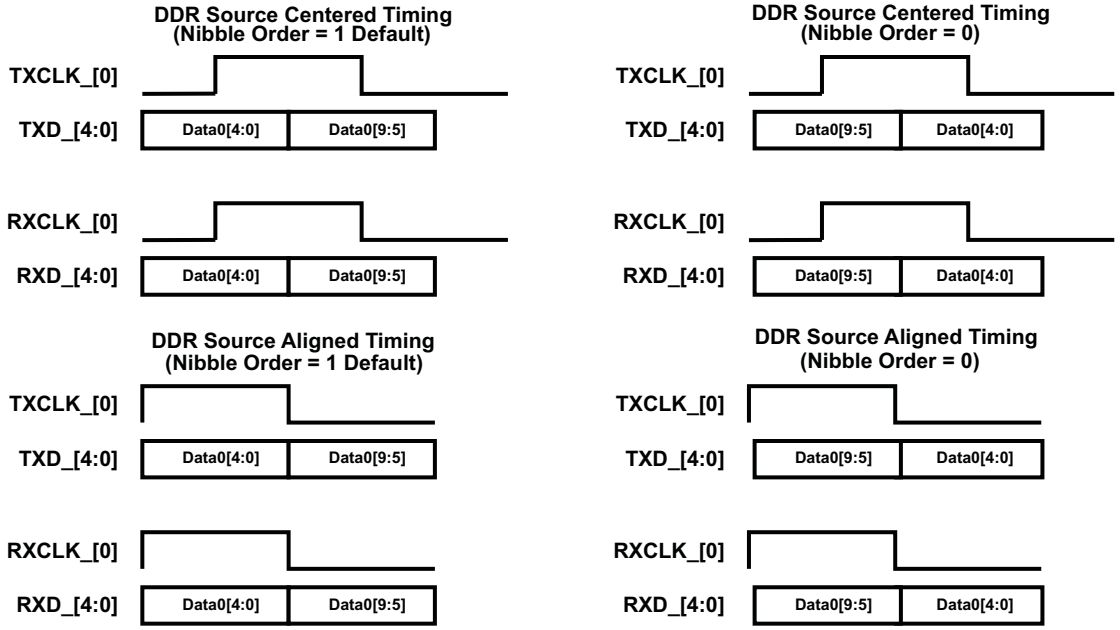


Figure 2-9. RTBI – Individual Channel Byte Ordering – Channel 0 Example

2.7.4 TBI Mode (Ten Bit Interface)

Table 2-7. TBI – Lane To Functional Pin Mapping

DATA CHANNEL NUMBER	TRANSMIT DATA 10 BITS (INPUT)	RECEIVE DATA 10 BITS (OUTPUT)	TRANSMIT CLOCK (INPUT)	RECEIVE CLOCK (OUTPUT)
Channel 0	{TXC_[4], TXC_[0],TXD_[7:0]}	{RXC_[4], RXC_[0],RXD_[7:0]}	TXCLK_[0]	RXCLK_ [0]
Channel 1	{TXC_[5],TXC_[1],TXD_[15:8]}	{RXC_[5], RXC_[1],RXD_[15:8]}	TXCLK_[1]	RXCLK_ [1]
Channel 2	{TXC_[6],TXC_[2],TXD_[23:16]}	{RXC_[6],RXC_[2],RXD_[23:16]}	TXCLK_[2]	RXCLK_ [2]
Channel 3	{TXC_[7],TXC_[3],TXD_[31:24]}	{RXC_[7],RXC_[3],RXD_[31:24]}	TXCLK_[3]	RXCLK_ [3]

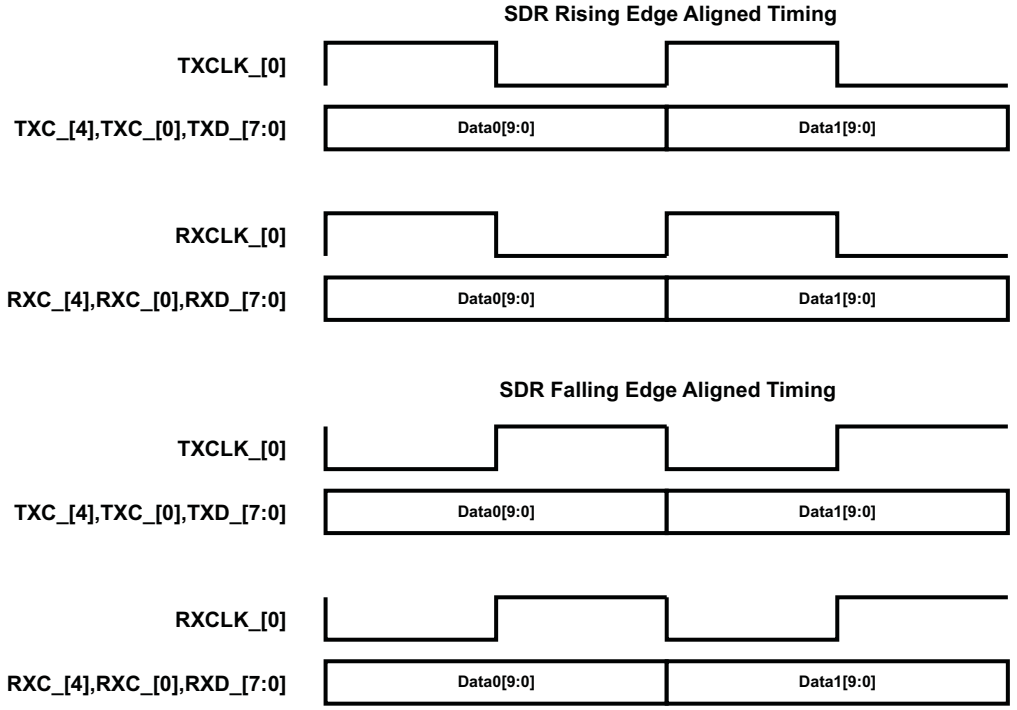


Figure 2-10. TBI – Individual Channel Byte Ordering – Channel 0 Example

2.7.5 GMII Mode (Gigabit Media Independent Interface)

Table 2-8. GMII – Lane To Functional Pin Mapping

DATA CHANNEL NUMBER	TX_EN CONTROL BIT (INPUT)	TX_ER CONTROL BIT (INPUT)	TRANSMIT DATA BYTE (INPUT)	RX_DV CONTROL BIT (OUTPUT)	RX_ER CONTROL BIT (OUTPUT)	RECEIVE DATA BYTE (OUTPUT)	TRANSMIT CLOCK (INPUT)	RECEIVE CLOCK (OUTPUT)
Channel 0	TXC_[0]	TXC_[4]	TXD_[7:0]	RXC_[0]	RXC_[4]	RXD_[7:0]	TXCLK_[0]	RXCLK_[0]
Channel 1	TXC_[1]	TXC_[5]	TXD_[15:8]	RXC_[1]	RXC_[5]	RXD_[15:8]	TXCLK_[1]	RXCLK_[1]
Channel 2	TXC_[2]	TXC_[6]	TXD_[23:16]	RXC_[2]	RXC_[6]	RXD_[23:16]	TXCLK_[2]	RXCLK_[2]
Channel 3	TXC_[3]	TXC_[7]	TXD_[31:24]	RXC_[3]	RXC_[7]	RXD_[31:24]	TXCLK_[3]	RXCLK_[3]

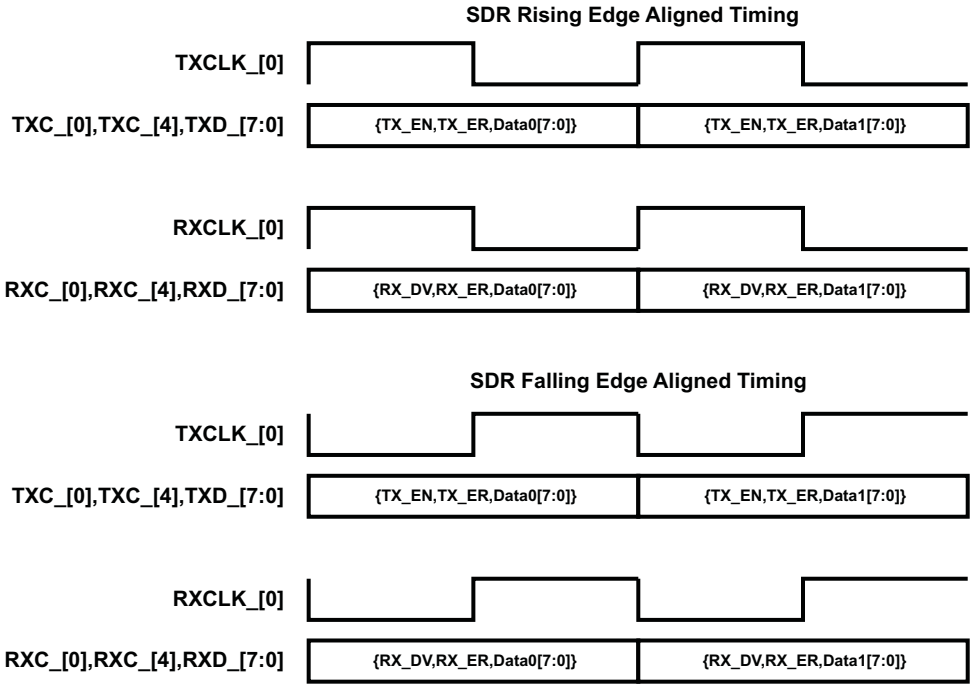


Figure 2-11. GMII – Individual Channel Byte Ordering – Channel 0 Example

2.7.6 EBI Mode (Eight Bit Interface)

Table 2-9. EBI – Lane To Functional Pin Mapping

DATA CHANNEL NUMBER	TRANSMIT DATA 8 BITS (INPUT)	RECEIVE DATA 8 BITS (OUTPUT)	TRANSMIT CLOCK (INPUT)	RECEIVE CLOCK (OUTPUT)
Channel 0	TXD_[7:0]	RXD_[7:0]	TXCLK_[0]	RXCLK_[0]
Channel 1	TXD_[15:8]	RXD_[15:8]	TXCLK_[1]	RXCLK_[1]
Channel 2	TXD_[23:16]	RXD_[23:16]	TXCLK_[2]	RXCLK_[2]
Channel 3	TXD_[31:24]	RXD_[31:24]	TXCLK_[3]	RXCLK_[3]

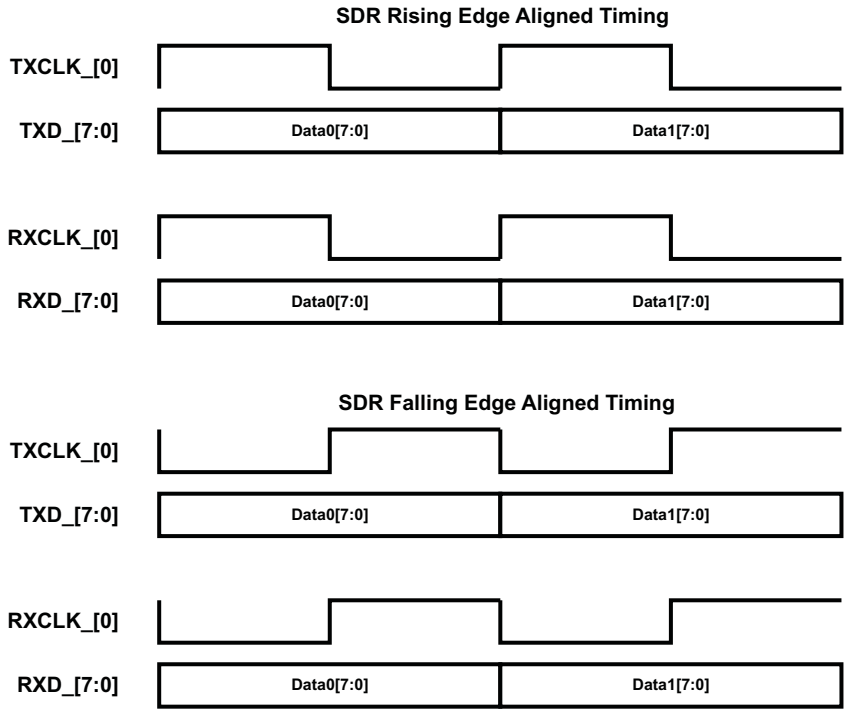


Figure 2-12. EBI – Individual Channel Byte Ordering – Channel 0 Example

2.7.7 REBI Mode (Reduced Eight Bit Interface)

Table 2-10. REBI – Lane To Functional Pin Mapping

DATA CHANNEL NUMBER	TRANSMIT DATA 4 BITS (INPUT)	RECEIVE DATA 4 BITS (OUTPUT)	TRANSMIT CLOCK (INPUT)	RECEIVE CLOCK (OUTPUT)
Channel 0	TXD_[3:0]	RXD_[3:0]	TXCLK_[0]	RXCLK_[0]
Channel 1	TXD_[11:8]	RXD_[11:8]	TXCLK_[1]	RXCLK_[1]
Channel 2	TXD_[19:16]	RXD_[19:16]	TXCLK_[2]	RXCLK_[2]
Channel 3	TXD_[27:24]	RXD_[27:24]	TXCLK_[3]	RXCLK_[3]

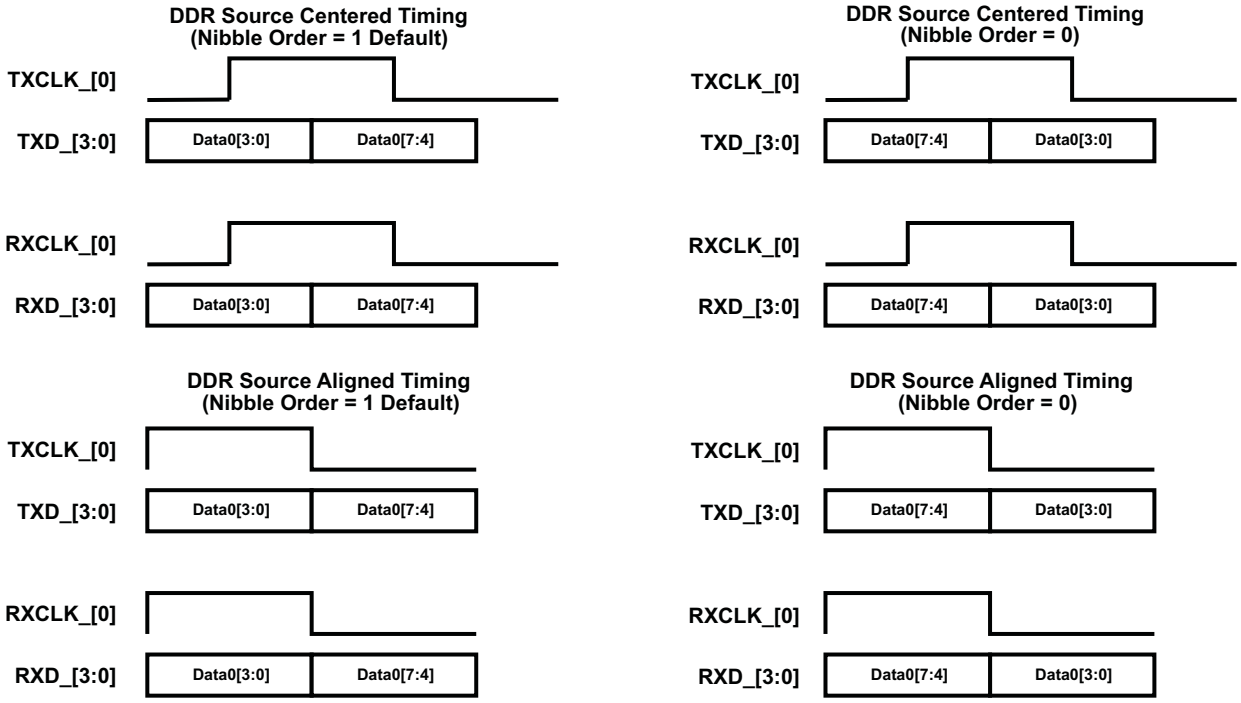


Figure 2-13. REBI – Individual Channel Byte Ordering – Channel 0 Example

2.7.8 NBI Mode (Nine Bit Interface Mode)

Table 2-11. NBI – Lane To Functional Pin Mapping

DATA CHANNEL NUMBER	TRANSMIT DATA 9 BITS (INPUT)	RECEIVE DATA 9 BITS (OUTPUT)	TRANSMIT CLOCK (INPUT)	RECEIVE CLOCK (OUTPUT)
Channel 0	{TXC_[0],TXD_[7:0]}	{RXC_[0],RXD_[7:0]}	TXCLK_[0]	RXCLK_[0]
Channel 1	{TXC_[1],TXD_[15:8]}	{RXC_[1],RXD_[15:8]}	TXCLK_[1]	RXCLK_[1]
Channel 2	{TXC_[2],TXD_[23:16]}	{RXC_[2],RXD_[23:16]}	TXCLK_[2]	RXCLK_[2]
Channel 3	{TXC_[3],TXD_[31:24]}	{RXC_[3],RXD_[31:24]}	TXCLK_[3]	RXCLK_[3]

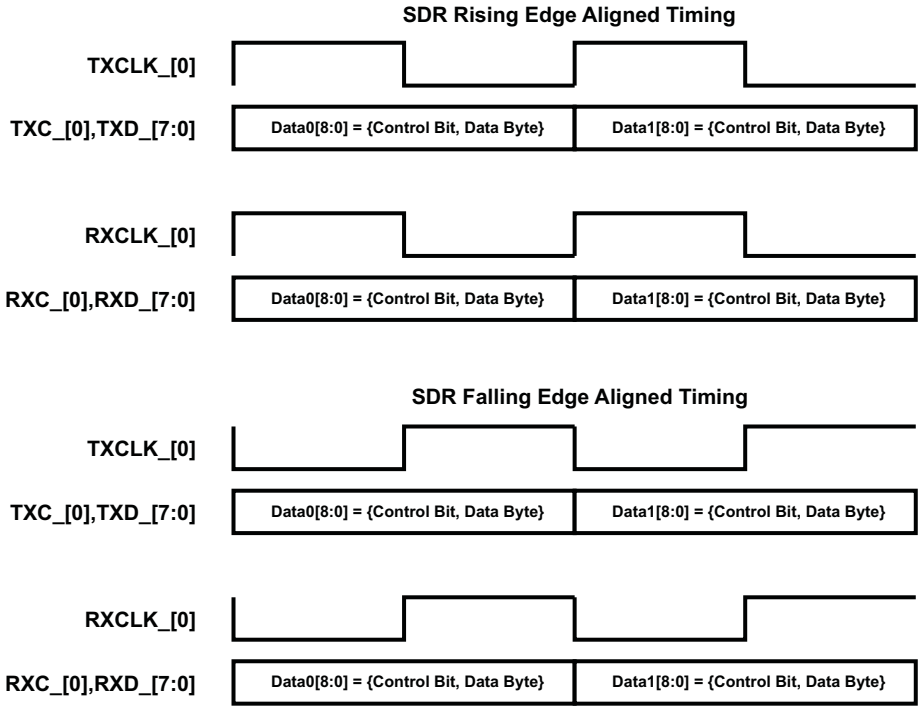


Figure 2-14. NBI – Individual Channel Byte Ordering – Channel 0 Example

2.7.9 RNBI Mode (Reduced Nine Bit Interface)

Table 2-12. RNBI – Lane To Functional Pin Mapping

DATA CHANNEL NUMBER	TRANSMIT DATA 5 BITS (INPUT)	RECEIVE DATA 5 BITS (OUTPUT)	TRANSMIT CLOCK (INPUT)	RECEIVE CLOCK (OUTPUT)
Channel 0	TXD_[4:0]	RXD_[4:0]	TXCLK_[0]	RXCLK_[0]
Channel 1	TXD_[12:8]	RXD_[12:8]	TXCLK_[1]	RXCLK_[1]
Channel 2	TXD_[20:16]	RXD_[20:16]	TXCLK_[2]	RXCLK_[2]
Channel 3	TXD_[28:24]	RXD_[28:24]	TXCLK_[3]	RXCLK_[3]

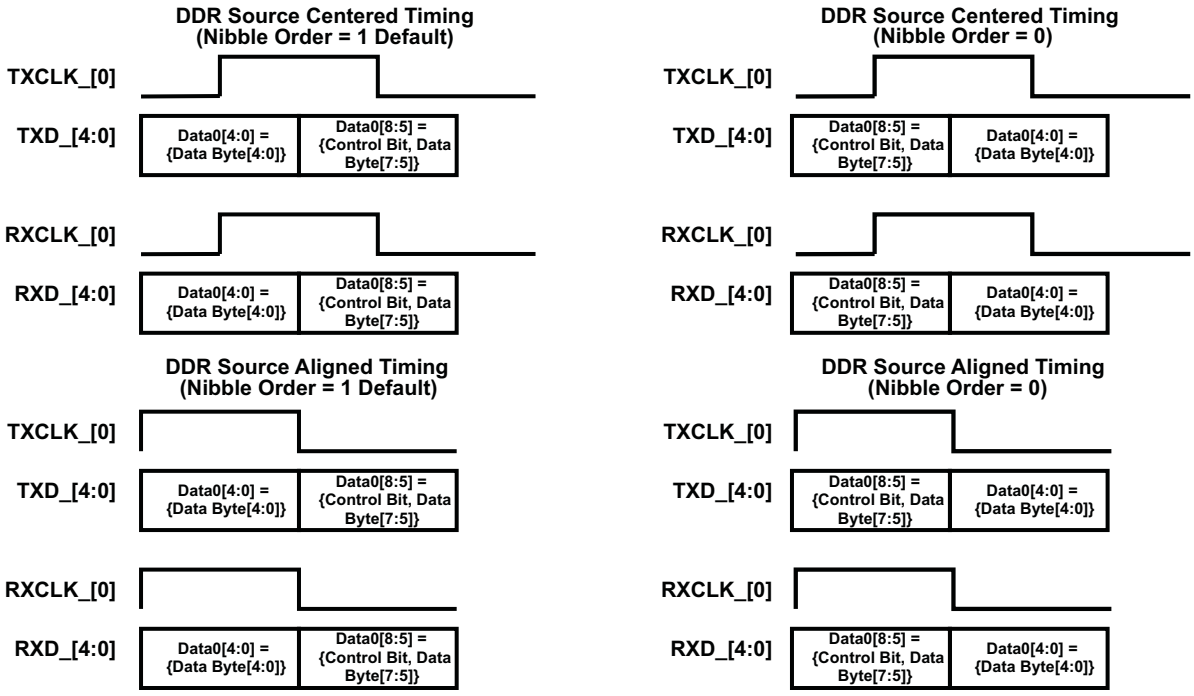


Figure 2-15. RNBI – Individual Channel Byte Ordering – Channel 0 Example

2.7.10 TBID Mode (Ten Bit Interface DDR)

Table 2-13. TBID – Lane To Functional Pin Mapping

DATA CHANNEL NUMBER	TRANSMIT DATA 10 BITS (INPUT)	RECEIVE DATA 10 BITS (OUTPUT)	TRANSMIT CLOCK (INPUT)	RECEIVE CLOCK (OUTPUT)
Channel 0	{TXC_[4], TXC_[0],TXD_[7:0]}	{RXC_[4], RXC_[0],RXD_[7:0]}	TXCLK_[0]	RXCLK_ [0]
Channel 1	{TXC_[5],TXC_[1],TXD_[15:8]}	{RXC_[5], RXC_[1],RXD_[15:8]}	TXCLK_[1]	RXCLK_ [1]
Channel 2	{TXC_[6],TXC_[2],TXD_[23:16]}	{RXC_[6],RXC_[2],RXD_[23:16]}	TXCLK_[2]	RXCLK_ [2]
Channel 3	{TXC_[7],TXC_[3],TXD_[31:24]}	{RXC_[7],RXC_[3],RXD_[31:24]}	TXCLK_[3]	RXCLK_ [3]

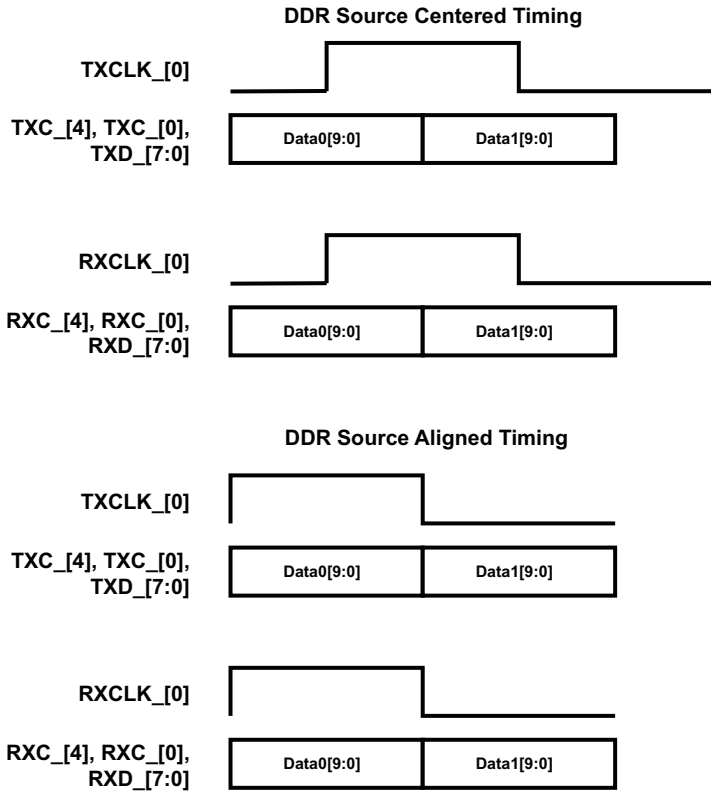


Figure 2-16. TBID – Individual Channel Byte Ordering – Channel 0 Example

2.7.11 NBID Mode (Nine Bit Interface DDR)

Table 2-14. NBID – Lane To Functional Pin Mapping

DATA CHANNEL NUMBER	TRANSMIT DATA 9 BITS (INPUT)	RECEIVE DATA 9 BITS (OUTPUT)	TRANSMIT CLOCK (INPUT)	RECEIVE CLOCK (OUTPUT)
Channel 0	{TXC_[0],TXD_[7:0]}	{RXC_[0],RXD_[7:0]}	TXCLK_[0]	RXCLK_ [0]
Channel 1	{TXC_[1],TXD_[15:8]}	{RXC_[1],RXD_[15:8]}	TXCLK_[1]	RXCLK_ [1]
Channel 2	{TXC_[2],TXD_[23:16]}	{RXC_[2],RXD_[23:16]}	TXCLK_[2]	RXCLK_ [2]
Channel 3	{TXC_[3],TXD_[31:24]}	{RXC_[3],RXD_[31:24]}	TXCLK_[3]	RXCLK_ [3]

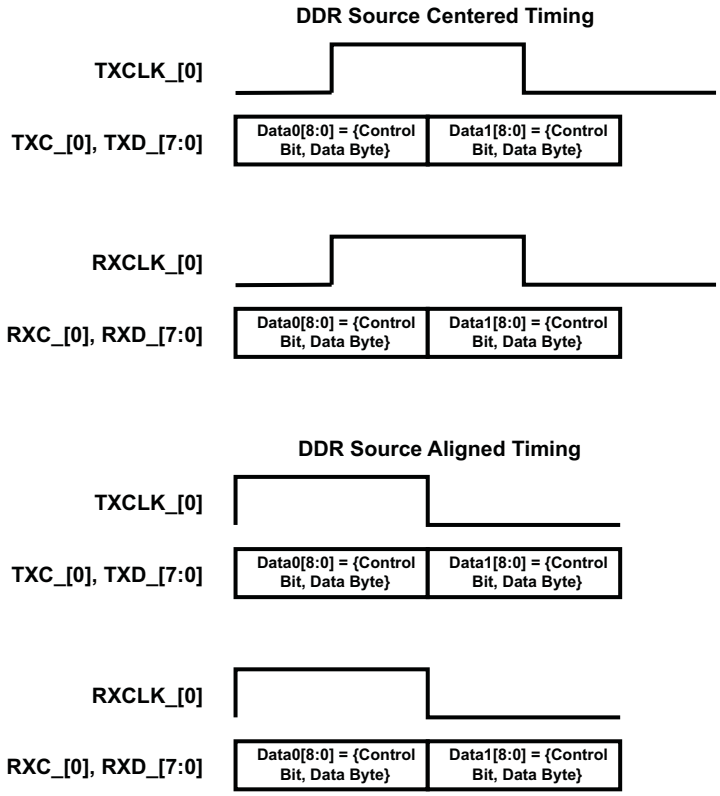


Figure 2-17. NBID – Individual Channel Byte Ordering – Channel 0 Example

2.7.12 Parallel Interface Clocking Modes

The TLK3134 supports source centered timing and source aligned DDR timing on the parallel receive output bus. TLK3134 also supports rising edge aligned and falling edge aligned SDR timing on the parallel receive output bus. See Figure 2-18 for more details.

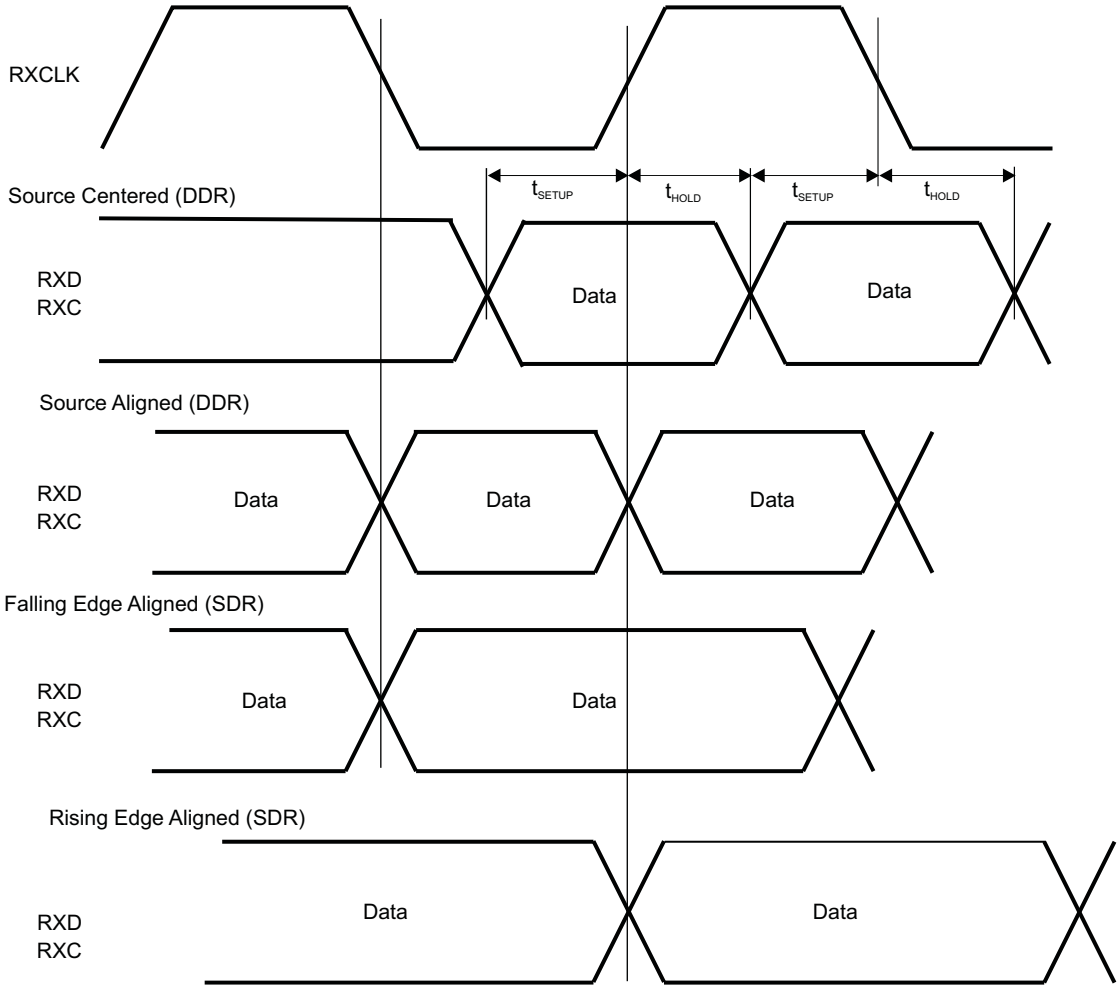


Figure 2-18. Receive Interface Timing – Source Centered/Aligned

The transmit input timing modes are shown in Figure 2-19.

In the receive data path a FIFO, placed on the output of the serial to parallel conversion logic for each serial link, compensates for channel skew, clock phase and frequency tolerance differences between the recovered clocks for each serial links and the receive output clock, RCLK.

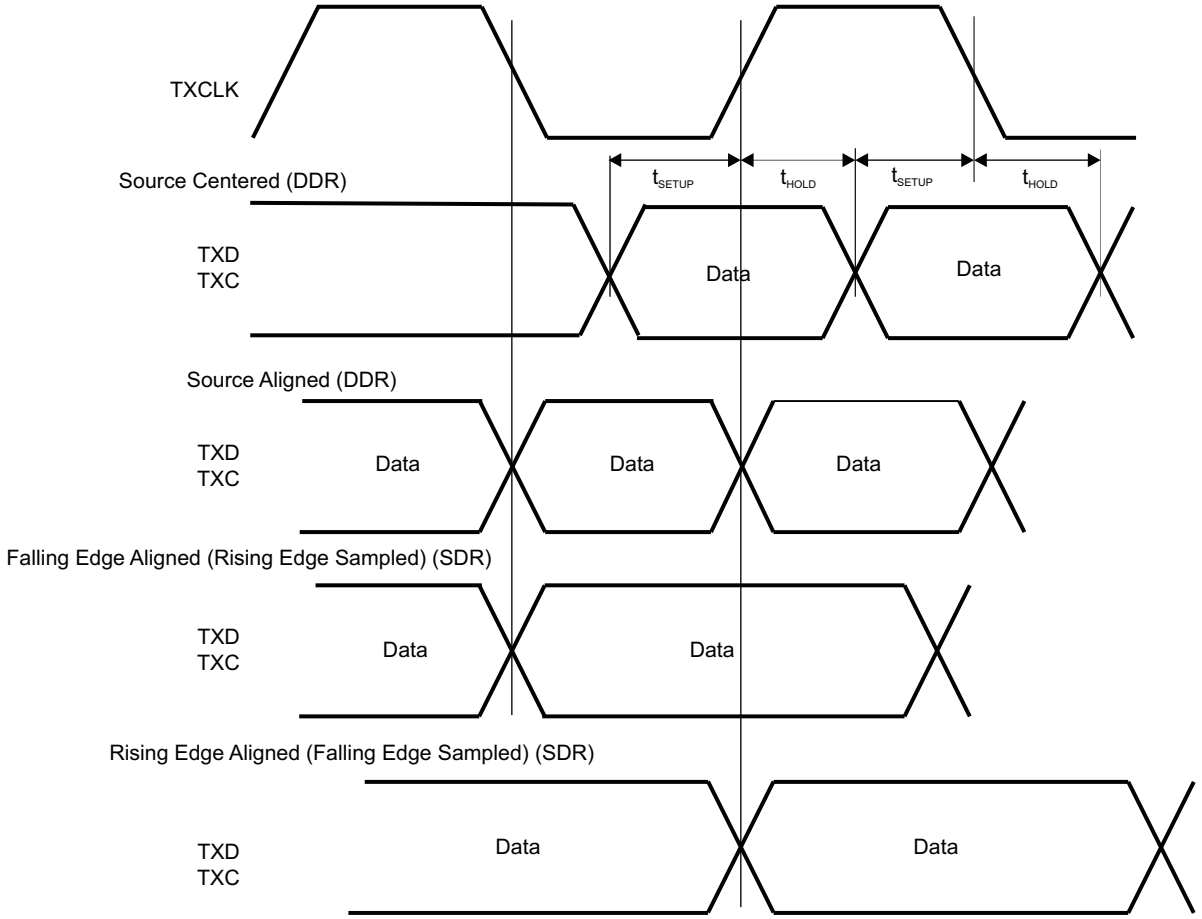


Figure 2-19. Transmit Interface Timing

2.7.13 Parallel Interface Data

Data placed on the XGMII transmit input bus is latched and then phase aligned to the internal version of the transmit reference clock, 8b/10b encoded, serialized, then transmitted sequentially beginning with the LSB of the encoded data byte over the differential high speed serial transmit pins.

The XGMII receive data bus outputs four bytes on RXD(31:0). Control character (K-characters) reporting for each byte is done by asserting the corresponding control pin, RXC(3:0). When RXC is asserted, the 8 bits of data corresponding to the control pin is to be interpreted as a K-character. If an error is uncovered in decoding the data, the control pin is asserted and 0xFE is output for the corresponding byte.

2.7.14 Transmission Latency

For each channel, the data transmission latency of the TLK3134 is defined as the delay from the rising or falling edge of the selected transmit clock when valid data is on the transmit data pins to the serial transmission of bit 0, as shown in Figure 2-20. The maximum transmit latency is a function of the mode of operation, and is detailed in Section 4.10: Serial Transmitter/Receiver characteristics.

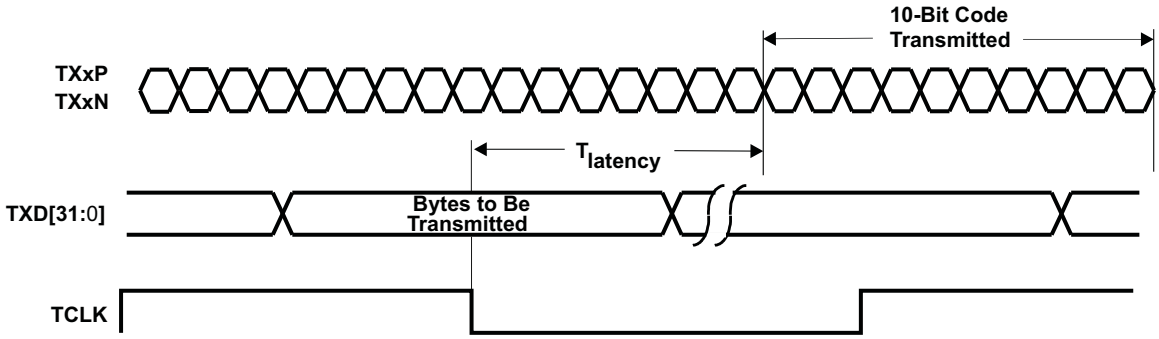


Figure 2-20. Transmission Latency

2.7.15 Channel Clock to Serial Transmit Clock Synchronization

In XAUI mode, the TLK3134 allows ±200 ppm difference between the serdes transmit reference on the XAUI side, versus the input TCLK on the XGMII side. There exists a FIFO capable of CTC operations, and has a depth of 32 locations (32 bits wide per location).

The reference clock and the transmit data clock(s) may be from a common source, but the design allows for up to ±200 ppm of frequency difference should the application require it.

NOTE

Note that there are no CTC operations in any of the independent channel modes.

2.7.16 Data Reception Latency

For each serial link, the serial-to-parallel data latency is the time from when the first bit arrives at the serial receiver input until it is output in the aligned parallel word on the XGMII, as shown in Figure 2-21. The maximum receive latency is a function of the mode of operation, and is detailed in Section 4.10: Serial Transmitter/Receiver characteristics.

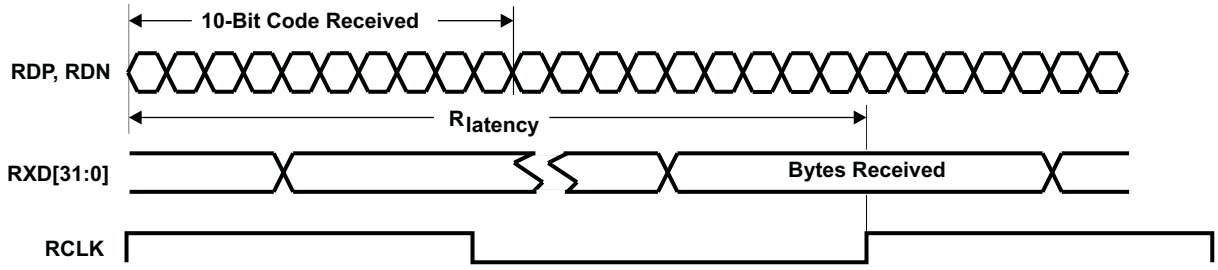


Figure 2-21. Receiver Latency

2.7.17 8B/10B Encoder

All true serial interfaces require a method of encoding to insure sufficient transition density for the receiving PLL to acquire and maintain lock. The encoding scheme also maintains the signal DC balance by keeping the number of ones and zeros balanced which allows for AC coupled data transmission. The TLK3134 uses the 8B/10B encoding algorithm that is used by 10Gbps and 1Gbps Ethernet and FibreChannel standards. This provides good transition density for clock recovery and improves error checking. The TLK3134 will internally encode and decode the data such that the user reads and writes actual 8-bit data on each channel. The encoder and decoder functions can optionally be enabled or disabled on a per channel basis.

The 8B/10B encoder converts 8-bit wide data to a 10-bit wide encoded data character to improve its transition density. This transmission code includes D Characters, used for transmitting data, and K Characters, used for transmitting protocol information. Each K or D character code word can also have both a positive and a negative disparity version. The disparity of a code word is selected by the encoder to balance the running disparity of the serialized data stream.

The generation of K-characters to be transmitted on each channel is controlled by transmit control pins, TXC(3:0). When the control pin is asserted along with the 8 bits of data, an 8B/10B K-character is transmitted. Similarly, reception of K-characters is reported by the receive control pins, RXC(3:0). When receive control pin is asserted, the corresponding byte on the receive data bus should be interpreted as a K-character. The TLK3134 will transmit and receive all of the twelve valid K-characters as defined in Table 2-15.

Table 2-15. Valid K-Codes

K-CODE	TXC(3:0) OR RXC(3:0)	DATA BUS BYTES (RXD[x: x-7] OR TXD[x: x-7])	ENCODED K-CODE		K-CODE DESCRIPTION
			NEGATIVE RUNNING DISPARITY	POSITIVE RUNNING DISPARITY	
00 through FF	0	DDD DDDDD	dddddd dddd	dddddd dddd	Normal data
K28.0	1	000 11100	001111 0100	110000 1011	IdleO/busy
K28.1	1	001 11100	001111 1001	110000 0110	IdleE/busy
K28.2	1	010 11100	001111 0101	110000 1010	
K28.3	1	011 11100	001111 0011	110000 1100	Channel Alignment (A)
K28.4	1	100 11100	001111 0010	110000 1101	
K28.5	1	101 11100	001111 1010	110000 0101	IdleE/not-busy (K)
K28.6	1	110 11100	001111 0110	110000 1001	
K28.7	1	111 11100	001111 1000	110000 0111	Code Violation or Parity Error
K23.7	1	111 10111	111010 1000	000101 0111	IdleO/not-busy
K27.7	1	111 11011	110110 1000	001001 0111	SOP(S)
K29.7	1	111 11101	101110 1000	010001 0111	EOP(T)
K30.7	1	111 11110	011110 1000	100001 0111	

Table 2-16 provides additional transmit data control coding and descriptions that have been incorporated into 10 Gbps Ethernet. Data patterns put on XGMII transmit data bus other than those defined in Table 2-16 when the transmit control pin is asserted will result in an invalid K-character being transmitted which will result in a code error at the receiver.

Table 2-16. Valid XGMII Channel Encodings

DATA BUS (TXD[x: x-7] OR RXD[x: x-7])	TXC(3:0) OR RXC(3:0)	DESCRIPTION
00 through FF	0	Normal Data Transmission
00 through 06	1	Reserved
07	1	Idle
08 through 9B	1	Reserved
9C	1	Sequence (only valid in Channel 0)
9D through FA	1	Reserved
FB	1	Start (only valid in Channel 0)
FC	1	Reserved
FD	1	Terminate
FE	1	Transmit error propagation

Table 2-16. Valid XGMII Channel Encodings (continued)

DATA BUS (TXD[x: x-7] OR RXD[x: x-7])	TXC(3:0) OR RXC(3:0)	DESCRIPTION
FF	1	Reserved

2.7.18 Comma Detect and 8B/10B Decoding

When parallel data is clocked into a parallel to serial converter, the byte boundary that was associated with the parallel data is lost in the serialization of the data. When the serial data is received and converted to parallel format again, a method is needed to be able to recognize the byte boundary again. Generally this is accomplished through the use of a synchronization pattern. This is a unique pattern of 1's and 0's that either cannot occur as part of valid data or is a pattern that repeats at defined intervals. 8B/10B encoding contains a character called the comma (b'0011111 or b'1100000) which is used by the comma detect circuit to align the received serial data back to its original byte boundary. The channel synchronization block detects the comma pattern found in the K28.5 character, generating a synchronization signal aligning the data to their 10-bit boundaries for decoding. It then converts the data back into 8-bit data. It is important to note that the comma can be either a (b'0011111) or the inverse (b'1100000) depending on the running disparity. The TLK3134 decoder will detect both patterns.

The reception of K-characters is reported by the assertion of receive control pin, RXC(3:0) for the corresponding byte on the XGMII receive bus. When a code word error or running disparity error is detected in the decoded data received on a serial link, the receive control pin is asserted and an 0xFE is placed on the receive data bus for that channel, as shown in Table 2-17.

Table 2-17. Receive Data Controls

EVENT	RECEIVE DATA BUS RXD[x:x–7]	RXC(3:0)
Normal Data	XX	0
Normal K-character	Valid K-code	1
Code word error or running disparity error	FE	1

2.7.19 Channel Initialization and Synchronization

The TLK3134 has a synchronization state machine which is responsible for handling link initialization and synchronization for each channel. The initialization and synchronization state diagram is provided in Figure 2-22. The status of any channel can be monitored by reading MDIO register 4/5.24.3:0.

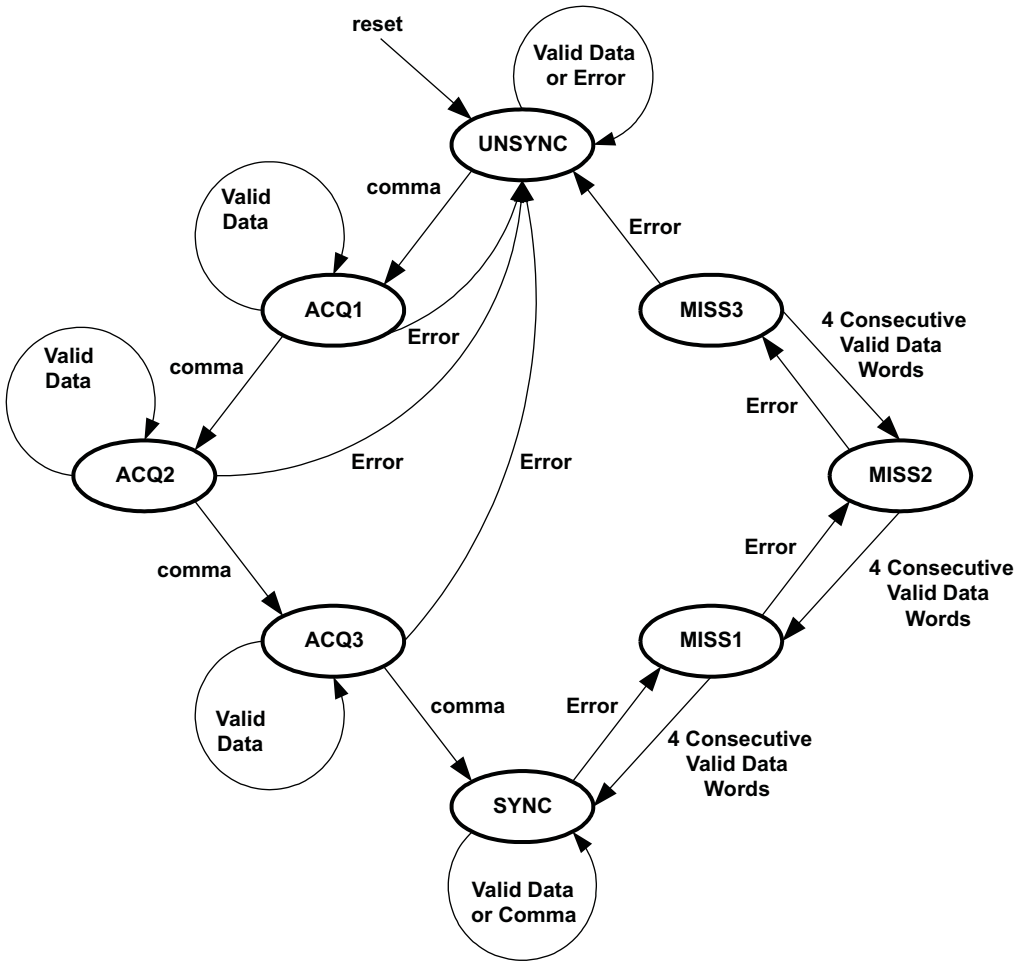


Figure 2-22. Channel Synchronization State Machine

2.7.20 Channel State Descriptions:

UNSYNC This is the initial state for each channel upon device power up or reset. In this state, the TLK3134 will have the comma detect circuit active and will make code word alignment adjustments based on the position of a comma in the incoming data stream. While in this state the TLK3134 will set the Lane Sync bit to '0' for the particular channel in MDIO register bits 4/5.24.3:0 indicating the lane is not synchronized.(1) The channel state will transition to the ACQ1 state upon the detection of a comma.

ACQ1 During this state the comma detect circuit is active but code word re-alignment is disabled. The TLK3134 will remain in this state until either a comma is detected in the same code word alignment position as found in state UNSYNC or a decode error is encountered. While in this state, the Lane Sync bit for the particular channel will remain de-asserted indicating the lane is not synchronized.(1) A decode or running disparity error will return the channel state to UNSYNC. A detected comma will cause the channel state to transition to ACQ2.

ACQ2 During this state, the comma detect circuit is active but code word re-alignment is disabled. The TLK3134 will remain in this state until either a comma is detected in the same code word alignment position as found in state UNSYNC or a decode error is encountered. While in this state, the Lane Sync bit for the particular channel will remain de-asserted indicating the lane is not synchronized.(1) A decode or running disparity error will return the channel state to UNSYNC. A detected comma will cause the channel state to transition to ACQ3.

(1) The Lane Sync bit = '0' bit from any/or all channels will cause a local fault to be output on the receive data bus.

ACQ3 During this state the comma detect circuit is active but code word re-alignment is disabled. The TLK3134 will remain in this state until either a comma is detected or a decode error encountered. While in this state, the Lane Sync bit for the particular channel will remain de-asserted indicating the lane is not synchronized.(1) A decode or running disparity error will return the channel state to UNSYNC. A detected comma will cause the channel state to transition to SYNC.

SYNC This is the normal state for receiving data. When in this state, the TLK3134 will set the Lane Sync bit to '1' for the particular channel in the MDIO register bits 4/5.24.3:0 indicating the lane has been synchronized. During this state the comma detect circuit is active but code word re-alignment is disabled. A decode or running disparity error will cause the channel state to transition to MISS1.

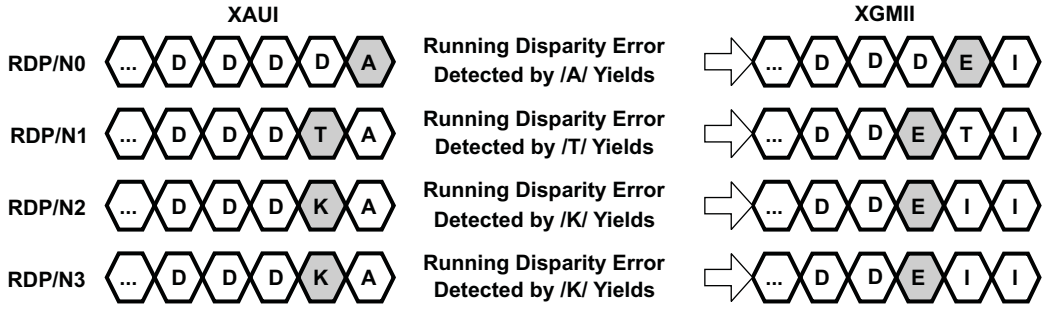
MISS1 When entering this state an internal error counter is cleared. If the next four consecutive codes are decoded without error, the channel state reverts back to SYNC. If a decode or running disparity error is detected, the channel state will transition to MISS2.

MISS2 When entering this state an internal error counter is cleared. If the next four consecutive codes are decoded without error, the channel state reverts back to MISS1. If a decode or running disparity error is detected, the channel state will transition to MISS3.

MISS3 When entering this state an internal error counter is cleared. If the next four consecutive codes are decoded without error, the channel state reverts back to MISS2. If a decode or running disparity error is detected, the channel state will transition to UNSYNC.

2.7.21 End of Packet Error Detection

Because of their unique data patterns, /A/ (K28.3), /K/ (K28.5), and /T/ (K29.7) will catch running disparity errors that may have propagated undetected from previous codes in a packet. Running disparity errors detected by these control codes at the end of packets will cause the previous data codes to be reported as errors (0xFE) to allow the protocol device to reject the packet (see Figure 2-23).



D = Data, T = K29.7, A = K28.3, K = K28.5, E = Error (0xFE), I = Idle

Figure 2-23. End of Packet Error Detection

2.7.22 Fault Detection and Reporting

The TLK3134 will detect and report local faults as well as forward both local and remote faults as defined in the IEEE 802.3ae 10Gbps Ethernet Standard to aid in fault diagnosis. All faults detected by the TLK3134 are reported as local faults to the upper layer protocols. Once a local fault is detected in the TLK3134, MDIO register bit 4/5.1.7 is set. Fault sequences, sequence ordered sets received by the TLK3134, either on the Transmit Data Bus or on the high speed receiver pins, are forwarded without change to the MDIO registers in the TLK3134. Also, note that the TLK3134 is capable of performing CTC operation where only RF and LF or any Q sequences are transported (not generated) in either the transmit or receive direction in XAUI mode.

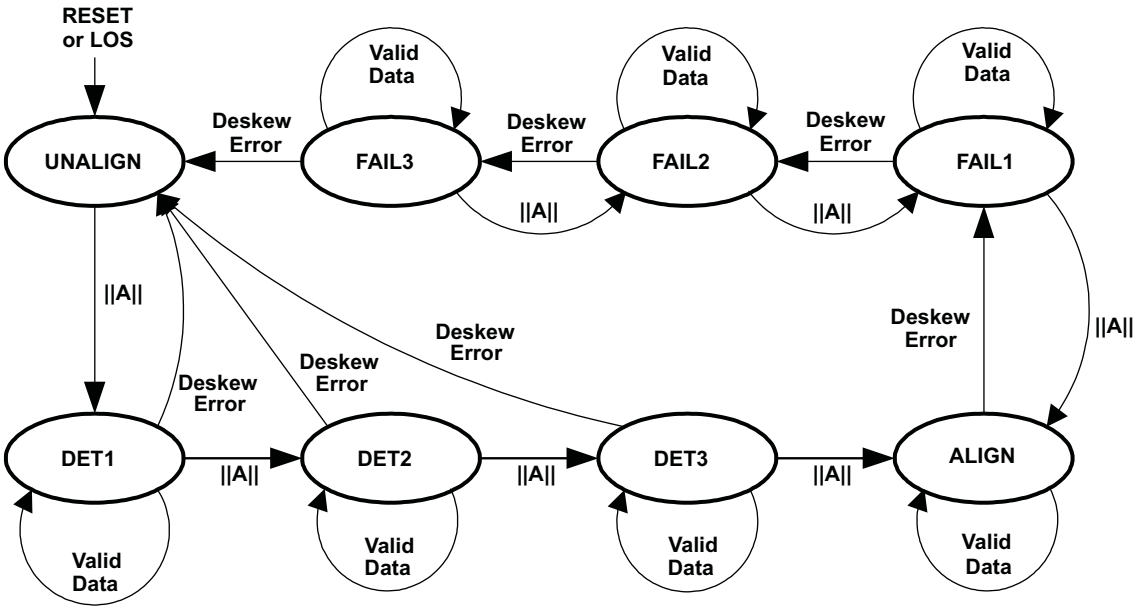
TLK3134 reports a fault by outputting a K28.4 (0x9C) on RXD(7:0), 0x00 on RXD(15:8) and RXD(23:16) and 0x01 for local faults on RXD(31:24). Forwarding of remote faults is handled as a normal transmission. Note that the TLK3134 will not generate a remote fault indication nor any other type of Q.

2.7.23 Receive Synchronization and Skew Compensation

In XAUI mode, the TLK3134 has a FIFO enabled on the receive data path coming from each serial link to compensate for channel skew and clock phase and frequency tolerance differences between the recovered clocks for each channel and the receive output clock RCLK. This FIFO has a depth of 16 locations (32 bits wide for each location).

The de-skew of the 4 serial links that make up each XAUI channel into a single 32 bit wide column of data is accomplished by alignment of the receive FIFOs on each serial link to a K28.3 control code sent during the inter-packet gap (IPG) between data packets or during initial link synchronization. Until the alignment code is recognized by the CTC FIFOs, the output of the FIFOs may be un-aligned and as such undefined, as shown in Figure 2-25. The K28.3 code (referred to as the “A” or alignment code) is transmitted on the first column following the end of the data packet as shown in Figure 2-26.

The column de-skew state machine is provided in Figure 2-24 . The status of column alignment can be monitored by reading MDIO registers 4/5.24.12 for global alignment.



Note: Deskew Error is at least one column containing an A character, but not all four simultaneously.

Figure 2-24. Column De-Skew State Machine

2.7.24 Column State Descriptions:

UNALIGN This is the initial state for the column state machine upon device power up or reset. If any of the channel state machines are set to UNSYNC, the column state is set to UNALIGN. In this state, the column state machine will search for alignment character codes (K28.3 or /A/) on each channel and align the FIFO pointers on each channel to the /A/ character code. While in this state, the Column Alignment Sync bit is set to '0' in MDIO registers 4/5.24.12, indicating the column is not aligned.(2) The column state will transition to the DET1 state upon the detection and alignment of /A/ character codes in all four channels.

DET1 During this state, the alignment character code detect circuit is active on each channel but the column re-alignment is disabled. The column state machine will remain in this state looking for a column of alignment character codes. If an incomplete alignment column is detected (alignment character codes not found on all channels) or a deskew error is detected, the column state machine will transition to state UNALIGN. While in this state, the Column Alignment Sync bit is set to '0' in MDIO registers 4/5.24.12 indicating the column is not aligned.(2) Detection of a complete alignment column will cause the column state machine to transition to state DET2.

DET2 During this state, the alignment character code detect circuit is active on each channel but the column re-alignment is disabled. The column state machine will remain in this state looking for a column of alignment character codes. If an incomplete alignment column is detected (alignment character codes not found on all channels) or a deskew error is detected, the column state machine will transition to state UNALIGN. While in this state, the Column Alignment Sync bit is set to '0' in MDIO registers 4/5.24.12 indicating the column is not aligned.(2) Detection of a complete alignment column will cause the column state machine to transition to state DET3.

DET3 During this state, the alignment character code detect circuit is active on each channel but the column re-alignment is disabled. The column state machine will remain in this state looking for a column of alignment character codes. If an incomplete alignment column is detected (alignment character codes not found on all channels) or a deskew error is detected, the column state machine will transition to state UNALIGN. While in this state, the Column Alignment Sync bit is set to '0' in MDIO registers 4/5.24.12 indicating the column is not aligned.(2) Detection of a complete alignment column will cause the column state machine to transition to state ALIGN.

ALIGN This is the normal state for receiving data. When in this state, the column state machine will set the Column Alignment Sync bit to '1' in MDIO registers 4/5.24.12 indicating all channels are aligned. During this state the alignment character code detect circuit is active on each channel but the column re-alignment is disabled. If a deskew error is detected in the correct position within the Inter-Packet Gap, the column state machine will transition to state FAIL1.

FAIL1 When in this state, the Column Alignment Sync bit is '1' in MDIO registers 4/5.24.12. During this state the alignment character code detect circuit is active on each channel but the column re-alignment is disabled. If a complete alignment column is not detected in the correct position within the Inter-Packet Gap, the column state machine will transition to state FAIL2. If a complete alignment column is detected in the correct position within the Inter-Packet Gap, the column state machine will transition to state ALIGN.

FAIL2 When in this state, the Column Alignment Sync bit is '1' in MDIO registers 4/5.24.12. During this state the alignment character code detect circuit is active on each channel but the column re-alignment is disabled. If a complete alignment column is not detected in the correct position within the Inter-Packet Gap, the column state machine will transition to state FAIL3. If a complete alignment column is detected in the correct position within the Inter-Packet Gap, the column state machine will transition to state FAIL1.

(2) The XGXS Lane Alignment bit = '0' will cause a local fault to be output on the receive data bus.

FAIL3 When in this state, the Column Alignment Sync bit is '1' in MDIO registers 4/5.24.12. During this state the alignment character code detect circuit is active on each channel but the column re-alignment is disabled. If complete alignment column is not detected in the correct position within the Inter-Packet Gap, the column state machine will transition to state UNALIGN. If a complete alignment column is detected in the correct position within the Inter-Packet Gap, the column state machine will transition to state FAIL2.

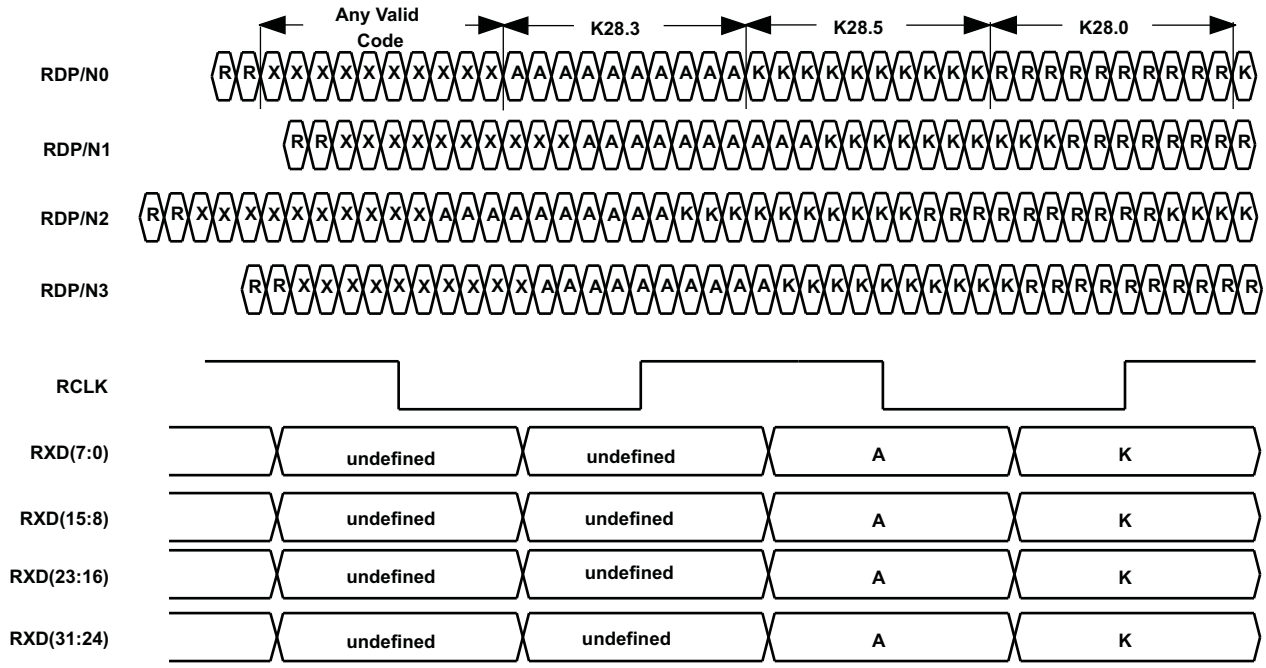


Figure 2-25. Channel Deskew Using Alignment Code

2.7.25 Inter-Packet Gap Management

When in XAUI mode, the TLK3134 replaces the idle codes (see Table 2-15) during the Inter-Packet Gap (IPG) with the necessary codes to perform all channel alignment, byte alignment, and clock tolerance compensation as defined in IEEE 802.3ae 10Gbps Ethernet Standard. According to the Ethernet Standard, a valid packet must begin on TXD(7:0) of the XGMII. However, due to variable packet sizes, the IPG can begin on any channel. The TLK3134 will replace idle codes latched on the same XGMII clock edge as the end of packet code with /K/ codes (as shown in Figure 2-26).

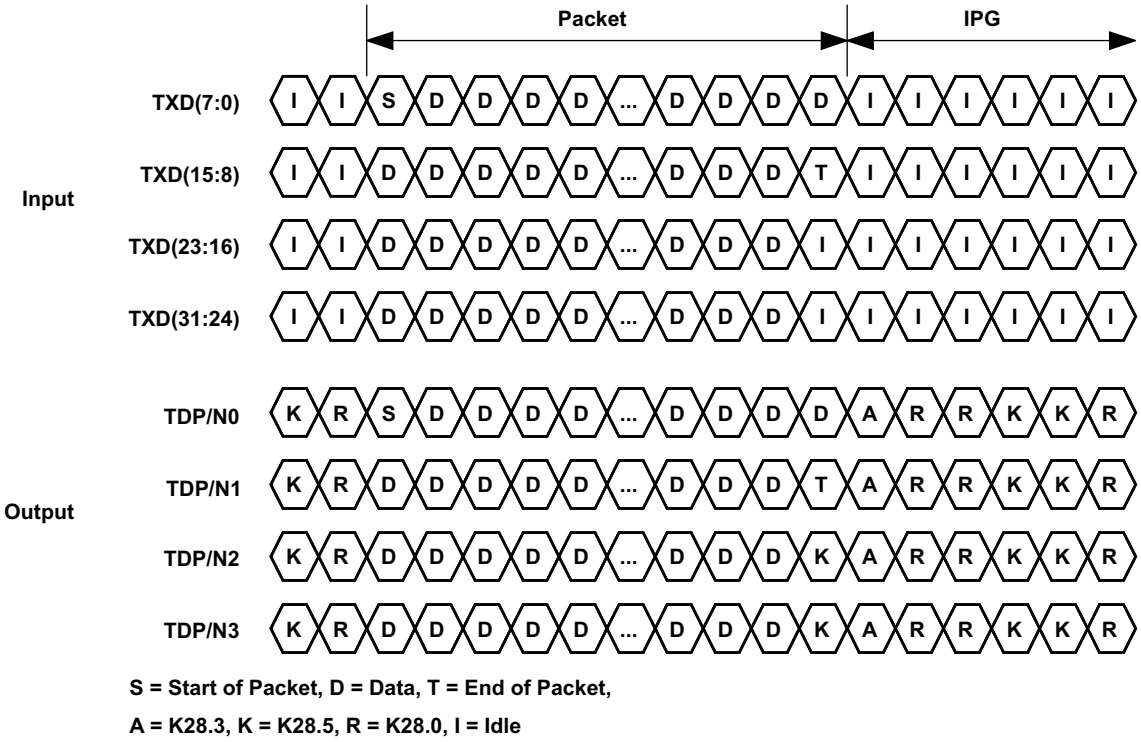


Figure 2-26. Inter-Packet Gap Management

The subsequent idles in the IPG will be replaced by “columns” of channel alignment codes (K28.3), byte alignment codes (K28.5), or clock tolerance compensation codes (K28.0). The state machine which governs the IPG replacement procedure is illustrated in Figure 2-27, with notation defined in Table 2-18. Note that any IPG management state will transition to send data if the IPG is terminated.

The repetition of the “/A/” pattern on each serial channel allows the FIFOs to remove or add the required phase and frequency difference to align the data from all four serial links of a XAUI channel and allow output of the aligned 32 bit wide data on a single edge of the receive clock, RCLK, as shown in Figure 2-25.

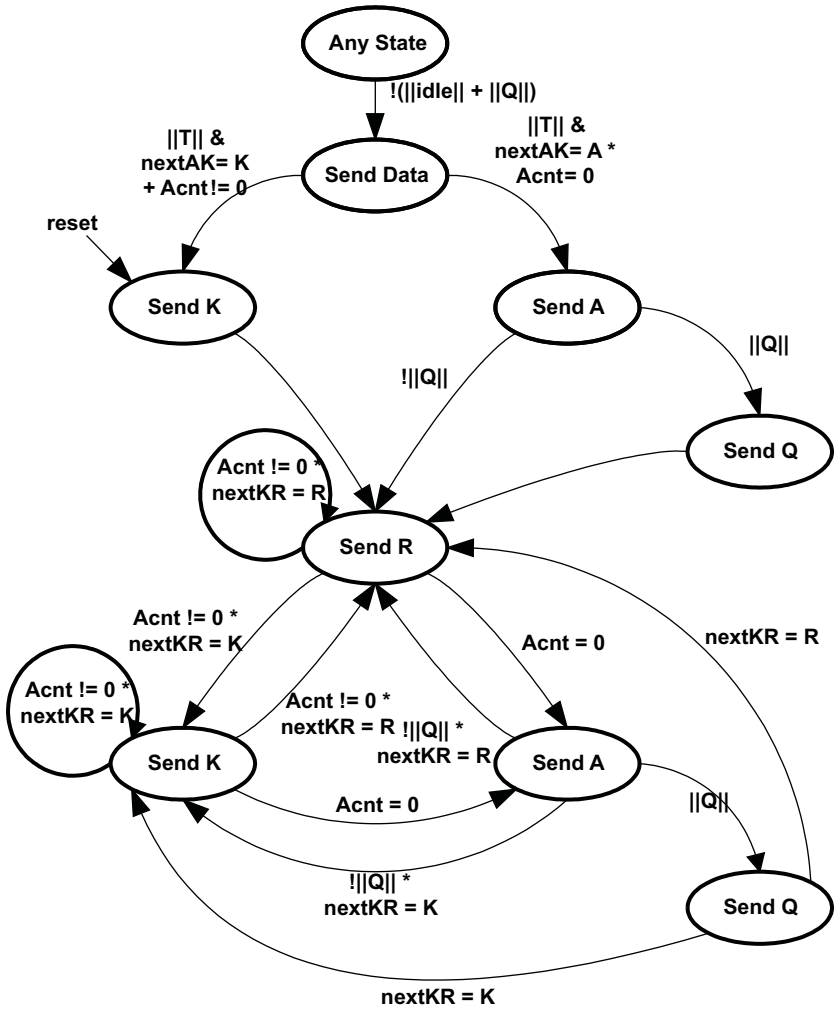


Figure 2-27. IPG Management State Machine

Table 2-18. IPG Management State Machine Notation

SYMBOL	DEFINITION
||idle||	XGMII idle. 0x07 on TXD(x:: :x-7),
||Q||	Link status message: K28.4, Dx.y, Dx.y, Dx.y.
nextAK	A Boolean variable. It takes the value K when an A is sent at the beginning of the IPG and the value A when a K is sent at the beginning of the IPG. Its initial value is K.
Acnt	When an A character is sent, variable Acnt is loaded with a random number such that 16 ≤ Acnt ≤ 31. Acnt is decremented each time a column of A characters is generated.
nextKR	A randomly-generated Boolean that can assume the value K or R.
||T||	Terminate Character Column (Terminate Character in Any Lane).

2.7.26 Clock Tolerance Compensation (CTC)

The XAUI interface is defined to allow for separate clock domains on each side of the link. Though the reference clocks for two devices on a XAUI link have the same specified frequencies, there are slight differences that, if not compensated for, will lead to over or under run of the FIFOs on the receive/transmit data path. The TLK3134 provides compensation for these differences in clock frequencies via the insertion or the removal of /R/ characters on all channels, as shown in Figure 2-28 and Figure 2-29.

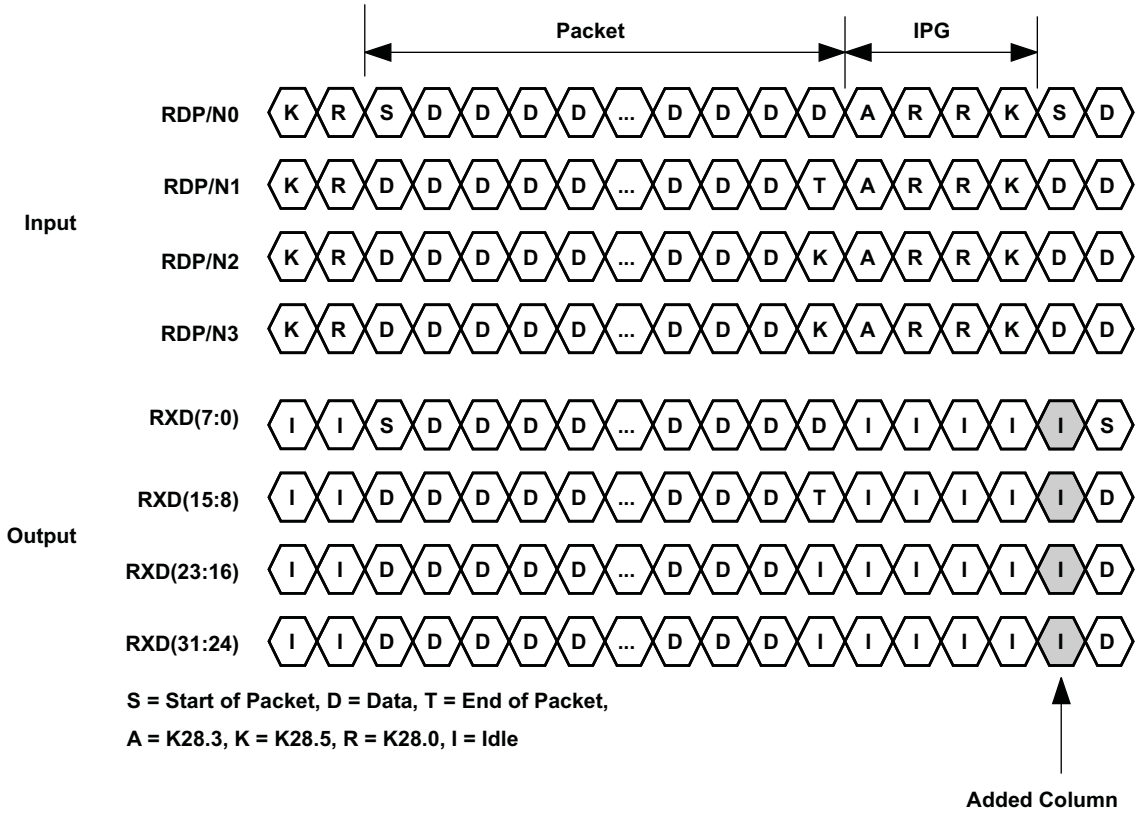


Figure 2-28. Clock Tolerance Compensation: Add

The /R/ code is disparity neutral, allowing its removal or insertion without affecting the current running disparity of each channel's serial stream.

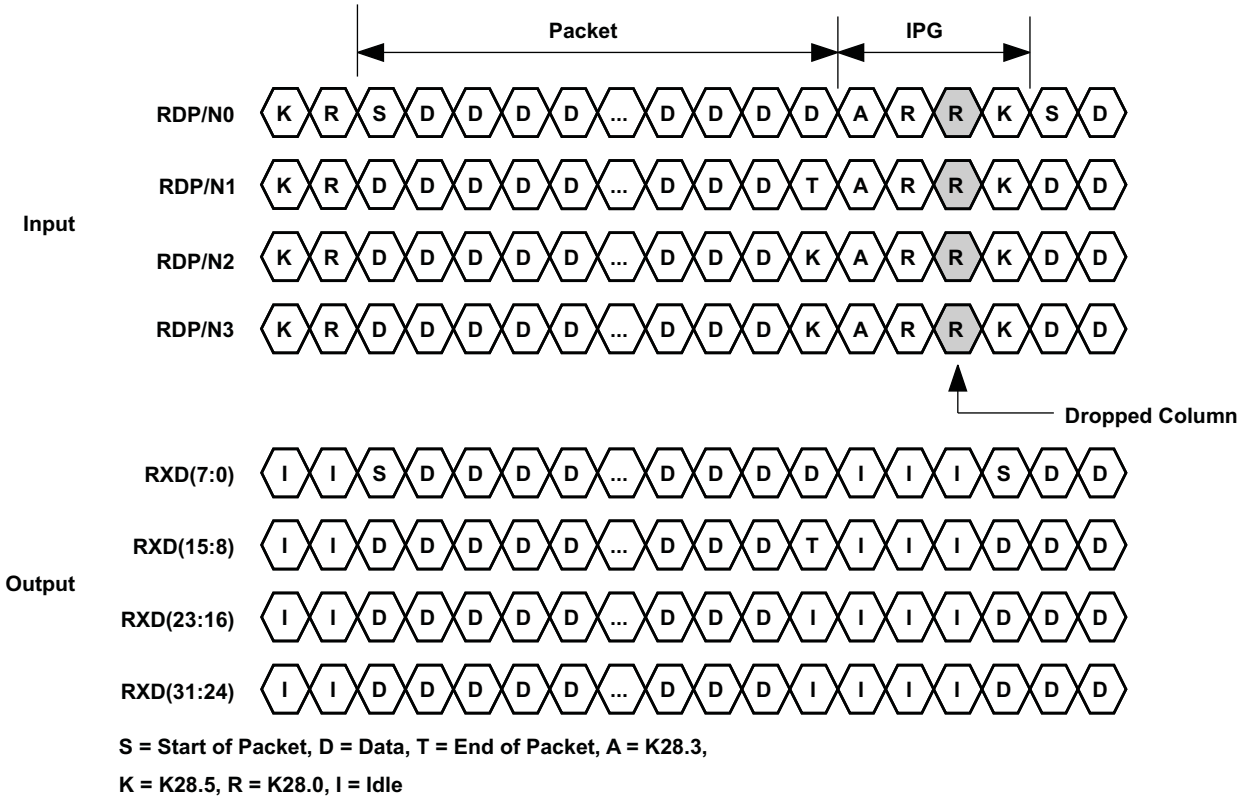


Figure 2-29. Clock Tolerance Compensation: Drop

2.7.27 Parallel to Serial

The parallel-to-serial shift register on each channel takes in data and converts it to a serial stream. The shift register is clocked by the internally generated bit clock, which is 10 times the reference clock (REFCLKP/REFCLKN) frequency. The least significant bit (LSB) for each channel is transmitted first.

2.7.28 Serial to Parallel

For each channel, serial data is received on the RDPx/RDNx pins. The interpolator and clock recovery circuit will lock to the data stream if the clock to be recovered is within ±200 PPM of the internally generated bit rate clock. The recovered clock is used to retime the input data stream. The serial data is then clocked into the serial-to-parallel shift registers. If enabled, the 10-bit wide parallel data is then fed into 8b/10b decoders.

2.7.29 High Speed CML Output

The high speed data output driver is implemented using Current Mode Logic (CML) with integrated pull up resistors requires no external components. The line can be directly coupled or AC coupled. Under many circumstances, AC coupling is desirable.

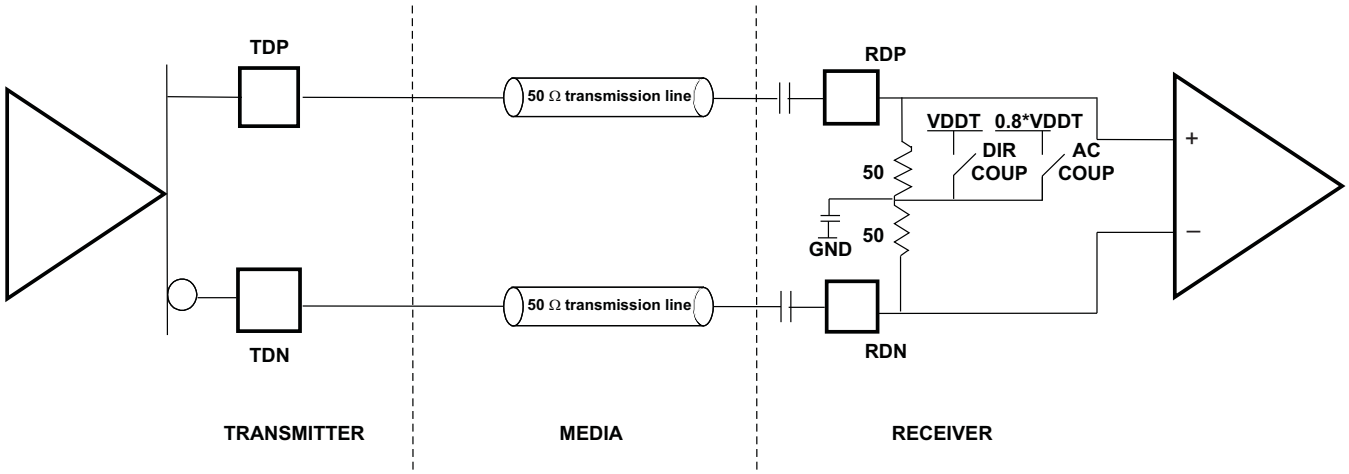


Figure 2-30. Example High Speed I/O AC Coupled Mode

Current Mode Logic (CML) drivers often require external components. The disadvantage of the external component is a limited edge rate due to package and line parasitic. The CML driver on TLK3134 has on-chip 50Ω termination resistors terminated to VDDT, providing optimum performance for increased speed requirements. The transmitter output driver is highly configurable allowing output amplitude and de-emphasis to be tuned to a channel's individual requirements. Software programmability allows for very flexible output amplitude control. AC Coupled and Direct Coupled modes are supported. When AC coupling is selected, the receiver input is internally biased 0.8 × VDDT which is the optimum voltage for input sensitivity. As the input and output references are derived from VDDT, the tolerance of this supply will dominate the accuracy of the internal reference.

When transmitting data across long lengths of PCB trace or cable, the high frequency content of the signal is attenuated due to the skin effect of the media. This causes a “smearing” of the data eye when viewed on an oscilloscope. The net result is reduced timing margins for the receiver and clock recovery circuits. In order to provide equalization for the high frequency loss, 1-tap finite impulse response (FIR) transmit de-emphasis is implemented. A highly configurable output driver maximizes flexibility in the end system by allowing de-emphasis and output amplitude to be tuned to a channel’s individual requirements. A total of 15 de-emphasis settings and 8 output amplitude settings can be independently selected.

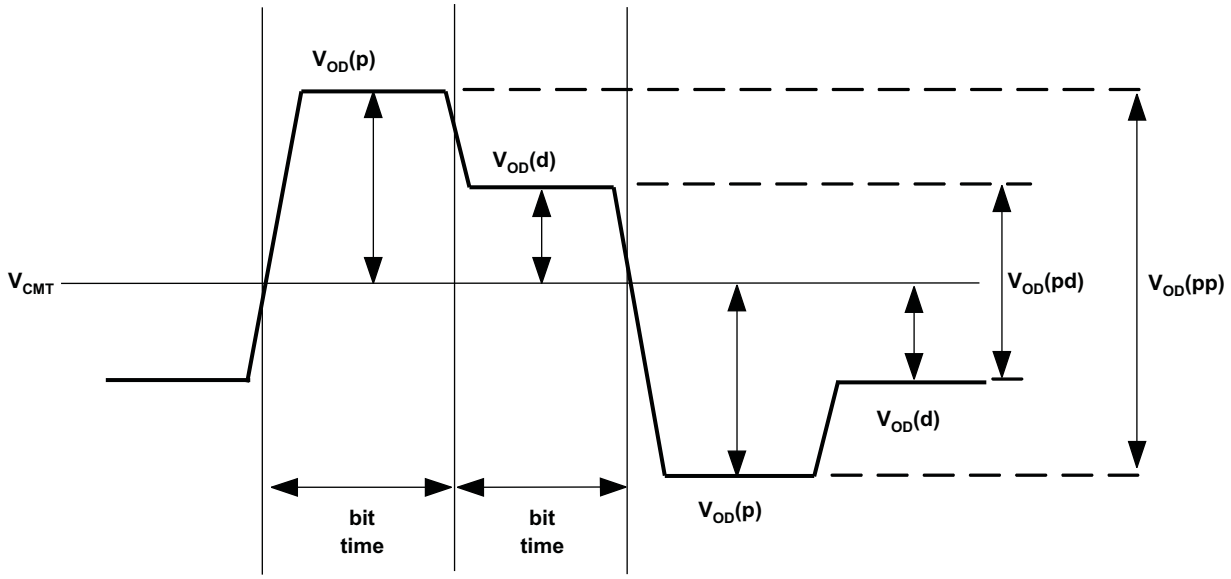


Figure 2-31. Output differential voltage with 1-tap FIR de-emphasis

The level of de-emphasis is programmable via MDIO Register bits. Users can control the strength of the de-emphasis to optimize for a specific system requirement.

2.7.30 High Speed Receiver

The high speed receiver conforms to the physical layer requirements of IEEE 802.3ae Clause 47(XAUI), Gigabit Ethernet, and FibreChannel 1 and 2. Register control gives selection between AC and DC coupling at the receiver. When the receiver is AC coupled, the termination impedances of the receivers are configured as 100 Ohms with the center tap weakly tied to 0.8 × VDDT with a capacitor to create an AC ground. When the receiver is DC coupled, the common mode will be determined by both receiver and transmitter characteristics.

All receive channels incorporate an adaptive equalizer. This circuit compensates for channel insertion loss by amplifying the high frequency components of the signal, reducing inter-symbol interference. Equalization can be enabled or disabled per register settings. Both the gain and bandwidth of the equalizer are controlled by the receiver equalization logic. There are ten available equalization settings.

2.7.31 Loopback

In XAUI Mode, two internal loopback modes are possible for the XAUI Channel Group. One, called XGMII loopback, allows the data input on the XGMII interface to be returned out the XGMII interface. The other, called XAUI loopback, allows serial data on the XAUI interface to be returned out the XAUI interface.

In independent channel mode, channels can independently be configured for parallel or serial side loopback similar to above.

An external loopback (requiring external connection) is also supported, which can be used with the PRBS patterns, as well as the CJPAT, CRPAT, Mixed/High/Low Frequency tests.

2.7.32 Link Test Functions

The TLK3134 has an extensive suite of built in test functions to support system diagnostic requirements. Each channel has built-in link test generator and verification logic. Several patterns can be selected via the MDIO that offer extensive test coverage. The patterns are: 2^7-1 or 2^{23}-1 PRBS (Pseudo Random Bit Stream), CJPAT, CRPAT, high and low and mixed frequency patterns.

2.7.33 MDIO Management Interface

The TLK3134 supports the Management Data Input/Output (MDIO) Interface as defined in Clauses 22 and 45 of the IEEE 802.3ae Ethernet specification. The MDIO allows register-based management and control of the serial links. Normal operation of the TLK3134 is possible without use of this interface. However, some additional features are accessible only through the MDIO.

The MDIO Management Interface consists of a bi-directional data path (MDIO) and a clock reference (MDC). The device id and port address are determined by control pins (see Table 3-3). Also, whether the device responds as a Clause 22 or Clause 45 device is also determined by control pin ST (see Table 3-3).

In Clause 45 (ST = 0), the top 4 control pins PRTAD[4:1] determine the device port address. Note that TLK3134 can accessed only through even port addresses in Clause 45 mode. In this mode, TLK3134 will respond if the PHY address field on the MDIO protocol (PA[4:0]) matches {PRTAD[4:1], 1'b0}. PRTAD[0] pin acts as device id pin where it determines whether TLK3134 is a DTE or PHY device. The device ID is required to be either 4 (PHY) or 5 (DTE), so only one bit is required to differentiate. If PRTAD[0] is a 0, then a PHY device is selected for the XGXS. If PRTAD[0] is a 1, then a DTE device is selected for the XGXS. In this mode, TLK3134 will respond as PHY if the Device address field (DA[4:0]) on the MDIO protocol is 5'b00100 and as DTE if it is 5'b00101. Note, each register is accessed as either DTE or PHY devices in the TLK3134, although physically there is only one register accessed two different ways.

In Clause 22 (ST = 1), the top 3 control pins PRTAD[4:2] determine the device port address. In this mode the 4 individual channels in TLK3134 are classified as 4 different ports. So for any PRTAD[4:2] value there will be 4 ports per TLK3134. TLK3134 will respond if the 3 MSB's of PHY address field on MDIO protocol (PA[4:2]) matches PRTAD[4:2]. 2 LSB's of PHY address field (PA[1:0]) will determine which channel/port within TLK3134 to respond.

If PA[1:0] = 2'b00, TLK3134 Channel 0 will respond.

If PA[1:0] = 2'b01, TLK3134 Channel 1 will respond.

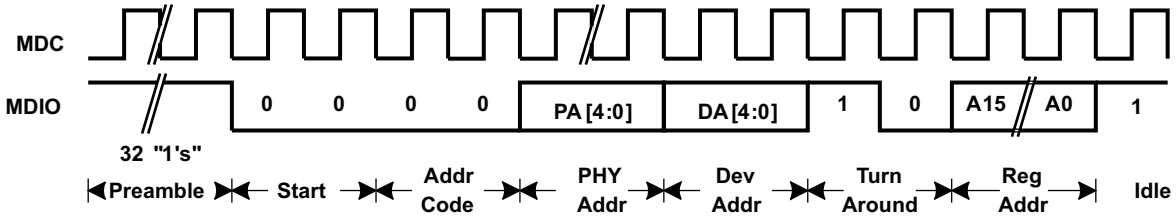
If PA[1:0] = 2'b10, TLK3134 Channel 2 will respond.

If PA[1:0] = 2'b11, TLK3134 Channel 3 will respond.

Write transactions which address an invalid register or device or a read only register will be ignored. Read transactions which address an invalid register will return a 0.

2.7.34 MDIO Protocol Timing

Timing for a Clause 45 address transaction is shown in Figure 2-32. The Clause 45 timing required to write to the internal registers is shown in Figure 2-33. The Clause 45 timing required to read from the internal registers is shown in Figure 2-34. The Clause 45 timing required to read from the internal registers and then increment the active address for the next transaction is shown in Figure 2-35. The Clause 22 timing required to read from the internal registers is shown in Figure 2-36. The Clause 22 timing required to write to the internal registers is shown in Figure 2-37.



Note that the 1 in the Turn Around section is externally pulled up, and driven to Z by TLK3134

Figure 2-32. CL45 - Management Interface Extended Space Address Timing

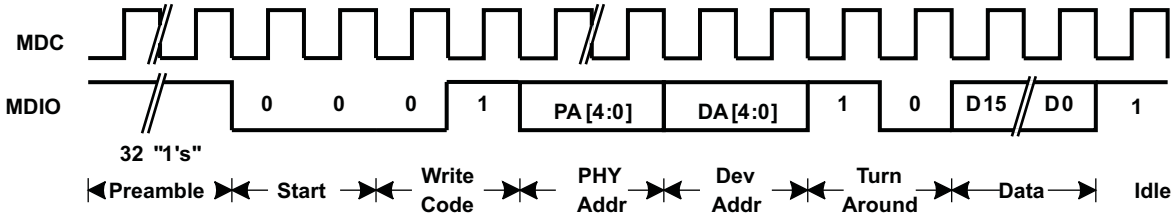


Figure 2-33. CL45 – Management Interface Extended Space Write Timing

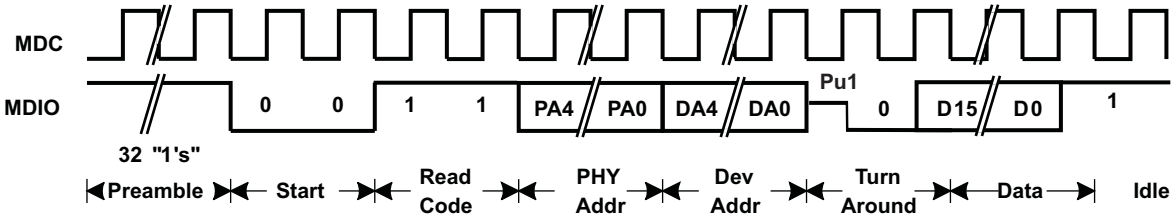


Figure 2-34. CL45 – Management Interface Extended Space Read Timing

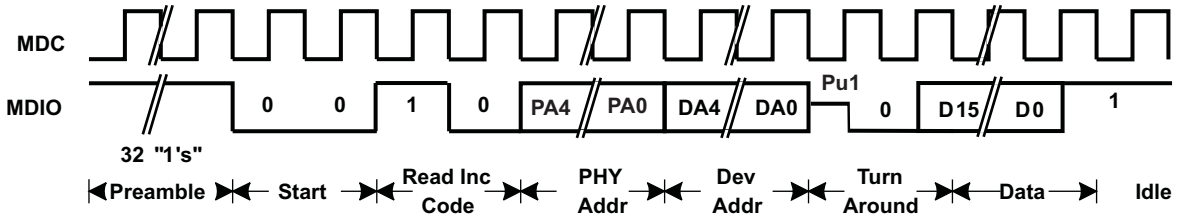
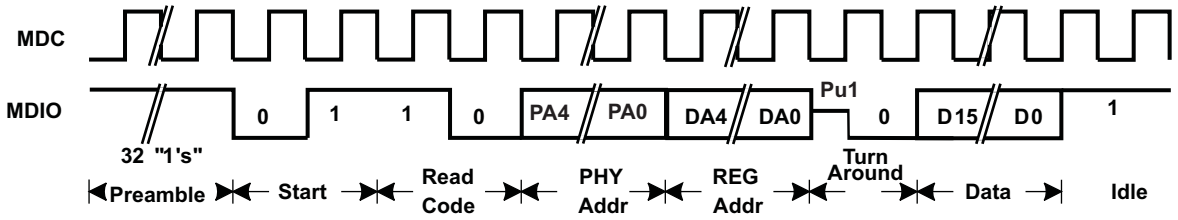


Figure 2-35. CL45 – Management Interface Extended Space Read And Increment Timing



Note that the 1 in the Turn Around section is externally pulled up, and driven to Z by TLK3134

Figure 2-36. CL22 – Management Interface Read Timing

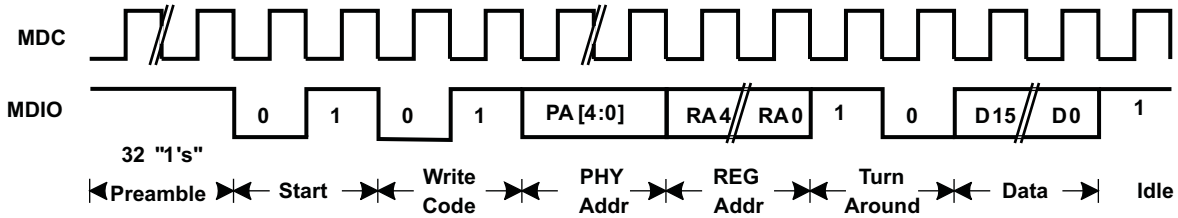


Figure 2-37. CL22 - Management Interface Write Timing

The IEEE 802.3 Clause 22/45 specification defines many of the registers, and additional registers have been implemented for expanded functionality.

2.7.35 Clause 22 Indirect Addressing

TLK3134 Register space is divided into 3 register groups. First register group that can be addressed only through Clause 45, second register group that can be addressed only through Clause 22 and third register group that can be addressed through both clause 45 and clause 22. Third register group which can be addressed through both clause 45 and clause 22 are implemented in vendor specific register space (16'h9000 onwards). This register space can be accessed directly using clause 45 addressing method. Due to clause 22 register space limitations, an indirect addressing method is implemented so that this register space can be accessed through clause 22. To access this register space (16'h9000 onwards), an address control register (Reg 30, 5'h1E) should be written with the register address followed by a read/write transaction to address content register (Reg 31, 5'h1F) to access the contents of the address specified in address control register. Following timing diagrams illustrate an example write transaction to Register 16'h9000 using indirect addressing in Clause 22.

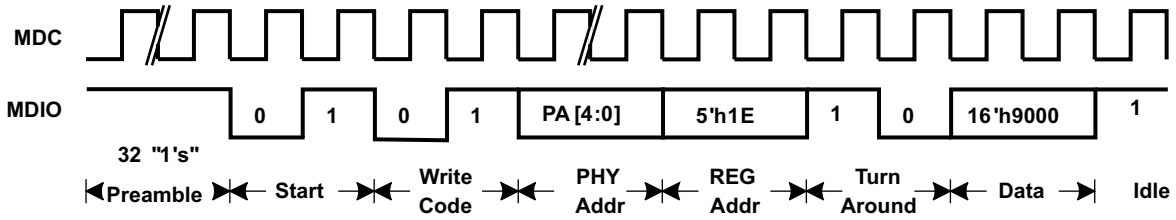


Figure 2-38. CL22 – Indirect Address Method – Address Write

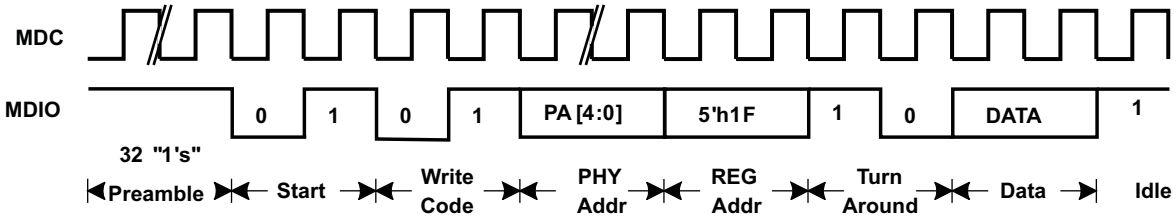


Figure 2-39. CL22 – Indirect Address Method – Data Write

Following timing diagrams illustrate an example read transaction to read contents of Register 16'h9000 using indirect addressing in Clause 22.

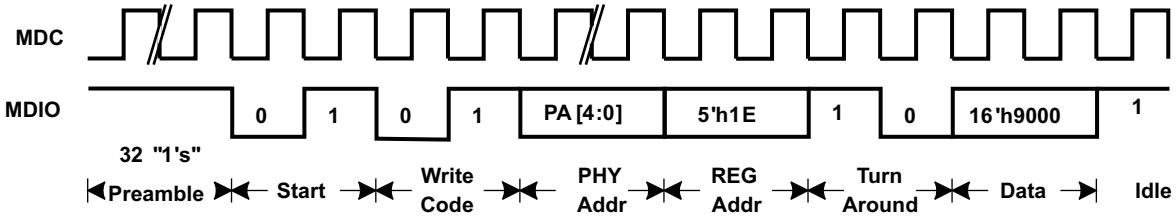


Figure 2-40. CL22 – Indirect Address Method – Address Write

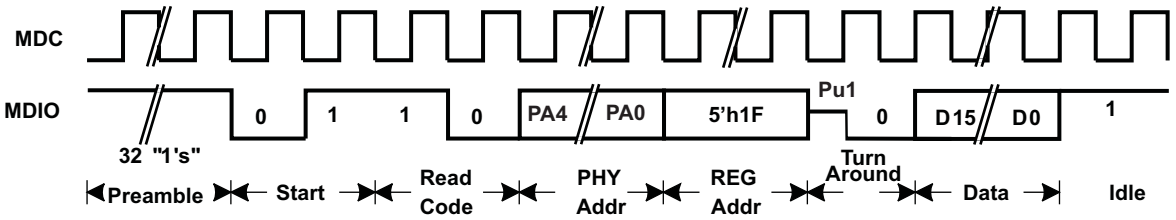


Figure 2-41. CL22 – Indirect Address Method – Data Read

The IEEE 802.3 Clause 22/45 specification defines many of the registers, and additional registers have been implemented for expanded functionality.

2.8 Programmers Reference

2.8.1 10G XAUI Programmers Reference (ST = 0)

Following 10G XAUI registers can be addressed only through Clause 45. Primary device input pin "ST" must be 0 to use Clause 45.

Table 2-19. XS_CONTROL_1(1)

ADDRESS: 0x0000		DEFAULT: 0x2040	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS(2)**
4/5.0.15	Reset	1 = XGXS reset (including all registers) 0 = Normal operation (Default)	RW SC
4/5.0.14	Loop Back	1 = Enable loop back mode. If the device is configured as PHY XS (PRTAD(0) = 0), then XAUI_DATA_LOOPBACK will be performed (Same as SLOOP). If the device is configured as DTE XS (PRTAD(0) = 1), then XGMII_DATA_LOOPBACK will be performed (Same as PLOOP) 0 = Disable loop back mode (Default)	RW
4/5.0.13	Speed Selection	This bit always reads 1 indicating operation at 10 Gbps and above.	RO
4/5.0.11	Low Power	1 = Low power mode 0 = Normal operation (Default) In low power mode all the internal clocks and datapaths are placed in shut down mode. After de-assertion of this bit, datapath reset (4/5.32800.15) needs to be performed to achieve proper datapath function. Serdes PLL's can be shut down by de-asserting bits 4/5.36864.12 and 4/5.36864.4. Jitter cleaner PLL can be shut down by de-asserting 4/5.37127.15	RW
4/5.0.6	Speed Selection	This bit always reads 1 indicating operation at 10Gbps and above.	RO
4/5.0.5:2	Speed Selection	These bits always read 0 indicating operation at 10Gbps.	

(1) In this section XS refers to either PHY or DTE XS device.
(2) RO: Read-Only, RW: Read-Write, SC: Self-Clearing, LL: Latching-Low, LH: Latching-High, COR: Clear-on-Read

Table 2-20. XS_STATUS_1

ADDRESS: 0x0001		DEFAULT: 0x0082	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.1.7	Fault	1 = Fault condition detected (either on TX or RX side. This bit is OR ed version of 4/5.8.10 and 4/5.8.11) 0 = No fault condition detected	RO
4/5.1.2	XS Transmit Link Status	1 = XS Transmit link is up. 0 = XS Transmit links is down. (This bit is latched low version of 4/5.24.12)	RO/LL
4/5.1.1	Low Power Ability	This bit always reads 1 indicating support for low power mode	RO

Table 2-21. XS_DEVICE_IDENTIFIER_1

ADDRESS: 0x0002		DEFAULT: 0x4000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.2.15.0	OUI c:r	Organizationally unique identifier.	RO

Table 2-22. XS_DEVICE_IDENTIFIER_2

ADDRESS: 0x0003		DEFAULT: 0x50D0	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.3.15:0	OUI c:r	Device identifier. Manufacturer model and revision number	RO

Table 2-23. XS_SPEED_ABILITY

ADDRESS: 0x0004		DEFAULT: 0x0001	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.4.0	10G Capable	This bit always reads 1 indicating operation at 10Gb/s	RO

Table 2-24. XS_DEVICES_IN_PACKAGE_1

ADDRESS: 0x0005		DEFAULT: 0x0011	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.5.5	DTE XS Present	1 = DTE XS present in the package. 0 = DTE XS not present in the package. Read will return 1, when PRTAD[0] is high	RO
4/5.5.4	PHY XS Present	1 = PHY XS present in the package. 0 = PHY XS not present in the package. Read will return 1, when PRTAD[0] is low	RO
4/5.5.3	PCS Present	Always reads 0	RO
4/5.5.2	WIS Present	Always reads 0	RO
4/5.5.1	PMD/PMA Present	Always reads 0	RO
4/5.5.0	Clause 22 Registers Present	Always reads 1	RO

Table 2-25. XS_DEVICES_IN_PACKAGE_2

ADDRESS: 0x0006		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.6.15	Vendor Specific Device 2 Present	This bit always reads 0 indicating that vendor specific device 2 not present in package	RO
4/5.6.14	Vendor Specific Device 1 Present	This bit always reads 0 indicating that vendor specific device 1 not present in package	RO

Table 2-26. XS_STATUS_2

ADDRESS: 0x0008		DEFAULT: 0x8C00	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.8.15:14	Device Present	Always read 2'b10 indicating that device responds at this address	RO
4/5.8.11	Transmit Fault	1 = Fault condition on transmit path. This bit is asserted when ppm difference between TX_CLK and XAUI serdes transmit reference clock is more than ±200. Local faults are sent on the transmit data stream during this condition. 0 = No fault condition on transmit path	RO/LH
4/5.8.10	Receive Fault	1 = Fault condition on receive path. This bit is asserted when there is loss of lane alignment or when ppm difference between XAUI serdes transmit reference versus RX recovered clock is more than ±200. Local faults are sent on the receive data stream during this condition. 0 = No fault condition on receive path	RO/LH

Table 2-27. XS_PACKAGE_IDENTIFIER_1

ADDRESS: 0x000E		DEFAULT: 0x4000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.14.15:0	OUI c:r	Organizationally unique identifier.	RO

Table 2-28. XS_PACKAGE_IDENTIFIER_2

ADDRESS: 0x000F		DEFAULT: 0x50D0	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.15.15:0	OUI c:r	Organizationally unique identifier Manufacturer model and revision number.	RO

Table 2-29. XS_LANE_STATUS

ADDRESS: 0x0018		DEFAULT: 0x0C00	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.24.12	Align Status	When 1, indicates all lanes are aligned	RO
4/5.24.11	Pattern Testing Ability	Always reads 1. Able to generate test patterns	RO
4/5.24.10	Loopback Ability	Always read 1. Has the ability to perform loopback function	RO
4/5.24.3	Lane 3 Sync	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized	RO
4/5.24.2	Lane 2 Sync	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized	RO
4/5.24.1	Lane 1 Sync	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized	RO
4/5.24.0	Lane 0 Sync	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized	RO

Table 2-30. XS_TEST_CONTROL

ADDRESS: 0x0019		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.25.2	Receive Test-Pattern Enable	1 = Enables test pattern generation/verification (High/Low/Medium) 0 = Test pattern generation/verification disabled (Default)	RW
4/5.25.1:0	Test-Pattern Select	00 = High frequency test pattern (Default) 01 = Low frequency test pattern 10 = Mixed frequency test pattern 11 = Reserved	RW

Table 2-31. TEST_CONFIG

ADDRESS: 0x8000		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32768.2	10GFC_CJPAT Enable	When set, enables the 10G Fiber channel compliant CJPAT test pattern generation on all 4 lanes. (Default 1'b0)	RW
4/5.32768.1	CRPAT enable	When set, enables the CRPAT test pattern generation on all 4 lanes. (Default 1'b0)	
4/5.32768.0	CJPAT enable	When set, enables the CJPAT test pattern generation on all 4 lanes. (Default 1'b0)	

Table 2-32. TEST_VERIFICATION_CONTROL

ADDRESS: 0x8001		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32769.2	10GFC_CJPAT check enable	When set, enables the verification of 10G Fiber channel compliant CJPAT test mode. (Default 1'b0)	RW
4/5.32769.1	CRPAT Check Enable	When set, enables the verification of CRPAT test mode. (Default 1'b0)	
4/5.32769.0	CJPAT Check Enable	When set, enables the verification of CJPAT test mode. (Default 1'b0)	

Table 2-33. TX_FIFO_STATUS

ADDRESS: 0x8002		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32770.9	Lane 3 Overflow	When high, indicates that transmit FIFO overflow condition occurred for the corresponding lane.	RO/LH
4/5.32770.8	Lane 2 Overflow		
4/5.32770.7	Lane 1 Overflow		
4/5.32770.6	Lane 0 Overflow		
4/5.32770.5	Lane 3 Underflow	When high, indicates that transmit FIFO underflow condition occurred for the corresponding lane.	RO/LH
4/5.32770.4	Lane 2 Underflow		
4/5.32770.3	Lane 1 Underflow		
4/5.32770.2	Lane 0 Underflow		
4/5.32770.1	Overflow	When high, indicates that transmit FIFO overflow condition occurred in any lane	RO/LH
4/5.32770.0	Underflow	When high, indicates that transmit FIFO underflow condition occurred in any lane	RO/LH

Table 2-34. TX_FIFO_DROP_COUNT

ADDRESS: 0x8003		DEFAULT: 0xFFFD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32771.15:0	Drop Count	Counter for number of idle drops in the transmit FIFO	RO/COR

Table 2-35. TX_FIFO_INSERT_COUNT

ADDRESS: 0x8004		DEFAULT: 0xFFFD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32772.15:0	Insert Count	Counter for number of idle inserts in the transmit FIFO	RO/COR

Table 2-36. TX_CODEGEN_STATUS

ADDRESS: 0x8005		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32773.6	Invalid XGMII character in lane 3	When high, indicates invalid XGMII character received in the corresponding lane.	RO/LH
4/5.32773.5	Invalid XGMII character in lane 2		
4/5.32773.4	Invalid XGMII character in lane 1		
4/5.32773.3	Invalid XGMII character in lane 0		
4/5.32773.2	Invalid XGMII character error	When high, indicates invalid XGMII character received in any lane	RO/LH
4/5.32773.1	Invalid T column error	When high, indicates invalid Terminate column (column that contains Terminate character not followed by Idle character(s)) received from the XGMII interface.	RO/LH
4/5.32773.0	Invalid S column error	When high, indicates invalid Start column (column that contains Start character in a lane other than lane 0) received from the XGMII interface.	RO/LH

Table 2-37. LANE_0_TEST_ERROR_COUNT

ADDRESS: 0x8006		DEFAULT: 0xFFFD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32774.15:0	Lane 0 test pattern error counter	This counter reflects errors for High, Medium or Low Frequency test patterns for lane 0. This counter increments by one for each received character that has error.	RO/COR

Table 2-38. LANE_1_ TEST_ERROR_COUNT

ADDRESS: 0x8007		DEFAULT: 0xFFFD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32775.15:0	Lane 1 test pattern error counter	This counter reflects errors for High, Medium or Low Frequency test patterns for lane 1. This counter increments by one for each received character that has error.	RO/COR

Table 2-39. LANE_2_ TEST_ERROR_COUNT

ADDRESS: 0x8008		DEFAULT: 0xFFFD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32776.15:0	Lane 2 test pattern error counter	This counter reflects errors for High, Medium or Low Frequency test patterns for lane 2. This counter increments by one for each received character that has error.	RO/COR

Table 2-40. LANE_3_ TEST_ERROR_COUNT

ADDRESS: 0x8009		DEFAULT: 0xFFFD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32777.15:0	Lane 3 test pattern error counter	This counter reflects errors for High, Medium or Low Frequency test patterns for lane 3. This counter increments by one for each received character that has error.	RO/COR

Table 2-41. 10GFCCJPAT_CRPAT_CJPAT_TEST_ERROR_COUNT_1 (1)

ADDRESS: 0x800A		DEFAULT: 0xFFFF	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32778.15:0	10GFC_CJPAT/CRPAT/CJ-PAT Test Error Counter[31:16]	MSW of 10GFC_CJPAT/CRPAT/CJPAT error counter for all 4 lanes	RO/COR

(1) User has to make sure that register 32778 is read first and then register 32779. If user reads register 32779 without reading register 32778 first, then the count value read through 32779 register may not be correct.

Table 2-42. 10GFCCJPAT_CRPAT_CJPAT_TEST_ERROR_COUNT_2 (1)

ADDRESS: 0x800B		DEFAULT: 0xFFFD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32779.15:0	10GFC_CJPAT/CRPAT/CJ-PAT Test Error Counter[15:0]	LSW of 10GFC_ CJPAT/CRPAT/CJPAT error counter for all 4 lanes	RO/COR

(1) User has to make sure that register 32778 is read first and then register 32779. If user reads register 32779 without reading register 32778 first, then the count value read through 32779 register may not be correct.

Table 2-43. LANE_0_EOP_ERROR_COUNT (1)

ADDRESS: 0x800C		DEFAULT: 0xFFFD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32780.15:0	Lane 0 end of packet error counter	End of packet termination error counter for lane 0. End of packet error for lane 0 is detected on the RX side. It is detected when Terminate character is in lane 0 and one or both of the following holds • Terminate character is not followed by /K/ characters in lanes 1, 2 and 3 • The column following the terminate column is neither ||K|| nor ||A||.	RO/COR

(1) Counter will increment by 1 when EOP error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter will hold on to its value when align_status goes low or when the counter reaches its maximum value. It will be cleared when it is read.

Table 2-44. LANE_1_EOP_ERROR_COUNT(1)

ADDRESS: 0x800D		DEFAULT: 0xFFFD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32781.15:0	Lane 1 end of packet error counter	End of packet termination error counter for lane 1. End of packet error for lane 1 is detected on the RX side. It is detected when Terminate character is in lane 1 and one or both of the following holds: • Terminate character is not followed by /K/ characters in lanes 2 and 3 • The column following the terminate column is neither ||K|| nor ||A||.	RO/COR

(1) Counter will increment by 1 when EOP error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter will hold on to its value when align_status goes low or when the counter reaches its maximum value. It will be cleared when it is read.

Table 2-45. LANE_2_EOP_ERROR_COUNT(1)

ADDRESS: 0x800E		DEFAULT: 0xFFFD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32782.15:0	Lane 2 end of packet error counter	End of packet termination error counter for lane 2. End of packet error for lane 2 is detected on the RX side. It is detected when Terminate character is in lane 2 and one or both of the following holds: • Terminate character is not followed by /K/ character in lane 3 • The column following the terminate column is neither ||K|| nor ||A||.	RO/COR

(1) Counter will increment by 1 when EOP error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter will hold on to its value when align_status goes low or when the counter reaches its maximum value. It will be cleared when it is read.

Table 2-46. LANE_3_EOP_ERROR_COUNT(1)

ADDRESS: 0x800F		DEFAULT: 0xFFFD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32783.15:0	Lane 3 end of packet error counter	End of packet termination error counter for lane 3. End of packet error for lane 3 is detected on the RX side. It is detected when Terminate character is in lane 3 and the column following the terminate column is neither ||K|| nor ||A||.	RO/COR

(1) Counter will increment by 1 when EOP error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter will hold on to its value when align_status goes low or when the counter reaches its maximum value. It will be cleared when it is read.

Table 2-47. LANE_0_CODE_ERROR_COUNT(1)

ADDRESS: 0x8010		DEFAULT: 0xFFFD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32784.15:0	Lane 0 Code Error Counter	Output 16-bit counter for invalid code group found in lane 0. Invalid code group is detected when the 8B10B decoder cannot decode the received code word.	RO/COR

(1) Counter will increment by 1 when code word error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter will hold on to its value when align_status goes low or when the counter reaches its maximum value. It will be cleared when it is read.

Table 2-48. LANE_1_CODE_ERROR_COUNT(1)

ADDRESS: 0x8011		DEFAULT: 0xFFFD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32785.15:0	Lane 1 Code Error Counter	Output 16-bit counter for invalid code group found in lane 1. Invalid code group is detected when the 8B10B decoder cannot decode the received code word.	RO/COR

(1) Counter will increment by 1 when code word error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter will hold on to its value when align_status goes low or when the counter reaches its maximum value. It will be cleared when it is read.

Table 2-49. LANE_2_CODE_ERROR_COUNT(1)

ADDRESS: 0x8012		DEFAULT: 0xFFFD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32786.15:0	Lane 2 Code Error Counter	Output 16-bit counter for invalid code group found in lane 2. Invalid code group is detected when the 8B10B decoder cannot decode the received code word.	RO/COR

(1) Counter will increment by 1 when code word error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter will hold on to its value when align_status goes low or when the counter reaches its maximum value. It will be cleared when it is read.

Table 2-50. LANE_3_CODE_ERROR_COUNT(1)

ADDRESS: 0x8013		DEFAULT: 0xFFFD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32787.15:0	Lane 3 Code Error Counter	Output 16-bit counter for invalid code group found in lane 3. Invalid code group is detected when the 8B10B decoder cannot decode the received code word.	RO/COR

(1) Counter will increment by 1 when code word error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter will hold on to its value when align_status goes low or when the counter reaches its maximum value. It will be cleared when it is read.

Table 2-51. RX_CHANNEL_SYNC_STATE

ADDRESS: 0x8014		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32788.11:9	Channel synchronization FSM state for lane 0	Current state of sync state machine in lane 0	RO
4/5.32788.8:6	Channel synchronization FSM state for Lane 1	Current state of sync state machine in lane 1	
4/5.32788.5:3	Channel synchronization FSM state for Lane 2	Current state of sync state machine in lane 2	
4/5.32788.2:0	Channel Synchronization FSM state for Lane 3	Current state of sync state machine in lane 3	

Table 2-52. RX_LANE_ALIGN_STATUS

ADDRESS: 0x8015		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32789.15:12	Align state	Current lane alignment FSM state	RO
4/5.32789.0	Lane Alignment FIFO collision	Collision status for lane alignment FIFO. When high, indicates that there is collision error in lane alignment FIFO.	RO/LH

Table 2-53. RX_CHANNEL_SYNC_STATUS

ADDRESS: 0x8016		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32790.11	Channel Synchronization status for all lanes	1 = Channel synchronization is achieved in all lanes. 0 = Channel synchronization is lost in one or more lanes	RO/LL

Table 2-54. BIT_ORDER

ADDRESS: 0x8017		DEFAULT: 0x0005	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32791. 3	XGMII RX bit order	When high, reverses the order of bits in the parallel data sent from XAUI RX for each lane. (Default 1'b0)	RW
4/5.32791. 2	XAUI RX bit order	When high, reverses the order of bits in the parallel data received from SERDES macros for XAUI RX for each lane. (Default 1'b1)	RW
4/5.32791. 1	XGMII TX bit order	When high, reverses the order of bits in the parallel data received from the XGMII interface each lane. (Default 1'b0)	RW

Table 2-54. BIT_ORDER (continued)

ADDRESS: 0x8017		DEFAULT: 0x0005	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32791. 0	XAUI TX bit order	When high, reverses the order of bits in the parallel data sent to the SERDES TX macro for each lane. (Default 1'b1)	RW

Table 2-55. LOOPBACK_CONTROL (1)

ADDRESS: 0x8018		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32792. 1	XAUI data loopback	When 1, loops back serial RX input on to serial TX output. (4/5.0.14 should be 0 else no effect). Performs same function as SLOOP. (Default 1'b0)	RW
4/5.32792. 0	XGMII data loopback	When 1, loops back parallel TX input onto parallel RX output (4/5.0.14 should be 0 else no effect). Performs same function as PLOOP. (Default 1'b0)	

(1) See Loopback section for more information.

Table 2-56. TX_MODE_CONTROL

ADDRESS: 0x8019		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32793.15	TX IPG management bypass	When high, bypasses IPG management (replacing Idle XGMII characters with /A/K/R/Q/ code-words) in transmit side. (Default 1'b0)	RW
4/5.32793.11	TX CTC disable	When high, disables clock tolerance compensation in transmit side. (Default 1'b0)	RW
4/5.32793.7	Lane 3 8B10B encoder disable	When high, disables XAUI 8B10B encoding on the corresponding lane. (Default 1'b0)	RW
4/5.32793.6	Lane 2 8B10B encoder disable		
4/5.32793.5	Lane 1 8B10B encoder disable		
4/5.32793.4	Lane 0 8B10B encoder disable		

Table 2-57. RX_CTC_STATUS

ADDRESS: 0x801A		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32794.9	Lane 3 overflow	When high, indicates overflow error in the corresponding lane.	RO/LH
4/5.32794.8	Lane 2 overflow		
4/5.32794.7	Lane 1 overflow		
4/5.32794.6	Lane 0 overflow		
4/5.32794.5	Lane 3 underflow	When high, indicates underflow error in the corresponding lane.	RO/LH
4/5.32794.4	Lane 2 underflow		
4/5.32794.3	Lane 1 underflow		
4/5.32794.2	Lane 0 underflow		
4/5.32794.1	Overflow	When high, indicates overflow error in any lane.	RO/LH
4/5.32794.0	Underflow	When high, indicates underflow error in any lane.	RO/LH

Table 2-58. RX_CTC_INSERT_COUNT

ADDRESS: 0x801B		DEFAULT: 0xFFFD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32795.15:0	Idle insert count	Counter for number of idle insertions in RX side	RO/COR

Table 2-59. RX_CTC_DELETE_COUNT

ADDRESS: 0x801C		DEFAULT: 0xFFFD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32796.15:0	Idle delete count	Counter for number of idle deletions	RO/COR

Table 2-60. DATA_DOWN

ADDRESS: 0x801D		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32797.3	Lane 3 data down	When high, indicates that link for the corresponding lane was inactive (data did not toggle) for 4095 cycles of recovered clock from serial input data The recovered clock is generated internally by the PLL from the 156Mhz Reference clock.	RO/COR
4/5.32797.2	Lane 2 data down		
4/5.32797.1	Lane 1 data down		
4/5.32797.0	Lane 0 data down		

Table 2-61. RX_MODE_CONTROL

ADDRESS: 0x801E		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32798.15	RX CTC disable	When set, disables clock tolerance compensation on the RX side. (Default 1'b0)	RW
4/5.32798.14	IPG Checker bypass	When set, disables the replacement of /A/K/R/ into Idles and also bypasses end-of-packet error checking. (Default 1'b0)	RW
4/5.32798.11	Lane 3 8B/10B decoder bypass	When set, disables the XAUI 8B/10B decoding for the corresponding lane. (Default 1'b0)	RW
4/5.32798.10	Lane 2 8B/10B decoder bypass		
4/5.32798.9	Lane 1 8B/10B decoder bypass		
4/5.32798.8	Lane 0 8B/10B decoder bypass		
4/5.32798.7	Consider sequence column part of IPG	When high, sequence columns are counted as part of IPG. When low, sequence columns are not counted as IPG (Default 1'b0)	RW
4/5.32798.3	RX Lane align bypass enable	When set, enables lane alignment bypass on the RX side	RW

Table 2-62. CLOCK_DOWN_STATUS

ADDRESS: 0x801F		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32799. 7	Lane 3 clock 312 down	When high, indicates that serial clock generated by SERDES TX is down on the corresponding lane for 255 or more cycles. The detection is done on the transmit side.	RO/LH
4/5.32799. 6	Lane 2 clock 312 down		
4/5.32799. 5	Lane 1 clock 312 down		
4/5.32799. 4	Lane 0 clock 312 down		
4/5.32799. 3	Lane 3 clock 156 down	When high, indicates that 156MHz XGMII clock is down on the corresponding lane for 255 or more cycles. The detection is done on the transmit side	RO/LH
4/5.32799. 2	Lane 2 clock 156 down		
4/5.32799. 1	Lane 1 clock 156 down		
4/5.32799. 0	Lane 0 clock 156 down		

Table 2-63. DATAPATH_RESET_CONTROL

ADDRESS: 0x8020		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32800. 15	XAUI datapath reset	When set, resets XAUI data path but does not reset any R/W registers. (Default 1'b0)	RW/SC

Table 2-64. TEST_PATTERN_STATUS

ADDRESS: 0x8021		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5/32801.15	Test pattern sync status	When high, indicates that preamble for 10GFC_CJPAT/CRPAT/CJPAT has been recovered.	RO

Table 2-65. LANE_0_ERROR_CODE

ADDRESS: 0x8022		DEFAULT: 0xCE00	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32802.15:7	Lane 0 error code select.	Error code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 0 corresponds to 8'h9C with the control bit being 1'b1. The default values for lanes 0~3 correspond to ||LF||	RW

Table 2-66. LANE_1_ERROR_CODE

ADDRESS: 0x8023		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32803.15:7	Lane 1 error code select.	Error code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 1 corresponds to 8'h00 with the control bit being 1'b0. The default values for lanes 0~3 correspond to ||LF||	RW

Table 2-67. LANE_2_ERROR_CODE

ADDRESS: 0x8024		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32804.15:7	Lane 2 error code select.	Error code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 2 corresponds to 8'h00 with the control bit being 1'b0. The default values for lanes 0~3 correspond to ||LF||	RW

Table 2-68. LANE_3_ERROR_CODE

ADDRESS: 0x8025		DEFAULT: 0x0080	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32805.15:7	Lane 3 error code select.	Error code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 3 corresponds to 8'h01 with the control bit being 1'b0. The default values for lanes 0~3 correspond to ||LF||	RW

Table 2-69. RX_PHASE_SHIFT_CONTROL

ADDRESS: 0x8026		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32806. 15	Lane 3 phase shift	When set, delays the RX data sent to the XGMII interface by one clock cycle. (Default 1'b0)	RW
4/5.32806. 14	Lane 2 phase shift		
4/5.32806. 13	Lane 1 phase shift		
4/5.32806. 12	Lane 0 phase shift		

Table 2-70. CHANNEL_SYNC_CONTROL

ADDRESS: 0x8027		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32807. 15	Lane 3 channel sync bypass	When set, channel synchronization for the corresponding lane is bypassed. (Default 1'b0)	RW
4/5.32807. 14	Lane 2 channel sync bypass		
4/5.32807. 13	Lane 1 channel sync bypass		
4/5.32807. 12	Lane 0 channel sync bypass		
4/5.32807. 11	Lane 3 channel sync freeze	When set, freezes the last acquired word alignment for the corresponding lane. (Default 1'b0)	RW
4/5.32807. 10	Lane 2 channel sync freeze		
4/5.32807. 9	Lane 1 channel sync freeze		
4/5.32807. 8	Lane 0 channel sync freeze		

Table 2-71. XGMII_IO_MODE_CONTROL

ADDRESS: 0x8028		DEFAULT: 0x0080	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32808. 15	XAUI Tx Edge Align	When set selects data relationship with the clock on the transmit side 0 – Source centered (Default 1'b0) 1 – Source aligned	RW
4/5.32808. 11	XAUI Rx Edge Align	When set selects data relationship with the clock on the receive side 0 – Source centered (Default 1'b0) 1 – Source aligned	RW
4/5.32808. 7	RCLK Output Enable	0 – Disables RCLK output 1 – Enables RCLK output (Default 1'b1)	RW
4/5.32808. 3	XAUI Isolate	Setting this bit high isolates the XGXS core from the XGMII interface. Inputs are ignored; Outputs are set to high impedance. 1 = Isolate is enabled 0 = Normal operation (Default 1'b0)	RW

Table 2-72. 10G_MODE_CONTROL

ADDRESS: 0x8029		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32809.15	XAUI order	When set selects XAUI/10GFC mode. Logically OR'ed with CODE pin. 0 = 10 GFC mode (Default 1'b0) 1 = XAUI mode	RW

Table 2-73. RX_CLK_OUTPUT_CONTROL

ADDRESS: 0x802A		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.32810. 15:14	RX_CLK output clock select	These control bits select the clock to be sent out on receive parallel output clock (RX_CLK) 00 = Selects SERDES TX clock 01 = Selects Jitter cleaned clock (Selecting the jitter cleaned clock while the jitter cleaner PLL is disabled is not recommended) 10 = Selects SERDES RX clock 11 = Reserved	RW

2.9 1G Programmers Reference

Following registers can be addressed directly only through Clause 22 (1G Related Registers). Clause 22 access is valid only when “ST” pin is set to 1. These bits are per channel basis. Channel identification is based on PHY (Port) address field.

Channel 0 can be accessed by setting 2 LSB’s of PHY address to 00.

Channel 1 can be accessed by setting 2 LSB’s of PHY address to 01.

Channel 2 can be accessed by setting 2 LSB’s of PHY address to 10.

Channel 3 can be accessed by setting 2 LSB’s of PHY address to 11.

Registers 30 (5’h1E) and 31 (5’h1F) are global in 1G mode. These registers contents are same when accessed through any of the 4 channels mentioned above.

Table 2-74. PHY_CONTROL_1

ADDRESS: 0x00		DEFAULT: 0x0140	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
0. 15	Reset	1 = PHY reset (including all registers and both Tx/Rx datapaths) 0 = Normal operation (Default 1’b0) This is a global bit (not per channel). Asserting this bit is equivalent to asserting the device primary input RST_N.	RW SC(1)
0. 14	Loopback	Logically OR’ed with PLOOP 1 = Enable loop back mode. In this mode, serial output of the channel is looped back onto serial input. 0 = Disable loop back mode (Default 1’b0)	RW
0. 13	Speed Selection(LSB)	This is the least significant bit of the speed selection bits (MSB is 0.6). {0.6,0.13} = 2’b10 1000Base-X Rate This bit always reads 0.	RO
0. 12	Auto-Negotiation Enable	Always reads 0. (Auto-Negotiation not supported)	RO
0. 11	Power Down	Setting this bit high powers down respective channel, with exception that MDIO interface stays active. Serdes PLL’s can be shut down by de-asserting bits 36864.12 and 36864.4. Jitter cleaner PLL can be shut down by de-asserting 37127.15 1 = Power Down mode is enabled. 0 = Normal operation (Default 1’b0)	RW
0. 10	Isolate	Setting this bit high isolates the channel from the parallel interface. Inputs are ignored; Outputs are set to high impedance. 1 = Isolate is enabled 0 = Normal operation (Default 1’b0)	RW
0. 9	Restart Auto-Negotiation	Always reads 0. (Auto-Negotiation not supported)	RO
0. 8	Duplex Mode	Always reads 1. (Only Full duplex supported)	RO
0. 7	Collision Test	Not Applicable. Read will return a 0.	RO
0. 6	Speed Selection (MSB)	This is the most significant bit of the speed selection bits (LSB is 0.13). {0.6,0.13} = 2’b10 1000Base-X Rate This bit always reads 1	RO

(1) After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

Table 2-75. PHY_STATUS_1

ADDRESS: 0x01		DEFAULT: 0x0101	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
1. 15	1000Base-T4	Always reads 0	RO
1. 14	100Base-X FD	Always reads 0	RO
1. 13	100Base-X HD	Always reads 0	RO
1. 12	10Mb/s FD	Always reads 0	RO
1. 11	10Mb/s HD	Always reads 0	RO
1. 10	100Base-T2 FD	Always reads 0	RO
1. 9	100Base-T2 HD	Always reads 0	RO
1. 8	Extended Status	Read will return 1 indicating extended status information is held in register 0x0F.	RO
1. 6	MF Prea Supp	Read will return 0 indicating MDIO doesn't accept command without preceding preamble (minimum 32 1's). Writes will be ignored	RO
1. 5	AN Complete	Always reads 0 (AN not supported)	RO
1. 4	Remote Fault	Always reads 0	RO
1. 3	AN Ability	Read will return 0, indicating that Auto negotiation is not supported	RO
1. 2	Link Status	Read will return the Link Status and is valid only when device is in GMII/RGMII mode or when bit 17.7 is set in Non-GMII/RGMII modes. Note: Link status will always indicate high when in loopback. In remote loopback mode, the bit represents the normal bit function. 1 = Link UP 0 = Link DOWN	RO/LL
1.1	Jabber Detect	Always reads 0	RO
1.0	Extended Capability	Read will return 1 indicating extended register capability	RO

Table 2-76. PHY_IDENTIFIER_1

ADDRESS: 0x02		DEFAULT: 0x4000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
2.15.0	OUI c:r	Organizationally unique identifier.	RO

Table 2-77. PHY_IDENTIFIER_2

ADDRESS: 0x03		DEFAULT: 0x50D0	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
3.15:0	OUI c:r	Device identifier. Manufacturer model and revision number	RO

Table 2-78. PHY_EXT_STATUS

ADDRESS: 0x0F		DEFAULT: 0x8000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
15.15	1000Base-X FD	Always reads 1, indicating device supports Full Duplex mode.	RO
15.14	1000Base-X HD	Read will return 0, writes will be ignored.	
15.13	1000Base-T FD	Read will return 0, writes will be ignored.	
15.12	1000Base-T HD	Read will return 0, writes will be ignored.	

Table 2-79. PHY_CH_CONTROL_1

ADDRESS: 0x10		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
16.15	Global Write	When written as 1 the settings in 16.14:0 will affect all channels of one device simultaneously. When written as 0 the settings in 16.14:0 are only valid for the addressed channel. This value always reads zero.	RW/SC
16.11	Datapath Reset Control	1 = Resets channel logic excluding MDIO registers (Resets both Tx and Rx datapaths)	RW/SC
16.10:9	Receive Parallel Output Clock Select	00 = Selects respective channel SERDES TX clock 01 = Selects Jitter cleaned clock(Selecting the jitter cleaned clock while the jitter cleaner PLL is disabled is not recommended) 10 = Selects respective channel SERDES RX clock 11 = Reserved	RW
16.8	Farend Loopback	Logically OR'ed with SLOOP When asserted high the data presented at the serial receive interface is looped back to the serial transmit interface of the same channel via the deserializer, the serializer and if enabled the PCS function. If 1GX PCS is not enabled, the incoming datarate must be frequency locked (ppm 0) with REFCLK. Also referred to as remote loopback. 0 = Farend Loopback is disabled. (Default 1'b0) 1 = Farend loopback is enabled.	RW
16.7	PRBS Verifier Enable	A logic 1 enables the PRBS (2^7) verifier in the receive datapath. Logically OR'ed with the PRBSEN pin. (Default 1'b0)	RW
16.6	PRBS Generator Enable	A logic 1 enables the PRBS (2^7) generator in the transmit datapath. Logically OR'ed with the PRBSEN pin. (Default 1'b0)	RW
16.5	Channel sync freeze control	When set, freezes last acquired word alignment. (Default 1'b0)	RW
16.4	Test Pattern Generator Enable	When high activates the generator selected by bits 16.2:0. (Default 1'b0)	RW
16.3	Test Pattern Verifier Enable	When high activates the verifier selected by bits 16.2:0. (Default 1'b0)	RW
16.2:0	Pattern Select	Test Pattern Selection 000 = High Frequency Test Pattern (Default 3'b000) 001 = Low Frequency Test Pattern 010 = Mixed Frequency Test Pattern 011 = CRPAT Long 100 = CRPAT Short Others = Reserved	RW

Table 2-80. PHY_CH_CONTROL_2

ADDRESS: 0x11		DEFAULT: 0x3590	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
17.15	Global write	When written as 1 the settings in 17.14:0 will affect all channels of one device simultaneously. When written as 0 the settings in 17.14:0 are only valid for the addressed channel. This value always reads zero.	RW/SC
17.14	Sync Status Override	1 = Causes an override of the sync state of 1000Base-X synchronization state machine to reflect a "1" in the sync_status (1.2) bit. 0 = Original (normal operation) sync_status value is represented in bit 1.2. (Default 1'b0)	RW
17.13	TX PMA Bit Order	When asserted, allows the ten bits of data given to the parallel side of the SERDES TX macro to be flipped. This is normally set since the SERDES transmits MSB first, and the 1000Base-X standard requires LSB to be transmitted first. For standard based operation, the customer may leave this bit alone. (Default 1'b1)	RW

Table 2-80. PHY_CH_CONTROL_2 (continued)

ADDRESS: 0x11		DEFAULT: 0x3590	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
17.12	RX PMA Bit Order	When asserted, allows the ten bits of data received from the parallel side of the SERDES RX macro to be flipped. This is normally set since the SERDES receives MSB first, and the 1000Base-X standard requires LSB to be received first. For standard based operation, the customer may leave this bit alone. (Default 1'b1)	RW
17.11	LOS Override	1 = Overrides Loss of signal (LOS) status coming from SERDES. Synchronization turned on irrespective of LOS status 0 = Synchronization depends on LOS status. (Default 1'b0)	RW
17.10	CTC enable	1 = Clock Tolerance Compensation on receive datapath is enabled (Default 1'b1) 0 = Clock Tolerance Compensation on receive datapath is disabled	RW
17.9	Full DDR mode	1 = Sets the device in full DDR mode (NBID/TBID modes) 0 = Disables full DDR mode (Default)	RW
17.8	RCLK out enable	1 = Enables RX_CLK out (Default 1'b1) 0 = Disables RX_CLK out. RX_CLK will be low when this bit is de-asserted	RW
17.7	Comma enable	1 = Enables comma detection (Default 1'b1) 0 = Disables comma detection	RW
17.6	FC enable	1 = Enables FC_PH overlay detection. This is needed in 1x/2x Fiber channel mode to allow proper detection of EOF 8B/10B disparity 0 = Disables FC_PH overlay detection (Default 1'b0)	RW
17.5	Data mode	Valid only when 17.9 (Full DDR mode) is LOW. 1 = Enables DDR data mode on parallel Transmit and Receive directions (data clocked on both rising and falling edge) 0 = Enables SDR data mode on parallel Transmit and Receive directions (data is clocked only on rising edge or only on falling edge) (Default 1'b0)	RW
17.4	Nibble order	Applicable only in non FULL DDR modes 1 = LSB on rising edge followed by MSB on falling edge (Default 1'b1) 0 = MSB on rising edge followed by LSB on falling edge	RW
17.3	PCS TX_RX Enable	1 = Enables 1000Base-X PCS Tx & PCS Rx functions 0 = Disables 1000Base-X PCS Tx Function (Default 1'b0)	RW
17.2	Encode Decode Enable	0 = 8B/10B encode decode functions are disabled (Default 1'b0) 1 = 8B/10B encode decode functions are enabled	RW
17.1	TX Edge Mode	When channel is in DDR mode 1 = Source aligned timing on transmit parallel interface. 0 = Source centered timing on transmit parallel interface. Data is latched on both rising and falling clock edges. When channel is in SDR mode 1 = Rising edge align mode. Incoming parallel data is aligned to rising edge of parallel input clock. Internally data is latched at the falling edge of the clock. 0 = Falling edge align mode. Incoming data is aligned to falling edge of parallel input clock. Internally data is latched at the rising edge of the clock	RW
17.0	RX Edge Mode	When channel is in DDR mode 1 = Source aligned timing on receive parallel interface. Data changes at clock edge. 0 = Source centered timing on receive parallel interface. When channel is in SDR mode 1 = Rising edge align mode. Outgoing parallel data is aligned to the rising edge of the parallel output clock 0 = Falling edge align mode. Outgoing parallel data is aligned to the falling edge of the parallel output clock	RW

Table 2-81. PHY_RX_CTC_FIFO_STATUS

ADDRESS: 0x12		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
18.15	RX_CTC_Reset	When high indicates overflow or underflow has occurred in CTC FIFO and FIFO has been reset.	RO/LH
18.14	RX_CTC_Insert	When high indicates RX CTC has inserted at least one ordered set.	
18.13	RX_CTC_Delete	When high indicates RX CTC has deleted at least one ordered set.	

Table 2-82. PHY_TX_CTC_FIFO_STATUS

ADDRESS: 0x13		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
19.15	TX_FIFO_Reset_1Gx	When high indicates collision has occurred in TX FIFO and the FIFO is reset in 1gx mode. Valid in Non-NBID, Non-TBID modes.	RO/LH

Table 2-83. PHY_TX_WIDE_FIFO _STATUS

ADDRESS: 0x14		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
20.15	TX_WIDE_FIFO_ Overflow	When high indicates Overflow condition has occurred in TX WIDE FIFO. Valid only when device is in NBID/TBID modes.	RO/LH
20.14	TX_WIDE_FIFO_ Underflow	When high indicates Underflow condition has occurred in TX WIDE FIFO. Valid only when device is in NBID/TBID modes.	

Table 2-84. PHY_TEST_PATTERN_SYNC_STATUS

ADDRESS: 0x15		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
21.1	Test Pattern Sync	When high indicates alignment has been determined and a correct pattern has been received for fixed test patterns.	RO
21.0	CRPAT Sync	When high indicates alignment has been determined and a correct pattern has been received for continuous test patterns.	

Table 2-85. PHY_TEST_PATTERN_COUNTER

ADDRESS: 0x16		DEFAULT: 0xFFFD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
22.15:0	Fixed Test Pattern Error Counter	This counter reflects error count for high, Mixed, and Low Frequency test patterns. Counter increments for each received character that has an error. Counter clears upon read.	COR

Table 2-86. PHY_CRPAT_PATTERN_COUNTER_1(1)

ADDRESS: 0x17		DEFAULT: 0xFFFF	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
23.15:0	CRPAT Error counter[31:16]	This counter reflects MSW part of error count for CRPAT Frequency test pattern. Counter increments for each received character that has an error. Counter clears upon read.	COR

(1) User has to make sure that register 23 is read first and then register 24. If user reads register 24 before reading register 23, then the count value read through register 24 may not be correct.

Table 2-87. PHY_CRPAT_PATTERN_COUNTER_2 (1)

ADDRESS: 0x18		DEFAULT: 0xFFFD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
24.15:0	CRPAT Error counter[15:0]	This counter reflects LSW part of error count for CRPAT Frequency test pattern. Counter increments for each received character that has an error. Counter clears upon read.	COR

(1) User has to make sure that register 23 is read first and then register 24. If user reads register 24 before reading register 23, then the count value read through register 24 may not be correct.

Table 2-88. PHY_TEST_MODE_CONTROL

ADDRESS: 0x1B		DEFAULT: 0x7000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
27.15	Global write	When written as 1 the settings in 27.14:12 will affect all channels of one device simultaneously. When written as 0 the settings in 27.14:12 are only valid for the addressed channel. This value always reads zero.	RW/SC
27.14:12	Test Mux Select	Mux control to select debug signals onto test mux data pins. For TI test purposes only	RW

Table 2-89. PHY_CHANNEL_STATUS

ADDRESS: 0x1C		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
28.15	Signal Detect	When high, indicates that the SERDES detected valid signal.	RO/LL
28.13	Encoder Invalid Code Word	When high, indicates that the 1000Base-X encoder received an invalid control word.	RO/LH
28:12	Decoder Invalid Code Word	When high, indicates that the 1000Base-X decoder received an invalid code word.	

Table 2-90. PHY_PRBS_HIGH_SPEED_TEST_COUNTER

ADDRESS: 0x1D		DEFAULT: 0xFFFD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
29.15:0	PRBS High Speed Test Counter	This counter reflects errors for PRBS (2^7) test pattern verification . Counter increments by one for each received character that has error. This counter saturates at 16'hffff. When read, it resets to zero and continues to count.	COR

Table 2-91. PHY_EXT_ADDRESS_CONTROL (1)

ADDRESS: 0x1E		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
30.15:0	Ext address control	This register should be written with the extended register address to be written/read. Contents of address written in this register can be accessed from Reg 31 (0x1F).	RW

(1) This register is not per channel basis. This register can be accessed through any of the 4 channels.

Table 2-92. PHY_EXT_ADDRESS_DATA (1)

ADDRESS: 0x1F		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
31.15:0	Ext address data register	This register contains the data associated with the register address written in Register 30 (0x1E)	RW

(1) This register is not per channel basis. This register can be accessed through any of the 4 channels.

2.10 Top Level Programmers Reference

Following registers can be addressed directly through Clause 45 and indirectly through Clause 22.

Table 2-93. SERDES_PLL_CONFIG(1)

ADDRESS: 0x9000		DEFAULT: 0x1515	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36864.14:13	Loop Bandwidth RX(LB_RX)	SERDES RX PLL Bandwidth settings 00 = Applicable when JC PLL is not engaged 01 = Reserved 10 = Reserved 11 = Applicable when JC PLL is engaged	RW
4/5.36864. 12	ENPLL_RX	0 = Disables PLL in SERDES RX 1 = Enable PLL in SERDES RX	RW
4/5.36864.11:8	PLL Multiplier factor RX (MPY_RX)	SERDES RX PLL multiplier setting See Table 94: PLL Multiplier Control	RW
4/5.36864.7	BUSWIDTH	1 = 8 bit mode. Applicable for only EBI and REBI modes 0 = 10 Bit mode. Applicable for all other modes	RW
4/5.36864.6:5	Loop Bandwidth TX (LB_TX)	SERDES TX PLL Bandwidth settings 00 = Applicable when JC PLL is not engaged 01 = Reserved 10 = Reserved 11 = Applicable when JC PLL is engaged	RW
4/5.36864.4	ENPLL_TX	0 = Disables PLL in SERDES TX 1 = Enable PLL in SERDES TX	RW
4/5.36864. 3:0	PLL Multiplier factor TX (MPY_TX)	SERDES TX PLL multiplier setting See Table 94: PLL Multiplier Control	RW

(1) These are global PLL control bits and will be applicable to all 4 channels.

Table 2-94. PLL Multiplier Control

36864[11:8]/ 36864[3:0]		36864[11:8]/ 36864[3:0]	
VALUE	**PLL MULTIPLIER FACTOR**	**VALUE**	**PLL MULTIPLIER FACTOR**
0000	4x	1000	15x
0001	5x	1001	20x
0010	6x	1010	25x
0011	Reserved	1011	Reserved
0100	8x	1100	Reserved
0101	10x	1101	50x
0110	12x	1110	60x
0111	12.5x	1111	Reserved

Table 2-95. SERDES_RATE_CONFIG_TX_RX(1)

ADDRESS: 0x9001		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36865.15:14	RATE_0_TX	TX Ch 0 Operating rate 00 = Full rate (2 data samples/output per PLL output clock cycle) 01 = Half rate (1 data sample/output per PLL output clock cycle) 10 = Quarter rate (1 data sample/output per 2 PLL output clock cycle) 11 = Reserved	RW

(1) These are global PLL control bits and will be applicable to all 4 channels.

Table 2-95. SERDES_RATE_CONFIG_TX_RX (1) (continued)

ADDRESS: 0x9001		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36865.13:12	RATE _1_TX	TX Ch 1 Operating rate 00 = Full rate (2 data samples/output per PLL output clock cycle) 01 = Half rate (1 data sample/output per PLL output clock cycle) 10 = Quarter rate (1 data sample/output per 2 PLL output clock cycle) 11 = Reserved	RW
4/5.36865.11:10	RATE _2_TX	TX Ch 2 Operating rate 00 = Full rate (2 data samples/output per PLL output clock cycle) 01 = Half rate (1 data sample/output per PLL output clock cycle) 10 = Quarter rate (1 data sample/output per 2 PLL output clock cycle) 11 = Reserved	RW
4/5.36865.9:8	RATE _3_TX	TX Ch 3 Operating rate 00 = Full rate (2 data samples/output per PLL output clock cycle) 01 = Half rate (1 data sample/output per PLL output clock cycle) 10 = Quarter rate (1 data sample/output per 2 PLL output clock cycle) 11 = Reserved	RW
4/5.36865.7:6	RATE_0_RX	RX Ch 0 Operating rate 00 = Full rate (2 data samples/output per PLL output clock cycle) 01 = Half rate (1 data sample/output per PLL output clock cycle) 10 = Quarter rate (1 data sample/output per 2 PLL output clock cycle) 11 = Reserved	RW
4/5.36865.5:4	RATE _1_RX	RX Ch 1 Operating rate 00 = Full rate (2 data samples/output per PLL output clock cycle) 01 = Half rate (1 data sample/output per PLL output clock cycle) 10 = Quarter rate (1 data sample/output per 2 PLL output clock cycle) 11 = Reserved	RW
4/5.36865.3:2	RATE _2_RX	RX Ch 2 Operating rate 00 = Full rate (2 data samples/output per PLL output clock cycle) 01 = Half rate (1 data sample/output per PLL output clock cycle) 10 = Quarter rate (1 data sample/output per 2 PLL output clock cycle) 11 = Reserved	RW
4/5.36865.1:0	RATE _3_RX	RX Ch 3 Operating rate 00 = Full rate (2 data samples/output per PLL output clock cycle) 01 = Half rate (1 data sample/output per PLL output clock cycle) 10 = Quarter rate (1 data sample/output per 2 PLL output clock cycle) 11 = Reserved	RW

Table 2-96. SERDES_RX0_CONFIG(1)

ADDRESS: 0x9002		DEFAULT: 0x0001	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36866.15:12	EQUALIZER	Adaptive equalization control 0000 = Adaptive equalization disabled. Equalizer provides flat response at maximum gain. 0001 = Full adaptive equalization 0010 to 1111 = Reserved	RW
4/5.36866.11:9	CDR	Clock data recovery algorithm selection	RW
4/5.36866.8	INVPAIR	1 = Inverts polarity of RXP and RXN	RW
4/5.36866.7:6	LOS	00 = Loss of signal detection disabled 01 = Reserved 10 = Loss of signal detection enabled with threshold in the range of 85-175 mVdfpp. 11 = Reserved.	RW
4/5.36866.5:4	ALIGN	Receiver symbol alignment selection 00 = Alignment disabled. 01 = Comma alignment enabled 10 = Symbol alignment will be performed by one bit position when this mode is selected (i.e ALIGN changes from 00 to 10) 11= Reserved	RW
4/5.36866.3:2	TERM	Receive Termination selection 00 = Common point connected to VDDT (For DC Coupled Systems) 01 = Common point set to 0.8 VDDT (For AC Coupled Systems) 10 = Reserved 11 = Reserved	RW
4/5.36866.1	ENTEST	1= Enables test modes specified in TESTCFG (Register 0x9012)	RW
4/5.36866.0	ENRX	1 = Enables receiver 0 = Disables receiver	RW

(1) These are SERDES receiver control bits for channel 0.

Table 2-97. SERDES_RX1_CONFIG(1)

ADDRESS: 0x9004		DEFAULT: 0x0001	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36868.15:12	EQUALIZER	Adaptive equalization control 0000 = Adaptive equalization disabled. Equalizer provides flat response at maximum gain. 0001 = Full adaptive equalization 0010 to 1111 = Reserved	RW
4/5.36868.11:9	CDR	Clock data recovery algorithm selection	RW
4/5.36868.8	INVPAIR	1 = Inverts polarity of RXP and RXN	RW
4/5.36868.7:6	LOS	00 = Loss of signal detection disabled 01 = Reserved 10 = Loss of signal detection enabled with threshold in the range of 85-175 mVdfpp. 11 = Reserved.	RW
4/5.36868.5:4	ALIGN	Receiver symbol alignment selection 00 = Alignment disabled. 01 = Comma alignment enabled 10 = Symbol alignment will be performed by one bit position when this mode is selected (i.e ALIGN changes from 00 to 10) 11= Reserved	RW
4/5.36868.3:2	TERM	Receive Termination selection 00 = Common point connected to VDDT (For DC Coupled Systems) 01 = Common point set to 0.8 VDDT (For AC Coupled Systems) 10 = Reserved 11 = Reserved	RW
4/5.36868.1	ENTEST	1= Enables test modes specified in TESTCFG (Register 0x9012)	RW

(1) These are SERDES receiver control bits for channel 1.

Table 2-97. SERDES_RX1_CONFIG (1) (continued)

ADDRESS: 0x9004		DEFAULT: 0x0001	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36868.0	ENRX	1 = Enables receiver 0 = Disables receiver	RW

Table 2-98. SERDES_RX2_CONFIG(1)

ADDRESS: 0x9006		DEFAULT: 0x0001	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36870.15:12	EQUALIZER	Adaptive equalization control 0000 = Adaptive equalization disabled. Equalizer provides flat response at maximum gain. 0001 = Full adaptive equalization 0010 to 1111 = Reserved	RW
4/5.36870.11:9	CDR	Clock data recovery algorithm selection	RW
4/5.36870.8	INVPAIR	1 = Inverts polarity of RXP and RXN	RW
4/5.36870.7:6	LOS	00 = Loss of signal detection disabled 01 = Reserved 10 = Loss of signal detection enabled with threshold in the range of 85-175 mVdfpp. 11 = Reserved.	RW
4/5.36870.5:4	ALIGN	Receiver symbol alignment selection 00 = Alignment disabled. 01 = Comma alignment enabled 10 = Symbol alignment will be performed by one bit position when this mode is selected (i.e ALIGN changes from 00 to 10) 11= Reserved	RW
4/5.36870.3:2	TERM	Receive Termination selection 00 = Common point connected to VDDT (For DC Coupled Systems) 01 = Common point set to 0.8 VDDT (For AC Coupled Systems) 10 = Reserved 11 = Reserved	RW
4/5.36870.1	ENTEST	1= Enables test modes specified in TESTCFG (Register 0x9012)	RW
4/5.36870.0	ENRX	1 = Enables receiver 0 = Disables receiver	RW

(1) These are SERDES receiver control bits for channel 2.

Table 2-99. SERDES_RX3_CONFIG(1)

ADDRESS: 0x9008		DEFAULT: 0x0001	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36872.15:12	EQUALIZER	Adaptive equalization control 0000 = Adaptive equalization disabled. Equalizer provides flat response at maximum gain. 0001 = Full adaptive equalization 0010 to 1111 = Reserved	RW
4/5.36872.11:9	CDR	Clock data recovery algorithm selection	RW
4/5.36872.8	INVPAIR	1 = Inverts polarity of RXP and RXN	RW
4/5.36872.7:6	LOS	00 = Loss of signal detection disabled 01 = Reserved 10 = Loss of signal detection enabled with threshold in the range of 85-175 mVdfpp. 11 = Reserved.	RW

(1) These are SERDES receiver control bits for channel 3.

Table 2-99. SERDES_RX3_CONFIG (1) (continued)

ADDRESS: 0x9008		DEFAULT: 0x0001	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36872.5:4	ALIGN	Receiver symbol alignment selection 00 = Alignment disabled. 01 = Comma alignment enabled 10 = Symbol alignment will be performed by one bit position when this mode is selected (i.e ALIGN changes from 00 to 10) 11= Reserved	RW
4/5.36872.3:2	TERM	Receive Termination selection 00 = Common point connected to VDDT (For DC Coupled Systems) 01 = Common point set to 0.8 VDDT (For AC Coupled Systems) 10 = Reserved 11 = Reserved	RW
4/5.36872.1	ENTEST	1= Enables test modes specified in TESTCFG (Register 0x9012)	RW
4/5.36872.0	ENRX	1 = Enables receiver 0 = Disables receiver	RW

Table 2-100. SERDES_TX0_CONFIG (1)

ADDRESS: 0x900A		DEFAULT: 0x0001	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36874.15:12	Reserved	Always reads 0	RW
4/5.36874.11:9	SWING	Transmitter Output swing control for SERDES transmitter. Refer Table 2-105: Output swing Control If swing is set to 750mV or more, CM bit (4/5.36874.8) needs to be set to 1. If swing is set to 625 mV or less, CM bit (4/5.36874.8) needs to be set to 0.	RW
4/5.36874.8	CM	1 = Applicable for SWING settings 750 mV or more. 0 = Applicable for SWING settings 625 mV or less.	RW
4/5.36874.7:4	DE-EMPHASIS	Transmitter Differential output De-emphasis control Refer Table 2-104: Transmit De-emphasis Control	RW
4/5.36874.3	INVPAIR	Transmitter Polarity 1 = Inverted polarity. TXP considered negative data and TXN considered positive data 0 = Normal polarity. TXP considered positive data and TXN considered negative data	RW
4/5.36874.2	Reserved	Always reads 0	RW
4/5.36874.1	ENTEST	1= Enables test modes specified in TESTCFG (Register 0x9011)	RW
4/5.36874.0	ENTX	1 = Enables transmitter 0 = Disables transmitter	RW

(1) These are SERDES transmitter control bits for channel 0.

Table 2-101. SERDES_TX1_CONFIG (1)

ADDRESS: 0x900C		DEFAULT: 0x0001	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36876.15:12	Reserved	Always reads 0	RW
4/5.36876.11:9	SWING	Transmitter Output swing control for SERDES transmitter. Refer Table 2-105: Output swing Control If swing is set to 750mV or more, CM bit (4/5.36876.8) needs to be set to 1. If swing is set to 625 mV or less, CM bit (4/5.36876.8) needs to be set to 0.	RW
4/5.36876.8	CM	1 = Applicable for SWING settings 750 mV or more. 0 = Applicable for SWING settings 625 mV or less.	RW

(1) These are SERDES transmitter control bits for channel 1.

Table 2-101. SERDES_TX1_CONFIG (1) (continued)

ADDRESS: 0x900C		DEFAULT: 0x0001	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36876.7:4	DE-EMPHASIS	Transmitter Differential output De-emphasis control Refer Table 2-104: Transmit De-emphasis Control	RW
4/5.36876.3	INVPAIR	Transmitter Polarity 1 = Inverted polarity. TXP considered negative data and TXN considered positive data 0 = Normal polarity. TXP considered positive data and TXN considered negative data	RW
4/5.36876.2	Reserved	Always reads 0	RW
4/5.36876.1	ENTEST	1= Enables test modes specified in TESTCFG (Register 0x9011)	RW
4/5.36876.0	ENTX	1 = Enables transmitter 0 = Disables transmitter	RW

Table 2-102. SERDES_TX2_CONFIG (1)

ADDRESS: 0x900E		DEFAULT: 0x0001	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36878.15:12	Reserved	Always reads 0	RW
4/5.36878.11:9	SWING	Transmitter Output swing control for SERDES transmitter Refer Table 2-105: Output swing Control If swing is set to 750mV or more, CM bit (4/5.36878.8) needs to be set to 1. If swing is set to 625 mV or less, CM bit (4/5.36878.8) needs to be set to 0.	RW
4/5.36878.8	CM	1 = Applicable for SWING settings 750 mV or more. 0 = Applicable for SWING settings 625 mV or less.	RW
4/5.36878.7:4	DE-EMPHASIS	Transmitter Differential output De-emphasis control Refer Table 2-104: Transmit De-emphasis Control	RW
4/5.36878.3	INVPAIR	Transmitter Polarity 1 = Inverted polarity. TXP considered negative data and TXN considered positive data 0 = Normal polarity. TXP considered positive data and TXN considered negative data	RW
4/5.36878.2	Reserved	Always reads 0	RW
4/5.36878.1	ENTEST	1= Enables test modes specified in TESTCFG (Register 0x9011)	RW
4/5.36878.0	ENTX	1 = Enables transmitter 0 = Disables transmitter	RW

(1) These are SERDES transmitter control bits for channel 2.

Table 2-103. SERDES_TX3_CONFIG (1)

ADDRESS: 0x9010		DEFAULT: 0x0001	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36880.15:12	Reserved	Always reads 0	RW
4/5.36880.11:9	SWING	Transmitter Output swing control for SERDES transmitter Refer Table 2-105: Output swing Control If swing is set to 750mV or more, CM bit (4/5.36880.8) needs to be set to 1. If swing is set to 625 mV or less, CM bit (4/5.36880.8) needs to be set to 0.	RW
4/5.36880.8	CM	1 = Applicable for SWING settings 750 mV or more. 0 = Applicable for SWING settings 625 mV or less.	RW
4/5.36880.7:4	DE-EMPHASIS	Transmitter Differential output De-emphasis control Refer Table 2-104: Transmit De-emphasis Control	RW

(1) These are SERDES transmitter control bits for channel 3.

Table 2-103. SERDES_TX3_CONFIG (1) (continued)

ADDRESS: 0x9010		DEFAULT: 0x0001	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36880.3	INVPAIR	Transmitter Polarity 1 = Inverted polarity. TXP considered negative data and TXN considered positive data 0 = Normal polarity. TXP considered positive data and TXN considered negative data	RW
4/5.36880.2	Reserved	Always reads 0	RW
4/5.36880.1	ENTEST	1= Enables test modes specified in TESTCFG (Register 0x9011)	RW
4/5.36880.0	ENTX	1 = Enables transmitter 0 = Disables transmitter	RW

Table 2-104. Transmit De-emphasis Control

4/5.36874/36876/36878/36880 [7:4]					
VALUE	**AMPLITUDE REDUCTION**		**VALUE**	**AMPLITUDE REDUCTION**	
	%	**dB**		**%**	**dB**
0000	0	0	1000	38.08	-4.16
0001	4.76	-0.42	1001	42.85	-4.86
0010	9.52	-0.87	1010	47.61	-5.61
0011	14.28	-1.34	1011	52.38	-6.44
0100	19.04	-1.83	1100	57.14	-7.35
0101	23.8	-2.36	1101	61.9	-8.38
0110	28.56	-2.92	1110	66.66	-9.54
0111	33.32	-3.52	1111	71.42	-10.87

Table 2-105. Output Swing Control

4/5.36874/36876/36878/36880 [11:9]			
VALUE	**AMPLITUDE (mVdfpp)**	**VALUE**	**AMPLITUDE (mVdfpp)**
000	125	100	750
001	250	101	1000
010	500	110	1250
011	625	111	1375

Table 2-106. SERDES_TEST_CONFIG_TX(1)

ADDRESS: 0x9011		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36881.10:8	Reserved	Reserved for TI test	RW
4/5.36881.7:6	LOOPBACK_TX	00 = Disabled 01 = Pad loopback. For TI purposes only 10 = Inner loopback (CML driver disabled) 11 = Inner loopback (CML driver enabled)	RW
4/5.36881.5:4	CLKBYPASS_TX	PLL Bypass control in test mode 00 = No bypass 01 = Reserved 10 = Functional bypass. Macros run using TESCLKT 11 = Refclk observe (Reserved. For TI purposes only)	RW
4/5.36881.3	ENRXPATT_TX	0 – Disables test pattern verification in SERDES TX macro. 1 – Enables test pattern verification in SERDES TX macro.	RW
4/5.36881.2	ENTXPATT_TX	0 – Disables test pattern generation in SERDES TX macro. 1 – Enables test pattern generation in SERDES TX macro.	RW

(1) Above control bits are only for vendor testing only. Customer should leave them at their default values

Table 2-106. SERDES_TEST_CONFIG_TX (1) (continued)

ADDRESS: 0x9011		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36881.1:0	TESTPATT_TX	Valid when ENTXPATT_TX, ENRXPATT_TX, ENTEST_TX are set 00 = Reserved (Default) 01 = Clock pattern (Half baud clock pattern with period of 2UI) 10 = 2^7 - 1 PRBS pattern 11 = 2^{23} – 1 PRBS pattern	RW

Table 2-107. SERDES_TEST_CONFIG_RX(1)

ADDRESS: 0x9012		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36882.10:8	Reserved	Reserved for TI test.	RW
4/5.36882.7:6	LOOPBACK_RX	00 = Disabled 01 = Pad loopback. For TI purposes only 10 = Inner loopback (CML driver disabled) 11 = Inner loopback (CML driver enabled)	RW
4/5.36882.5:4	CLKBYPASS_RX	PLL Bypass control in test mode 00 = No bypass 01 = Reserved 10 = Functional bypass. Macros run using TESCLKR 11 = Refclk observe (Reserved. For TI purposes only)	RW
4/5.36882.3	ENRXPATT_RX	0 – Disables test pattern verification in SERDES RX macro. 1 – Enables test pattern verification in SERDES RX macro.	RW
4/5.36882.2	ENTXPATT_RX	0 – Disables test pattern generation in SERDES RX macro. 1 – Enables test pattern generation in SERDES RX macro.	RW
4/5.36882.1:0	TESTPATT_RX	Valid when ENTXPATT_RX, ENRXPATT_RX, ENTEST_RX are set 00 = Reserved (Default) 01 = Clock pattern (Half baud clock pattern with period of 2UI) 10 = 2^7 – 1 PRBS pattern 11 = 2^{23} – 1 PRBS pattern	RW

(1) Above control bits are only for vendor testing only. Customer should leave them at their default values

Table 2-108. SERDES_RX0_STATUS(1)

ADDRESS: 0x9013		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36883.3	LOSDTCT	When HIGH indicates Loss of Signal condition is detected for RX CH 0	RO
4/5.36883.2	ODDCG	LOW when SYNC is HIGH. After that toggles every cycle.	RO
4/5.36883.1	SYNC	When comma detection is enabled, this bit is HIGH when an aligned comma is received.	RO
4/5.36883.0	RX CH 0 TESTFAIL	When HIGH, indicates an error occurred during test pattern verification for SERDES RX CH 0. When ST = 0, this bit status is valid when PRBS_EN pin is set or when SERDES RX test pattern registers bits are set When ST = 1, this bit status is valid only when SERDES RX test pattern verification bits are set	RO

(1) Above status bits are only for Receive CH 0.

Table 2-109. SERDES_RX1_STATUS(1)

ADDRESS: 0x9014		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36884.3	LOSDTCT	When HIGH indicates Loss of Signal condition is detected for RX CH 1	RO
4/5.36884.2	ODDCG	LOW when SYNC is HIGH. After that toggles every cycle.	RO
4/5.36884.1	SYNC	When comma detection is enabled, this bit is HIGH when an aligned comma is received.	RO
4/5.36884.0	RX CH 1 TESTFAIL	When HIGH, indicates an error occurred during test pattern verification for SERDES RX CH 1. When ST = 0, this bit status is valid when PRBS_EN pin is set or when SERDES RX test pattern registers bits are set When ST = 1, this bit status is valid only when SERDES RX test pattern verification bits are set	RO

(1) Above status bits are only for Receive CH 1.

Table 2-110. SERDES_RX2_STATUS(1)

ADDRESS: 0x9015		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36885.3	LOSDTCT	When HIGH indicates Loss of Signal condition is detected for RX CH 2	RO
4/5.36885.2	ODDCG	LOW when SYNC is HIGH. After that toggles every cycle.	RO
4/5.36885.1	SYNC	When comma detection is enabled, this bit is HIGH when an aligned comma is received.	RO
4/5.36885.0	RX CH 2 TESTFAIL	When HIGH, indicates an error occurred during test pattern verification for SERDES RX CH 2. When ST = 0, this bit status is valid when PRBS_EN pin is set or when SERDES RX test pattern registers bits are set When ST = 1, this bit status is valid only when SERDES RX test pattern verification bits are set	RO

(1) Above status bits are only for Receive CH 2.

Table 2-111. SERDES_RX3_STATUS(1)

ADDRESS: 0x9016		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36886.3	LOSDTCT	When HIGH indicates Loss of Signal condition is detected for RX CH 3	RO
4/5.36886.2	ODDCG	LOW when SYNC is HIGH. After that toggles every cycle.	RO
4/5.36886.1	SYNC	When comma detection is enabled, this bit is HIGH when an aligned comma is received.	RO
4/5.36886.0	RX CH 3 TESTFAIL	When HIGH, indicates an error occurred during test pattern verification for SERDES RX CH 3 When ST = 0, this bit status is valid when PRBS_EN pin is set or when SERDES RX test pattern registers bits are set When ST = 1, this bit status is valid only when SERDES RX test pattern verification bits are set	RO

(1) Above status bits are only for Receive CH 3.

Table 2-112. SERDES_TX0_STATUS(1)

ADDRESS: 0x9017		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36887.0	TX CH 0 TESTFAIL	When HIGH, indicates an error occurred during test pattern verification for SERDES TX CH 0.	RO

(1) Above status bits are only for Transmit CH 0.

Table 2-113. SERDES_TX1_STATUS(1)

ADDRESS: 0x9018		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36888.0	TX CH 1 TESTFAIL	When HIGH, indicates an error occurred during test pattern verification for SERDES TX CH 1.	RO

(1) Above status bits are only for Transmit CH 1.

Table 2-114. SERDES_TX2_STATUS(1)

ADDRESS: 0x9019		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36889.0	TX CH 2 TESTFAIL	When HIGH, indicates an error occurred during test pattern verification for SERDES TX CH 2.	RO

(1) Above status bits are only for Transmit CH 2.

Table 2-115. SERDES_TX3_STATUS(1)

ADDRESS: 0x901A		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36890.0	TX CH 3 TESTFAIL	When HIGH, indicates an error occurred during test pattern verification for SERDES TX CH 3.	RO

(1) Above status bits are only for Transmit CH 3.

Table 2-116. SERDES_PLL_STATUS

ADDRESS: 0x901B		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.36891.4	PLL_LOCK_RX	1 = Indicates PLL is locked within 10ppm of REFCLKP/N in SERDES RX macro	RO/LL
4/5.36891.0	PLL_LOCK_TX	1 = Indicates PLL is locked within 10ppm of REFCLKP/N in SERDES TX macro	

Table 2-117. JC_CLOCK_MUX_CONTROL

ADDRESS: 0x9100		DEFAULT: 0x3FF0	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37120.15:14	REF_SEL[1:0]	Jitter Cleaner Reference clock select control 00 = Selects differential REFCLKP/N as jitter cleaner clock input 01 = Selects CMOS REFCLK as jitter cleaner clock input 10 = Selects recovered clock as jitter cleaner clock input 11 = Reserved	RW
4/5.37120.13:12	RXB_SEL[1:0]	Jitter Cleaner RXBYTECLK select control 00 = Selects RXB_DIV divider output clock as RXBYTECLK 01 = Selects recovered clock as RXBYTECLK 10 = Selects CMOS REFCLK as RXBYTECLK 11 = Selects differential REFCLKP/N as RXBYTECLK	RW
4/5.37120.11:10	TX_SEL[1:0]	Jitter Cleaner SERDES TX Reference clock input select control 00 = Selects jitter cleaner output clock as TX SERDES reference clock input 01 = Selects recovered clock as TX SERDES reference clock input 10 = Selects CMOS REFCLK as TX SERDES reference clock input 11 = Selects differential REFCLKP/N as TX SERDES reference clock input	RW
4/5.37120.9:8	RX_SEL[1:0]	Jitter Cleaner SERDES RX Reference clock input select control 00 = Selects jitter cleaner output clock as RX SERDES reference clock input 01 = Selects recovered clock as RX SERDES reference clock input (Not Recommended) 10 = Selects CMOS REFCLK as RX SERDES reference clock input 11 = Selects differential REFCLKP/N as RX SERDES reference clock input	RW
4/5.37120.7:6	DEL_SEL[1:0]	Delay stopwatch clock input select control 00 = Selects delay clock divider output clock as delay stopwatch clock input 01 = Selects recovered clock as delay stopwatch clock input 10 = Selects CMOS REFCLK as delay stopwatch clock input 11 = Selects differential REFCLKP/N as delay stopwatch clock input	RW
4/5.37120.5:4	HSTL_SEL[1:0]	HSTL VTP 2x clock divider input select control 00 = Selects HSTL DIV clock output as HSTL VTP 2x clock divider input 01 = Selects recovered clock as HSTL VTP 2x clock divider input 10 = Selects CMOS REFCLK as HSTL VTP 2x clock divider input 11 = Selects differential REFCLKP/N as HSTL VTP 2x clock divider input	RW

Table 2-118. JC_VTP_CLK_DIV_CONTROL

ADDRESS: 0x9101		DEFAULT: 0x0E06	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37121.14:8	HSTL_DIV[6:0]	HSTL Output Divider 1 Value. See Figure 1-3. This value is the divider value for the clock which runs the HSTL impedance compensation controller. The target output frequency for the impedance controller clock is 40 Mhz. If the jitter cleaner is not enabled, this value is not used. Legal programmed values are greater than or equal to 6	RW
4/5.37121.6:0	HSTL_DIV2[6:0]	HSTL Output Divider 2 Value. See Figure 1-3. This value is the divider value for the HSTL impedance compensation controller. The target output frequency for this clock is 40 MHz. When the jitter cleaner (HSTL_DIV1) is used, this value should be provisioned to 6 decimal. When the jitter cleaner (HSTL_DIV1) is not used, this divider value should be provisioned according to the following equation: Value = (Parallel Output Byte Clock Frequency / 40 Mhz) Legal programmed values are 1, and greater than or equal to 4	RW

Table 2-119. JC_DELAY_STOPWATCH_CLK_DIV_CONTROL

ADDRESS: 0x9102		DEFAULT: 0x0600	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37122.14:8	DEL_DIV[6:0]	Delay Measurement Clock Output Divider Value. See Figure 1-3. Controls the clock divider for the delay stop watch function. This value should be provisioned to decimal 6.This value is only used when the delay calculator circuit is enabled. Legal programmed values are greater than or equal to 6	RW
4/5.37122.2:1	Delay stop watch lane select[1:0]	Lane select to enable comma monitor. Valid only when 37122:0 is “1” 00 = Comma monitor enabled on Lane 0 01 = Comma monitor enabled on Lane 1 10 = Comma monitor enabled on Lane 2 11 = Comma monitor enabled on Lane 3	RW
4/5.37122.0	Delay stop watch clock enable	When set, enables Delay stop watch clock	RW

Table 2-120. JC_DELAY_STOPWATCH_COUNTER

ADDRESS: 0x9103		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37123.15:0	Delay stop watch counter[15:0]	Delay Counter. This value represents the latency in number of clock cycles. This counter resets on read and will return 16’h0000 if its read before rx comma is received. If latency is more than 16’hFFFF clock cycles then this counter returns 16’hFFFF.	RO

Table 2-121. JC_REFCLK_FB_DIV_CONTROL

ADDRESS: 0x9104		DEFAULT: 0x018E	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37124.15	REFDIV_EN	1 = Enables Reference clock divider 0 = Disables Reference clock divider	RW
4/5.37124.14:8	REF_DIV[0:6]	Controls the clock divider value for the reference clock. See Figure 1-3, and Appendix A for provisioning details Note: REF_DIV[6:0] = 4/5.37124.8:14. (Example: To program REF_DIV to decimal value 4, 14:8 needs to be set to 7’b0010000)	RW
4/5.37124.7	FBDIV_EN	1 = Enables Feedback divider 0 = Disables feedback divider	RW

Table 2-121. JC_REFCLK_FB_DIV_CONTROL (continued)

ADDRESS: 0x9104		DEFAULT: 0x018E	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37124.6:0	FB_DIV[6:0]	Controls the feedback divider value See Figure 1-3, and Appendix A for provisioning details. Note: JC_CHARGE_PUMP_ CONTROL (4/5.37126) needs to be set accordingly based on FB_DIV range. Refer Table 2-124: Charge Pump Control Setting (CP_CTRL)	RW

Table 2-122. JC_RXB_OUTPUT_CLK_DIV_CONTROL

ADDRESS: 0x9105		DEFAULT: 0x0E8E	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37125.14:8	RXB_DIV[6:0]	Receive Byte Clock Output Divider Value. This divider value is always provisioned with the same value as RXTX_DIV[6:0]. See Figure 1-3, and Appendix A for provisioning details. This value is only used when the jitter cleaner is used to source the receive parallel interface output clock. Legal programmed values are greater than or equal to 6	RW
4/5.37125.7	OUTDIV_EN	1 = Enables output divider (RXTX_DIV) 0 = Disables output divider	RW
4/5.37125.6:0	RXTX_DIV[6:0]	RX/TX SERDES Output Divider Value See Figure 1-3, and Appendix A for provisioning details Legal programmed values are greater than or equal to 6	RW

Table 2-123. JC_CHARGE_PUMP_ CONTROL(1)

ADDRESS: 0x9106		DEFAULT: 0x00C0	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37126.15:14	CP_BUF_CTRL[1:0]	Charge pump buffer control	RW
4/5.37126.13:0	CP_CTRL[13:0]	Charge pump control. When JC PLL is used, CP_CTRL[13:0] values need to be set according to FB_DIV[6:0] range. Refer Table 2-124: Charge Pump Control Setting (CP_CTRL)	

(1) When JC PLL is used, this register value should be set according to the values specified in Charge Pump Control Setting Table

Table 2-124. Charge Pump Control Setting (CP_CTRL)

FB DIV VALUE RANGE (4/5.37124[6:0]) (IN DECIMAL)	JC_CHARGE_PUMP_ CONTROL SETTING (4/5. 37126 [15:0])
1 - 15	0x00FF
16 - 18	0x00C1
19 - 30	0x0081
31 - 33	0x017F
34 - 45	0x017D
46 - 53	0x011F
54 - 59	0x0151
60 - 68	0x0121
69 - 77	0x01C3
78 - 85	0x0101
86 - 88	0x02FB
89 - 91	0x0183
92 - 99	0x0237
100 - 107	0x0181
108 - 113	0x0261
114 - 127	0x0215

Table 2-125. JC_PLL_CONTROL

ADDRESS: 0x9107		DEFAULT: 0x30C4	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37127.15	JC_EN_PLL	0 = Disables Jitter Cleaner 1 = Enables Jitter Cleaner	RW
4/5.37127.14:12	VCO_BIAS_CTRL[2:0]	Control bits for VCO tail current	
4/5.37127.11:8	VCO_CAPBANK_CTRL[3:0]	Control bits for VCO band select	
4/5.37127.7	DIFFTX_EN	Enable signal for TX differential path	
4/5.37127.6	DIFFRX_EN	Enable signal for RX differential path	
4/5.37127.5:4	PFD_CTRL[1:0]	Control bits for phase frequency detector	
4/5.37127.3	AD_SEL_TST	Control bit to select either digital or analog TST_OUT	
4/5.37127.2	REFCLK_CML_EN	Enable signal for CML buffer inside output divider	

Table 2-126. JC_TEST_CONTROL_1 (1)

ADDRESS: 0x9108		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37128.15:12	REFCK_DIV_TST[3:0]	Test bits for Reference divider	RW
4/5.37128.11:8	FB_DIV_TST[3:0]	Test bits for Feedback divider	
4/5.37128.7:4	TXRX_DIV_TST[3:0]	Test bits for TXRX output divider. Should be set to 4'b1010 when JC PLL is used	
4/5.37128.3:2	RXBCLK_DIV_TST[1:0]	Test bits for RXBYTECLK divider	

(1) This register value should be written 0x00A0 when JC PLL is used

Table 2-127. JC_TEST_CONTROL_2

ADDRESS: 0x9109		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37129.15:14	DEL_DIV_TST[1:0]	Test bits for Delay clock divider	RW
4/5.37129.13:12	HSTL_DIV_TST[1:0]	Test bits for HSTL VTP divider	
4/5.37129.11:10	HSTL_DIV2_TST[1:0]	Test bits for HSTL VTP 2X divider	
4/5.37129.9:8	PFD_TST[1:0]	Test bits for Phase frequency detector	
4/5.37129.7:4	CP_TST[3:0]	Test bits for Charge pump	
4/5.37129.3:0	CP_BUF_TST[3:0]	Test bits for Charge pump Buffer	

Table 2-128. JC_TI_TEST_CONTROL_1

ADDRESS: 0x9150		DEFAULT:0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37200.15:8	CML_BIAS_TST[7:0]	Test bits for Bias generator for CML divider. For TI purposes only.	RW
4/5.37200.7:4	CML_BIAS_CTRL[3:0]	Control bits for Bias generator for CML divider. For TI purposes only.	
4/5.37200.3	DIFFTX_ENTST	Enable for TX clock out from SERDES REFCLK MUX. For TI purposes only.	
4/5.37200.2	DIFFRX_ENTST	Enable for RX clock out from SERDES REFCLK MUX. For TI purposes only.	

Table 2-129. JC_TI_TEST_CONTROL_2

ADDRESS: 0x9151		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37201.15:13	VCO_FILCAP_CTRL[2:0]	Control bits for VCO tail current noise filter. For TI purposes only.	RW
4/5.37201.12:10	ANA_MUX_CTRL[2:0]	Control bits to select the tested signals. For TI purposes only.	

Table 2-130. JC_TRIM_STATUS

ADDRESS: 0x9152		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37202.9:0	JC_TRIM[9:0]	Jitter Cleaner Resistor Trim value	RO

Table 2-131. DIE_ID_7

ADDRESS: 0x9200		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37376.15:0	Die ID [127:112]	Bits [127:112] of the Die ID. Unique TI DIE identifier.	RO

Table 2-132. DIE_ID_6

ADDRESS: 0x9201		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37377.15:0	Die ID [111:96]	Bits [111:96] of the Die ID. Unique TI DIE identifier.	RO

Table 2-133. DIE_ID_5

ADDRESS: 0x9202		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37378.15:0	Die ID [95:80]	Bits [95:80] of the Die ID. Unique TI DIE identifier.	RO

Table 2-134. DIE_ID_4

ADDRESS: 0x9203		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37379.15:0	Die ID [79:64]	Bits [79:64] of the Die ID. Unique TI DIE identifier.	RO

Table 2-135. DIE_ID_3

ADDRESS: 0x9204		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37380.15:0	Die ID [63:48]	Bits [63:48] of the Die ID. Unique TI DIE identifier.	RO

Table 2-136. DIE_ID_2

ADDRESS: 0x9205		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37381.15:0	Die ID [47:32]	Bits [47:32] of the Die ID. Unique TI DIE identifier.	RO

Table 2-137. DIE_ID_1

ADDRESS: 0x9206		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37382.15:0	Die ID [31:16]	Bits [31:16] of the Die ID. Unique TI DIE identifier.	RO

Table 2-138. DIE_ID_0

ADDRESS: 0x9207		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37383.15:0	Die ID [15:0]	Bits [15:0] of the Die ID. Unique TI DIE identifier.	RO

Table 2-139. EFUSE_STATUS

ADDRESS: 0x9208		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37384.8	EFC ready	When high, indicates that EFUSE autoload operation has completed	RO
4/5.37384.4:0	EFC error[4:0]	Efuse error bus. Updated when EFC_ready goes high or when instruction is complete. Non-zero value indicates error condition.	

Table 2-140. EFUSE_CONTROL

ADDRESS: 0x9209		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37385.15	EFUSE Auto Load Enable	When HIGH, Re-enables EFUSE Auto load function. Needs to set back to LOW to complete Auto load function.	RW

Table 2-141. HSTL_INPUT_TERMINATION_CONTROL

ADDRESS: 0x9300		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37632.15:14	HSTL_TERM_3[1:0]	Termination setting for input HSTL cells (for CH 3) 00 = Termination disable (High Impedance) 01 = Half termination strength (300 Ω to VHSTL&GND) 10 = 3/4 termination strength (200 Ω to VHSTL&GND) 11 = Full termination strength (150 Ω to VHSTL&GND)	RW
4/5.37632.11:10	HSTL_TERM_2[1:0]	Termination setting for input HSTL cells (for CH 2) 00 = Termination disable (High Impedance) 01 = Half termination strength (300 Ω to VHSTL&GND) 10 = 3/4 termination strength (200 Ω to VHSTL&GND) 11 = Full termination strength (150 Ω to VHSTL&GND)	RW
4/5.37632.7:6	HSTL_TERM_1[1:0]	Termination setting for input HSTL cells (for CH 1) 00 = Termination disable (High Impedance) 01 = Half termination strength (300 Ω to VHSTL&GND) 10 = 3/4 termination strength (200 Ω to VHSTL&GND) 11 = Full termination strength (150 Ω to VHSTL&GND)	RW
4/5.37632.3:2	HSTL_TERM_0[1:0]	Termination setting for input HSTL cells (for CH 0) 00 = Termination disable 01 = Half termination strength (300 Ω to VHSTL&GND) 10 = 3/4 termination strength (200 Ω to VHSTL&GND) 11 = Full termination strength (150 Ω to VHSTL&GND)	RW

Table 2-142. HSTL_OUTPUT_SLEWRATE_CONTROL

ADDRESS: 0x9301		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37633.15:14	HSTL_SLEW_RATE_3 [1:0]	Slew Rate setting for output HSTL cells (for CH 3) 00 = No slew control (fastest edge) 01 = 33% slew control 10 = 66 % slew control termination strength 11 = Full slew control (slowest edge)	RW
4/5.37633.11:10	HSTL_SLEW_RATE_2 [1:0]	Slew Rate setting for output HSTL cells (for CH 2) 00 = No slew control (fastest edge) 01 = 33% slew control 10 = 66 % slew control termination strength 11 = Full slew control (slowest edge)	RW
4/5.37633.7:6	HSTL_SLEW_RATE_1 [1:0]	Slew Rate setting for output HSTL cells (for CH 1) 00 = No slew control (fastest edge) 01 = 33% slew control 10 = 66 % slew control termination strength 11 = Full slew control (slowest edge)	RW
4/5.37633.3:2	HSTL_SLEW_RATE_0 [1:0]	Slew Rate setting for output HSTL cells (for CH 0) 00 = No slew control (fastest edge) 01 = 33% slew control 10 = 66 % slew control termination strength 11 = Full slew control (slowest edge)	RW

Table 2-143. HSTL_INPUT_VTP_CONTROL

ADDRESS: 0x9302		DEFAULT: 0x0640	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37634.15	I_FORCE_UP_N	When set, increases NFET strength in all HSTL input cells. For TI purposes Only	RW
4/5.37634.14	I_FORCE_UP_P	When set, increases PFET strength in all HSTL input cells. For TI purposes Only	
4/5.37634.13	I_FORCE_DOWN_N	When set, decreases NFET strength in all HSTL input cells. For TI purposes Only	
4/5.37634.12	I_FORCE_DOWN_P	When set, decreases PFET strength in all HSTL input cells. For TI purposes Only	
4/5.37634.11:9	I_VTP_DRIVE[2:0]	Drive strength control for HSTL input cells 3'b000 = 30 % drive strength increase 3'b001 = 20% drive strength increase 3'b010 = 10% drive strength increase 3'b011 = Normal drive strength (default) 3'b100 = 10% drive strength decrease 3'b101 = 20% drive strength decrease 3'b110 = 30% drive strength decrease 3'b111 = 40% drive strength decrease	RW
4/5.37634.7:5	I_FILTER_CONTROL[2:0]	Filter Control 3'b000 = Impedance change filtering off 3'b001 = Update on 2 consecutive update requests 3'b010 = Update on 3 consecutive update requests(default) 3'b011 = Update on 4 consecutive update requests 3'b100 = Update on 5 consecutive update requests 3'b101 = Update on 6 consecutive update requests 3'b110 = Update on 7 consecutive update requests 3'b111 = Update on 8 consecutive update requests	RW
4/5.37634.3	I_LOCK	Impedance Lock Control When set, disables dynamic impedance control updates for HSTL input cells	RW

Table 2-144. HSTL_OUTPUT_VTP_CONTROL

ADDRESS: 0x9303		DEFAULT: 0x0640	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37635.15	O_FORCE_UP_N	When set, increases NFET strength in all HSTL output cells . For TI purposes Only	RW
4/5.37635.14	O_FORCE_UP_P	When set, increases PFET strength in all HSTL output cells . For TI purposes Only	
4/5.37635.13	O_FORCE_DOWN_N	When set, decreases NFET strength in all HSTL output cells . For TI purposes Only	
4/5.37635.12	O_FORCE_DOWN_P	When set, decreases PFET strength in all HSTL output cells . For TI purposes Only	
4/5.37635.11:9	O_VTP_DRIVE[2:0]	Drive strength control for HSTL output cells 3'b000 = 30 % drive strength increase 3'b001 = 20% drive strength increase 3'b010 = 10% drive strength increase 3'b011 = Normal drive strength(default) 3'b100 = 10% drive strength decrease 3'b101 = 20% drive strength decrease 3'b110 = 30% drive strength decrease 3'b111 = 40% drive strength decrease	RW
4/5.37635.7:5	O_FILTER_CONTROL[2:0]	Filter Control 3'b000 = Impedance change filtering off 3'b001 = Update on 2 consecutive update requests 3'b010 = Update on 3 consecutive update requests(default) 3'b011 = Update on 4 consecutive update requests 3'b100 = Update on 5 consecutive update requests 3'b101 = Update on 6 consecutive update requests 3'b110 = Update on 7 consecutive update requests 3'b111 = Update on 8 consecutive update requests	RW
4/5.37635.3	O_LOCK	Impedance Lock Control When set, disables dynamic impedance control updates for HSTL output cells	RW

Table 2-145. HSTL_GLOBAL_CONTROL

ADDRESS: 0x9304		DEFAULT: 0x0088	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37636.15	HSTL power down control	When set, triggers HSTL power down sequence and places all HSTL cells in power down state.	RW
4/5.37636.14	HSTL Retrain	When set, triggers retraining of all HSTL inputs and outputs to match the impedance. Retraining is triggered only when this bit value goes from 0 to 1. HSTL retraining should occur at the end of device provisioning.	RW
4/5.37636.11	HSTL_CLK_EN	HSTL impedance control clock (CLK2X) selection 1 = Uses MDC (MDIO clock) as CLK2X 0 = Uses clock generated from Jitter cleaner as CLK2X	RW
4/5.37636.7	Voltage reference selection	1 = Internal voltage reference used for HSTL input signals 0 = External voltage reference used for HSTL input signals	RW
4/5.37636.3	VTP POWERSAVE	When set, enables power save mode on HSTL VTP controllers	RW
4/5.37636.2	GP 3-state Control	When set, 3-states GP outputs	RW

Table 2-146. TX0_DLL_CONTROL

ADDRESS: 0x9400		DEFAULT: 0x0008	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37888.15	Lock_en	For TI use only	RW
4/5.37888.14	Write_en	For TI use only	
4/5.37888.13:8	Delay_sel[5:0]	DLL delay control. For TI use only	
4/5.37888.7:5	Offset[2:0]	Phase shift control. Adds or removes delay element. Each delay element is 0.15ns. Refer Table 2-154: DLL Offset Control	
4/5.37888.3	Filter_en	When asserted, the internal filter is used to reduce the cycle to cycle jitter of the output clock.	

Table 2-147. TX1_DLL_CONTROL

ADDRESS: 0x9401		DEFAULT: 0x0008	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37889.15	Lock_en	For TI use only	RW
4/5.37889.14	Write_en	For TI use only	
4/5.37889.13:8	Delay_sel[5:0]	DLL delay control. For TI use only	
4/5.37889.7:5	Offset[2:0]	Phase shift control. Adds or removes delay element. Each delay element is 0.15ns. Refer Table 2-154: DLL Offset Control	
4/5.37889.3	Filter_en	When asserted, the internal filter is used to reduce the cycle to cycle jitter of the output clock.	

Table 2-148. TX2_DLL_CONTROL

ADDRESS: 0x9402		DEFAULT: 0x0008	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37890.15	Lock_en	For TI use only	RW
4/5.37890.14	Write_en	For TI use only	
4/5.37890.13:8	Delay_sel[5:0]	DLL delay control. For TI use only	
4/5.37890.7:5	Offset[2:0]	Phase shift control. Adds or removes delay element. Each delay element is 0.15ns. Refer Table 2-154: DLL Offset Control	
4/5.37890.3	Filter_en	When asserted, the internal filter is used to reduce the cycle to cycle jitter of the output clock.	

Table 2-149. TX3_DLL_CONTROL

ADDRESS: 0x9403		DEFAULT: 0x0008	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37891.15	Lock_en	For TI use only	RW
4/5.37891.14	Write_en	For TI use only	
4/5.37891.13:8	Delay_sel[5:0]	DLL delay control. For TI use only	
4/5.37891.7:5	Offset[2:0]	Phase shift control. Adds or removes delay element. Each delay element is 0.15 ns. Refer Table 2-154: DLL Offset Control	
4/5.37891.3	Filter_en	When asserted, the internal filter is used to reduce the cycle to cycle jitter of the output clock.	

Table 2-150. RX0_DLL_CONTROL

ADDRESS: 0x9404		DEFAULT: 0x0008	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37892.15	Lock_en	For TI use only	RW
4/5.37892.14	Write_en	For TI use only	
4/5.37892.13:8	Delay_sel[5:0]	DLL delay control. For TI use only	
4/5.37892.7:5	Offset[2:0]	Phase shift control. Adds or removes delay element. Each delay element is 0.15 ns. Refer Table 2-154: DLL Offset Control	
4/5.37892.3	Filter_en	When asserted, the internal filter is used to reduce the cycle to cycle jitter of the output clock.	

Table 2-151. RX1_DLL_CONTROL

ADDRESS: 0x9405		DEFAULT: 0x0008	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37893.15	Lock_en	For TI use only	RW
4/5.37893.14	Write_en	For TI use only	
4/5.37893.13:8	Delay_sel[5:0]	DLL delay control. For TI use only	
4/5.37893.7:5	Offset[2:0]	Phase shift control. Adds or removes delay element. Each delay element is 0.15 ns. Refer Table 2-154: DLL Offset Control	
4/5.37893.3	Filter_en	When asserted, the internal filter is used to reduce the cycle to cycle jitter of the output clock.	

Table 2-152. RX2_DLL_CONTROL

ADDRESS: 0x9406		DEFAULT: 0x0008	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37894.15	Lock_en	For TI use only	RW
4/5.37894.14	Write_en	For TI use only	
4/5.37894.13:8	Delay_sel[5:0]	DLL delay control. For TI use only	
4/5.37894.7:5	Offset[2:0]	Phase shift control. Adds or removes delay element. Each delay element is 0.15 ns. Refer Table 2-154: DLL Offset Control	
4/5.37894.3	Filter_en	When asserted, the internal filter is used to reduce the cycle to cycle jitter of the output clock.	

Table 2-153. RX3_DLL_CONTROL

ADDRESS: 0x9407		DEFAULT: 0x0008	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37895.15	Lock_en	For TI use only	RW
4/5.37895.14	Write_en	For TI use only	
4/5.37895.13:8	Delay_sel[5:0]	DLL delay control. For TI use only	
4/5.37895.7:5	Offset[2:0]	Phase shift control. Adds or removes delay element. Each delay element is 0.15 ns. Refer Table 2-154: DLL Offset Control	
4/5.37895.3	Filter_en	When asserted, the internal filter is used to reduce the cycle to cycle jitter of the output clock.	

Table 2-154. DLL Offset Control

OFFSET[2:0]	
VALUE	**RESULT**
000	No delay elements are added

Table 2-154. DLL Offset Control (continued)

OFFSET[2:0]	
VALUE	**RESULT**
001	1 extra delay element is added
010	2 extra delay elements are added
011	3 extra delay elements are added
100	No delay elements are removed
101	1 extra delay element is removed
110	2 extra delay elements are removed
111	3 extra delay elements are removed

Table 2-155. TX0_DLL_STATUS

ADDRESS: 0x9408		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37896.5:0	Delay_status[5:0]	For TI use only.	RO

Table 2-156. TX1_DLL_STATUS

ADDRESS: 0x9409		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37897.5:0	Delay_status[5:0]	For TI use only.	RO

Table 2-157. TX2_DLL_STATUS

ADDRESS: 0x940A		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37898.5:0	Delay_status[5:0]	For TI use only.	RO

Table 2-158. TX3_DLL_STATUS

ADDRESS: 0x940B		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37899.5:0	Delay_status[5:0]	For TI use only.	RO

Table 2-159. RX0_DLL_STATUS

ADDRESS: 0x940C		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37900.5:0	Delay_status[5:0]	For TI use only.	RO

Table 2-160. RX1_DLL_STATUS

ADDRESS: 0x940D		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37901.5:0	Delay_status[5:0]	For TI use only.	RO

Table 2-161. RX2_DLL_STATUS

ADDRESS: 0x940E		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37902.5:0	Delay_status[5:0]	For TI use only.	RO

Table 2-162. RX3_DLL_STATUS

ADDRESS: 0x940F		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.37903.5:0	Delay_status[5:0]	For TI use only.	RO

Table 2-163. CH0_TESTFAIL_ERR_COUNTER

ADDRESS: 0x9500		DEFAULT: 0x00FD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.38144.7:0	Ch0_Testfail error counter[7:0]	This counter reflects error count during PRBS test. Counter increments for each received character that has an error. Counter clears upon read. When ST = 0, counter value is valid when PRBS_EN pin is set or when SERDES RX test pattern registers bits are set When ST = 1, counter value is valid only when SERDES RX test pattern verification bits are set	COR

Table 2-164. CH1_TESTFAIL_ERR_COUNTER

ADDRESS: 0x9501		DEFAULT: 0x00FD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.38145.7:0	Ch1_Testfail error counter[7:0]	This counter reflects error count during PRBS test. Counter increments for each received character that has an error. Counter clears upon read. When ST = 0, counter value is valid when PRBS_EN pin is set or when SERDES RX test pattern registers bits are set When ST = 1, counter value is valid only when SERDES RX test pattern verification bits are set	COR

Table 2-165. CH2_TESTFAIL_ERR_COUNTER

ADDRESS: 0x9502		DEFAULT: 0x00FD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.38146.7:0	Ch2_Testfail error counter	This counter reflects error count during PRBS test. Counter increments for each received character that has an error. Counter clears upon read. When ST = 0, counter value is valid when PRBS_EN pin is set or when SERDES RX test pattern registers bits are set When ST = 1, counter value is valid only when SERDES RX test pattern verification bits are set	COR

Table 2-166. CH3_TESTFAIL_ERR_COUNTER

ADDRESS: 0x9503		DEFAULT: 0x00FD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.38147.7:0	Ch3_Testfail error counter	This counter reflects error count during PRBS test. Counter increments for each received character that has an error. Counter clears upon read. When ST = 0, counter value is valid when PRBS_EN pin is set or when SERDES RX test pattern registers bits are set When ST = 1, counter value is valid only when SERDES RX test pattern verification bits are set	COR

Table 2-167. STCI_CONTROL_STATUS

ADDRESS: 0x9600		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.38400.15	STCI_CLK	Bit to generate STCI clock in functional mode.	RW
4/5.38400.11:10	STCI_CFG[1:0]	STCI CFG control	
4/5.38400.7	STCI_D	STCI data in	
4/5.38400.3	STCI_Q	STCI read data	RO

Table 2-168. TESTCLK_CONTROL

ADDRESS: 0x9601		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.38401.15	TESTCLKT	Bit to generate TESTCLKT clock in functional mode. For TI test purposes only	RW

Table 2-169. BIDI_CMOS_CONTROL

ADDRESS: 0x9700		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.38656.15	MDIO Disable Comp Test Control	0 = MDIO/MDC Bidi cells automatically detects operating voltage (Default) 1 = MDIO/MDC Bidi cells expects 2.5 V operating voltage	RW

Table 2-170. DEBUG_CONTROL

ADDRESS: 0x9800		DEFAULT: 0x001F	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.38912:8	DEBUG_SEL_EN	1 = Sends debug status signals onto debug outputs (GPO) 0 = Debug outputs are tied to 0. For TI test purposes only	RW
4/5.38912.7	DIG_TST_OUT_EN	1 = Enables sending DIG TST debug signal onto GPO4 0 = Disables sending DIG TST debug signal onto GPO4. For TI test purposes only	
4/5.38912.4:0	DEBUG_SEL	Debug select bits. For TI test purposes only	

Table 2-171. DUTY_CYCLE_CONTROL

ADDRESS: 0x9900		DEFAULT: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4/5.39168.15	Duty Cycle Correction Bypass	1 = Bypasses duty cycle corrected RX/TXBCLK. (Duty cycle set to 40-60, same clocks as SERDES parallel launch and capture clocks) 0 = Uses duty cycle corrected RX/TXBCLK. (Duty cycle set to 50-50, no phase relationship to SERDES parallel launch and capture clock)(Default) For TI test purposes only	RW

3 Device Reset Requirements/Procedure

3.1 XAUI MODE (XGMII)

REFCLK frequency = 156.25 MHz, Serdes Data Rate = Full Rate, Mode = Transceiver, Edge Mode = Source Centered, RX_CLK out = TXBCLK, Jitter Cleaner PLL Multiplier Ratio = 1X or Off

- Device Pin Setting(s) – Pin settings allow for maximum software configurability.
  - Ensure ST input pin is Low.
  - Ensure CODE input pin is Low.
  - Ensure PLOOP input pin is Low.
  - Ensure SLOOP input pin is Low.
  - Ensure SPEED [1:0] input pins are both High.
  - Ensure ENABLE input pin is High.
  - Ensure PRBS_EN input pin is Low.
- Reset Device
  - Issue a hard or soft reset (RST_N asserted for at least 10 us -or- Write 1'b1 to 4/5.0.15)
- Clock Configuration
  - If using JCPLL (JCPLL 1X)
    - JCPLL Mux Settings (see Figure 1-3)
      - Select REFCLK input (Default = Differential)
        - If Single Ended REFCLK used – Write 2'b01 to 4/5.37120.15:14
        - If Differential REFCLK used – Write 2'b00 to 4/5.37120.15:14
    - Write 2'b11 to 4/5.37120.13:12 to select differential REFCLKP/N as RXBYTECLK
    - Write 4'b0000 to 4/5.37120.11:8 to select jitter cleaned clock for SERDES TX/RX.
    - Write 2'b00 to 4/5.37120.5:4 to select jitter cleaned clock for HSTL VTP 2x
    - Write 2'b00 to 4/5.32810.15:14 to select SERDES TX clock as RX_CLK output
    - Write 16'h0081 to 4/5.37126 to set Charge pump control
    - Write 16'h00A0 to 4/5.37128 to set TXRX output divider
    - Clock Divide Settings (see Figure A-13)
      - Write 7'b1000000 to 4/5.37124.14:8 to set REF_DIV to value of 1
      - Write 1'b1 to 4/5.37124.15 REFDIV_EN to enable reference clock divider
      - Write 7'h14 to 4/5.37124.6:0 to set FB_DIV to value of 20
      - Write 1'b1 to 4/5.37124.7 FBDIV_EN to enable feedback divider
      - Write 7'h14 to 4/5.37125.6:0 to set RXTX_DIV to value of 20
      - Write 1'b1 to 4/5.37125.7 OUTDIV_EN to enable output divider
      - Write 7'h0D to 4/5.37121.14:8 to set HSTL_DIV to value of 13
      - Write 7'h06 to 4/5.37121.6:0 to set HSTL_DIV2 to value of 6
      - Write 2'b11 to 4/5.36864.14:13 to set RX Loop Bandwidth
      - Write 2'b11 to 4/5.36864.6:5 to set TX Loop Bandwidth
      - Write 4'b0101 to 4/5.36864.11:8 to set MPY RX multiplier factor to 10
      - Write 4'b0101 to 4/5.36864.3:0 to set MPY TX multiplier factor to 10
      - Write 16'h0000 to 4/5.36865 SERDES_RATE_CONFIG_TX_RX to set Full Rate
      - Write 3'b000 to 4/5.37127.14:12 to set control bits for VCO tail current to 0
      - Write 1'b1 to 4/5.37127.15 to enable Jitter Cleaner
      - Wait 50 ms in order for JCPLL to lock
  - If using clock bypass mode (JCPLL Off)
    - JCPLL Mux Settings (see Figure 1-3)
      - Select REFCLK input (Default = Differential)

  - If Single Ended REFCLK used – Write 2'b01 to 4/5.37120.15:14
  - If Differential REFCLK used – Write 2'b00 to 4/5.37120.15:14
- Select RXBYTE_CLK (Default = Differential)
  - If Single Ended REFCLK used – Write 2'b10 to 4/5.37120.13:12
  - If Differential REFCLK used – Write 2'b11 to 4/5.37120.13:12
- Select SERDES TX Reference Clock Input (Default = Differential)
  - If Single Ended REFCLK used – Write 2'b10 to 4/5.37120.11:10
  - If Differential REFCLK used – Write 2'b11 to 4/5.37120.11:10
- Select SERDES RX Reference Clock Input (Default = Differential)
  - If Single Ended REFCLK used – Write 2'b10 to 4/5.37120.9:8
  - If Differential REFCLK used – Write 2'b11 to 4/5.37120.9:8
- Select HSTL_2X_CLK (Default = Differential)
  - Write 2'b01 to 4/5.37120.5:4 to select RX SERDES recovered clock as HSTL_2X_CLK
- Write 2'b00 to 4/5.32810.15:14 to select SERDES TX clock as RX_CLK output
- Write 7'h04 to 4/5.37121.6:0 to set HSTL_DIV2 to value of 4.
- Write 16'h0000 to 4/5.36865 SERDES_RATE_CONFIG_TX_RX to set Full Rate

- Mode Control (see Table 2-2)
  - Write 1'b1 to 4/5.32809.15 XAUI_ORDER
  - Write 1'b0 to 4/5.32808.15 to set source centered data for TX side
  - Write 1'b0 to 4/5.32808.11 to set source centered data for RX side
  - Write 1'b0 to 4/5.32792.1 to disable XAUI data loop back
  - Write 1'b0 to 4/5.32792.0 to disable XGMII data loop back
  - Write 1'b0 to 4/5.0.14 to disable loop back mode
  - Write 3'b110 to 4/5.36874.11:9 to set lane 0 TX swing setting amplitude to 1250 mVdfpp
  - Write 1'b1 to 4/5.36874.8 to set channel 0 TX CM bit
  - Write 3'b110 to 4/5.36876.11:9 to set lane 1 TX swing setting amplitude to 1250 mVdfpp
  - Write 1'b1 to 4/5.36876.8 to set channel 1 TX CM bit
  - Write 3'b110 to 4/5.36878.11:9 to set lane 2 TX swing setting amplitude to 1250 mVdfpp
  - Write 1'b1 to 4/5.36878.8 to set channel 2 TX CM bit
  - Write 3'b110 to 4/5.36880.11:9 to set lane 3 TX swing setting amplitude to 1250 mVdfpp
  - Write 1'b1 to 4/5.36880.8 to set channel 3 TX CM bit
- RX equalization settings
  - Write 4'b0001 to 4/5.36866.15:12 to turn on adaptive equalization (4'b0000 is off)
  - Write 4'b0001 to 4/5.36868.15:12 to turn on adaptive equalization (4'b0000 is off)
  - Write 4'b0001 to 4/5.36870.15:12 to turn on adaptive equalization (4'b0000 is off)
  - Write 4'b0001 to 4/5.36872.15:12 to turn on adaptive equalization (4'b0000 is off)
  - Write 2'b01 to 4/5.36866.3:2 for AC coupled mode (2'b00 is DC coupled mode)
  - Write 2'b01 to 4/5.36868.3:2 for AC coupled mode (2'b00 is DC coupled mode)
  - Write 2'b01 to 4/5.36870.3:2 for AC coupled mode (2'b00 is DC coupled mode)
  - Write 2'b01 to 4/5.36872.3:2 for AC coupled mode (2'b00 is DC coupled mode)
- TX DLL Offset
  - Write 16'h0028 to 4/5.37888 TX0_DLL_CONTROL
  - Write 16'h0028 to 4/5.37889 TX1_DLL_CONTROL
  - Write 16'h0028 to 4/5.37890 TX2_DLL_CONTROL
  - Write 16'h0028 to 4/5.37891 TX3_DLL_CONTROL
- Poll Serdes PLL Status for Locked State
  - Read 4/5.36891.4,0 SERDES_PLL_STATUS – PLL_LOCK_TX/RX

  - Keep polling until both bits are high.
- Issue Data path Reset
  - Write 1'b1 to 4/5.32800.15
- Clear Latched Registers
  - Read 4/5.1 XS_STATUS_1 to clear
  - Read 4/5.8 XS_STATUS_2 to clear
  - Read 4/5.32770 TX_FIFO_STATUS to clear
  - Read 4/5.32771 TX_FIFO_DROP_COUNT to clear
  - Read 4/5.32772 TX_FIFO_INSERT_COUNT to clear
  - Read 4/5.32773 TX_CODEGEN_STATUS to clear
  - Read 4/5.(32780,1,2,3) LANE_0~3_EOP_ERROR_COUNT to clear
  - Read 4/5.(32784,5,6,7) LANE_0~3_CODE_ERROR_COUNT to clear
  - Read 4/5.32789 RX_LANE_ALIGN_STATUS to clear
  - Read 4/5.32790 RX_CHANNEL_SYNC_STATUS to clear
  - Read 4/5.32794 RX_CTC_STATUS to clear
  - Read 4/5.32795 RX_CTC_INSERT_COUNT to clear
  - Read 4/5.32796 RX_CTC_DELETE_COUNT to clear
  - Read 4/5.32797 DATA_DOWN to clear
  - Read 4/5.32799 CLOCK_DOWN_STATUS to clear
  - Read 4/5.36891 SERDES_PLL_STATUS to clear
- Operational Mode Status
  - Read Verify 4/5.1.7 XS_STATUS_1 – Fault (1'b0)
  - Read Verify 4/5.1.2 XS_STATUS_1 – XS Transmit Link Status (1'b1)
  - Read Verify 4/5.8.11 XS_STATUS_2 – Transmit fault (1'b0)
  - Read Verify 4/5.8.10 XS_STATUS_2 – Receive fault (1'b0)
  - Read Verify 4/5.24.12 XS_LANE_STATUS – Align status (1'b1)
  - Read Verify 4/5.32773.6:0 TX_CODEGEN_STATUS (6'b000000)
  - Read Verify 4/5.24.3:0 XS_LANE_STATUS – Lane (3-0) sync (4'b1111)
  - Read Verify 4/5.36891.4 SERDES_PLL_STATUS – PLL_LOCK_RX (1'b1)
  - Read Verify 4/5.36891.0 SERDES_PLL_STATUS – PLL_LOCK_TX (1'b1)

3.2 Gigabit Ethernet Mode (RGMII)

NOTE

All global registers must be accessed indirectly through Clause 22.

REFCLK frequency = 125 MHz, Serdes Data Rate = Half Rate, Mode = Transceiver, Edge Mode = Source Centered Mode, RX_CLK[n] out = TXBCLK[n], Jitter Cleaner PLL Multiplier Ratio = 1X or Off

- Device Pin Setting(s) – Pin settings allow for maximum software configurability.
  - Ensure ST input pin is high.
  - Ensure CODE input pin is Low.
  - Ensure PLOOP input pin is Low.
  - Ensure SLOOP input pin is Low.
  - Ensure SPEED [1:0] input pins are both High.
  - Ensure ENABLE input pin is High.
  - Ensure PRBS_EN input pin is Low.
- Reset Device
  - Issue a hard or soft reset (RST_N asserted for at least 10 us -or- Write 1'b1 to 0.15)
- Clock Configuration
  - If using JCPLL (JCPLL 1X)
    - JCPLL Mux Settings (see Figure 1-3)
      - Select REFCLK input (Default = Differential)
        - If Single Ended REFCLK used – Write 2'b01 to 4/5.37120.15:14
        - If Differential REFCLK used – Write 2'b00 to 4/5.37120.15:14
      - Write 2'b11 to 4/5.37120.13:12 to select differential REFCLKP/N as RXBYTECLK
      - Write 4'b0000 to 4/5.37120.11:8 to select jitter cleaned clock for SERDES TX/RX.
      - Write 2'b11 to 4/5.37120.7:6 to select differential REFCLKP/N as Delay Stopwatch clock input
      - Write 2'b00 to 4/5.37120.5:4 to select jitter cleaned clock for HSTL VTP 2x
      - Write 2'b00 to 16.10:9 to select SERDES TX clock as RX_CLK output (per channel)
      - Write 16'h0081 to 4/5.37126 to set Charge pump control
      - Write 16'h00A0 to 4/5.37128 to set TXRX output divider
    - Clock Divide Settings (see Figure A-13)
      - Write 7'b1000000 to 4/5.37124.14:8 to set REF_DIV to value of 1
      - Write 1'b1 to 4/5.37124.15 REFDIV_EN to enable reference clock divider
      - Write 7'h18 to 4/5.37124.6:0 to set FB_DIV to value of 24
      - Write 1'b1 to 4/5.37124.7 FBDIV_EN to enable feedback divider
      - Write 7'h18 to 4/5.37125.6:0 to set RXTX_DIV to value of 24
      - Write 1'b1 to 4/5.37125.7 OUTDIV_EN to enable RXTX_DIV output divider
      - Write 7'h0D to 4/5.37121.14:8 to set HSTL_DIV to value of 13
      - Write 7'h06 to 4/5.37121.6:0 to set HSTL_DIV2 to value of 6
      - Write 2'b11 to 4/5.36864.14:13 to set RX Loop Bandwidth
      - Write 2'b11 to 4/5.36864.6:5 to set TX Loop Bandwidth
      - Write 4'b0101 to 4/5.36864.11:8 to set MPY RX multiplier factor to 10
      - Write 4'b0101 to 4/5.36864.3:0 to set MPY TX multiplier factor to 10
      - Write 16'h5555 to 4/5.36865 SERDES_RATE_CONFIG_TX_RX to set Half Rate
      - Write 3'b000 to 4/5.37127.14:12 to set control bits for VCO tail current to 0
      - Write 1'b1 to 4/5.37127.15 to enable Jitter Cleaner
      - Wait 50 ms in order for JCPLL to lock

- Else if using clock bypass mode (JCPLL Off)
  - JCPLL Mux Settings (see Figure 1-3)
    - Select REFCLK input (Default = Differential)
      - If Single Ended REFCLK used – Write 2'b01 to 4/5.37120.15:14
      - If Differential REFCLK used – Write 2'b00 to 4/5.37120.15:14
    - Select RXBYTE_CLK (Default = Differential)
      - If Single Ended REFCLK used – Write 2'b10 to 4/5.37120.13:12
      - If Differential REFCLK used – Write 2'b11 to 4/5.37120.13:12
    - Select SERDES TX Reference Clock Input (Default = Differential)
      - If Single Ended REFCLK used – Write 2'b10 to 4/5.37120.11:10
      - If Differential REFCLK used – Write 2'b11 to 4/5.37120.11:10
    - Select SERDES RX Reference Clock Input (Default = Differential)
      - If Single Ended REFCLK used – Write 2'b10 to 4/5.37120.9:8
      - If Differential REFCLK used – Write 2'b11 to 4/5.37120.9:8
    - Select DELAY_CLK (Default = Differential)
      - If Single Ended REFCLK used – Write 2'b10 to 4/5.37120.7:6
      - If Differential REFCLK used – Write 2'b11 to 4/5.37120.7:6
    - Select HSTL_2X_CLK (Default = Differential)
      - Write 2'b01 to 4/5.37120.5:4 to select RX SERDES recovered clock as HSTL_2X_CLK
    - Write 2'b00 to 16.10:9 to select SERDES TX clock as RX_CLK output (per channel)
    - Write 7'h04 to 4/5.37121.6:0 to set HSTL_DIV2 to value of 4.
    - Write 15'h1515 to 4/5.36864.14:0 SERDES_PLL_CONFIG to set MPY RX/TX multiplier factor to 10
    - Write 16'h5555 to 4/5.36865 SERDES_RATE_CONFIG_TX_RX to set Half Rate
- Mode Control (see Table 2-2)
  - Write 1'b0 to 17.0 for RX source centered mode (per channel)
  - Write 1'b0 to 17.1 for TX source centered mode (per channel)
  - Write 1'b1 to 17.2 to enable 8B/10B encode decode functions (per channel)
  - Write 1'b1 to 17.3 to enable 1000Base-X PCS TX & PCS RX functions (per channel)
  - Write 1'b1 to 17.4 to set nibble order, LSB on rising edge, MSB on falling edge (per channel)
  - Write 1'b1 to 17.5 to enable DDR data on TX/RX directions (per channel)
  - Write 1'b0 to 17.6 to disable FC_PH overlay detection (per channel)
  - Write 1'b1 to 17.7 to enable comma detection (per channel)
  - Write 1'b0 to 17.9 to disable full DDR mode (per channel)
  - Write 1'b0 to 16.8 to disable Farend Loop back (per channel)
  - Write 1'b0 to 0.14 to disable loop back mode (per channel)
  - Write 3'b111 to 4/5.36874.11:9 to set channel 0 TX swing setting amplitude to 1375 mVdfpp
  - Write 1'b1 to 4/5.36874.8 to set channel 0 TX CM bit
  - Write 3'b111 to 4/5.36876.11:9 to set channel 1 TX swing setting amplitude to 1375 mVdfpp
  - Write 1'b1 to 4/5.36876.8 to set channel 1 TX CM bit
  - Write 3'b111 to 4/5.36878.11:9 to set channel 2 TX swing setting amplitude to 1375 mVdfpp
  - Write 1'b1 to 4/5.36878.8 to set channel 2 TX CM bit
  - Write 3'b111 to 4/5.36880.11:9 to set channel 3 TX swing setting amplitude to 1375 mVdfpp
  - Write 1'b1 to 4/5.36880.8 to set channel 3 TX CM bit
- RX equalization settings
  - Write 4'b0001 to 4/5.36866.15:12 to turn on adaptive equalization (4'b0000 is off)

  - Write 4'b0001 to 4/5.36868.15:12 to turn on adaptive equalization (4'b0000 is off)
  - Write 4'b0001 to 4/5.36870.15:12 to turn on adaptive equalization (4'b0000 is off)
  - Write 4'b0001 to 4/5.36872.15:12 to turn on adaptive equalization (4'b0000 is off)
  - Write 2'b01 to 4/5.36866.3:2 for AC coupled mode (2'b00 is DC coupled mode)
  - Write 2'b01 to 4/5.36868.3:2 for AC coupled mode (2'b00 is DC coupled mode)
  - Write 2'b01 to 4/5.36870.3:2 for AC coupled mode (2'b00 is DC coupled mode)
  - Write 2'b01 to 4/5.36872.3:2 for AC coupled mode (2'b00 is DC coupled mode)
- TX DLL Offset
  - Write 16'h0028 to 4/5.37888 TX0_DLL_CONTROL
  - Write 16'h0028 to 4/5.37889 TX1_DLL_CONTROL
  - Write 16'h0028 to 4/5.37890 TX2_DLL_CONTROL
  - Write 16'h0028 to 4/5.37891 TX3_DLL_CONTROL
- Poll Serdes PLL Status for Locked State
  - Read 4/5.36891.4,0 SERDES_PLL_STATUS – PLL_LOCK_TX/RX
  - Keep polling until both bits are high
- Issue Data path Reset
  - Write 1'b1 to 16.11 (per channel)
  - Write 1'b0, 1'b1, followed by 1'b0 to 37636.14.
- Clear Latched Registers
  - Read 1 PHY_STATUS_1 to clear (per channel)
  - Read 18 PHY_RX_CTC_FIFO_STATUS to clear (per channel)
  - Read 19 PHY_TX_CTC_FIFO_STATUS to clear (per channel)
  - Read 28 PHY_CHANNEL_STATUS to clear (per channel)
  - Read 4/5.36891 SERDES_PLL_STATUS to clear
- Operational Mode Status
  - Read Verify 1.2 PHY_STATUS_1 – Link Status (1'b1) (per channel)
  - Read Verify 18.15 PHY_RX_CTC_FIFO_STATUS – RX_CTC_Reset (1'b0) (per channel)
  - Read Verify 19.15 PHY_TX_CTC_FIFO_STATUS – TX_FIFO_Reset_1Gx (1'b0) (per channel)
  - Read Verify 28.13:12 PHY_CHANNEL_STATUS – Enc/Dec Invalid Code Word (2'b00) (per channel)
  - Read Verify 4/5.36891.4 SERDES_PLL_STATUS – PLL_LOCK_RX (1'b1)
  - Read Verify 4/5.36891.0 SERDES_PLL_STATUS – PLL_LOCK_TX (1'b1)

3.3 Jitter Test Pattern Generation and Verification Procedures

Use one of the following procedures to generate and verify the respective test patterns. It is assumed that an appropriate external cable has been connected between serial outputs and serial inputs. No functional parallel side connections are necessary.

- XAUI Based High Frequency Test Pattern:
  - Device Pin Setting(s):
    - Ensure ST primary input pin is low.
  - Reset Device:
    - Issue a hard or soft reset (RST_N asserted –or- Write 1 to 4/5.0.15)
  - Select single ended or differential REFCLK input:
    - If Single Ended REFCLK used - Write 2'b01 to 4/5.37120.15:14
    - If Differential REFCLK used – Write 2'b00 to 4/5.37120.15:14
  - Select SERDES TX Reference Clock Input:
    - If Single Ended REFCLK used - Write 2'b10 to 4/5.37120.11:10
    - If Differential REFCLK used – Write 2'b11 to 4/5.37120.11:10
  - Select SERDES RX Reference Clock Input:
    - If Single Ended REFCLK used - Write 2'b10 to 4/5.37120.9:8
    - If Differential REFCLK used – Write 2'b11 to 4/5.37120.9:8
  - Ensure a legal reference clock operation frequency is selected based on Appendix A, and provision control settings accordingly. It is also possible to use the Jitter Cleaner during these tests, and the user should consult Appendix A for further Jitter Cleaner provisioning details.
  - Issue Datapath Reset:
    - Write 1'b1 to 4/5.32800.15
  - Verify RX Link Up:
    - Read 4/5.8.10, and discard value read.
    - Poll 4/5.8.10 deasserted.
  - Bypass Lane Alignment Logic:
    - Write 1'b1 to 4/5.32798.3
  - Select Test Pattern:
    - Write 2'b00 to 4/5.25.1:0.
  - Enable Pattern Generation/Verification
    - Write 1'b1 to 4/5.25.2.
  - Clear Error Counters:
    - Read 4/5.32774, 4/5.32775, 4/5.32776, 4/5.32777
  - The pattern verification is now in progress.
  - Verify Error Free Operation (as many times as desired during the duration of the test period):
    - Read 4/5.32774, and verify 16'h0000 is read to confirm error free operation.
    - Read 4/5.32775, and verify 16'h0000 is read to confirm error free operation.
    - Read 4/5.32776, and verify 16'h0000 is read to confirm error free operation.
    - Read 4/5.32777, and verify 16'h0000 is read to confirm error free operation.
- XAUI Based Low Frequency Test Pattern:
  - Follow the XAUI Based High Frequency Test Pattern procedure above, with the following exception:
    - Write 2'b01 to 4/5.25.1:0 instead of 2'b00.
- XAUI Based Mixed Frequency Test Pattern:
  - Follow the XAUI Based High Frequency Test Pattern procedure above, with the following exception:
    - Write 2'b10 to 4/5.25.1:0 instead of 2'b00.

- XAUI Based Continuous Random Test Pattern (CRPAT):
  - Device Pin Setting(s):
    - Ensure ST primary input pin is low.
    - Ensure CODE primary input pin is low.
  - Reset Device:
    - Issue a hard or soft reset (RST_N asserted –or- Write 1 to 4/5.0.15)
  - Select single ended or differential REFCLK input:
    - If Single Ended REFCLK used - Write 2'b01 to 4/5.37120.15:14
    - If Differential REFCLK used – Write 2'b00 to 4/5.37120.15:14
  - Select SERDES TX Reference Clock Input:
    - If Single Ended REFCLK used - Write 2'b10 to 4/5.37120.11:10
    - If Differential REFCLK used – Write 2'b11 to 4/5.37120.11:10
  - Select SERDES RX Reference Clock Input:
    - If Single Ended REFCLK used - Write 2'b10 to 4/5.37120.9:8
    - If Differential REFCLK used – Write 2'b11 to 4/5.37120.9:8
  - Set XAUI mode:
    - Write 1'b1 to 4/5.32809.15
  - Ensure a legal reference clock operation frequency is selected based on Appendix A, and provision control settings accordingly. It is also possible to use the Jitter Cleaner during these tests, and the user should consult Appendix A for further Jitter Cleaner provisioning details.
  - Issue Datapath Reset:
    - Write 1'b1 to 4/5.32800.15
  - Clear Counters:
    - Read the test pattern error counters in the following order
      - 4/5.32778
      - 4/5.32779
  - Enable Pattern Generation:
    - Write 1'b1 to 4/5.32768.1
  - Enable Pattern Verification:
    - Write 1'b1 to 4/5.32769.1
  - Poll Lane Align Status Asserted:
    - Read 4/5.1.2, and discard value read.
    - Poll 4/5.1.2 asserted
  - Verify that the test pattern preamble has been received:
    - Poll 4/5.32801.15 asserted
  - The pattern verification is now in progress.
  - Verify Error Free Operation (as many times as desired during the duration of the test period):
    - Poll 4/5.1.2 asserted (Lane Align Status)
    - Read 4/5.32778, and verify 16'h0000 is read to confirm error free operation.
    - Read 4/5.32779, and verify 16'h0000 is read to confirm error free operation.
- XAUI Based Continuous Jitter Test Pattern (CJPAT):
  - Follow the XAUI Based Continuous Random Test Pattern procedure above, with the following exceptions:
    - Write 1'b1 to 4/5.32768.0 instead of 4/5.32768.1.
    - Write 1'b1 to 4/5.32769.0 instead of 4/5.32769.1.
- 10GFC Based Continuous Jitter Test Pattern (CJPAT):
  - Follow the XAUI Based Continuous Random Test Pattern procedure above, with the following

exceptions:
- Write 1'b1 to 4/5.32768.2 instead of 4/5.32768.1.
- Write 1'b1 to 4/5.32769.2 instead of 4/5.32769.1.
- Write 1'b0 to 4/5.32809.15 instead of 1'b1.

- 1000Base-X Based High/Mixed/Low Frequency Test Pattern:
  - Device Pin Setting(s):
    - Ensure ST primary input pin is high.
    - Ensure CODE primary input pin is low.
  - Reset Device:
    - Issue a hard or soft reset (RST_N asserted –or- Write 1 to 0.15)
  - Select single ended or differential REFCLK input:
    - If Single Ended REFCLK used - Write 2'b01 to 4/5.37120.15:14
    - If Differential REFCLK used – Write 2'b00 to 4/5.37120.15:14
  - Select SERDES TX Reference Clock Input:
    - If Single Ended REFCLK used - Write 2'b10 to 4/5.37120.11:10
    - If Differential REFCLK used – Write 2'b11 to 4/5.37120.11:10
  - Select SERDES RX Reference Clock Input:
    - If Single Ended REFCLK used - Write 2'b10 to 4/5.37120.9:8
    - If Differential REFCLK used – Write 2'b11 to 4/5.37120.9:8
  - Disable Comma Detection:
    - Write 1'b0 to 17.7
  - Ensure a legal reference clock operation frequency is selected based on Appendix A, and provision control settings accordingly. It is also possible to use the Jitter Cleaner during these tests, and the user should consult Appendix A for further Jitter Cleaner provisioning details.
  - Issue Datapath Reset:
    - Write 1'b1 to 16.11
    - Write 1'b0, 1'b1, followed by 1'b0 to 37636.14.
  - Select Test Pattern:
    - If High Frequency Pattern is desired:
      - Write 3'b000 to 16.2:0
    - If Low Frequency Pattern is desired:
      - Write 3'b001 to 16.2:0
    - If Mixed Frequency Pattern is desired:
      - Write 3'b010 to 16.2:0
  - Enable Test Pattern Generation:
    - Write 1'b1 to 16.4
  - Clear Counters:
    - Read 22.15:0 and discard the value.
  - Enable Test Pattern Verification:
    - Write 1'b1 to 16.3
  - Verify Test In Progress:
    - Poll 21.1 asserted.
  - The pattern verification is now in progress.
  - Verify Error Free Operation (as many times as desired during the duration of the test period):
    - Read 22.15:0, and verify 16'h0000 is read to confirm error free operation.

- 1000Base-X Based Continuous Random Pattern (CRPAT) Long/Short Test Pattern:
  - Device Pin Setting(s):

- Ensure ST primary input pin is high.
- Ensure CODE primary input pin is high.

– Reset Device:
- Issue a hard or soft reset (RST_N asserted –or- Write 1 to 0.15)

– Select single ended or differential REFCLK input:
- If Single Ended REFCLK used - Write 2'b01 to 4/5.37120.15:14
- If Differential REFCLK used – Write 2'b00 to 4/5.37120.15:14

– Select SERDES TX Reference Clock Input:
- If Single Ended REFCLK used - Write 2'b10 to 4/5.37120.11:10
- If Differential REFCLK used – Write 2'b11 to 4/5.37120.11:10

– Select SERDES RX Reference Clock Input:
- If Single Ended REFCLK used - Write 2'b10 to 4/5.37120.9:8
- If Differential REFCLK used – Write 2'b11 to 4/5.37120.9:8

– Ensure a legal reference clock operation frequency is selected based on Appendix A, and provision control settings accordingly. It is also possible to use the Jitter Cleaner during these tests, and the user should consult Appendix A for further Jitter Cleaner provisioning details.

– Enable Encoder/Decoder
- Write 1'b1 to 17.2

– Issue Datapath Reset:
- Write 1'b1 to 16.11
- Write 1'b0, 1'b1, followed by 1'b0 to 37636.14.

– Select Test Pattern:
- If CRPAT Long Pattern is desired:
  - Write 3'b011 to 16.2:0
- If CRPAT Short Pattern is desired:
  - Write 3'b100 to 16.2:0

– Enable Test Pattern Generation:
- Write 1'b1 to 16.4

– Clear Counters:
- Read 23.15:0 and 24.15:0 and discard the values.

– Enable Test Pattern Verification:
- Write 1'b1 to 16.3

– Verify Test In Progress:
- Poll 21.0 asserted.

– The pattern verification is now in progress.

– Verify Error Free Operation (as many times as desired during the duration of the test period):
- Read 23.15:0, and verify 16'h0000 is read to confirm error free operation.
- Read 24.15:0, and verify 16'h0000 is read to confirm error free operation.

If more than one test is specified results are unpredictable.

If another test type is desired, begin at the first step of that procedure.

3.4 PRBS Test Generation and Verification Procedures

Use one of the following procedures to generate and verify the respective PRBS test patterns. It is assumed that an appropriate external cable has been connected between serial outputs and serial inputs. No functional parallel side connections are necessary.

- 1000Base-X 2^7-1 PRBS Register Based Testing
  - Device Pin Setting(s):
    - Ensure ST primary input pin is high.
    - Ensure CODE primary input pin is low.
  - Reset Device:
    - Issue a hard or soft reset (RST_N asserted –or- Write 1 to 0.15)
  - Select single ended or differential REFCLK input:
    - If Single Ended REFCLK used - Write 2'b01 to 4/5.37120.15:14
    - If Differential REFCLK used – Write 2'b00 to 4/5.37120.15:14
  - Select SERDES TX Reference Clock Input:
    - If Single Ended REFCLK used - Write 2'b10 to 4/5.37120.11:10
    - If Differential REFCLK used – Write 2'b11 to 4/5.37120.11:10
  - Select SERDES RX Reference Clock Input:
    - If Single Ended REFCLK used - Write 2'b10 to 4/5.37120.9:8
    - If Differential REFCLK used – Write 2'b11 to 4/5.37120.9:8
  - Ensure a legal reference clock operation frequency is selected based on Appendix A, and provision control settings accordingly. It is also possible to use the Jitter Cleaner during these tests, and the user should consult Appendix A for further Jitter Cleaner provisioning details.
  - Issue Datapath Reset:
    - Write 1'b1 to 16.11
    - Write 1'b0, 1'b1, followed by 1'b0 to 37636.14.
  - Enable PRBS Generator (On Channel Desired):
    - Write 1'b1 to 16.6
  - Enable Test Pattern Verification:
    - Write 1'b1 to 16.7
  - Clear Counters:
    - Read 29.15:0 and discard the value.
  - The pattern verification is now in progress.
  - Verify Error Free Operation (as many times as desired during the duration of the test period):
    - Read 29.15:0, and verify 16'h0000 is read to confirm error free operation.
  - GPO3 contains a real time output that when high indicates if the input PRBS pattern on TD × 3/RD × 3 is errored.
  - GPO2 contains a real time output that when high indicates if the input PRBS pattern on TD × 2/RD × 2 is errored.
  - GPO1 contains a real time output that when high indicates if the input PRBS pattern on TD × 1/RD × 1 is errored.
  - GPO0 contains a real time output that when high indicates if the input PRBS pattern on TD × 0/RD × 0 is errored.
- 2^7-1/2^{23}-1 PRBS Pin Based Testing
  - Device Pin Setting(s):
    - Ensure PRBS_EN primary input pin is high.
    - PRBS Selection:
      - For PRBS 2^7-1- Ensure ST primary input pin is high.
      - For PRBS 2^{23}-1- Ensure ST primary input pin is low.

- Reset Device:
  - Issue a hard or soft reset (RST_N asserted –or- ST=0: Write 1 to 4/5.0.15 ST=1: Write 1 to 0.15)
- Select single ended or differential REFCLK input:
  - If Single Ended REFCLK used - Write 2'b01 to 4/5.37120.15:14
  - If Differential REFCLK used – Write 2'b00 to 4/5.37120.15:14
- Select SERDES TX Reference Clock Input:
  - If Single Ended REFCLK used - Write 2'b10 to 4/5.37120.11:10
  - If Differential REFCLK used – Write 2'b11 to 4/5.37120.11:10
- Select SERDES RX Reference Clock Input:
  - If Single Ended REFCLK used - Write 2'b10 to 4/5.37120.9:8
  - If Differential REFCLK used – Write 2'b11 to 4/5.37120.9:8
- Ensure a legal reference clock operation frequency is selected based on Appendix A, and provision control settings accordingly. It is also possible to use the Jitter Cleaner during these tests, and the user should consult Appendix A for further Jitter Cleaner provisioning details.
- Issue Datapath Reset:
  - If ST=1: Write 1'b1 to 16.11
  - If ST=0: Write 1'b1 to 4/5.32800.15
  - Write 1'b0, 1'b1, followed by 1'b0 to 37636.14.
- GPO3 contains a real time output that when high indicates if the input PRBS pattern on TD × 3/RD × 3 is errored.
- GPO2 contains a real time output that when high indicates if the input PRBS pattern on TD × 2/RD × 2 is errored.
- GPO1 contains a real time output that when high indicates if the input PRBS pattern on TD × 1/RD × 1 is errored.
- GPO0 contains a real time output that when high indicates if the input PRBS pattern on TD × 0/RD × 0 is errored.

- SERDES Macro 2^7-1/2^{23}-1 PRBS Register Based Testing
  - Reset Device:
    - Issue a hard or soft reset (RST_N asserted –or- ST=0: Write 1 to 4/5.0.15 ST=1: Write 1 to 0.15)
  - Select single ended or differential REFCLK input:
    - If Single Ended REFCLK used - Write 2'b01 to 4/5.37120.15:14
    - If Differential REFCLK used – Write 2'b00 to 4/5.37120.15:14
  - Select SERDES TX Reference Clock Input:
    - If Single Ended REFCLK used - Write 2'b10 to 4/5.37120.11:10
    - If Differential REFCLK used – Write 2'b11 to 4/5.37120.11:10
  - Select SERDES RX Reference Clock Input:
    - If Single Ended REFCLK used - Write 2'b10 to 4/5.37120.9:8
    - If Differential REFCLK used – Write 2'b11 to 4/5.37120.9:8
  - Ensure a legal reference clock operation frequency is selected based on Appendix A, and provision control settings accordingly. It is also possible to use the Jitter Cleaner during these tests, and the user should consult Appendix A for further Jitter Cleaner provisioning details.
  - PRBS Selection:
    - For PRBS 2^7-1-
      - Write 2'b10 4/5.36881.1:0.
      - Write 2'b10 4/5.36882.1:0.
    - For PRBS 2^{23}-1-

  - Write 2'b11 4/5.36881.1:0.
  - Write 2'b11 4/5.36882.1:0.
- Enable PRBS Generation:
  - Write 1'b1 to 4/5.36881.2
  - Write 1'b1 to 4/5.36874.1
  - Write 1'b1 to 4/5.36876.1
  - Write 1'b1 to 4/5.36878.1
  - Write 1'b1 to 4/5.36880.1
- Enable PRBS Verification:
  - Write 1'b1 to 4/5.36882.3
  - Write 1'b1 to 4/5.36866.1
  - Write 1'b1 to 4/5.36868.1
  - Write 1'b1 to 4/5.36870.1
  - Write 1'b1 to 4/5.36872.1
- Clear Counters:
  - Read 4/5.38144.7:0, 4/5.38145.7:0, 4/5.38146.7:0, 4/5.38147.7:0 and discard the value.
- The pattern verification is now in progress
- Verify Error Free Operation (as many times as desired during the duration of the test period):
  - Read 4/5.38147.7:0, and verify 8'h00 is read to confirm error free operation on TD × 3/RD × 3.
  - Read 4/5.38146.7:0, and verify 8'h00 is read to confirm error free operation on TD × 2/RD × 2.
  - Read 4/5.38145.7:0, and verify 8'h00 is read to confirm error free operation on TD × 1/RD × 1.
  - Read 4/5.38144.7:0, and verify 8'h00 is read to confirm error free operation on TD × 0/RD × 0.
- GPO3 contains a real time output that when high indicates if the input PRBS pattern on TD × 3/RD × 3 is errored, provided that ST=0. If ST=1, GPO3 does not indicate test failure status. It is acceptable to de-assert ST (ST=0) at this point in the test (if not already de-asserted).
- GPO2 contains a real time output that when high indicates if the input PRBS pattern on TD × 2/RD × 2 is errored, provided that ST=0. If ST=1, GPO2 does not indicate test failure status. It is acceptable to de-assert ST (ST=0) at this point in the test (if not already de-asserted).
- GPO1 contains a real time output that when high indicates if the input PRBS pattern on TD × 1/RD × 1 is errored, provided that ST=0. If ST=1, GPO1 does not indicate test failure status. It is acceptable to de-assert ST (ST=0) at this point in the test (if not already de-asserted).
- GPO0 contains a real time output that when high indicates if the input PRBS pattern on TD × 0/RD × 0 is errored, provided that ST=0. If ST=1, GPO0 does not indicate test failure status. It is acceptable to de-assert ST (ST=0) at this point in the test (if not already de-asserted).

3.5 Signal Pin Description

Table 3-1. Global Signals

SIGNAL	LOCATION	VOLTAGE	TYPE	DESCRIPTION
RST_N	P1	VDDO	2.5 V LVCMOS Input	Chip Reset (Active Low) When asserted (low logic level), this signal reinitializes the entire device. Must be held asserted (low logic level) for at least 10 µS after device power up.
ENABLE	U1	VDDO	2.5 V LVCMOS Input	Device Enable. When this pin is held low, the device is in a low power state. When high the device operates normally. A hard or soft reset must be applied after a change of state occurs on this input signal.
SPEED[1:0]	R16 N14	VDDO	2.5 V LVCMOS Input	Speed Selection pins. These pins put all four channels of TLK3134 into one of the three supported (full/half/quarter) channel operation speeds. 00 – All Four Channels in Full Rate mode 01 – All Four Channels in Half Rate mode 10 – All Four Channels in Quarter rate mode 11 – Software Selectable Rate In the software selectable rate mode, the rate for each channel may be configured independently by the MDIO interface. The SPEED[1:0] inputs control both RX and TX directions for all four channels (Including XAUI and 10GFC modes). See Appendix A for further information on speed selection (full/half/quarter) for proper settings as a function of the application mode and reference clock frequency. Note that if these pins are not configured on the application board to select “Software Selectable Rate”, then the internal speed register bits cannot be used to control the rate settings, and the full/half/quarter rate selection is fixed.
PLOOP	N16	VDDO	2.5 V LVCMOS Input	Parallel Loop Enable. When high, the serial output for each channel is internally looped back to its serial input so that the transmit parallel interface input data is output onto the receive parallel interface.
SLOOP	R17	VDDO	2.5 V LVCMOS Input	Serial Loop Enable. When high, the serial input from each channel is internally looped back to that channel’s serial output, making that channel a serial repeater. In device configurations where clock tolerance compensation is not performed in the transmit direction, there are two options for error free serial loopback operation: 1. Frequency lock (0 ppm) the incoming serial data rate to the local reference clock device input. 2. Provision the TX SERDES REFCLK to run from a jitter cleaned version of the RX SERDES RXBCLK (Receive Byte Clock).
PRBS_EN	U2	VDDO	2.5 V LVCMOS Input	PRBS Enable. When this pin is asserted high, the internal PRBS generator and comparator circuits are enabled on the transmit and receive data paths of all channels. The PRBS results for each channel can be read through MDIO counters. Primary chip output signals GPO3/GPO2/GPO1/GPO0 remain low during PRBS testing when the input serial stream PRBS pattern is correct, and pulse high when PRBS errors are detected on the input serial stream on a per channel basis. GPO3 contains the Channel 3 PRBS currently passing (when low) indication. GPO2 contains the Channel 2 PRBS currently passing (when low) indication. GPO1 contains the Channel 1 PRBS currently passing (when low) indication. GPO0 contains the Channel 0 PRBS currently passing (when low) indication. An external loopback connection (via external cables) is required during PRBS testing. **ST=0:** PRBS 2^{23}-1 is transmitted on each transmit channel serial output, and compared on each receive channel serial input. **ST=1:** PRBS 2^{7}-1 is transmitted on each transmit serial output, and compared on each receive serial input.

Table 3-1. Global Signals (continued)

SIGNAL	LOCATION	VOLTAGE	TYPE	DESCRIPTION
CODE	M3	VDDO	2.5 V LVCMOS Input	Code Enable. This signal selects different functionality based on the setting of the ST primary chip input pin. **ST=0:** This signal is logically OR'd with the XAUI_ORDER register bit (Register Bit 32809.15). XAUI applications can either tie this input signal high (preferred) or tie this signal low (must program the XAUI_ORDER register bit after device reset to high if CODE is tied off low). 10GFC applications must tie this signal low. **ST=1:** This signal is logically OR'd with the PCS_EN register bit (Register Bit 17.3). RGMII/GMII applications can either tie this input signal high (preferred) or tie this signal low (must program the PCS_EN 17.3 register bit after device reset to high if CODE is tied off low). Non RGMII/GMII applications must tie this input signal low.

Table 3-2. JTAG Signals

SIGNAL	LOCATION	VOLTAGE	TYPE	DESCRIPTION
TDI	N13	VDDO	2.5 V LVCMOS Input (Internal Pullup)	JTAG Input Data. TDI is used to serially shift test data and test instructions into the device during the operation of the test port.
TDO	R15	VDDO	2.5 V LVCMOS Output	JTAG Output Data. TDO is used to serially shift test data and test instructions out of the device during operation of the test port. When the JTAG port is not in use, TDO is in a high impedance state.
TMS	P15	VDDO	2.5 V LVCMOS Input (Internal Pullup)	JTAG Mode Select. TMS is used to control the state of the internal test-port controller.
TCK	P17	VDDO	2.5 V LVCMOS Input	JTAG Clock. TCK is used to clock state information and test data into and out of the device during the operation of the test port.
TRST_N	N15	VDDO	2.5 V LVCMOS Input (Internal Pullup)	JTAG Test Reset. TRST_N is used to reset the JTAG logic into system operational mode.

Table 3-3. MDIO Related Signals

SIGNAL	LOCATION	VOLTAGE	TYPE	DESCRIPTION
MDC	T16	VDDM	1.2 V OR 2.5 V LVCMOS Input	Management Interface Clock This clock is used to sample the MDIO signal.
MDIO	U16	VDDM	1.2 V OR 2.5 V LVCMOS Input/ Output	Management Interface Data This bidirectional data line for MDIO Port is sampled on the rising edge of MDC. THIS SIGNAL MUST BE EXTERNALLY PULLED UP TO VDDM. Consult IEEE802.3 Clause 22/45 for an appropriate resistance value.
PRTAD[4:0]	N5, N4, N3, N2, T1	VDDO	2.5 V LVCMOS Input	Port Address Used to select the Device Id/Port ID in Clause 22/Clause 45 MDIO modes. ST=0 (Clause 45 Mode): If PRTAD[0] is a 0, then a PHY device is selected for XAUI/10GFC register accesses (4.xxxxx.x). If PRTAD[0] is a 1, then a DTE device is selected for XAUI/10GFC register accesses (5.xxxxx.x). PRTAD[4:1] selects the Clause 45 port address (TLK3134 must be located on even boundaries since the lowest port address bit determines DTE/PHY, and is used as a device address instead of port address). ST=1 (Clause 22 Mode): PRTAD[4:2] selects a block of four sequential Clause 22 port addresses. Each channel is implemented as a different port address, and can be accessed by setting the appropriate port address field within the Clause 22 MDIO transaction. PRTAD[1:0] pins are not used in Clause 22 mode. Channel 0 responds to port address 0 within the block of four port addresses. Channel 1 responds to port address 1 within the block of four port addresses. Channel 2 responds to port address 2 within the block of four port addresses. Channel 3 responds to port address 3 within the block of four port addresses.

Table 3-3. MDIO Related Signals (continued)

SIGNAL	LOCATION	VOLTAGE	TYPE	DESCRIPTION
ST	M5	VDDO	2.5 V LVCMOS Input	MDIO Select Used to select Clause 22 (=1) or Clause 45 (=0) operation. A hard or soft reset must be applied after a change of state occurs on this input signal.
REFCLK	M2	VDDO	2.5 V LVCMOS Input	Single Ended Reference Clock Single ended reference clock input. By default, the differential reference clock (REFCLKP/N) is selected. This default value may be changed by a mdio register (4/5.37120.15:14). The acceptable input frequency range on this input signal is 50 Mhz → 150 Mhz. Jitter performance is optimal when using the differential REFCLK input.

Table 3-4. Parallel Data Pins

SIGNAL	LOCATION	VOLTAGE	TYPE	DESCRIPTION
TXCLK_[3:0]	C11 F16 K13 M14	VDDQ/ VREF1/2	1.5/1.8 V HSTL Input	Transmit Data Clocks (XGMII) These four signals are the parallel (XGMII) side input clocks per channel. In XAUI/10GFC mode, TXCLK_1 is used.
TXD_[31:0]	B11 A13 B13 C12 E12 B14 D13 C15 D14 E13 B16 D15 F13 C16 D17 E15 E16 E17 F15 G16 G13 G17 J13 J14 J15 J17 K15 M17 L16 L13 L14 M16	VDDQ/ VREF1/2	1.5/1.8 V HSTL Input	Transmit Data Pins (XGMII) Parallel interface data pins. See the following tables for functionality per application mode: Table 2-3 XAUI - Lane To Functional Pin Mapping (XAUI_ORDER = 1) Table 2-4 10GFC - Lane To Functional Pin Mapping (XAUI_ORDER = 0) Table 2-5 RGMII - Lane To Functional Pin Mapping Table 2-6 RTBI - Lane To Functional Pin Mapping Table 2-7 TBI - Lane To Functional Pin Mapping Table 2-8 GMII - Lane To Functional Pin Mapping Table 2-9 EBI - Lane To Functional Pin Mapping Table 2-10 REBI - Lane To Functional Pin Mapping Table 2-11 NBI - Lane To Functional Pin Mapping Table 2-12 RNBI - Lane To Functional Pin Mapping Table 2-13 TBID - Lane To Functional Pin Mapping Table 2-15 NBID - Lane To Functional Pin Mapping
TXC_[7:0]	B12 D12 A16 C17 F14 H16 K17 L15	VDDQ/ VREF1/2	1.5/1.8 V HSTL Input	See the following tables for functionality per application mode: Table 2-3 XAUI - Lane To Functional Pin Mapping (XAUI_ORDER = 1) Table 2-4 10GFC - Lane To Functional Pin Mapping (XAUI_ORDER = 0) Table 2-5 RGMII - Lane To Functional Pin Mapping Table 2-6 RTBI - Lane To Functional Pin Mapping Table 2-7 TBI - Lane To Functional Pin Mapping Table 2-8 GMII - Lane To Functional Pin Mapping Table 2-9 EBI - Lane To Functional Pin Mapping Table 2-10 REBI - Lane To Functional Pin Mapping Table 2-11 NBI - Lane To Functional Pin Mapping Table 2-12 RNBI - Lane To Functional Pin Mapping Table 2-13 TBID - Lane To Functional Pin Mapping Table 2-15 NBID - Lane To Functional Pin Mapping
RXCLK_[3:0]	C2 C6 D7 D9	VDDQ	1.5/1.8 V HSTL Output	Receive Data Clocks (XGMII) These four signals are the parallel (XGMII) side output clocks per channel. In XAUI/10GFC mode, RXCLK_1 is used.

Table 3-4. Parallel Data Pins (continued)

SIGNAL	LOCATION	VOLTAGE	TYPE	DESCRIPTION
RXD_[31:0]	H2 H1 H5 G3 G4 F1 F5 E2 E1 E3 D2 E5 B1 D4 B2 E6 A3 B3 C5 B4 A4 B6 A6 A8 B8 D8 B9 A10 C9 A11 D10 E10	VDDQ	1.5/1.8 V HSTL Output	Receive Data Pins (XGMII) Parallel interface data pins. See the following tables for functionality per application mode: Table 2-3 XAUI - Lane To Functional Pin Mapping (XAUI_ORDER = 1) Table 2-4 10GFC - Lane To Functional Pin Mapping (XAUI_ORDER = 0) Table 2-5 RGMII - Lane To Functional Pin Mapping Table 2-6 RTBI - Lane To Functional Pin Mapping Table 2-7 TBI - Lane To Functional Pin Mapping Table 2-8 GMII - Lane To Functional Pin Mapping Table 2-9 EBI - Lane To Functional Pin Mapping Table 2-10 REBI - Lane To Functional Pin Mapping Table 2-11 NBI - Lane To Functional Pin Mapping Table 2-12 RNBI - Lane To Functional Pin Mapping Table 2-13 TBID - Lane To Functional Pin Mapping Table 2-15 NBID - Lane To Functional Pin Mapping
RXC_[7:0]	H4 F4 D3 D5 E7 B7 E8 C10	VDDQ	1.5/1.8 V HSTL Output	Receive Data Control (XGMII) XGMII Control inputs. See the following tables for functionality per application mode: Table 2-3 XAUI - Lane To Functional Pin Mapping (XAUI_ORDER = 1) Table 2-4 10GFC - Lane To Functional Pin Mapping (XAUI_ORDER = 0) Table 2-5 RGMII - Lane To Functional Pin Mapping Table 2-6 RTBI - Lane To Functional Pin Mapping Table 2-7 TBI - Lane To Functional Pin Mapping Table 2-8 GMII - Lane To Functional Pin Mapping Table 2-9 EBI - Lane To Functional Pin Mapping Table 2-10 REBI - Lane To Functional Pin Mapping Table 2-11 NBI - Lane To Functional Pin Mapping Table 2-12 RNBI - Lane To Functional Pin Mapping Table 2-13 TBID - Lane To Functional Pin Mapping Table 2-15 NBID - Lane To Functional Pin Mapping

Table 3-5. Serial Side Data/Clock Pins

SIGNAL	LOCATION	VOLTAGE	TYPE	DESCRIPTION
TDP3/TDN3 TDP2/TDN2 TDP1/TDN1 TDP0/TDN0	U8 U7 R6 R7 U5 U4 R3 R4	AVDD	CML Output	Transmit Differential Pairs, XAUI Lane, High speed serial outputs. The data rate of these signals is from 600 Mbps minimum to 3.75 Gbps maximum.
RDP3/RDN3 RDP2/RDN2 RDP1/RDN1 RDP0/RDN0	U13 U14 R13 R12 U10 U11 R10 R9	AVDD	CML Input	Receive Differential Pairs, XAUI Lane, High speed serial inputs with on-chip 100 ohm differential termination. Each input pair is terminated differentially across an on chip 100 ohm resistor. The data rate of these signals is from 600 Mbps minimum to 3.75 Gbps maximum.

Table 3-6. Miscellaneous Pins

SIGNAL	LOCATION	VOLTAGE	TYPE	DESCRIPTION
VPP	D11 E11	DVDD	P	Efuse Controller Voltage (1.2 V). Must be tied to 1.2 V (DVDD) in the system application.
TESTEN	M6	VDDO	LVCMOS 2.5 V Input	Test Mode Enable Input – Must Be Grounded in the System Application.
AMUX1	T12	VDDA	Analog Output	SERDES Analog Mux 1 RX – Must be Unconnected/Open in the System Application
AMUX0	T6	VDDA	Analog Output	SERDES Analog Mux 0 TX – Must be Unconnected/Open in the System Application
RES[4:1]	C14 H15 G2 C4	VDDQ	Resistive Connection	HSTL Impedance Control Resistors – 0.5% Tolerance Resistor required of the following values: 150 Ohms between RES4 and GND 150 Ohms between RES3 and GND 50 Ohms between RES2 and GND 50 Ohms between RES1 and GND Note: These resistors cannot be shared between output pins.
GPI1	R2	VDDO	LVCMOS 2.5 V Input	General Purpose Input – Must be Grounded in the System Application.
GPO[4:0]	J6 K6 L6 L3 N1	VDDO	LVCMOS 2.5 V Output	General Purpose Outputs – Must be Unconnected/Open in the System Application. It is recommended that these output ports go to headers or non-populated resistor pads to facilitate probing of internal device functions/settings during the initial system bring up process. Also, to monitor PRBS testing real time, these outputs must be available for probing on the application board.

Table 3-7. Voltage Supply and Reference Pins

SIGNAL	LOCATION	TYPE	DESCRIPTION
DVDD	F11, F6, F8, F9, G12, G6, J12, J7 M12 N10, N12, N17, N6, N8 T2	P	Digital Core Power Supply (1.2 V ±5%)
VDDO	L2 N9 P14, P16, P3 R1	P	LVCMOS and Bias Power (2.5 V ±5%)
VDDM	T17	P	MDIO Power (2.5 V or 1.2 V ±5%)
VDDQ	A12, A15, A2, A5, A9 B15, B17, B5 C1, C7, C8 D1 E14, E4 F10, F17, F3, F7 G1, G14 H13, H17, H3, H6 J16 K16 L12 M15	P	XGMII HSTL Power (1.5/1.8 V) 1.5 V Operation Range: 1.4 V → 1.6 V 1.8 V Operation Range: 1.7V → 1.9 V
VREF1, VREF2	H14 A14	P	XGMII HSTL Reference Voltage (.75 V or .9 V) These signals should be equal to VDDQ divided by 2.
DGND	A1, A17, A7 B10 C13, C3 D16, D6 E9 F12, F2 G10, G11, G15, G5, G7, G8, G9 H10, H11, H12, H7, H8, H9 J10, J11, J8, J9 K10, K11, K12, K14, K7, K8, K9 L10, L11, L17, L7, L8, L9 M10, M11, M13, M4, M7, M8, M9 P2 T15 U17	G	Digital Ground
AVDD	N11, N7 R11, R14, R5, R8 U12, U6, U9	P	Analog Power (1.2 V ±5%)
AGND	P10, P12, P13 , P4, P5,P6, P8 T11, T14, T3, T5, T8	G	Analog Ground
VDDR	P9	P	SERDES Voltage Regulator Input (1.5 V –or– 1.8 V)
VDDT	P11, P7 T4, T9	P	SERDES Termination Voltage (1.2 V)
VDDD	T10, T13, T7 U15, U3	P	SERDES Digital Power (1.2 V)

Table 3-8. Jitter Cleaner Related Pins

SIGNAL	LOCATION	VOLTAGE	TYPE	DESCRIPTION
REFCLKP/ REFCLKN	L1 K1	VDD_CML	I	Differential Reference Clock Inputs By default, the differential reference clock (REFCLKP/N) is selected. This default value may be changed by a mdio register (4/5.37120.15:14). Must Be Externally AC Coupled REFCLKP – DPECL REFCLK P Input REFCLKN – DPECL REFCLK N Input Acceptable input frequency range is 50 MHz → 375 MHz. Jitter performance is optimal when using the differential REFCLK input.
VDDA_VCO	K2	P	P	Jitter Cleaner – VCO Supply - 1.2 V
VSSA_VCO	K3	G	G	Jitter Cleaner Ground
VDDA_CP	L4	P	P	Jitter Cleaner – Charge Pump - 1.2 V
VSSA_CP	L5	G	G	Jitter Cleaner Ground
VDD_CML	M1	P	P	Jitter Cleaner – REFCLKP/N Input Supply - 1.2 V
VSS_CML	J1	G	G	Jitter Cleaner Ground
VDD_PLL	J5	P	P	Jitter Cleaner Digital Power (1.2 V)
VSS_PLL	J4	G	G	Jitter Cleaner Ground
VCO_TL_TST	J3	G	Analog Input	VCO Testability Input. This signal should be grounded in the application.
TST_OUT	J2	VDD_PLL	Analog Input/Output	Jitter Cleaner Testability Pin. This signal should be left open (unconnected) in the application.
CP_OUT	K5	VDDA_CP	Analog Output	Charge Pump Output. If the internal Jitter Cleaner PLL is used, this signal should be connected to the input of the external loop filter (See Figure B-1). If the internal Jitter Cleaner PLL is not used, this node should be left open (unconnected).
VTUNE	K4	VDDA_VCO	Analog Input	LC VCO Bias Voltage. This signal should be connected to the output of the external loop filter if the Jitter Cleaner PLL is used (Figure B-1). If the internal Jitter Cleaner PLL is not used, this node should be grounded.

	1	2	3	4	5	6	7	8	9
A	DGND	VDDQ	RXD_15	RXD_11	VDDQ	RXD_9	DGND	RXD_8	VDDQ
B	RXD_19	RXD_17	RXD_14	RXD_12	VDDQ	RXD_10	RXC_2	RXD_7	RXD_5
C	VDDQ	RXCLK_3	DGND	RES1	RXD_13	RXCLK_2	VDDQ	VDDQ	RXD_3
D	VDDQ	RXD_21	RXC_5	RXD_18	RXC_4	DGND	RXCLK_1	RXD_6	RXCLK_0
E	RXD_23	RXD_24	RXD_22	VDDQ	RXD_20	RXD_16	RXC_3	RXC_1	DGND
F	RXD_26	DGND	VDDQ	RXC_6	RXD_25	DVDD	VDDQ	DVDD	DVDD
G	VDDQ	RES2	RXD_28	RXD_27	DGND	DVDD	DGND	DGND	DGND
H	RXD_30	RXD_31	VDDQ	RXC_7	RXD_29	VDDQ	DGND	DGND	DGND
J	VSS_CML	TST_OUT	VCO_TL_TST	VSS_PLL	VDD_PLL	GPO4	DVDD	DGND	DGND
K	REFCLKN	VDDA_VCO	VSSA_VCO	VTUNE	CP_OUT	GPO3	DGND	DGND	DGND
L	REFCLKP	VDDO	GPO1	VDDA_CP	VSSA_CP	GPO2	DGND	DGND	DGND
M	VDD_CML	REFCLK	CODE	DGND	ST	TESTEN	DGND	DGND	DGND
N	GPO0	PRTAD1	PRTAD2	PRTAD3	PRTAD4	DVDD	AVDD	DVDD	VDDO
P	RST_N	DGND	VDDO	AGND	AGND	AGND	VDDT	AGND	VDDR
R	VDDO	GPI1	TDP0	TDN0	AVDD	TDP2	TDN2	AVDD	RDN0
T	PRTAD0	DVDD	AGND	VDDT	AGND	AMUX0	VDDD	AGND	VDDT
U	ENABLE	PRBS_EN	VDDD	TDN1	TDP1	AVDD	TDN3	TDP3	AVDD

Figure 3-1. Device Pinout Diagram – Part 1 (Top View)

	10	11	12	13	14	15	16	17
A	RXD_4	RXD_2	VDDQ	TXD_30	VREF2	VDDQ	TXC_5	DGND
B	DGND	TXD_31	TXC_7	TXD_29	TXD_26	VDDQ	TXD_21	VDDQ
C	RXC_0	TXCLK_3	TXD_28	DGND	RES4	TXD_24	TXD_18	TXC_4
D	RXD_1	VPP	TXC_6	TXD_25	TXD_23	TXD_20	DGND	TXD_17
E	RXD_0	VPP	TXD_27	TXD_22	VDDQ	TXD_16	TXD_15	TXD_14
F	VDDQ	DVDD	DGND	TXD_19	TXC_3	TXD_13	TXCLK_2	VDDQ
G	DGND	DGND	DVDD	TXD_11	VDDQ	DGND	TXD_12	TXD_10
H	DGND	DGND	DGND	VDDQ	VREF1	RES3	TXC_2	VDDQ
J	DGND	DGND	DVDD	TXD_9	TXD_8	TXD_7	VDDQ	TXD_6
K	DGND	DGND	DGND	TXCLK_1	DGND	TXD_5	VDDQ	TXC_1
L	DGND	DGND	VDDQ	TXD_2	TXD_1	TXC_0	TXD_3	DGND
M	DGND	DGND	DVDD	DGND	TXCLK_0	VDDQ	TXD_0	TXD_4
N	DVDD	AVDD	DVDD	TDI	SPEED0	TRST_N	PLOOP	DVDD
P	AGND	VDDT	AGND	AGND	VDDO	TMS	VDDO	TCK
R	RDP0	AVDD	RDN2	RDP2	AVDD	TDO	SPEED1	SLOOP
T	VDDD	AGND	AMUX1	VDDD	AGND	DGND	MDC	VDDM
U	RDP1	RDN1	AVDD	RDP3	RDN3	VDDD	MDIO	DGND

Figure 3-2. Device Pinout Diagram – Part 2 (Top View)

4 Electrical Specifications

4.1 ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

		UNIT
Supply voltage	AVDD, DVDD, VDDT, VDDD, VDDA_VCO, VDD_PLL, VDDA_CP, VDD_CML, VREF1/2	–0.3 to 1.5 V
Supply voltage	VDDQ, VDDR	–0.3 to 2.0 V
Supply voltage	VDDO, VDDM	–0.3 to 3.0 V
Input Voltage (LVCMOS)	VI	–0.3 to Supply + 0.3 V
Input Voltage (HSTL CLASS 1)	VI	–0.3 to 2.0 V
Storage temperature		–65°C to 150°C
Electrostatic Discharge		HBM: 1.5KV, CDM:500V
Characterized free-air operating temperature range		–40°C to 85°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

4.2 RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
DVDD	Core supply voltage		1.14	1.2	1.26	V
AVDD	Analog supply voltage		1.14	1.2	1.26	V
VDDQ	Parallel HSTL I/O supply voltage	1.5 V Application	1.4	1.5	1.6	V
		1.8 V Application	1.7	1.8	1.9	
VDDO	LVCMOS I/O supply voltage		2.37	2.5	2.63	V
VDDM	MDIO CMOS I/O supply voltage	1.2 V Application	1.14	1.2	1.26	V
		2.5 V Application	2.37	2.5	2.63	
VREF1/2	HSTL reference voltage	1.5 V Application	0.65	0.75	0.85	V
		1.8 V Application	0.85	0.9	0.95	
AVDD, VDDD, VDDT	Supply current	3.75 Gbps			440	mA
DVDD	Supply current	3.75 Gbps			290	mA
VDDR	Supply current	3.75 Gbps			25	mA
VDDQ	Supply current (1.6 V)	3.75 Gbps			520	mA
	Supply current (1.9 V)	3.75 Gbps			640	
VDDO	Supply current	3.75 Gbps			30	mA
VDDA_VCO, VDD_PLL, VDD_CML, VDDA_CP	Supply current	3.75 Gbps			100	mA
PD	Total power consumption	See Figure 4-18				W
AVDD, VDDD, VDDT	Shutdown current (1.26V)	ENABLE low(1)			40	mA
DVDD	Shutdown current (1.26V)	ENABLE low(1), HSTL powerdown			30	mA
		ENABLE low(1), HSTL active			130	
VDDR	Shutdown current (1.9V)	ENABLE low(1)			1	mA
VDDQ	Shutdown current (1.9V)	ENABLE low(1), HSTL powerdown			10	mA
		ENABLE low(1), HSTL active			230	
VDDO	Shutdown current (2.63V)	ENABLE low(1)			10	mA
VDDA_VCO, VDD_PLL, VDD_CML, VDDA_CP	Shutdown current (1.26V)	ENABLE low(1)			1	mA

(1) Toggle RST_N before setting ENABLE low for proper shutdown.

4.3 REFERENCE CLOCK TIMING REQUIREMENTS (REFCLKP/N)(1)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Frequency	Minimum data rate	60	–	375	MHz
Accuracy	XAUI/10GFC/1G PCS Mode	–100		100	ppm
Accuracy	Independent Channel Mode	0	0	0	ppm
Duty Cycle		45%	50%	55%	
Jitter	Random and deterministic			40	ps

(1) This clock should be crystal referenced to meet the requirements of the above table

4.4 REFERENCE CLOCK ELECTRICAL CHARACTERISTICS (REFCLKP/N)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
V_{id}	Differential Input Voltage		100		2000	mV_{PP}
C_{IN}	Input Capacitance				3	pF
R_{IN}	Input Differential Impedance		80	100	120	Ω
t_{rise}	Rise Time	20% to 80%	50		600	ps

4.5 SINGLE ENDED REFERENCE CLOCK ELECTRICAL CHARACTERISTICS (REFCLK)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
V_{IH}	High-Level Input Voltage		1.7		VDDO + 0.3	V
V_{IL}	Low-Level Input Voltage		–0.3		0.7	V
I_{IH}/I_{IL}	High/Low Input Current				±10	µA
t_{rise}	Rise Time	20% → 80%			1	ns
Jitter	Peak to Peak Jitter	Jitter Cleaner not used on REFCLK			40	ps
Tcyc	Duty Cycle		40%	50%	60%	Period

4.6 JITTER CLEANER TIMING PARAMETERS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
PLL Bandwidth	–3dB			1	MHz
Jitter Peaking				0.1	dB
VCO Output Jitter (rms)	2 MHz → 30 MHz			2	ps
VCO Output Jitter (rms)	1.2 MHz → 30 MHz			2.5	ps
VCO Output Jitter (rms)	600 kHz → 30 MHz			4	ps
VCO Output Jitter (rms)	300 kHz → 30 MHz			8	ps

4.7 LVCMOS ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –100 µA, Driver Enabled	2.1		VDDO	V
V_{OL}	Low-level output voltage	I_{OL} = 100 µA, Driver Enabled	0		0.2	V
V_{IH}	High-level input voltage		1.7		VDDO + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.7	V
I_{IH}, I_{IL}	Receiver Only Low/High Input Current				±10	µA
I_{OZ}	Driver Only	Driver Disabled			±35	µA
I_{OZ}	Driver/Receiver With Pullup/Pulldown	Driver Disabled With Pull Up/Down Enabled			±100	µA
C_{IN}	Input capacitance				5	pF

4.8 MDIO ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
V_{IH}	High-level input voltage	VDDM = 2.5 V	2.1		VDDM + 0.3	V
V_{IL}	Low-level input voltage	VDDM = 2.5 V	–0.3		0.7	V
V_{IH}	High-level input voltage	VDDM = 1.2 V	0.84		VDDM + 0.3	V
V_{IL}	Low-level input voltage	VDDM = 1.2 V	–0.3		0.36	V
V_{OL}	Low Level Output Voltage	VDDM = 2.5 V (I_{OL} = 100 µA)	0		0.2	V
V_{OL}	Low Level Output Voltage	VDDM = 1.2 V (I_{OL} = 100 µA)	0		0.2	V
V_{OH}	High Level Output Voltage	VDDM = 1.2/2.5 V (Open Drain Driver) Must be pulled up to VDDM on the customer board.	–	–	–	V
I_{IH}, I_{IL}	Low/High Input Current	MDC Signal			±20	µA
I_Z	Low/High input current	MDIO – Driver disabled			±50	µA
C_{IN}	Input capacitance				5	pF

4.9 HSTL SIGNALS (VDDQ = 1.5/1.8 V) ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
$V_{OH(dc)}$	High-level output voltage		VDDQ– 0.4		VDDQ	V
$V_{OL(dc)}$	Low-level output voltage				0.40	V
$V_{OH(ac)}$	High-level output voltage		VDDQ– 0.5		VDDQ	V
$V_{OL(ac)}$	Low-level output voltage				0.50	V
$V_{IH(dc)}$	High-level DC input voltage	DC input, logic high	VREF1/2 + 0.10		VDDQ + 0.3	V
$V_{IL(dc)}$	Low-level DC input voltage	DC input, logic low	-0.30		VREF1/2 – 0.1	V
$V_{IH(ac)}$	High-level AC input voltage	AC input, logic high	VREF1/2 + 0.20		VDDQ+ 0.3	V
$V_{IL(ac)}$	Low-level AC input voltage	AC input, logic low	-0.30		VREF1/2 – 0.20	V
$I_{OH(dc)}$	High output current		–8			mA
$I_{OL(dc)}$	Low output current		8			mA
C_{IN}	Input Capacitance				4	pF
Tacr	AC Test Condition	Rise Time (20 → 80%)	1	1	1	ns
Tacs	AC Test Condition	Signal Swing	1	1	1	V

4.10 SERIAL TRANSMITTER/RECEIVER CHARACTERISTICS

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
$V_{OD(pp)}$	TX Output Differential Peak-to-Peak voltage swing. De-emphasis Amount = 0%.	SWING = 000 (See Table 2-105)	80	125	180	mV_{PP}
		SWING = 001 (See Table 2-105)	210	250	330	
		SWING = 010 (See Table 2-105)	425	500	630	
		SWING = 011 (See Table 2-105)	530	625	780	
		SWING = 100 (See Table 2-105)	635	750	900	
		SWING = 101 (See Table 2-105)	900	1000	1200	
		SWING = 110 (See Table 2-105)	1000	1250	1500	
		SWING = 111 (See Table 2-105)	1080	1375	1650	
V_{DE}	TX Output De-Emphasis ($V_{OD(dpp)}$ = V_{DE} × Percentage of nominal $V_{OD(pp)}$)	See Table 2-104 for details on de-emphasis settings.	4.7%		72%	
V_{CMT}	TX output common mode voltage	See Figure 4-1.		AVDD – (0.25 × $V_{OD(pp)}$)		mV
V_{ID}	RX input differential voltage |RXP – RXN|	See Figure 4-3. Direct Coupled Mode Only	100		600	mV
		See Figure 4-3. AC Coupled Mode Only	100		1100	
$V_{ID(pp)}$	RX input differential peak-to-peak voltage swing 2 × |RXP – RXN|	See Figure 4-3. Direct Coupled Mode Only	200		1200	mV_{PP}
		See Figure 4-3. AC Coupled Mode Only	200		2200	
V_{CMR}	RX input common mode voltage range	See Figure 4-3. Direct Coupled Mode Only	800		0.9 × AVDD	mV
I_{LKG}	RX input leakage current		–10		10	µA
C_I	RX input capacitance				2	pF
t_r, t_f	Differential output signal rise, fall time (20% to 80%)	R_L = 50 Ω, C_L = 5 pF, See Figure 4-1	80		160	ps
J_{TOL}	Jitter Tolerance, Total Jitter at Serial Input	Zero crossing, See Figure 4-4.			0.65	UI(1)
J_{DR}	Serial Input Deterministic Jitter	Zero crossing, See Figure 4-4.			0.37	UI
J_T	Serial Output Total Jitter	3.125 GHz.		0.20	0.35	UI
J_D	Serial Output Deterministic Jitter	3.125 GHz.			0.17	UI
$R_{(LATENCY)}$	Total delay from RX input to RD output	See Figure 2-21. XAUI/10GFC Mode			950	Bit Times
$T_{(LATENCY)}$	Total delay from TD input to TX output	See Figure 2-20. XAUI/10GFC Mode			900	Bit Times
$R_{(LATENCY)}$	Total delay from RX input to RD output	See Figure 2-21. 1000Base-X Mode			190	Bit Times
$T_{(LATENCY)}$	Total delay from TD input to TX output	See Figure 2-20. 1000Base-X Mode			130	Bit Times
$R_{(LATENCY)}$	Total delay from RX input to RD output	See Figure 2-21. NBID Mode	110		200	Bit Times
$T_{(LATENCY)}$	Total delay from TD input to TX output	See Figure 2-20. NBID Mode	90		250	Bit Times
$R_{(LATENCY)}$	Total delay from RX input to RD output	See Figure 2-21. TBID Mode	90		200	Bit Times
$T_{(LATENCY)}$	Total delay from TD input to TX output	See Figure 2-20. TBID Mode	80		250	Bit Times

(1) Unit Interval = one serial bit time (min. 320 ps)

4.11 Parameter Measurement

Table 4-1. XAUI Driver Template Parameters

PARAMETER	NEAR END VALUE	FAR END VALUE	UNIT
X1 (See Figure 4-2)	0.175	0.275	UI
X2 (See Figure 4-2)	0.390	0.400	UI
A1 (See Figure 4-2)	400	100	mV
A2 (See Figure 4-2)	800	800	mV

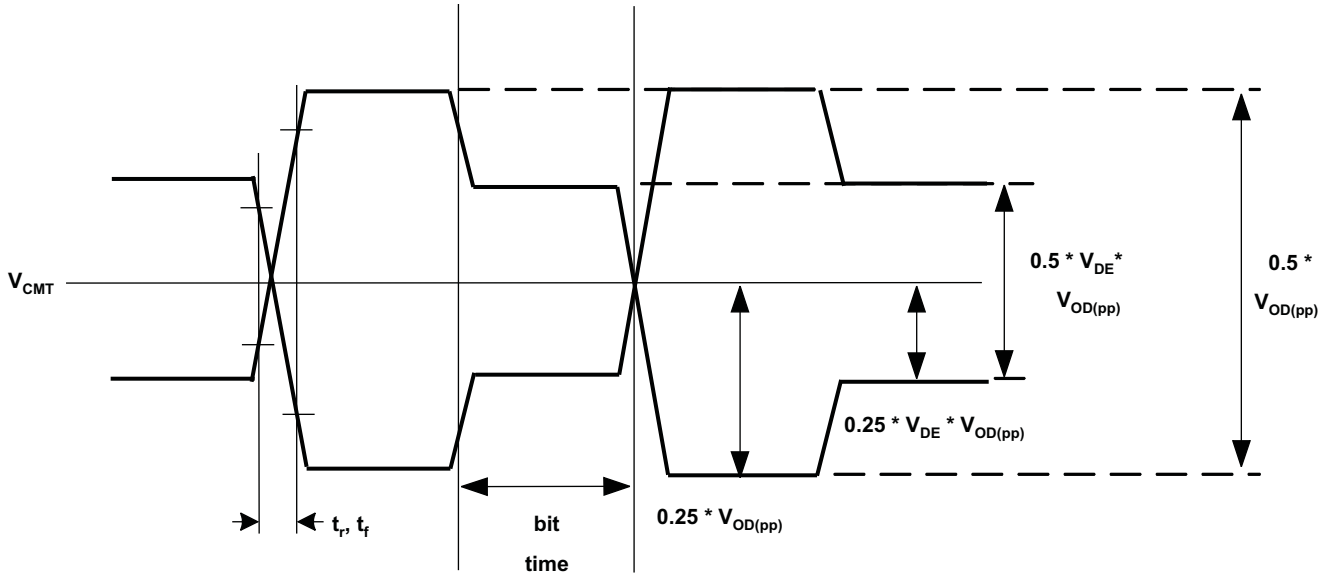


Figure 4-1. Transmit Output Waveform Parameter Definitions

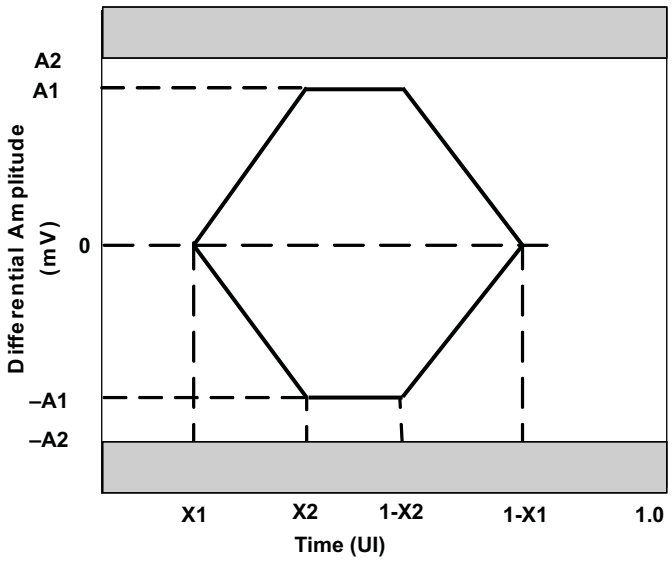


Figure 4-2. Transmit Template

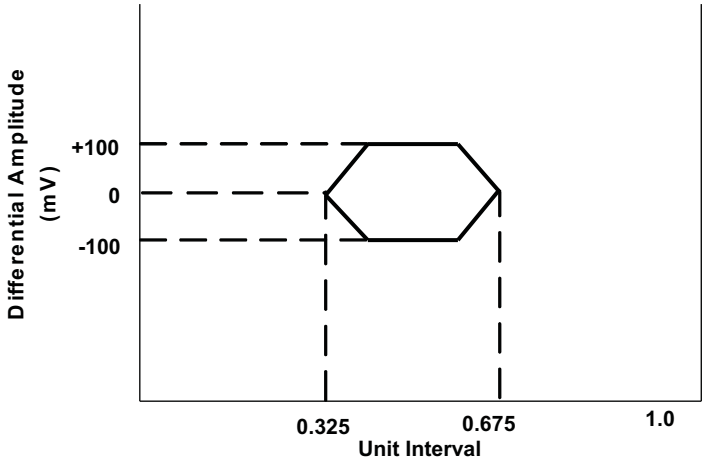
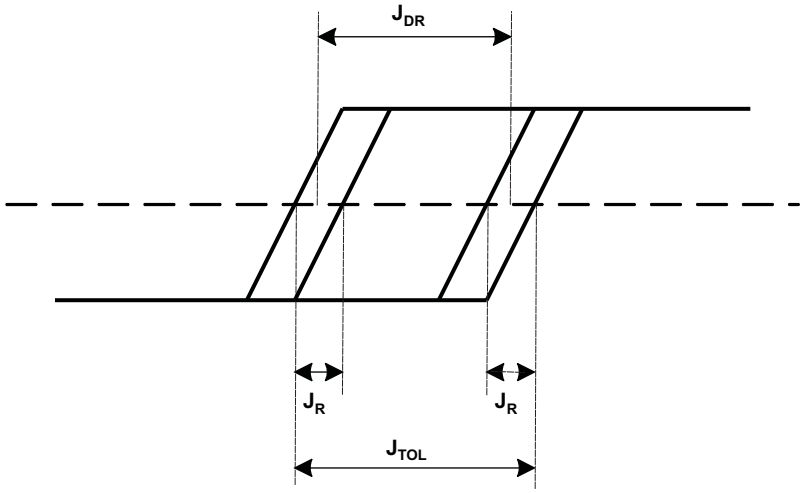


Figure 4-3. Receive Template



Note: $J_{TOL} = J_R + J_{DR}$, where J_{TOL} is the receive jitter tolerance, J_{DR} is the received deterministic jitter, and J_R is the Gaussian random edge jitter distribution at a maximum BER = 10^{-12}.

Figure 4-4. Input Jitter

The TLK3134 has several different application modes, which impact parallel interface I/O timing definitions. Each of the modes is defined below, and then subsequently referred to in the detailed timing parameter definitions. RXDATA and RXCLK, and TXDATA and TXCLK in the detailed timing specification will be defined by the exact following signal definitions.

Table 4-2. Parallel Interface – Valid Signal Operational Mode Definitions

TIMING MODE NAME	USAGE MODE	TX SIGNALS USED	RX SIGNALS USED
XGMII	XAUI Applications, 10 Gigabit Fibre Channel Applications. Only DDR Timing Supported See Section 4.12: HSTL Output Switching Characteristics (DDR Timing Mode Only) and Section 4.14: HSTL (DDR Timing Mode Only) Input Timing Requirements for AC timing details.	TXDATA = TXD_[31:0] and TXC_[3:0]. TXCLK = TXCLK_[1].	RXDATA = RXD_[31:0] and RXC_[3:0]. RXCLK = RXCLK_[1].
RGMII, RTBI	1000Base-X Applications Reduced Ten Bit Applications (RTBI) Only DDR Timing Supported See Section 4.12: HSTL Output Switching Characteristics (DDR Timing Mode Only) and Section 4.14: HSTL (DDR Timing Mode Only) Input Timing Requirements for AC timing details. Note: In RGMII Mode CH0: TX_EN/TX_ER = TXD_[4] CH1: TX_EN/TX_ER = TXD_[12] CH2: TX_EN/TX_ER = TXD_[20] CH3: TX_EN/TX_ER = TXD_[28] CH0: RX_DV/RX_ER = RXD_[4] CH1: RX_DV/RX_ER = RXD_[12] CH2: RX_DV/RX_ER = RXD_[20] CH3: RX_DV/RX_ER = RXD_[28]	TXDATA = TXD_[4:0] TXCLK = TXCLK_[0] -or- TXDATA = TXD_[12:8] TXCLK = TXCLK_ [1] -or- TXDATA = TXD_ [20:16] TXCLK = TXCLK_ [2] -or- TXDATA = TXD_ [28:24] TXCLK = TXCLK_ [3]	RXDATA = RXD_[4:0] RXCLK = RXCLK_[0] -or- RXDATA = RXD_ [12:8] RXCLK = RXCLK_ [1] -or- RXDATA = RXD_ [20:16] RXCLK = RXCLK_ [2] -or- RXDATA = RXD_ [28:24] RXCLK = RXCLK_ [3]
TBI, GMII	Ten Bit Interface Mode (TBI) Only SDR Timing Supported See Section 4.13: HSTL Output Switching Characteristics (SDR Timing Mode Only) and Section 4.15: HSTL (SDR Timing Mode Only) Input Timing Requirements for AC timing details. Note: In GMII Mode CH0: TX_EN = TXC_[0] CH1: TX_EN = TXC_[1] CH2: TX_EN = TXC_[2] CH3: TX_EN = TXC_[3] CH0: TX_ER = TXC_[4] CH1: TX_ER = TXC_[5] CH2: TX_ER = TXC_[6] CH3: TX_ER = TXC_[7] CH0: RX_DV = RXC_[0] CH1: RX_DV = RXC_[1] CH2: RX_DV = RXC_[2] CH3: RX_DV = RXC_[3] CH0: RX_ER = RXC_[4] CH1: RX_ER = RXC_[5] CH2: RX_ER = RXC_[6] CH3: RX_ER = RXC_[7] Note: In TBI Mode CH0: TX Data Bit 8 = TXC_[0] CH1: TX Data Bit 8 = TXC_[1] CH2: TX Data Bit 8 = TXC_[2] CH3: TX Data Bit 8 = TXC_[3] CH0: TX Data Bit 9 = TXC_[4] CH1: TX Data Bit 9 = TXC_[5] CH2: TX Data Bit 9 = TXC_[6] CH3: TX Data Bit 9 = TXC_[7] CH0: RX Data Bit 8 = RXC_[0] CH1: RX Data Bit 8 = RXC_[1] CH2: RX Data Bit 8 = RXC_[2] CH3: RX Data Bit 8 = RXC_[3] CH0: RX Data Bit 9 = RXC_[4] CH1: RX Data Bit 9 = RXC_[5] CH2: RX Data Bit 9 = RXC_[6] CH3: RX Data Bit 9 = RXC_[7]	TXDATA = TXC_ [4],TXC_ [0], TXD[7:0] TXCLK = TXCLK_ [0] -or- TXDATA = TXC_ [5],TXC_ [1], TXD_ [15:8] TXCLK = TXCLK_ [1] -or- TXDATA = TXC_ [6],TXC_ [2], TXD_ [23:16] TXCLK = TXCLK_ [2] -or- TXDATA = TXC_ [7],TXC_ [3], TXD_ [31:24] TXCLK = TXCLK_ [3]	RXDATA = RXC_ [4],RXC_ [0], RXD[7:0] RXCLK = RXCLK_ [0] -or- RXDATA = RXC_ [5],RXC_ [1], RXD_ [15:8] RXCLK = RXCLK_ [1] -or- RXDATA = RXC_ [6],RXC_ [2], RXD_ [23:16] RXCLK = RXCLK_ [2] -or- RXDATA = RXC_ [7],RXC_ [3], RXD_ [31:24] RXCLK = RXCLK_ [3]
EBI	Eight Bit Interface Mode (EBI) SDR Timing Support See Section 4.13: HSTL Output Switching Characteristics (SDR Timing Mode Only) and Section 4.15: HSTL (SDR Timing Mode Only) Input Timing Requirements for AC timing details.	TXDATA = TXD_ [7:0] TXCLK = TXCLK_ [0] -or- TXDATA = TXD_ [15:8] TXCLK = TXCLK_ [1] -or- TXDATA = TXD_ [23:16] TXCLK = TXCLK_ [2] -or- TXDATA = TXD_ [31:24] TXCLK = TXCLK_ [3]	RXDATA = RXD_ [7:0] RXCLK = RXCLK_ [0] -or- RXDATA = RXD_ [15:8] RXCLK = RXCLK_ [1] -or- RXDATA = RXD_ [23:16] RXCLK = RXCLK_ [2] -or- RXDATA = RXD_ [31:24] RXCLK = RXCLK_ [3]
REBI	Reduced Eight Bit Interface Mode (REBI) DDR Timing Support See Section 4.12: HSTL Output Switching Characteristics (DDR Timing Mode Only) and Section 4.14: HSTL (DDR Timing Mode Only) Input Timing Requirements for AC timing details.	TXDATA = TXD_ [3:0] TXCLK = TXCLK_ [0] -or- TXDATA = TXD_ [11:8] TXCLK = TXCLK_ [1] -or- TXDATA = TXD_ [19:16] TXCLK = TXCLK_ [2] -or- TXDATA = TXD_ [27:24] TXCLK = TXCLK_ [3]	RXDATA = RXD_ [3:0] RXCLK = RXCLK_ [0] -or- RXDATA = RXD_ [11:8] RXCLK = RXCLK_ [1] -or- RXDATA = RXD_ [19:16] RXCLK = RXCLK_ [2] -or- RXDATA = RXD_ [27:24] RXCLK = RXCLK_ [3]

Table 4-2. Parallel Interface – Valid Signal Operational Mode Definitions (continued)

TIMING MODE NAME	USAGE MODE	TX SIGNALS USED	RX SIGNALS USED
NBI	Nine Bit Interface Mode (NBI) (Un-encoded Data Byte + 1 Control Bit) SDR Timing Support See Section 4.13: HSTL Output Switching Characteristics (SDR Timing Mode Only) and Section 4.15: HSTL (SDR Timing Mode Only) Input Timing Requirements for AC timing details. Note: In NBI Mode CH0: TX Control Bit = TXC_[0] CH1: TX Control Bit = TXC_[1] CH2: TX Control Bit = TXC_[2] CH3: TX Control Bit = TXC_[3] CH0: RX Control Bit = RXC_[0] CH1: RX Control Bit = RXC_[1] CH2: RX Control Bit = RXC_[2] CH3: RX Control Bit = RXC_[3]	TXDATA = TXC_ [0], TXD[7:0] TXCLK = TXCLK_ [0] -or- TXDATA = TXC_ [1], TXD_ [15:8] TXCLK = TXCLK_ [1] -or- TXDATA = TXC_ [2], TXD_ [23:16] TXCLK = TXCLK_ [2] -or- TXDATA = TXC_ [3], TXD_ [31:24] TXCLK = TXCLK_ [3]	RXDATA = RXC_ [0], RXD[7:0] RXCLK = RXCLK_ [0] -or- RXDATA = RXC_ [1], RXD_ [15:8] RXCLK = RXCLK_ [1] -or- RXDATA = RXC_ [2], RXD_ [23:16] RXCLK = RXCLK_ [2] -or- RXDATA = RXC_ [3], RXD_ [31:24] RXCLK = RXCLK_ [3]
RNBI	Reduced Nine Bit Interface Mode (RNBI) (Un-encoded Data Byte + 1 Control Bit) DDR Timing Support See Section 4.12: HSTL Output Switching Characteristics (DDR Timing Mode Only) and Section 4.14: HSTL (DDR Timing Mode Only) Input Timing Requirements for AC timing details. Note: In RNBI Mode CH0: TX Control Bit = TXD_[4] CH1: TX Control Bit = TXD_[12] CH2: TX Control Bit = TXD_[20] CH3: TX Control Bit = TXD_[28] CH0: RX Control Bit = RXD_[4] CH1: RX Control Bit = RXD_[12] CH2: RX Control Bit = RXD_[20] CH3: RX Control Bit = RXD_[28]	TXDATA = TXD_[4:0] TXCLK = TXCLK_[0] -or- TXDATA = TXD_[12:8] TXCLK = TXCLK_ [1] -or- TXDATA = TXD_ [20:16] TXCLK = TXCLK_ [2] -or- TXDATA = TXD_ [28:24] TXCLK = TXCLK_ [3]	RXDATA = RXD_[4:0] RXCLK = RXCLK_[0] -or- RXDATA = RXD_ [12:8] RXCLK = RXCLK_ [1] -or- RXDATA = RXD_ [20:16] RXCLK = RXCLK_ [2] -or- RXDATA = RXD_ [28:24] RXCLK = RXCLK_ [3]
TBID	Ten Bit Interface DDR Mode (TBID) Only DDR Timing Supported See Section 4.12: HSTL Output Switching Characteristics (DDR Timing Mode Only) and Section 4.14: HSTL (DDR Timing Mode Only) Input Timing Requirements for AC timing details. Note: In TBID Mode CH0: TX Data Bit 8 = TXC_[0] CH1: TX Data Bit 8 = TXC_[1] CH2: TX Data Bit 8 = TXC_[2] CH3: TX Data Bit 8 = TXC_[3] CH0: TX Data Bit 9 = TXC_[4] CH1: TX Data Bit 9 = TXC_[5] CH2: TX Data Bit 9 = TXC_[6] CH3: TX Data Bit 9 = TXC_[7] CH0: RX Data Bit 8 = RXC_[0] CH1: RX Data Bit 8 = RXC_[1] CH2: RX Data Bit 8 = RXC_[2] CH3: RX Data Bit 8 = RXC_[3] CH0: RX Data Bit 9 = RXC_[4] CH1: RX Data Bit 9 = RXC_[5] CH2: RX Data Bit 9 = RXC_[6] CH3: RX Data Bit 9 = RXC_[7]	TXDATA = TXC_ [4],TXC_ [0], TXD[7:0] TXCLK = TXCLK_ [0] -or- TXDATA = TXC_ [5],TXC_ [1], TXD_ [15:8] TXCLK = TXCLK_ [1] -or- TXDATA = TXC_ [6],TXC_ [2], TXD_ [23:16] TXCLK = TXCLK_ [2] -or- TXDATA = TXC_ [7],TXC_ [3], TXD_ [31:24] TXCLK = TXCLK_ [3]	RXDATA = RXC_ [4],RXC_ [0], RXD[7:0] RXCLK = RXCLK_ [0] -or- RXDATA = RXC_ [5],RXC_ [1], RXD_ [15:8] RXCLK = RXCLK_ [1] -or- RXDATA = RXC_ [6],RXC_ [2], RXD_ [23:16] RXCLK = RXCLK_ [2] -or- RXDATA = RXC_ [7],RXC_ [3], RXD_ [31:24] RXCLK = RXCLK_ [3]
NBID	Nine Bit Interface DDR Mode (NBID) (Un-encoded Data Byte + 1 Control Bit) DDR Timing Support See Section 4.12: HSTL Output Switching Characteristics (DDR Timing Mode Only) and Section 4.14: HSTL (DDR Timing Mode Only) Input Timing Requirements for AC timing details. Note: In NBID Mode CH0: TX Control Bit = TXC_[0] CH1: TX Control Bit = TXC_[1] CH2: TX Control Bit = TXC_[2] CH3: TX Control Bit = TXC_[3] CH0: RX Control Bit = RXC_[0] CH1: RX Control Bit = RXC_[1] CH2: RX Control Bit = RXC_[2] CH3: RX Control Bit = RXC_[3]	TXDATA = TXC_ [0], TXD[7:0] TXCLK = TXCLK_ [0] -or- TXDATA = TXC_ [1], TXD_ [15:8] TXCLK = TXCLK_ [1] -or- TXDATA = TXC_ [2], TXD_ [23:16] TXCLK = TXCLK_ [2] -or- TXDATA = TXC_ [3], TXD_ [31:24] TXCLK = TXCLK_ [3]	RXDATA = RXC_ [0], RXD[7:0] RXCLK = RXCLK_ [0] -or- RXDATA = RXC_ [1], RXD_ [15:8] RXCLK = RXCLK_ [1] -or- RXDATA = RXC_ [2], RXD_ [23:16] RXCLK = RXCLK_ [2] -or- RXDATA = RXC_ [3], RXD_ [31:24] RXCLK = RXCLK_ [3]

4.12 HSTL Output Switching Characteristics (DDR Timing Mode Only)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{setup}	RXDATA setup prior to RXCLK transition high or low	Source Centered, See Figure 4-5. Note: C_{load} = 10 pF, using timing reference of VDDQ/2	0.15 × t_{period}			ps
t_{hold}	RXDATA hold after RXCLK transition high or low	Source Centered, See Figure 4-5. Note: C_{load} = 10 pF, using timing reference of VDDQ/2	0.15 × t_{period}			ps
T_{duty}	RXCLK Duty Cycle	Source Centered and Source Aligned. Note: C_{load} = 10 pF, using timing reference of VDDQ/2.	45%		55%	
t_{period}	RXCLK Period	Source Centered and Source Aligned	6.25		16.67 (1)	ns
T_{freq}	RXCLK Frequency	Source Centered and Source Aligned	60 (2)		160	MHz
T_{pd}	RXCLK rising or falling to RXDATA valid.	Source Aligned, See Figure 4-6. Note: C_{load} = 10 pF, using timing reference of VDDQ/2	–0.10 × t_{period}		+0.10 × t_{period}	ps

(1) In TBID/NBID Modes Only, the maximum allowed RXCLK period is 33.33 ns.
(2) In TBID/NBID Modes Only, the minimum allowed RXCLK frequency is 30 MHz.

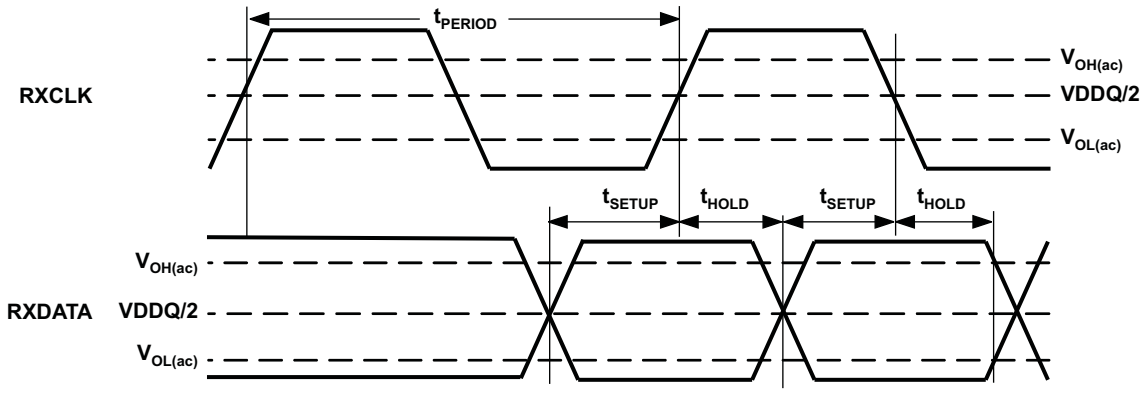


Figure 4-5. HSTL (DDR Timing Mode Only) Source Centered Output Timing Requirements

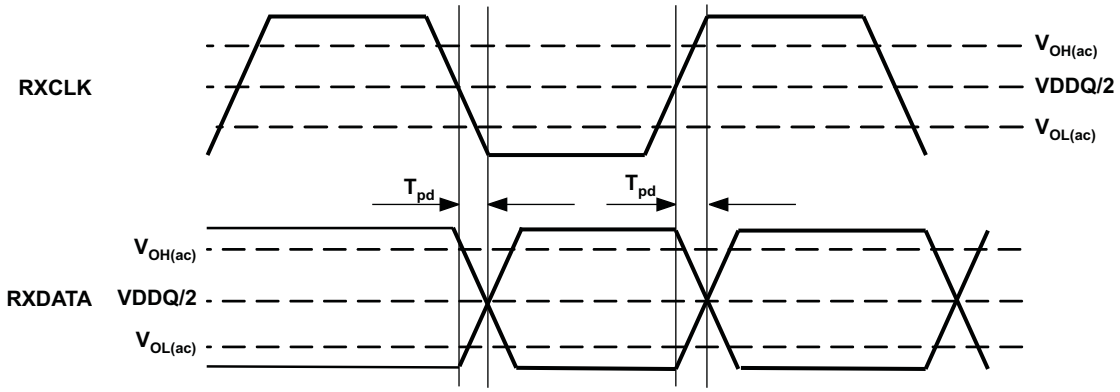


Figure 4-6. HSTL (DDR Timing Mode Only) Source Aligned Output Timing Requirements

4.13 HSTL Output Switching Characteristics (SDR Timing Mode Only)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
T_{duty}	RXCLK Duty Cycle	Rising and Falling Edge Aligned Data Note: C_{load} = 10pF, using timing reference of VDDQ/2.	40%	60%	
t_{period}	RXCLK Period	Rising and Falling Edge Aligned Data	2.67	16.67	ns
T_{freq}	RXCLK Frequency	Rising and Falling Edge Aligned Data	60	375	MHz
T_{pd}	RXCLK rising to RXDATA valid.	Rising Edge Aligned Note: C_{load} = 10pF, using timing reference of VDDQ/2.	–0.10 × t_{period}	+0.10 × t_{period}	ps
T_{pd}	RXCLK falling to RXDATA valid.	Falling Edge Aligned Note: C_{load} = 10pF, using timing reference of VDDQ/2.	–0.10 × t_{period}	+0.10 × t_{period}	ps

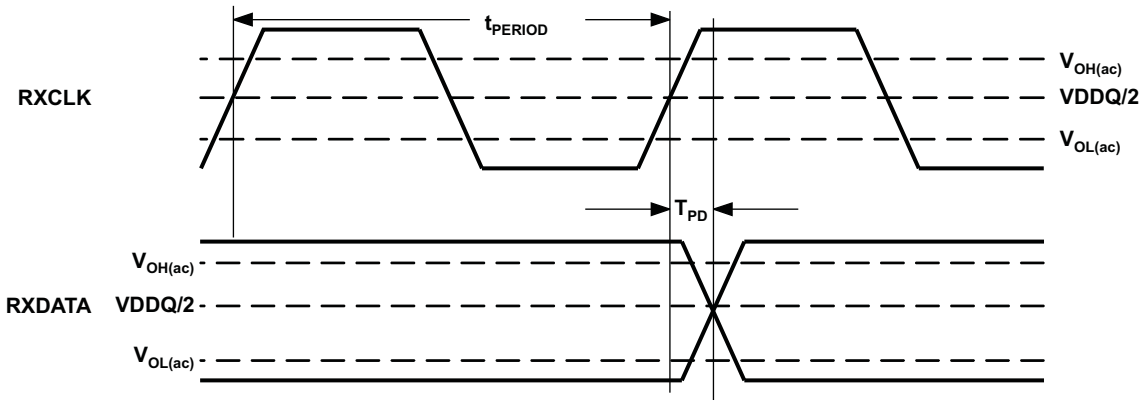


Figure 4-7. HSTL (SDR Timing Mode Only) Rising Edge Aligned Output Timing Requirements

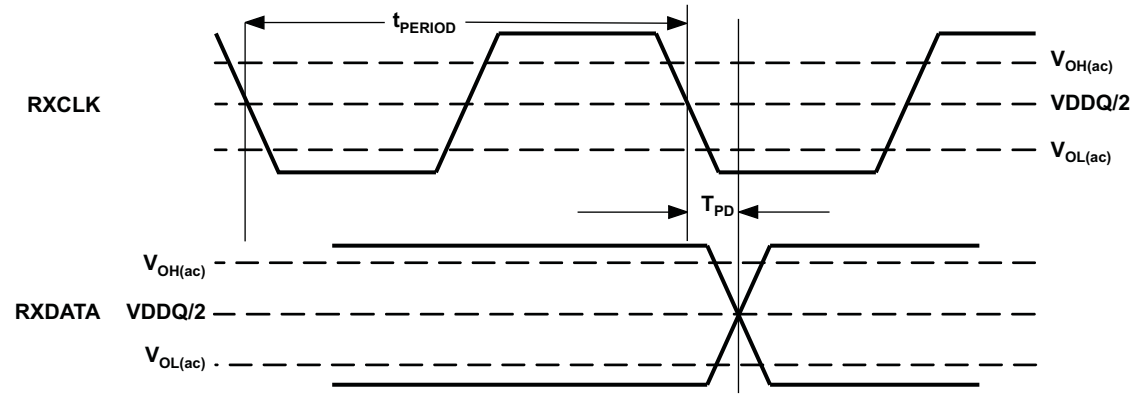


Figure 4-8. HSTL (SDR Timing Mode Only) Falling Edge Aligned Output Timing Requirements

4.14 HSTL (DDR Timing Mode Only) Input Timing Requirements

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM(1)	MAX	UNIT
t_{setup}	TXDATA setup prior to TXCLK transition high or low	Source Centered. See Figure 4-9. Note: Input timing reference of VDDQ/2, with ±1 ns/V rise time on all inputs signals.	0.075 × t_{period}			ps
t_{hold}	TXDATA hold after TXCLK transition high or low	Source Centered. See Figure 4-9. Note: Input timing reference of VDDQ/2, with ±1 ns/V rise time on all inputs signals.	0.075 × t_{period}			ps
t_{duty}	TXCLK Duty Cycle	Source Centered Note: Input timing reference of VDDQ/2, with ±1 ns/V rise time on all inputs signals.	40%		60%	
t_{duty}	TXCLK Duty Cycle	Source Aligned. Note: Input timing reference of VDDQ/2, with ±1 ns/V rise time on all inputs signals.	45%		55%	
t_{period}	TXCLK Period	Source Centered and Aligned.	6.25		16.67(2)	ns
Tfreq	TXCLK Frequency	Source Centered and Aligned.	60(3)		160	MHz
T_{skew}	TXCLK rising or falling to TXDATA valid.	Source Aligned. See Figure 4-10. Note: Input timing reference of VDDQ/2, with ±1 ns/V rise time on all inputs signals.	–0.175 × t_{period} (4)		+0.175 × t_{period} (5)	ps

(1) All typical values are at 25°C and with a nominal supply.
(2) In TBID/NBID Modes Only, the maximum allowed TXCLK period is 33.33 ns.
(3) In TBID/NBID Modes Only, the minimum allowed TXCLK frequency is 30 Mhz.
(4) In TBID/NBID Modes, when the TXCLK is in the 30 → 60 Mhz range, this parameter becomes -0.10 × t_{period}
(5) In TBID/NBID Modes, when the TXCLK is in the 30→ 60 Mhz range, this parameter becomes +0.10 × t_{period}

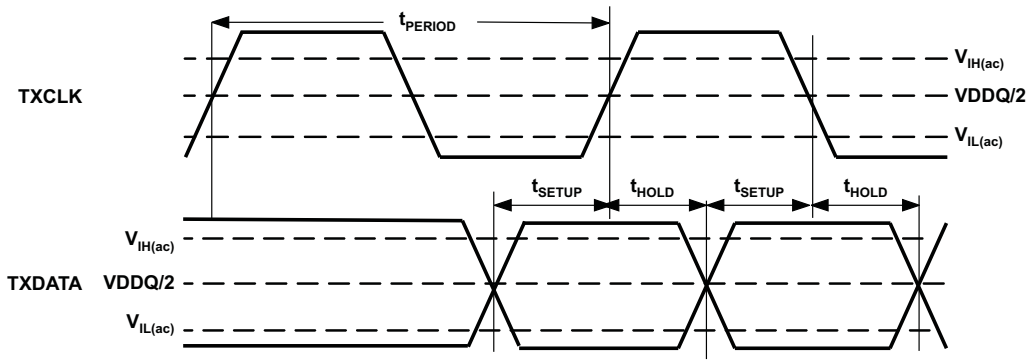


Figure 4-9. HSTL (DDR Timing Mode Only) Source Centered Data Input Timing Requirements

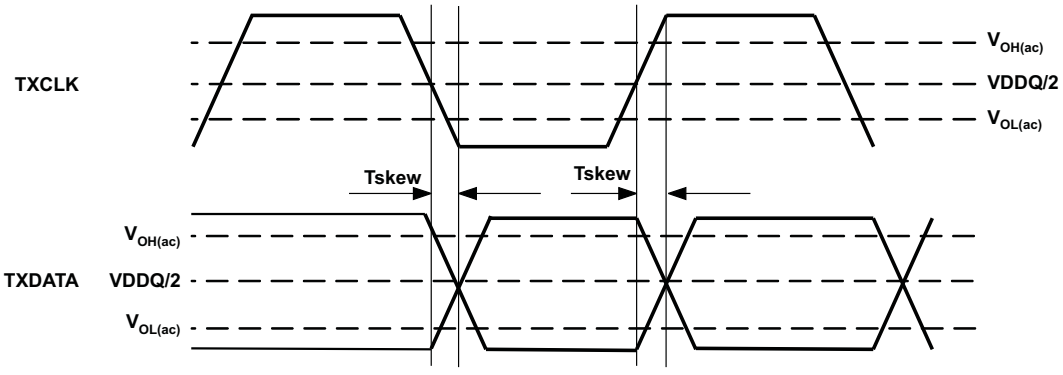


Figure 4-10. HSTL (DDR Timing Mode Only) Source Aligned Data Input Timing Requirements

4.15 HSTL (SDR Timing Mode Only) Input Timing Requirements

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM(1)	MAX	UNIT
t_{setup}	TXDATA setup prior to TXCLK transition high	Falling Edge Aligned (Rising Edge Sampled) Data See Figure 4-11. Note: Input timing reference of VDDQ/2, with ±1 ns/V rise time on all inputs signals.	480			ps
t_{hold}	TXDATA hold after TXCLK transition high	Falling Edge Aligned (Rising Edge Sampled) Data See Figure 4-11. Note: Input timing reference of VDDQ/2, with ±1 ns/V rise time on all inputs signals.	480			ps
t_{setup}	TXDATA setup prior to TXCLK transition low	Rising Edge Aligned (Falling Edge Sampled) Data See Figure 4-12. Note: Input timing reference of VDDQ/2, with ±1 ns/V rise time on all inputs signals.	480			ps
t_{hold}	TXDATA hold after TXCLK transition low	Rising Edge Aligned (Falling Edge Sampled) Data See Figure 4-12. Note: Input timing reference of VDDQ/2, with ±1 ns/V rise time on all inputs signals.	480			ps
t_{duty}	TXCLK Duty Cycle	Rising and Falling Edge Sampled Data Note: Input timing reference of VDDQ/2, with ±1 ns/V rise time on all inputs signals.	40%		60%	
t_{period}	TXCLK Period	Rising and Falling Edge Aligned Data	2.67		16.67	ns
T_{freq}	TXCLK Frequency	Rising and Falling Edge Aligned Data	60		375	MHz

(1) All typical values are at 25°C and with a nominal supply.

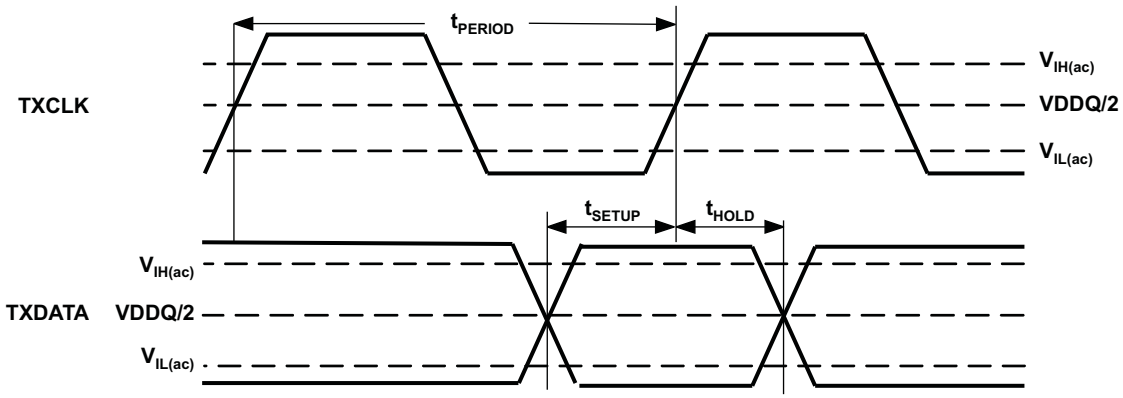


Figure 4-11. HSTL (SDR Timing Mode Only) Falling Edge Aligned (Rising Edge Sampled) Data Input Timing Requirements

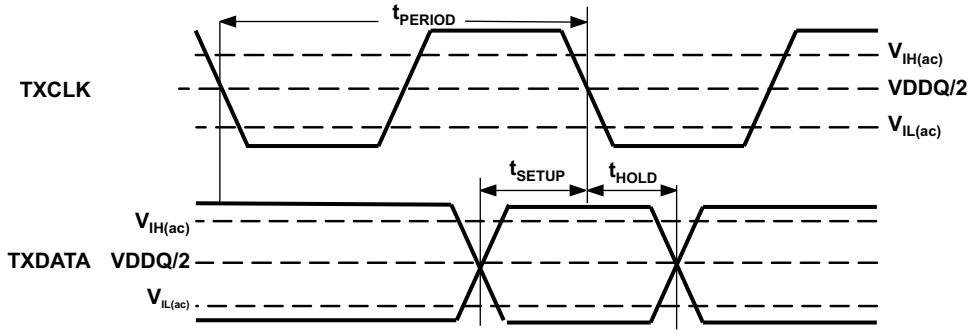


Figure 4-12. HSTL (SDR Timing Mode Only) Rising Edge Aligned (Falling Edge Sampled) Data Input Timing Requirements

4.16 MDIO Timing Requirements Over Recommended Operating Conditions(1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{period}	MDC period	See Figure 4-13.	100			ns
t_{setup}	MDIO setup to ↑ MDC	See Figure 4-13.	10			ns
t_{hold}	MDIO hold to ↑ MDC	See Figure 4-13.	10			ns
T_{valid}	MDIO valid from MDC ↑		0		40	ns

(1) Unless otherwise noted.

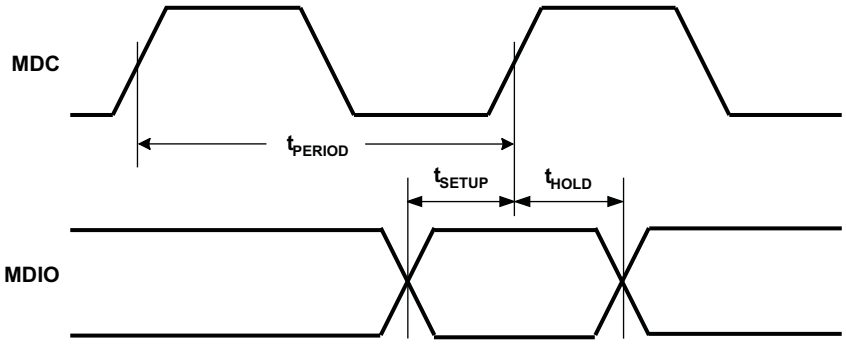


Figure 4-13. MDIO Read/Write Timing

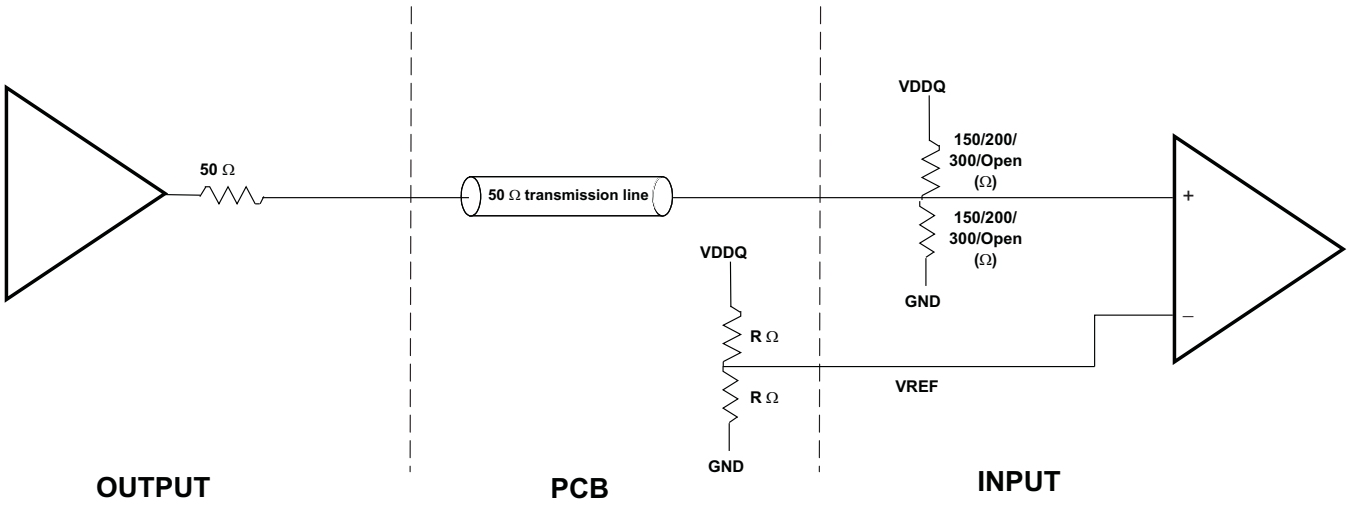


Figure 4-14. HSTL I/O Schematic

4.17 JTAG Timing Requirements Over Recommended Operating Conditions[1]

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{period}	TCK period	See Figure 4-15.	66.67			ns
t_{setup}	TDI/TMS/TRST_N setup to ↑ TCK	See Figure 4-15.	3			ns
t_{hold}	TDI/TMS/TRST_N hold from ↑ TCK	See Figure 4-15.	5			ns
T_{valid}	TDO delay from TCK falling	See Figure 4-15.	0		5	ns

(1) Unless otherwise noted.

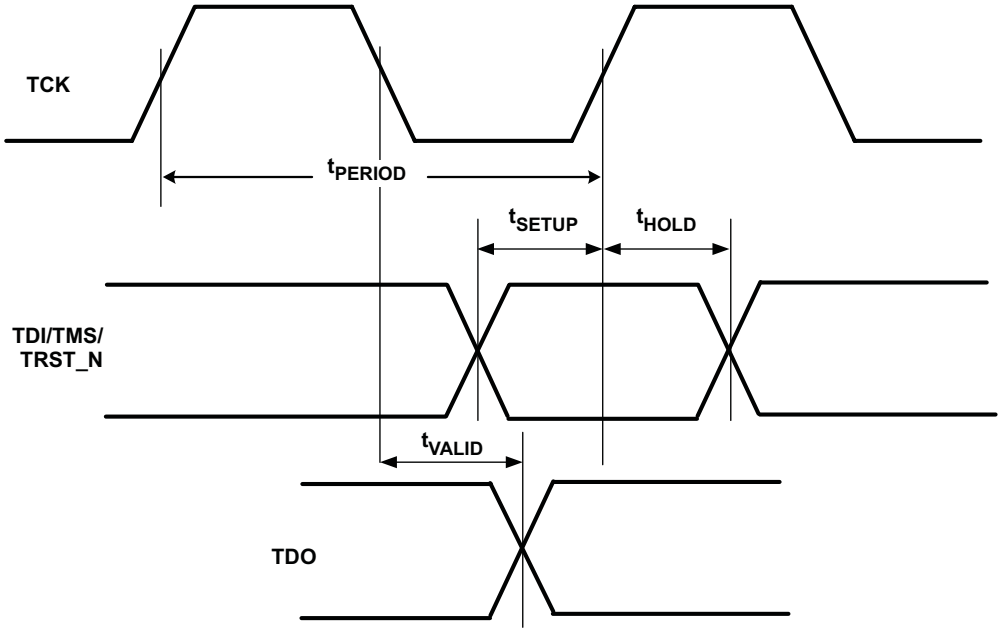
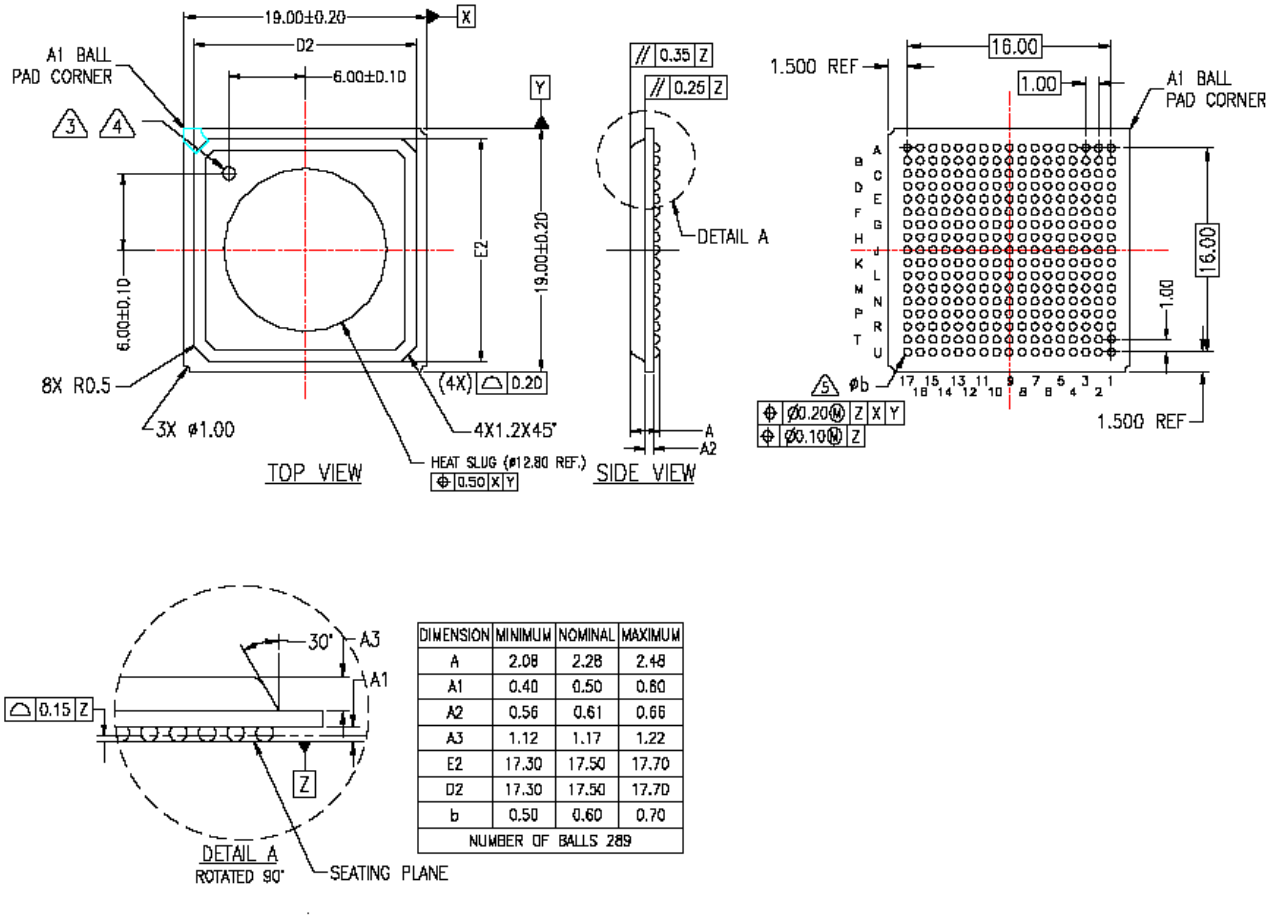


Figure 4-15. JTAG Timing

Application Mode	XGMII	RGMII	GMII	TBI	RTBI	NBI	RNBI	EBI	REBI	TBID	NBID
Gigabit Ethernet (1000Base-X) 1.25 Gbps	N	Y	Y	N	N	N	N	N	N	N	N
CPRI x1 0.6144 Gbps	N	N	N	Y	Y	Y	Y	N	N	Y	Y
CPRI x2 1.2288 Gbps	N	N	N	Y	Y	Y	Y	N	N	Y	Y
CPRI x4 2.4576 Gbps	N	N	N	Y	N	Y	N	N	N	Y	Y
OBSAI x1 0.768 Gbps	N	N	N	Y	Y	Y	Y	N	N	Y	Y
OBSAI x2 1.536 Gbps	N	N	N	Y	Y	Y	Y	N	N	Y	Y
OBSAI x4 3.072 Gbps	N	N	N	Y	N	Y	N	N	N	Y	Y
10 Gigabit Ethernet (XAUI) 4x3.125 Gbps	Y	N	N	N	N	N	N	N	N	N	N
10 Gigabit Fibre Channel (10GFC) 4x3.1875 Gbps	Y	N	N	N	N	N	N	N	N	N	N
Fibre Channel 1X 1.0625 Gbps	N	N	N	Y	Y	Y	Y	N	N	Y	Y
Fibre Channel 2X 2.125 Gbps	N	N	N	Y	N	Y	N	N	N	Y	Y
8 Bit SERDES Mode 0.600 → 1.28 Gbps	N	N	N	N	N	N	N	Y	Y	N	N
8 Bit SERDES Mode 1.28 → 3.0 Gbps	N	N	N	N	N	N	N	Y	N	N	N
10 Bit SERDES Mode 0.600 → 1.6 Gbps	N	N	N	Y	Y	N	N	N	N	Y	N
10 Bit SERDES Mode 1.6 → 3.2 Gbps	N	N	N	Y	N	N	N	N	N	Y	N
10 Bit SERDES Mode 3.2 → 3.75 Gbps	N	N	N	Y	N	N	N	N	N	N	N
9 Bit SERDES Mode 0.600 → 1.6 Gbps	N	N	N	N	N	Y	Y	N	N	N	Y
9 Bit SERDES Mode 1.6 → 3.2 Gbps	N	N	N	N	N	Y	N	N	N	N	Y
9 Bit SERDES Mode 3.2 → 3.75 Gbps	N	N	N	N	N	Y	N	N	N	N	N

A. Latency measurement only operates in TBI, TBID, and RTBI modes.

Figure 4-16. TLK3134 Application Mode vs Interface Timing Mode Support



DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	2.08	2.28	2.48
A1	0.40	0.50	0.60
A2	0.56	0.61	0.66
A3	1.12	1.17	1.22
E2	17.30	17.50	17.70
D2	17.30	17.50	17.70
b	0.50	0.60	0.70
NUMBER OF BALLS 289			

Figure 4-17. PACKAGE Information (Package Designator = ZEL)

4.18 Package Dissipation Rating

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
θ_{JA}	Junction to free air thermal resistance	Airflow = 0 lfpm		14.45		°C/W
θ_{JA}	Junction to free air thermal resistance	Airflow = 150 lfpm		7.50		°C/W

Device Total Worst Case Power (All Channels Active, All Supplies +5%, T=85C)								
Serial Bit Rate = 3.75Gbps								
VDDQ Voltage	1.6V				1.9V			
JC PLL Enabled	N		Y		N		Y	
HSTL Input Termination	None	Max.	None	Max.	None	Max.	None	Max.
Total Power (mW)	1489	1828	1557	1893	1730	2201	1795	2278
Serial Bit Rate = 3.125Gbps (XAUI)								
VDDQ Voltage	1.6V				1.9V			
JC PLL Enabled	N		Y		N		Y	
HSTL Input Termination	None	Max.	None	Max.	None	Max.	None	Max.
Total Power (mW)	1253	1691	1295	1740	1424	2039	1472	2091
Serial Bit Rate = 1.25Gbps (Gigabit Ethernet)								
VDDQ Voltage	1.6V				1.9V			
JC PLL Enabled	N		Y		N		Y	
HSTL Input Termination	None	Max.	None	Max.	None	Max.	None	Max.
Total Power (mW)	1078	1490	1178	1591	1264	1845	1366	1947

Figure 4-18. Worst Case Device Power Dissipation

A APPENDIX A – Frequency Ranges Supported

The following tables show the details of REFCLK input frequency versus Jitter Cleaner PLL multiplier value for each application TLK3134 supports.

If the desired serial bit rate is between 2.0 Gbps and 3.75 Gbps, full rate should be selected for the RATE[1:0] bits for that channel.

If the desired serial bit rate is between 1.0 Gbps and 2.125 Gbps, half rate should be selected for the RATE[1:0] bits for that channel.

If the desired serial bit rate is between 600 Mbps and 1.0625 Gbps, quarter rate should be selected for the RATE[1:0] bits for that channel.

If the desired serial bit rate falls in the overlap between the full and half rate ranges defined above, then either setting is appropriate.

If the desired serial bit rate falls in the overlap between the half and quarter rate ranges defined above, then either setting is appropriate.

In general, there are many different settings that will yield the same serial bit rate. It should be noted that selecting the setting with the highest SERDES REFCLK and the lowest SERDES PLL Multiplier will give the best serial performance.

XAUI Mode - Legal Clocking Mode Settings						
TLK3134	Jitter	SERDES	SERDES	Serial Data Rate = f(SPEED[1:0]) (Mbps)		
REFCLK	Cleaner	REFCLK	PLL	Full (00)	Half (01)	Qrtr. (10)
Input (MHz)	Multiplier	Input (MHz)	Multiplier			
78.12500	OFF	78.12500	20	**3125.000**	1562.500	781.250
78.12500	0.25	19.53125				
78.12500	0.5	39.06250				
78.12500	1	78.12500	20	**3125.000**	1562.500	781.250
78.12500	2	156.25000	10	**3125.000**	1562.500	781.250
156.25000	OFF	156.25000	10	**3125.000**	1562.500	781.250
156.25000	0.25	39.06250				
156.25000	0.5	78.12500	20	**3125.000**	1562.500	781.250
156.25000	1	156.25000	10	**3125.000**	1562.500	781.250
156.25000	2	312.50000	5	**3125.000**	1562.500	781.250
312.50000	OFF	312.50000	5	**3125.000**	1562.500	781.250
312.50000	0.25	78.12500	20	**3125.000**	1562.500	781.250
312.50000	0.5	156.25000	10	**3125.000**	1562.500	781.250
312.50000	1	312.50000	5	**3125.000**	1562.500	781.250
312.50000	2	625.00000				

Figure A-1. Reference Clock Selection – XAUI – 10 GbE Mode

10GFC Mode - Legal Clocking Mode Settings						
TLK3134	Jitter	SERDES	SERDES	Serial Data Rate = f(SPEED[1:0]) (Mbps)		
REFCLK	Cleaner	REFCLK	PLL	Full (00)	Half (01)	Qrtr. (10)
Input (MHz)	Multiplier	Input (MHz)	Multiplier			
79.68750	OFF	79.68750	20	**3187.500**	1593.750	796.875
79.68750	0.25	19.92188				
79.68750	0.5	39.84375				
79.68750	1	79.68750	20	**3187.500**	1593.750	796.875
79.68750	2	159.37500	10	**3187.500**	1593.750	796.875
159.37500	OFF	159.37500	10	**3187.500**	1593.750	796.875
159.37500	0.25	39.84375				
159.37500	0.5	79.68750	20	**3187.500**	1593.750	796.875
159.37500	1	159.37500	10	**3187.500**	1593.750	796.875
159.37500	2	318.75000				
318.75000	OFF	318.75000	5	**3187.500**	1593.750	796.875
318.75000	0.25	79.68750	20	**3187.500**	1593.750	796.875
318.75000	0.5	159.37500	10	**3187.500**	1593.750	796.875
318.75000	1	318.75000				
318.75000	2	637.50000				

Figure A-2. Reference Clock Selection – 10 Gigabit Fibre Channel Mode

Gigabit Ethernet Mode - Legal Clocking Mode Settings						
TLK3134	Jitter	SERDES	SERDES	Serial Data Rate = f(SPEED[1:0]) (Mbps)		
REFCLK	Cleaner	REFCLK	PLL	Full (00)	Half (01)	Qrtr. (10)
Input (MHz)	Multiplier	Input (MHz)	Multiplier			
62.50000	OFF	62.50000	20	2500.000	**1250.000**	625.000
62.50000	0.25	15.62500				
62.50000	0.5	31.25000				
62.50000	1	62.50000	20	2500.000	**1250.000**	625.000
62.50000	2	125.00000	10	2500.000	**1250.000**	625.000
125.00000	OFF	125.00000	10	2500.000	**1250.000**	625.000
125.00000	0.25	31.25000				
125.00000	0.5	62.50000	20	2500.000	**1250.000**	625.000
125.00000	1	125.00000	10	2500.000	**1250.000**	625.000
125.00000	2	250.00000	5	2500.000	**1250.000**	625.000
250.00000	OFF	250.00000	5	2500.000	**1250.000**	625.000
250.00000	0.25	62.50000	20	2500.000	**1250.000**	625.000
250.00000	0.5	125.00000	10	2500.000	**1250.000**	625.000
250.00000	1	250.00000	5	2500.000	**1250.000**	625.000
250.00000	2	500.00000				

Figure A-3. Reference Clock Selection – Gigabit Ethernet Mode

Fibre Channel Mode - Legal Clocking Mode Settings						
TLK3134 REFCLK Input (MHz)	Jitter Cleaner Multiplier	SERDES REFCLK Input (MHz)	SERDES PLL Multiplier	Serial Data Rate = f(SPEED[1:0]) (Mbps) Full (00)	Half (01)	Qrtr. (10)
53.12500	OFF	53.12500	20	**2125.000**	**1062.500**	
53.12500	0.25	13.28125				
53.12500	0.5	26.56250				
53.12500	1	53.12500	20	**2125.000**	**1062.500**	
53.12500	2	106.25000	10	**2125.000**	**1062.500**	
106.25000	OFF	106.25000	10	**2125.000**	**1062.500**	
106.25000	0.25	26.56250				
106.25000	0.5	53.12500	20	**2125.000**	**1062.500**	
106.25000	1	106.25000	10	**2125.000**	**1062.500**	
106.25000	2	212.50000	5	**2125.000**	**1062.500**	
212.50000	OFF	212.50000	5	**2125.000**	**1062.500**	
212.50000	0.25	53.12500	20	**2125.000**	**1062.500**	
212.50000	0.5	106.25000	10	**2125.000**	**1062.500**	
212.50000	1	212.50000	5	**2125.000**	**1062.500**	

Figure A-4. Reference Clock Selection – 1X/2X Fibre Channel Mode

OBSAI Mode - Legal Clocking Mode Settings						
TLK3134 REFCLK Input (MHz)	Jitter Cleaner Multiplier	SERDES REFCLK Input (MHz)	SERDES PLL Multiplier	Serial Data Rate = f(SPEED[1:0]) (Mbps) Full (00)	Half (01)	Qrtr. (10)
76.80000	OFF	76.80000	20	**3072.000**	**1536.000**	**768.000**
76.80000	0.25	19.20000				
76.80000	0.5	38.40000				
76.80000	1	76.80000	20	**3072.000**	**1536.000**	**768.000**
76.80000	2	153.60000	10	**3072.000**	**1536.000**	**768.000**
153.60000	OFF	153.60000	10	**3072.000**	**1536.000**	**768.000**
153.60000	0.25	38.40000				
153.60000	0.5	76.80000	20	**3072.000**	**1536.000**	**768.000**
153.60000	1	153.60000	10	**3072.000**	**1536.000**	**768.000**
153.60000	2	307.20000	5	**3072.000**	**1536.000**	**768.000**
307.20000	OFF	307.20000	5	**3072.000**	**1536.000**	**768.000**
307.20000	0.25	76.80000	20	**3072.000**	**1536.000**	**768.000**
307.20000	0.5	153.60000	10	**3072.000**	**1536.000**	**768.000**
307.20000	1	307.20000	5	**3072.000**	**1536.000**	**768.000**
307.20000	2	614.40000				

Figure A-5. Reference Clock Selection – OBSAI Mode

CPRI Mode - Legal Clocking Mode Settings						
TLK3134	Jitter	SERDES	SERDES	Serial Data Rate = f(SPEED[1:0]) (Mbps)		
REFCLK	Cleaner	REFCLK	PLL	Full (00)	Half (01)	Qrtr. (10)
Input (MHz)	Multiplier	Input (MHz)	Multiplier			
61.44000	OFF	61.44000	20	**2457.600**	**1228.800**	**614.400**
61.44000	0.25	15.36000				
61.44000	0.5	30.72000				
61.44000	1	61.44000	20	**2457.600**	**1228.800**	**614.400**
61.44000	2	122.88000	10	**2457.600**	**1228.800**	**614.400**
122.88000	OFF	122.88000	10	**2457.600**	**1228.800**	**614.400**
122.88000	0.25	30.72000				
122.88000	0.5	61.44000	20	**2457.600**	**1228.800**	**614.400**
122.88000	1	122.88000	10	**2457.600**	**1228.800**	**614.400**
122.88000	2	245.76000	5	**2457.600**	**1228.800**	**614.400**
245.76000	OFF	245.76000	5	**2457.600**	**1228.800**	**614.400**
245.76000	0.25	61.44000	20	**2457.600**	**1228.800**	**614.400**
245.76000	0.5	122.88000	10	**2457.600**	**1228.800**	**614.400**
245.76000	1	245.76000	5	**2457.600**	**1228.800**	**614.400**

Figure A-6. Reference Clock Selection – CPRI Mode

Nine/Ten Bit SERDES Mode - Clock Range Support (RATE[1:0] == 00) (Full)							
REFCLK		Jitter	SERDES	REFCLK	SERDES	Serial Data Rate (Mbps)	
Minimum	Maximum	Cleaner	Minimum	Maximum	PLL	**Full**	
(MHz)	(MHz)	Multiplier	(MHz)	(MHz)	Multiplier	Minimum	Maximum
200.0000	375.0000	OFF	200.0000	375.0000	5	2000.00	3750.00
100.0000	187.5000	OFF	100.0000	187.5000	10	2000.00	3750.00
50.0000	93.7500	OFF	50.0000	93.7500	20	2000.00	3750.00
		0.25			5		
		0.25			10		
200.0000	375.0000	0.25	50.0000	93.7500	20	2000.00	3750.00
		0.5			5		
200.0000	375.0000	0.5	100.0000	187.5000	10	2000.00	3750.00
100.0000	187.5000	0.5	50.0000	93.7500	20	2000.00	3750.00
		1			5		
100.0000	187.5000	1	100.0000	187.5000	10	2000.00	3750.00
50.0000	93.7500	1	50.0000	93.7500	20	2000.00	3750.00
		2			5		
50.0000	93.7500	2	100.0000	187.5000	10	2000.00	3750.00
		2			20		

Figure A-7. Reference Clock Selection – 9/10 Bit SERDES Mode – Full Rate (SPEED[1:0] == 00)

Nine/Ten Bit SERDES Mode - Clock Range Support (RATE[1:0] == 01) (Half)							
REFCLK		Jitter	SERDES	REFCLK	SERDES	Serial Data Rate (Mbps)	
Minimum	Maximum	Cleaner	Minimum	Maximum	PLL	**Half**	
(MHz)	(MHz)	Multiplier	(MHz)	(MHz)	Multiplier	Minimum	Maximum
200.0000	375.0000	OFF	200.0000	375.0000	5	1000.00	1875.00
100.0000	212.5000	OFF	100.0000	212.5000	10	1000.00	2125.00
50.0000	106.2500	OFF	50.0000	106.2500	20	1000.00	2125.00
		0.25			5		
		0.25			10		
200.0000	375.0000	0.25	50.0000	93.7500	20	1000.00	1875.00
		0.5			5		
200.0000	375.0000	0.5	100.0000	187.5000	10	1000.00	1875.00
100.0000	212.5000	0.5	50.0000	106.2500	20	1000.00	2125.00
		1			5		
100.0000	200.0000	1	100.0000	200.0000	10	1000.00	2000.00
50.0000	106.2500	1	50.0000	106.2500	20	1000.00	2125.00
		2			5		
50.0000	100.0000	2	100.0000	200.0000	10	1000.00	2000.00
		2			20		

Figure A-8. Reference Clock Selection – 9/10 Bit SERDES Mode – Half Rate (SPEED[1:0] == 01)

Nine/Ten Bit SERDES Mode - Clock Range Support (RATE[1:0] == 10) (Quarter)							
REFCLK		Jitter	SERDES	REFCLK	SERDES	Serial Data Rate (Mbps)	
Minimum	Maximum	Cleaner	Minimum	Maximum	PLL	**Quarter**	
(MHz)	(MHz)	Multiplier	(MHz)	(MHz)	Multiplier	Minimum	Maximum
240.0000	375.0000	OFF	240.0000	375.0000	5	600.00	937.50
120.0000	212.5000	OFF	120.0000	212.5000	10	600.00	1062.50
60.0000	106.2500	OFF	60.0000	106.2500	20	600.00	1062.50
		0.25			5		
		0.25			10		
240.0000	375.0000	0.25	60.0000	93.7500	20	600.00	937.50
		0.5			5		
240.0000	375.0000	0.5	120.0000	187.5000	10	600.00	937.50
120.0000	212.5000	0.5	60.0000	106.2500	20	600.00	1062.50
		1			5		
120.0000	200.0000	1	120.0000	200.0000	10	600.00	1000.00
60.0000	106.2500	1	60.0000	106.2500	20	600.00	1062.50
		2			5		
60.0000	100.0000	2	120.0000	200.0000	10	600.00	1000.00
		2			20		

Figure A-9. Reference Clock Selection –9/10 Bit SERDES Mode – Quarter Rate (SPEED[1:0] == 10)

Eight Bit SERDES Mode - Clock Range Support (RATE[1:0] == 00) (Full)							
REFCLK		Jitter	SERDES	REFCLK	SERDES	Serial Data Rate (Mbps)	
Minimum	Maximum	Cleaner	Minimum	Maximum	PLL	**Full**	
(MHz)	(MHz)	Multiplier	(MHz)	(MHz)	Multiplier	Minimum	Maximum
250.0000	375.0000	OFF	250.0000	375.0000	4	2000.00	3000.00
125.0000	187.5000	OFF	125.0000	187.5000	8	2000.00	3000.00
		0.25			4		
		0.25			8		
		0.5			4		
250.0000	375.0000	0.5	125.0000	187.5000	8	2000.00	3000.00
		1			4		
125.0000	187.5000	1	125.0000	187.5000	8	2000.00	3000.00
		2			4		
62.5000	93.7500	2	125.0000	187.5000	8	2000.00	3000.00

Figure A-10. Reference Clock Selection – 8 Bit SERDES Mode – Full Rate (SPEED[1:0] == 00)

Eight Bit SERDES Mode - Clock Range Support (RATE[1:0] == 01) (Half)							
REFCLK		Jitter	SERDES	REFCLK	SERDES	Serial Data Rate (Mbps)	
Minimum	Maximum	Cleaner	Minimum	Maximum	PLL	**Half**	
(MHz)	(MHz)	Multiplier	(MHz)	(MHz)	Multiplier	Minimum	Maximum
250.0000	375.0000	OFF	250.0000	375.0000	4	1000.00	1500.00
125.0000	265.6250	OFF	125.0000	265.6250	8	1000.00	2125.00
		0.25			4		
		0.25			8		
		0.5			4		
250.0000	375.0000	0.5	125.0000	187.5000	8	1000.00	1500.00
		1			4		
125.0000	200.0000	1	125.0000	200.0000	8	1000.00	1600.00
		2			4		
62.5000	100.0000	2	125.0000	200.0000	8	1000.00	1600.00

Figure A-11. Reference Clock Selection – 8 Bit SERDES Mode – Half Rate (SPEED[1:0] == 01)

Eight Bit SERDES Mode - Clock Range Support (RATE[1:0] == 10) (Quarter)							
REFCLK		Jitter	SERDES	REFCLK	SERDES	Serial Data Rate (Mbps)	
Minimum	Maximum	Cleaner	Minimum	Maximum	PLL	**Quarter**	
(MHz)	(MHz)	Multiplier	(MHz)	(MHz)	Multiplier	Minimum	Maximum
300.0000	375.0000	OFF	300.0000	375.0000	4	600.00	750.00
150.0000	265.6250	OFF	150.0000	265.6250	8	600.00	1062.50
		0.25			4		
		0.25			8		
		0.5			4		
300.0000	375.0000	0.5	150.0000	187.5000	8	600.00	750.00
		1			4		
150.0000	200.0000	1	150.0000	200.0000	8	600.00	800.00
		2			4		
75.0000	100.0000	2	150.0000	200.0000	8	600.00	800.00

Figure A-12. Reference Clock Selection – 8 Bit SERDES Mode – Quarter Rate (SPEED[1:0] == 10)

Application Mode	REFCLK (Mhz)	Jitter Cleaner PLL Multiplier Ratio								SERDES RATE[1:0]
		REF_DIV[6:0] 4/5.37124:14:8 (Decimal)	FB_DIV[6:0] 4/5.37124:6:0 (Decimal)	2X		1X		0.5X		0.25X		
				PLL_MULT[3:0] See Note 1 Below	RXTX_DIV[6:0] 4/5.37125:6:0	PLL_MULT[3:0] See Note 1 Below	RXTX_DIV[6:0] 4/5.37125:6:0	PLL_MULT[3:0] See Note 1 Below	RXTX_DIV[6:0] 4/5.37125:6:0	PLL_MULT[3:0] See Note 1 Below	RXTX_DIV[6:0] 4/5.37125:6:0	See Note 2 Below
Gigabit Ethernet	62.5	1	48	10	24	20	48	20	48			2'b01 (Half)
	125	1	24	5	12	10	24	10	24	20	48	
	250	4	48			5	12					
CPRI (1x/2x/4x)	61.44	1	48	10	24	20	48	20	48			If 1x --> 2'b10 (1/4)
	122.88	1	24	5	12	10	24	10	24			If 2x --> 2'b01 (Half)
	245.76	4	48			5	12					If 4x --> 2'b00 (Full)
OBSAI (1x/2x/4x)	76.8	1	40	10	20	20	40	20	40			If 1x --> 2'b10 (1/4)
	153.6	1	20	5	10	10	20	10	20			If 2x --> 2'b01 (Half)
	307.2	4	40			5	10					If 4x --> 2'b00 (Full)
XAUI (10 GbE)	78.125	1	40	10	20	20	40	20	40			2'b00 (Full)
	156.25	1	20	5	10	10	20	10	20			
	312.5	4	40			5	10					
10GFC	79.6875	1	38	10	19	20	38	20	38			2'b00 (Full)
	159.375	1	19			10	19	10	19			
	318.75	4	38									
FC (1x/2x)	53.125	1	56	10	28	20	56	20	56			If 1x --> 2'b01 (Half)
	106.25	1	28	5	14	10	28	10	28			If 2x --> 2'b00 (Full)
	212.5	4	56			5	14					

Note 1: PLL_MULT[3:0] bits are found in bits 11:8 and 3:0 in register SERDES_PLL_CONFIG a: address 4/5.36864.

Note 2: RATE[1:0] bits are found in the SERDES_RATE_CONFIG_TX_RX register at address 4/5.36865.

Figure A-13. Standard Based Jitter Cleaner/SERDES Provisioning

REFCLK (Mhz)		REF_DIV[6:0] 4/5.37124:14:8 (Decimal)	FB_DIV[6:0] 4/5.37124:6:0 (Decimal)	PLL_MULT[3:0] See Note 1 Below	RXTX_DIV[6:0] 4/5.37125:6:0	SERDES RATE [1:0] (See Note 2 Below) 2'b00 (Full)		2'b01 (Half)		2'b10 (Quarter)	
Min	Max					Min	Max	Min	Max	Min	Max
50.0000	52.0833	1	60	10	30	2000.000	2083.333	1000.000	1041.667		
50.4310	53.8793	1	58	10	29	2017.241	2155.172	1008.621	1077.586		
52.2321	55.8036	1	56	10	28	2089.286	2232.143	1044.643	1116.071		
54.1667	57.8704	1	54	10	27	2166.667	2314.815	1083.333	1157.407		
56.2500	60.0962	1	52	10	26	2250.000	2403.846	1125.000	1201.923		
58.5000	62.5000	1	50	10	25	2340.000	2500.000	1170.000	1250.000	600.000	625.000
60.9375	65.1042	1	48	10	24	2437.500	2604.167	1218.750	1302.083	609.375	651.042
63.5870	67.9348	1	46	10	23	2543.478	2717.391	1271.739	1358.696	635.870	679.348
66.4773	71.0227	1	44	10	22	2659.091	2840.909	1329.545	1420.455	664.773	710.227
69.6429	74.4048	1	42	10	21	2785.714	2976.190	1392.857	1488.095	696.429	744.048
73.1250	78.1250	1	40	10	20	2925.000	3125.000	1462.500	1562.500	731.250	781.250
76.9737	82.2368	1	38	10	19	3078.947	3289.474	1539.474	1644.737	769.737	822.368
81.2500	86.8056	1	36	10	18	3250.000	3472.222	1625.000	1736.111	812.500	868.056
86.0294	91.9118	1	34	10	17	3441.176	3676.471	1720.588	1838.235	860.294	919.118
91.4063	97.6563	1	32	10	16	3656.250	3750.000	1828.125	1953.125	914.063	976.563
97.5000	100.0000	1	30	10	15			1950.000	2000.000	975.000	1000.000

Note 1: PLL_MULT[3:0] bits are found in bits 11:8 and 3:0 in register SERDES_PLL_CONFIG at address 4/5.36864.
Note 2: RATE[1:0] bits are found in the SERDES_RATE_CONFIG_TX_RX register at address 4/5.36865.

Note that REFCLK is limited to 93.75 Mhz when in full rate mode to achieve 3750 Mbps serial data rate.

Figure A-14. 9/10 BIT SERDES Mode – Jitter Cleaner/SERDES (2x) Provisioning

REFCLK (Mhz)		REF_DIV[6:0] 4/5.37124:14:8	FB_DIV[6:0] 4/5.37124:6:0	PLL_MULT[3:0]	RXTX_DIV[6:0]	SERDES RATE [1:0] (See Note 2 Below)					
						RATE[1:0] =2'b00 Full		RATE[1:0] =2'b01 Half		RATE[1:0] =2'b10 Qrtr.	
Min	Max	(Decimal)	(Decimal)	See Note 1 Below	4/5.37125:6:0	Min	Max	Min	Max	Min	Max
50.0000	53.8793	1	58	20	58	2000.000	2155.172	1000.000	1077.586		
51.3158	54.8246	1	57	20	57	2052.632	2192.982	1026.316	1096.491		
52.2321	55.8036	1	56	20	56	2089.286	2232.143	1044.643	1116.071		
53.1818	56.8182	1	55	20	55	2127.273	2272.727	1063.636	1136.364		
54.1667	57.8704	1	54	20	54	2166.667	2314.815	1083.333	1157.407		
55.1887	58.9623	1	53	20	53	2207.547	2358.491	1103.774	1179.245		
56.2500	60.0962	1	52	20	52	2250.000	2403.846	1125.000	1201.923		
57.3529	61.2745	1	51	20	51	2294.118	2450.980	1147.059	1225.490	600.000	612.745
58.5000	62.5000	1	50	20	50	2340.000	2500.000	1170.000	1250.000	600.000	625.000
59.6939	63.7755	1	49	20	49	2387.755	2551.020	1193.878	1275.510	600.000	637.755
60.9375	65.1042	1	48	20	48	2437.500	2604.167	1218.750	1302.083	609.375	651.042
62.2340	66.4894	1	47	20	47	2489.362	2659.574	1244.681	1329.787	622.340	664.894
63.5870	67.9348	1	46	20	46	2543.478	2717.391	1271.739	1358.696	635.870	679.348
65.0000	69.4444	1	45	20	45	2600.000	2777.778	1300.000	1388.889	650.000	694.444
66.4773	71.0227	1	44	20	44	2659.091	2840.909	1329.545	1420.455	664.773	710.227
68.0233	72.6744	1	43	20	43	2720.930	2906.977	1360.465	1453.488	680.233	726.744
69.6429	74.4048	1	42	20	42	2785.714	2976.190	1392.857	1488.095	696.429	744.048
71.3415	76.2195	1	41	20	41	2853.659	3048.780	1426.829	1524.390	713.415	762.195
73.1250	78.1250	1	40	20	40	2925.000	3125.000	1462.500	1562.500	731.250	781.250
75.0000	80.1282	1	39	20	39	3000.000	3205.128	1500.000	1602.564	750.000	801.282
76.9737	82.2368	1	38	20	38	3078.947	3289.474	1539.474	1644.737	769.737	822.368
79.0541	84.4595	1	37	20	37	3162.162	3378.378	1581.081	1689.189	790.541	844.595
81.2500	86.8056	1	36	20	36	3250.000	3472.222	1625.000	1736.111	812.500	868.056
83.5714	89.2857	1	35	20	35	3342.857	3571.429	1671.429	1785.714	835.714	892.857
86.0294	91.9118	1	34	20	34	3441.176	3676.471	1720.588	1838.235	860.294	919.118
88.6364	94.6970	1	33	20	33	3545.455	3750.000	1772.727	1893.939	886.364	946.970
91.4063	97.6563	1	32	20	32	3656.250	3750.000	1828.125	1953.125	914.063	976.563
94.3548	100.8065	1	31	20	31			1887.097	2016.129	943.548	1008.065
97.5000	104.1667	1	30	20	30			1950.000	2083.333	975.000	1041.667
100.8621	106.2500	1	29	20	29			2017.241	2125.000	1008.621	1062.500
104.4643	106.2500	1	28	20	28			2089.286	2125.000	1044.643	1062.500
100.0000	104.1667	1	30	10	30	2000.000	2083.333	1000.000	1041.667		
100.0000	107.7586	1	29	10	29	2000.000	2155.172	1000.000	1077.586		
104.4643	111.6071	1	28	10	28	2089.286	2232.143	1044.643	1116.071		
108.3333	115.7407	1	27	10	27	2166.667	2314.815	1083.333	1157.407		
112.5000	120.1923	1	26	10	26	2250.000	2403.846	1125.000	1201.923		
117.0000	125.0000	1	25	10	25	2340.000	2500.000	1170.000	1250.000	600.000	625.000
121.8750	130.2083	1	24	10	24	2437.500	2604.167	1218.750	1302.083	600.000	651.042
127.1739	135.8696	1	23	10	23	2543.478	2717.391	1271.739	1358.696	635.870	679.348
132.9545	142.0455	1	22	10	22	2659.091	2840.909	1329.545	1420.455	664.773	710.227
139.2857	148.8095	1	21	10	21	2785.714	2976.190	1392.857	1488.095	696.429	744.048
146.2500	156.2500	1	20	10	20	2925.000	3125.000	1462.500	1562.500	731.250	781.250
153.9474	164.4737	1	19	10	19	3078.947	3289.474	1539.474	1644.737	769.737	822.368
162.5000	173.6111	1	18	10	18	3250.000	3472.222	1625.000	1736.111	812.500	868.056
172.0588	183.8235	1	17	10	17	3441.176	3676.471	1720.588	1838.235	860.294	919.118
182.8125	195.3125	1	16	10	16	3656.250	3750.000	1828.125	1953.125	914.063	976.563
195.0000	200.0000	1	15	10	15			1950.000	2000.000	975.000	1000.000
Note 1: PLL_MULT[3:0] bits are found in bits 11:8 and 3:0 in register SERDES_PLL_CONFIG at address 4/5.36864.											
Note 2: RATE[1:0] bits are found in the SERDES_RATE_CONFIG_TX_RX register at address 4/5.36865.											

Note that REFCLK is limited to 187.5 Mhz when in full rate mode to achieve 3750 Mbps serial data rate.

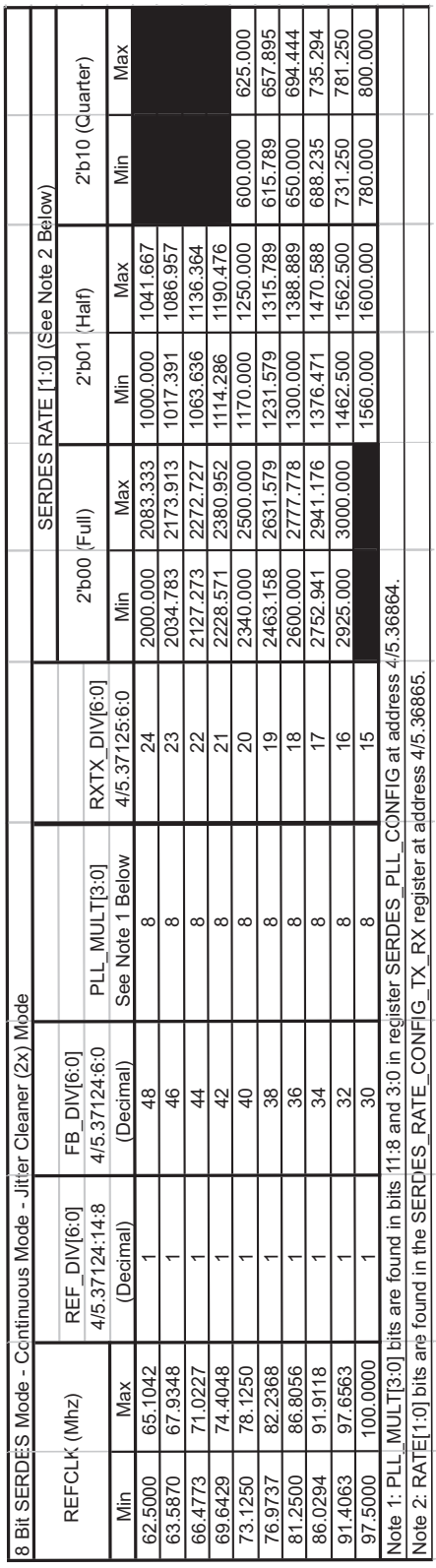
Figure A-15. 9/10 BIT SERDES Mode – Jitter Cleaner/SERDES (1x) Provisioning

REFCLK (Mhz)		REF_DIV[6:0]	FB_DIV[6:0]			SERDES RATE[1:0] (See Note 2 Below)					
		4/5.37124:14:8	4/5.37124:6:0	PLL_MULT[3:0]	RXTX_DIV[6:0]	RATE[1:0] =2'b00 Full		RATE[1:0] =2'b01 Half		RATE[1:0] =2'b10 Qrtr.	
Min	Max	(Decimal)	(Decimal)	See Note 1 Below	4/5.37125:6:0	Min	Max	Min	Max	Min	Max
100.0000	105.9322	4	118	20	59	2000.000	2118.644	1000.000	1059.322		
100.8621	107.7586	4	116	20	58	2017.241	2155.172	1008.621	1077.586		
102.6316	109.6491	4	114	20	57	2052.632	2192.982	1026.316	1096.491		
104.4643	111.6071	4	112	20	56	2089.286	2232.143	1044.643	1116.071		
106.3636	113.6364	4	110	20	55	2127.273	2272.727	1063.636	1136.364		
108.3333	115.7407	4	108	20	54	2166.667	2314.815	1083.333	1157.407		
110.3774	117.9245	4	106	20	53	2207.547	2358.491	1103.774	1179.245		
112.5000	120.1923	4	104	20	52	2250.000	2403.846	1125.000	1201.923		
114.7059	122.5490	4	102	20	51	2294.118	2450.980	1147.059	1225.490	600.000	612.745
117.0000	125.0000	4	100	20	50	2340.000	2500.000	1170.000	1250.000	600.000	625.000
119.3878	127.5510	4	98	20	49	2387.755	2551.020	1193.878	1275.510	600.000	637.755
121.8750	130.2083	4	96	20	48	2437.500	2604.167	1218.750	1302.083	609.375	651.042
124.4681	132.9787	4	94	20	47	2489.362	2659.574	1244.681	1329.787	622.340	664.894
127.1739	135.8696	4	92	20	46	2543.478	2717.391	1271.739	1358.696	635.870	679.348
130.0000	138.8889	4	90	20	45	2600.000	2777.778	1300.000	1388.889	650.000	694.444
132.9545	142.0455	4	88	20	44	2659.091	2840.909	1329.545	1420.455	664.773	710.227
136.0465	145.3488	4	86	20	43	2720.930	2906.977	1360.465	1453.488	680.233	726.744
139.2857	148.8095	4	84	20	42	2785.714	2976.190	1392.857	1488.095	696.429	744.048
142.6829	152.4390	4	82	20	41	2853.659	3048.780	1426.829	1524.390	713.415	762.195
146.2500	156.2500	4	80	20	40	2925.000	3125.000	1462.500	1562.500	731.250	781.250
150.0000	160.2564	4	78	20	39	3000.000	3205.128	1500.000	1602.564	750.000	801.282
153.9474	164.4737	4	76	20	38	3078.947	3289.474	1539.474	1644.737	769.737	822.368
158.1081	168.9189	4	74	20	37	3162.162	3378.378	1581.081	1689.189	790.541	844.595
162.5000	173.6111	4	72	20	36	3250.000	3472.222	1625.000	1736.111	812.500	868.056
167.1429	178.5714	4	70	20	35	3342.857	3571.429	1671.429	1785.714	835.714	892.857
172.0588	183.8235	4	68	20	34	3441.176	3676.471	1720.588	1838.235	860.294	919.118
177.2727	189.3939	4	66	20	33	3545.455	3750.000	1772.727	1893.939	886.364	946.970
182.8125	195.3125	4	64	20	32	3656.250	3750.000	1828.125	1953.125	914.063	976.563
188.7097	201.6129	4	62	20	31			1887.097	2016.129	943.548	1008.065
195.0000	208.3333	4	60	20	30			1950.000	2083.333	975.000	1041.667
201.7241	212.5000	4	58	20	29			2017.241	2125.000	1008.621	1062.500
208.9286	212.5000	4	56	20	28			2089.286	2125.000	1044.643	1062.500
200.0000	208.3333	4	60	10	30	2000.000	2083.333	1000.000	1041.667		
201.7241	215.5172	4	58	10	29	2017.241	2155.172	1008.621	1077.586		
208.9286	223.2143	4	56	10	28	2089.286	2232.143	1044.643	1116.071		
216.6667	231.4815	4	54	10	27	2166.667	2314.815	1083.333	1157.407		
225.0000	240.3846	4	52	10	26	2250.000	2403.846	1125.000	1201.923		
234.0000	250.0000	4	50	10	25	2340.000	2500.000	1170.000	1250.000	600.000	625.000
243.7500	260.4167	4	48	10	24	2437.500	2604.167	1218.750	1302.083	609.375	651.042
254.3478	271.7391	4	46	10	23	2543.478	2717.391	1271.739	1358.696	635.870	679.348
265.9091	284.0909	4	44	10	22	2659.091	2840.909	1329.545	1420.455	664.773	710.227
278.5714	297.6190	4	42	10	21	2785.714	2976.190	1392.857	1488.095	696.429	744.048
292.5000	312.5000	4	40	10	20	2925.000	3125.000	1462.500	1562.500	731.250	781.250
307.8947	328.9474	4	38	10	19	3078.947	3289.474	1539.474	1644.737	769.737	822.368
325.0000	347.2222	4	36	10	18	3250.000	3472.222	1625.000	1736.111	812.500	868.056
344.1176	367.6471	4	34	10	17	3441.176	3676.471	1720.588	1838.235	860.294	919.118
365.6250	375.0000	4	32	10	16	3656.250	3750.000	1828.125	1875.000	914.063	937.500
Note 1: PLL_MULT[3:0] bits are found in bits 11:8 and 3:0 in register SERDES_PLL_CONFIG at address 4/5.36864.											
Note 2: RATE[1:0] bits are found in the SERDES_RATE_CONFIG_TX_RX register at address 4/5.36865.											

Figure A-16. 9/10 BIT SERDES Mode – Jitter Cleaner/SERDES (0.5x) Provisioning

REFCLK (Mhz)		REF_DIV[6:0] 4/5.37124:14:8	FB_DIV[6:0] 4/5.37124:6:0	PLL_MULT[3:0]	RXTX_DIV[6:0]	SERDES RATE[1:0] (See Note 2 Below)					
						RATE[1:0] =2'b00 Full		RATE[1:0] =2'b01 Half		RATE[1:0] =2'b10 Qrtr	
Min	Max	(Decimal)	(Decimal)	See Note 1 Below	4/5.37125:6:0	Min	Max	Min	Max	Min	Max
200.0000	211.8644	4	59	20	59	2000.000	2118.644	1000.000	1059.322		
201.7241	215.5172	4	58	20	58	2017.241	2155.172	1008.621	1077.586		
205.2632	219.2982	4	57	20	57	2052.632	2192.982	1026.316	1096.491		
208.9286	223.2143	4	56	20	56	2089.286	2232.143	1044.643	1116.071		
212.7273	227.2727	4	55	20	55	2127.273	2272.727	1063.636	1136.364		
216.6667	231.4815	4	54	20	54	2166.667	2314.815	1083.333	1157.407		
220.7547	235.8491	4	53	20	53	2207.547	2358.491	1103.774	1179.245		
225.0000	240.3846	4	52	20	52	2250.000	2403.846	1125.000	1201.923		
229.4118	245.0980	4	51	20	51	2294.118	2450.980	1147.059	1225.490		
234.0000	250.0000	4	50	20	50	2340.000	2500.000	1170.000	1250.000		
238.7755	255.1020	4	49	20	49	2387.755	2551.020	1193.878	1275.510	600.000	637.755
243.7500	260.4167	4	48	20	48	2437.500	2604.167	1218.750	1302.083	609.375	651.042
248.9362	265.9574	4	47	20	47	2489.362	2659.574	1244.681	1329.787	622.340	664.894
254.3478	271.7391	4	46	20	46	2543.478	2717.391	1271.739	1358.696	635.870	679.348
260.0000	277.7778	4	45	20	45	2600.000	2777.778	1300.000	1388.889	650.000	694.444
265.9091	284.0909	4	44	20	44	2659.091	2840.909	1329.545	1420.455	664.773	710.227
272.0930	290.6977	4	43	20	43	2720.930	2906.977	1360.465	1453.488	680.233	726.744
278.5714	297.6190	4	42	20	42	2785.714	2976.190	1392.857	1488.095	696.429	744.048
285.3659	304.8780	4	41	20	41	2853.659	3048.780	1426.829	1524.390	713.415	762.195
292.5000	312.5000	4	40	20	40	2925.000	3125.000	1462.500	1562.500	731.250	781.250
300.0000	320.5128	4	39	20	39	3000.000	3205.128	1500.000	1602.564	750.000	801.282
307.8947	328.9474	4	38	20	38	3078.947	3289.474	1539.474	1644.737	769.737	822.368
316.2162	337.8378	4	37	20	37	3162.162	3378.378	1581.081	1689.189	790.541	844.595
325.0000	347.2222	4	36	20	36	3250.000	3472.222	1625.000	1736.111	812.500	868.056
334.2857	357.1429	4	35	20	35	3342.857	3571.429	1671.429	1785.714	835.714	892.857
344.1176	367.6471	4	34	20	34	3441.176	3676.471	1720.588	1838.235	860.294	919.118
354.5455	375.0000	4	33	20	33	3545.455	3750.000	1772.727	1875.000	886.364	937.500
Note 1: PLL_MULT[3:0] bits are found in bits 11:8 and 3:0 in register SERDES_PLL_CONFIG at address 4/5.36864.											
Note 2: RATE[1:0] bits are found in the SERDES_RATE_CONFIG_TX_RX register at address 4/5.36865.											

Figure A-17. 9/10 BIT SERDES Mode – Jitter Cleaner/SERDES (0.25x) Provisioning



8 Bit SERDES Mode - Continuous Mode - Jitter Cleaner (2x) Mode						SERDES RATE [1:0] (See Note 2 Below)					
REFCLK (Mhz)		REF_DIV[6:0] 4/5.37124:14:8	FB_DIV[6:0] 4/5.37124:6:0	PLL_MULT[3:0]	RXTX_DIV[6:0]	2'b00 (Full)		2'b01 (Half)		2'b10 (Quarter)	
Min	Max	(Decimal)	(Decimal)	See Note 1 Below	4/5.37125:6:0	Min	Max	Min	Max	Min	Max
62.5000	65.1042	1	48	8	24	2000.000	2083.333	1000.000	1041.667		
63.5870	67.9348	1	46	8	23	2034.783	2173.913	1017.391	1086.957		
66.4773	71.0227	1	44	8	22	2127.273	2272.727	1063.636	1136.364		
69.6429	74.4048	1	42	8	21	2228.571	2380.952	1114.286	1190.476		
73.1250	78.1250	1	40	8	20	2340.000	2500.000	1170.000	1250.000	600.000	625.000
76.9737	82.2368	1	38	8	19	2463.158	2631.579	1231.579	1315.789	615.789	657.895
81.2500	86.8056	1	36	8	18	2600.000	2777.778	1300.000	1388.889	650.000	694.444
86.0294	91.9118	1	34	8	17	2752.941	2941.176	1376.471	1470.588	688.235	735.294
91.4063	97.6563	1	32	8	16	2925.000	3000.000	1462.500	1562.500	731.250	781.250
97.5000	100.0000	1	30	8	15			1560.000	1600.000	780.000	800.000
Note 1: PLL_MULT[3:0] bits are found in bits 11:8 and 3:0 in register SERDES_PLL_CONFIG at address 4/5.36864.											
Note 2: RATE[1:0] bits are found in the SERDES_RATE_CONFIG_TX_RX register at address 4/5.36865.											

A. Note that REFCLK is limited to 93.75 Mhz when in Full rate mode to achieve 3000 Mbps serial data rate.

Figure A-18. 8 BIT SERDES Mode – Jitter Cleaner/SERDES (2x) Provisioning

8 Bit SERDES Mode - Continuous Mode - Jitter Cleaner (1x) Mode						SERDES RATE [1:0] (See Note 2 Below)					
REFCLK (Mhz)		REF_DIV[6:0] 4/5.37124:14:8 (Decimal)	FB_DIV[6:0] 4/5.37124:6:0 (Decimal)	PLL_MULT[3:0] See Note 1 Below	RXTX_DIV[6:0] 4/5.37125:6:0	2'b00 (Full)		2'b01 (Half)		2'b10 (Quarter)	
Min	Max					Min	Max	Min	Max	Min	Max
125.0000	130.2083	1	24	8	24	2000.000	2083.333	1000.000	1041.667		
127.1739	135.8696	1	23	8	23	2034.783	2173.913	1017.391	1086.957		
132.9545	142.0455	1	22	8	22	2127.273	2272.727	1063.636	1136.364		
139.2857	148.8095	1	21	8	21	2228.571	2380.952	1114.286	1190.476		
146.2500	156.2500	1	20	8	20	2340.000	2500.000	1170.000	1250.000	600.000	625.000
153.9474	164.4737	1	19	8	19	2463.158	2631.579	1231.579	1315.789	615.789	657.895
162.5000	173.6111	1	18	8	18	2600.000	2777.778	1300.000	1388.889	650.000	694.444
172.0588	183.8235	1	17	8	17	2752.941	2941.176	1376.471	1470.588	688.235	735.294
182.8125	195.3125	1	16	8	16	2925.000	3000.000	1462.500	1562.500	731.250	781.250
195.0000	200.0000	1	15	8	15			1560.000	1600.000	780.000	800.000
Note 1: PLL_MULT[3:0] bits are found in bits 11:8 and 3:0 in register SERDES_PLL_CONFIG at address 4/5.36864.											
Note 2: RATE[1:0] bits are found in the SERDES_RATE_CONFIG_TX_RX register at address 4/5.36865.											

Note that REFCLK is limited to 187.5 Mhz when in Full rate mode to achieve 3000 Mbps serial data rate.

Figure A-19. 8 BIT SERDES Mode – Jitter Cleaner/SERDES (1x) Provisioning

REFCLK (Mhz)		REF_DIV[6:0] 4/5.37124:14:8	FB_DIV[6:0] 4/5.37124:6:0	PLL_MULT[3:0]	RXTX_DIV[6:0]	SERDES RATE [1:0] (See Note 2 Below)					
						2'b00 (Full)		2'b01 (Half)		2'b10 (Quarter)	
Min	Max	(Decimal)	(Decimal)	See Note 1 Below	4/5.37125:6:0	Min	Max	Min	Max	Min	Max
250.0000	260.4167	4	48	8	24	2000.000	2083.333	1000.000	1041.667		
254.3478	271.7391	4	46	8	23	2034.783	2173.913	1017.391	1086.957		
265.9091	284.0909	4	44	8	22	2127.273	2272.727	1063.636	1136.364		
278.5714	297.6190	4	42	8	21	2228.571	2380.952	1114.286	1190.476		
292.5000	312.5000	4	40	8	20	2340.000	2500.000	1170.000	1250.000	600.000	625.000
307.8947	328.9474	4	38	8	19	2463.158	2631.579	1231.579	1315.789	615.789	657.895
325.0000	347.2222	4	36	8	18	2600.000	2777.778	1300.000	1388.889	650.000	694.444
344.1176	367.6471	4	34	8	17	2752.941	2941.176	1376.471	1470.588	688.235	735.294
365.6250	375.0000	4	32	8	16	2925.000	3000.000	1462.500	1500.000	731.250	750.000

Note 1: PLL_MULT[3:0] bits are found in bits 11:8 and 3:0 in register SERDES_PLL_CONFIG at address 4/5.36864.

Note 2: RATE[1:0] bits are found in the SERDES_RATE_CONFIG_TX_RX register at address 4/5.36865.

Figure A-20. 8 BIT SERDES Mode – Jitter Cleaner/SERDES (0.5x) Provisioning

A.1 Recovered Byte Clock Jitter Cleaner Mode:

If it is desired to dedicate the Jitter Cleaner PLL to clean the RX SERDES recovered byte clock, then the following procedure must be followed:

1. Program REF_SEL[1:0] to 2'b10.
2. Program RXB_SEL[1:0] to 2'b00.
3. Program RX_SEL to 2'b10 -or- 2'b11.
4. Program TX_SEL as desired.
5. Program 4/5.32810.15:14 -or- 16.10:9 as desired on a per channel basis.
6. Consult the rows in the appropriate Appendix A table to find the appropriate REFCLK and SERDES mode settings. Note that only rows indicating that the Jitter Cleaner PLL is OFF may be used. Provision the SERDES settings appropriately.
7. Divide the selected SERDES serial rate by 8 if in EBI/REBI modes, or 10 otherwise, and use that frequency as the input to Figure A-21 Recovered Byte Clock Jitter Cleaner Mode, to determine the appropriate Jitter Cleaner PLL settings. Note that only a 1:1 frequency ratio is supported between the SERDES output byte clock and the parallel interface output recovered byte clock. Depending upon the selection of TX_SEL, it may also be necessary to provision RXTX_DIV with the same value as RXB_DIV.

Recovered Byte Clock Cleaning Mode - Jitter Cleaner (1x) Mode				
Recovered Byte Clock (Mhz)		REF_DIV[6:0] 4/5.37124:14:8	FB_DIV[6:0] 4/5.37124:6:0	RXB_DIV[6:0] 4/5.37125:14:8
Min	Max	(Decimal)	(Decimal)	
50.0000	53.8793	1	58	58
51.3158	54.8246	1	57	57
52.2321	55.8036	1	56	56
53.1818	56.8182	1	55	55
54.1667	57.8704	1	54	54
55.1887	58.9623	1	53	53
56.2500	60.0962	1	52	52
57.3529	61.2745	1	51	51
58.5000	62.5000	1	50	50
59.6939	63.7755	1	49	49
60.9375	65.1042	1	48	48
62.2340	66.4894	1	47	47
63.5870	67.9348	1	46	46
65.0000	69.4444	1	45	45
66.4773	71.0227	1	44	44
68.0233	72.6744	1	43	43
69.6429	74.4048	1	42	42
71.3415	76.2195	1	41	41
73.1250	78.1250	1	40	40
75.0000	80.1282	1	39	39
76.9737	82.2368	1	38	38
79.0541	84.4595	1	37	37
81.2500	86.8056	1	36	36
83.5714	89.2857	1	35	35
86.0294	91.9118	1	34	34
88.6364	94.6970	1	33	33
91.4063	97.6563	1	32	32
94.3548	100.8065	1	31	31
97.5000	104.1667	1	30	30
100.8621	107.7586	1	29	29
104.4643	111.6071	1	28	28
108.3333	115.7407	1	27	27
112.5000	120.1923	1	26	26
117.0000	125.0000	1	25	25
121.8750	130.2083	1	24	24
127.1739	135.8696	1	23	23
132.9545	142.0455	1	22	22
139.2857	148.8095	1	21	21
146.2500	156.2500	1	20	20
153.9474	164.4737	1	19	19
162.5000	173.6111	1	18	18
172.0588	183.8235	1	17	17
182.8125	195.3125	1	16	16
195.0000	208.3333	1	15	15
208.9286	223.2143	1	14	14
225.0000	240.3846	1	13	13
243.7500	260.4167	1	12	12
265.9091	284.0909	1	11	11
292.5000	312.5000	1	10	10
325.0000	347.2222	1	9	9
365.6250	375.0000	1	8	8

Figure A-21. Recovered Byte Clock Jitter Cleaner Mode

B APPENDIX B – Jitter Cleaner PLL External Loop Filter

The following external loop filter is required anytime the Jitter Cleaner PLL is enabled.

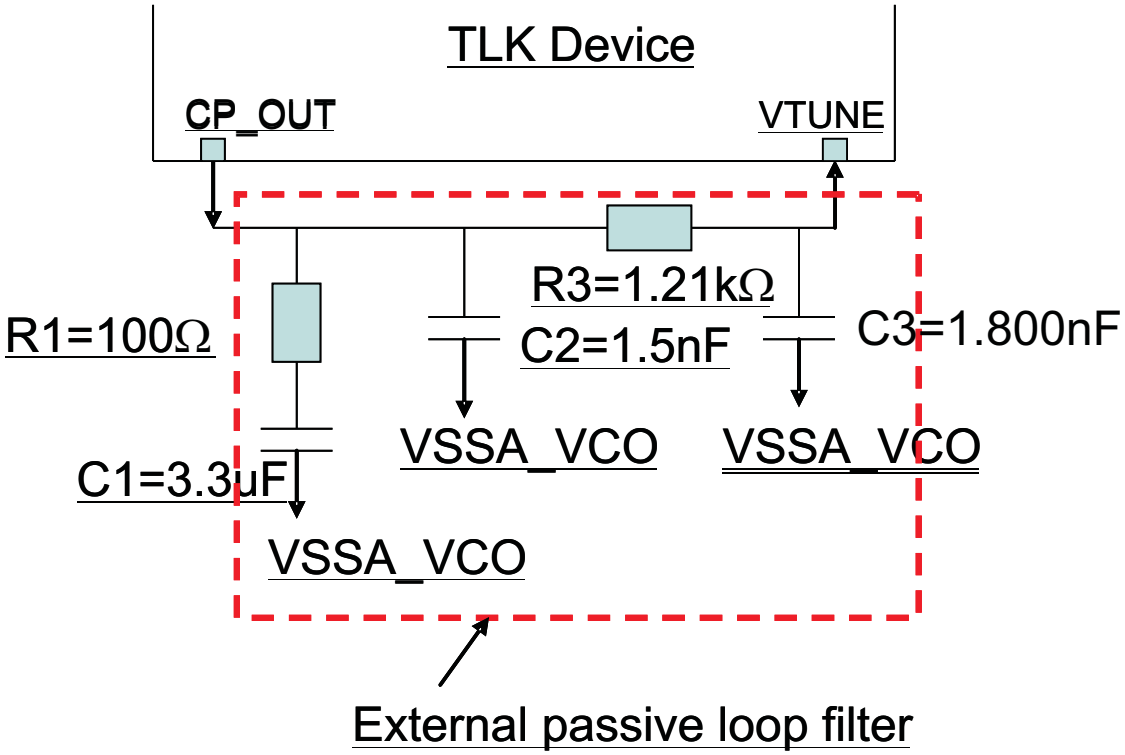


Figure B-1. Jitter Cleaner External Loop Filter

C APPENDIX C – Device Test Mode

This device can be placed into one of the three modes: functional mode including JTAG testing mode, scan testing mode, and Jadis/eFuse testing mode. The scan testing mode and Jadis/eFuse testing modes are for TI use only, and may be ignored by external users of this device.

Table C-1. Device Mode Configuration

FUNCTIONAL DEVICE PIN NAME	FUNCTIONAL MODE/JTAG TESTING	SCAN MODE	Jadis/eFuse MODE
TESTEN	0 or 1	0	1
GPI1	0	1	1

Table C-2. Device Test Mode Pin Configuration

FUNCTIONAL DEVICE PIN NAME	FUNCTIONAL MODE SIGNAL DIRECTION	TEST MODE SIGNAL DIRECTION	FUNCTIONAL MODE/JTAG TESTING	SCAN MODE	Jadis/eFuse MODE
SPEED1	I	I	SPEED1	Scan In 5	STCI_D
SPEED0	I	I	SPEED0	Scan In 4	EFUSE_TMS
PLOOP	I	I	PLOOP	Scan In 3	EFUSE_TDI
SLOOP	I	I	SLOOP	Scan In 2	STCICFG1
PRBS_EN	I	I	PRBS_EN	Scan In 1	EFUSE_INITZ
CODE	I	I	CODE	Scan Enable	TESTCLK_T
TDI	I	I	TDI	Adaptive Scan Enable (Test Mode)	JADIS_EFUSE_SEL
PRTAD4	I	I	PRTAD4	Scan HS Enable (Transition Fault)	TESTCLK_R
PRTAD3	I	I	PRTAD3	Scan Clock	STCICLK
PRTAD2	I	I: Jadis/eFuse O: Scan	PRTAD2	Scan Out 5	STCICFG0
PRTAD1	I	I	PRTAD1	Scan Clock Select (0: from device pin, 1: from Jadis), also EFUSE_SYS_CLK	EFUSE_SYS_CLK
PRTAD0	I	I	PRTAD0	HSTL Force Down	EFUSE_TCK
GPO0	O	O	TEST_DOUT0	Scan Out 4	Tied LOW
GPO1	O	O	TEST_DOUT1	Scan Out 3	Tied LOW
GPO2	O	O	TEST_DOUT2	Scan Out 2	STCI_Q
GPO3	O	O	TEST_DOUT3	Scan Out 1	EFUSE_TDO
GPO4	O	O	TEST_DOUT4 or JC PLL Digital Test Out	Burnin_Output	Burnin_Output

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLK3134ZEL	ACTIVE	BGA	ZEL	289	84	Green (RoHS & no Sb/Br)	SNAGCU	Level-4-260C-72 HR	-40 to 85	TLK3134	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

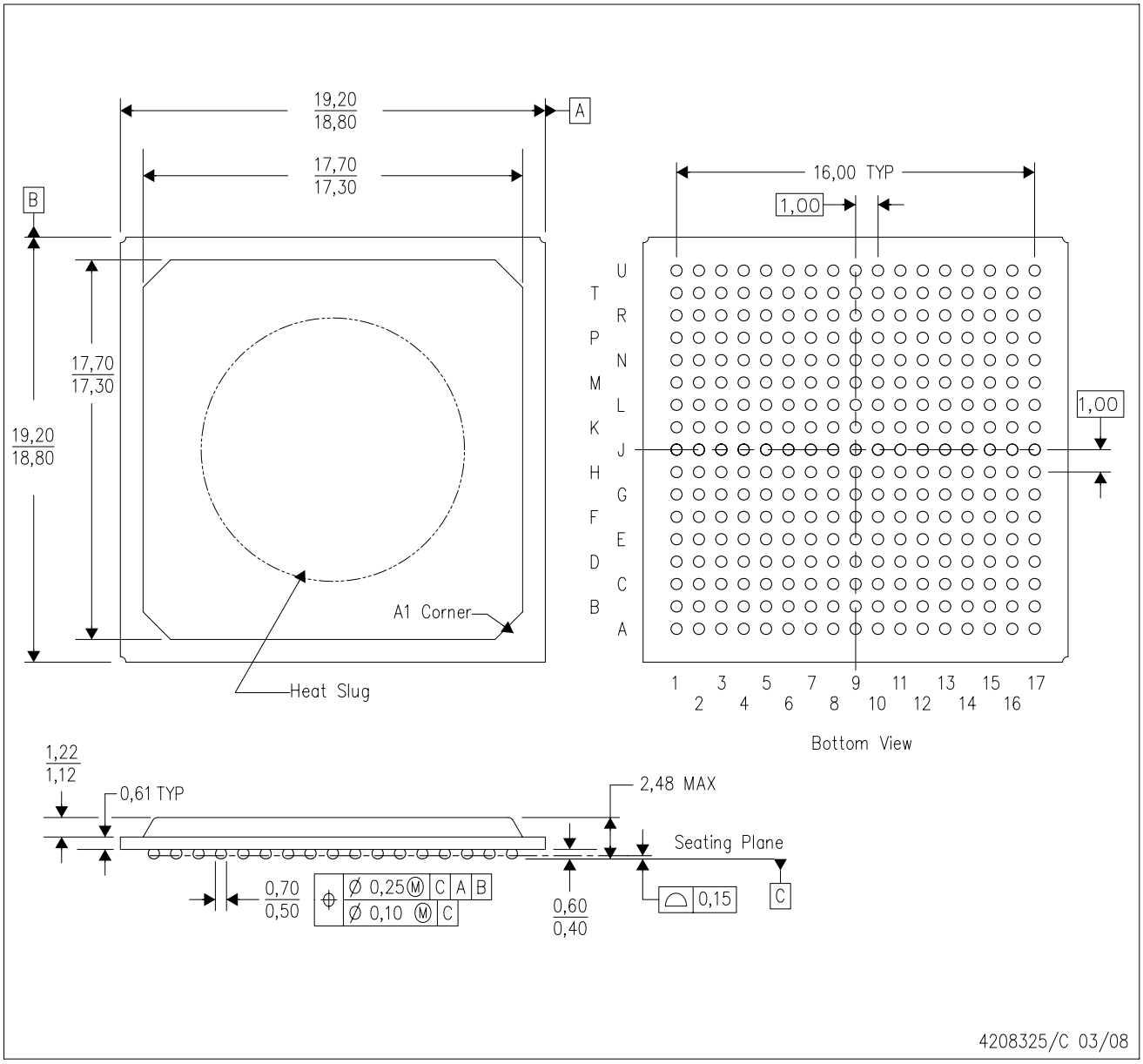
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

ZEL (S–PBGA–N289) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This is a lead–free solder ball design
D. Thermally enhanced molded plastic package with heat slug (HSL).

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