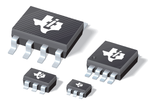


40-ns, microPOWER, Push-Pull Output Comparators

Check for Samples: TLV3201, TLV3202

FEATURES

- **Low Propagation Delay: 40 ns**
- **Low Quiescent Current: 40 μA per Channel**
- **Input Common-Mode Range Extends 200 mV Beyond Either Rail**
- **Low Input Offset Voltage: 1 mV**
- **Push-Pull Outputs**
- **Supply Range: +2.7 V to +5.5 V**
- **Industrial Temperature Range: –40°C to +125°C**
- **Small Packages: SC70-5, SOT23-5, SOIC-8, MSOP-8**

APPLICATIONS

- **Inspection Equipment**
- **Test and Measurement**
- **High-Speed Sampling Systems**
- **Telecom**
- **Portable Communications**

DESCRIPTION

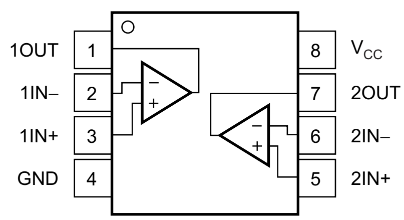
The TLV3201 and TLV3202 are single- and dual-channel comparators that offer the ultimate combination of high-speed (40 ns) and low-power consumption (40 μA), all in extremely small packages with features such as rail-to-rail inputs, low offset voltage (1 mV), and large output drive current. The devices are also very easy to implement in a wide variety of applications where response time is critical.

The TLV320x family is available in single (TLV3201) and dual (TLV3202) channel versions, both with push-pull outputs. The TLV3201 is available in SOT23-5 and SC70-5 packages. The TLV3202 is available in SOIC-8 and MSOP-8 packages. All devices are specified for operation across the expanded industrial temperature range of –40°C to +125°C.

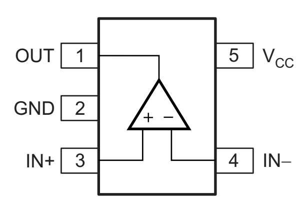
RELATED PRODUCTS

DEVICE	DESCRIPTION
TLV3011	5-μA (max) open-drain, 1.8-V to 5.5-V with integrated voltage reference in 1.5-mm × 1.5-mm micro-sized packages
TLV3012	5-μA (max) push-pull, 1.8-V to 5.5-V with integrated voltage reference in micro-sized packages
TLV3501	4.5-ns, rail-to-rail, push-pull comparator in micro-sized packages
LMV7235	75-ns, 65-μA, 2.7-V to 5.5-V, rail-to-rail input comparator with open-drain output
REF3333	30-ppm/°C drift, 3.9-μA, SOT23-3, SC70-3 voltage reference

D AND DGK PACKAGES
SOIC-8 AND MSOP-8
(TOP VIEW)



DCK AND DBV PACKAGES
SC70-5 AND SOT23-5
(TOP VIEW)



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD(2)	PACKAGE DESIGNATOR	PACKAGE MARKING	ORDERING NUMBER
TLV3201	SOT23-5	DBV	RAI	TLV3201AIDBV
	SC70-5	DCK	SDP	TLV3201AIDCK
TLV3202	SOIC-8	D	TL3202	TLV3202AID
	MSOP-8	DGK	VUDC	TLV3202AIDGK

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available at www.ti.com/sc/package.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
Supply voltage		7	V
Signal input terminals	Voltage(2)	–0.5 to (V_{CC}) + 0.5	V
	Current(2)	±10	mA
Output short circuit(3)		100	mA
Operating temperature range		–55 to +125	°C
Storage temperature range, T_{stg}		–65 to +150	°C
Junction temperature, T_J		+150	°C
Electrostatic discharge (ESD) ratings TLV3201	Human body model (HBM)	2000	V
Electrostatic discharge (ESD) ratings TLV3202	Human body model (HBM)	1000	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.
(3) Short-circuit to ground.

ELECTRICAL CHARACTERISTICS: V_{CC} = 5.0 V

At T_A = +25°C and V_{CC} = 5.0 V, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{IO}	Input offset voltage		V_{CM} = V_{CC} / 2		1	5	mV
			T_A = –40°C to +125°C			6	mV
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to +125°C		1	10	µV/°C
PSRR	Power-supply rejection ratio		V_{CM} = V_{CC} / 2, V_{CC} = 2.5 V to 5.5 V	65	85		dB
	Input hysteresis				1.2		mV
INPUT BIAS CURRENT							
I_{IB}	Input bias current		V_{CM} = V_{CC} / 2		1	50	pA
			T_A = –40°C to +125°C			5	nA
I_{IO}	Input offset current		V_{CM} = V_{CC} / 2		1	50	pA
			T_A = –40°C to +125°C			2.5	nA
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range		T_A = –40°C to +125°C	(V_{EE}) – 0.2		(V_{CC}) + 0.2	V
CMRR	Common-mode rejection ratio		–0.2 V < V_{CM} < 5.2 V	60	70		dB
INPUT IMPEDANCE							
	Common-mode				10^{13} || 2		Ω || pF
	Differential				10^{13} || 4		Ω || pF
SWITCHING CHARACTERISTICS							
t_{pd}	Propagation delay time	Low to high	Input overdrive = 20 mV, C_L = 15 pF		47	50	ns
			Input overdrive = 100 mV, C_L = 15 pF		43	50	ns
			T_A = –40°C to +125°C			55	ns
		High to low	Input overdrive = 20 mV, C_L = 15 pF		45	50	ns
			Input overdrive = 100 mV, C_L = 15 pF		42	50	ns
			T_A = –40°C to +125°C			55	ns
	Propagation delay skew		Input overdrive = 20mV, C_L = 15 pF		2		ns
	Propagation delay matching (TLV3202)	High to low, Low to High	Input overdrive = 20 mV, C_L = 15 pF			5	ns
t_r	Rise time		10% to 90%		2.9		ns
t_f	Fall time		10% to 90%		3.7		ns
OUTPUT							
V_{OL}	Voltage output swing	From lower rail	I_{SINK} = 4 mA		175	190	mV
			T_A = –40°C to +125°C			225	mV
V_{OH}		From upper rail	I_{SOURCE} = 4 mA		120	140	mV
			T_A = –40°C to +125°C			170	mV
I_{SC}	Short-circuit current (per comparator)		I_{SC} sinking	40	48		mA
			T_A = –40°C to +125°C		See Typical Curve		mA
			I_{SC} sourcing	52	60		mA
			T_A = –40°C to +125°C		See Typical Curve		mA
POWER SUPPLY							
V_{CC}	Specified voltage			2.7		5.5	V
I_Q	Quiescent current				40	50	µA
			T_A = –40°C to +125°C			65	µA
TEMPERATURE							
	Specified range			–40		+125	°C
	Storage range			–65		+150	°C

ELECTRICAL CHARACTERISTICS: V_{CC} = 2.7 V

At T_A = +25°C and V_{CC} = 2.7 V, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{IO}	Input offset voltage		$V_{CM} = V_{CC} / 2$		1	5	mV
			T_A = –40°C to +125°C			6	mV
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to +125°C		1	10	μV/°C
PSRR	Power-supply rejection ratio		$V_{CM} = V_{CC} / 2$, V_{CC} = 2.5 V to 5.5 V	65	85		dB
	Input hysteresis				1.2		mV
INPUT BIAS CURRENT							
I_{IB}	Input bias current		$V_{CM} = V_{CC} / 2$		1	50	pA
			T_A = –40°C to +125°C			5	nA
I_{IO}	Input offset current		$V_{CM} = V_{CC} / 2$		1	50	pA
			T_A = –40°C to +125°C			2.5	nA
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range		T_A = –40°C to +125°C	(V_{EE}) – 0.2		(V_{CC}) + 0.2	V
CMRR	Common-mode rejection ratio		–0.2 V < V_{CM} < 2.9 V	56	68		dB
INPUT IMPEDANCE							
	Common-mode				10^{13} || 2		Ω || pF
	Differential				10^{13} || 4		Ω || pF
SWITCHING CHARACTERISTICS							
t_{pd}	Propagation delay time	Low to high	Input overdrive = 20 mV, C_L = 15 pF		47	50	ns
			Input overdrive = 100 mV, C_L = 15 pF		42	50	ns
			T_A = –40°C to +125°C			55	ns
		High to low	Input overdrive = 20 mV, C_L = 15 pF		40	50	ns
			Input overdrive = 100 mV, C_L = 15 pF		38	50	ns
			T_A = –40°C to +125°C			55	ns
	Propagation delay skew		Input overdrive = 20mV, C_L = 15 pF		2		ns
	Propagation delay matching (TLV3202)	High to low, Low to High	Input overdrive = 20 mV, C_L = 15 pF			5	ns
t_r	Rise time		10% to 90%		4.8		ns
t_f	Fall time		10% to 90%		5.2		ns
OUTPUT							
V_{OL}	Voltage output swing	From lower rail	I_{SINK} = 4 mA		230	260	mV
			T_A = –40°C to +125°C			325	mV
V_{OH}		From upper rail	I_{SOURCE} = 4 mA		210	250	mV
			T_A = –40°C to +125°C			350	mV
I_{SC}	Short-circuit current (per comparator)		I_{SC} sinking	13	19		mA
			T_A = –40°C to +125°C		See Typical Curve		mA
			I_{SC} sourcing	15	21		mA
			T_A = –40°C to +125°C		See Typical Curve		mA
POWER SUPPLY							
V_{CC}	Specified voltage			2.7		5.5	V
I_Q	Quiescent current				36	46	μA
			T_A = –40°C to +125°C			60	μA
TEMPERATURE							
	Specified range			–40		+125	°C
	Storage range			–65		+150	°C

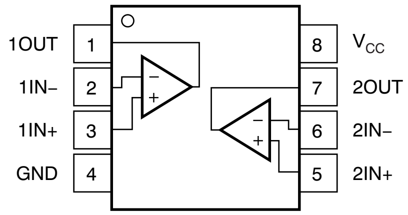
THERMAL INFORMATION

THERMAL METRIC(1)		TLV3201		TLV3202		UNITS
		DBV (SOT23)	DCK (SC70)	D (SOIC)	DGK (MSOP)	
		5 PINS	5 PINS	8 PINS	8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	237.8	281.9	146.3	201.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	108.7	97.6	97.2	92.5	
θ_{JB}	Junction-to-board thermal resistance	64.1	68.3	84.2	123.3	
ψ_{JT}	Junction-to-top characterization parameter	12.1	2.6	45.5	23.0	
ψ_{JB}	Junction-to-board characterization parameter	63.3	67.3	83.7	121.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	

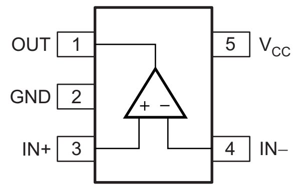
(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PIN CONFIGURATIONS

D AND DGK PACKAGES
SOIC-8 AND MSOP-8
(TOP VIEW)



DCK AND DBV PACKAGES
SC70-5 AND SOT23-5
(TOP VIEW)



PIN DESCRIPTIONS: D, DGK

NAME	NO.	DESCRIPTION
1IN–	2	Negative input, comparator 1
1IN+	3	Positive input, comparator 1
1OUT	1	Output, comparator 1
2IN–	6	Negative input, comparator 2
2IN+	5	Positive input, comparator 2
2OUT	7	Output, comparator 2
GND	4	Negative supply, ground
V_{CC}	8	Positive supply

PIN DESCRIPTIONS: DCK, DBV

NAME	NO.	DESCRIPTION
OUT	1	Output
GND	2	Negative supply, ground
IN+	3	Positive input
V_{CC}	5	Positive supply
IN–	4	Negative input

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_{CC} = +5 V, and input overdrive (V_{OD}) = 20 mV, unless otherwise noted.

OFFSET VOLTAGE DISTRIBUTION

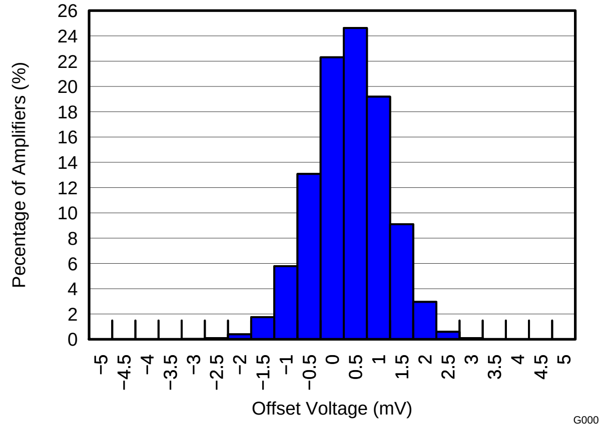


Figure 1.

HYSTERESIS DISTRIBUTION

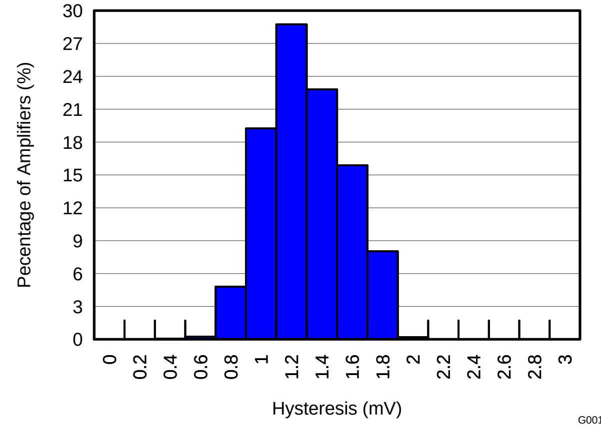


Figure 2.

OFFSET VOLTAGE vs TEMPERATURE

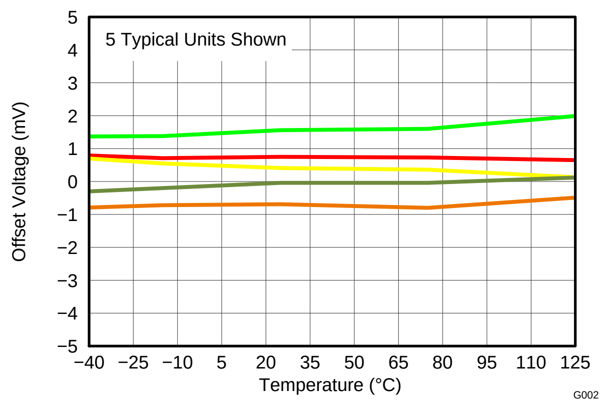


Figure 3.

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

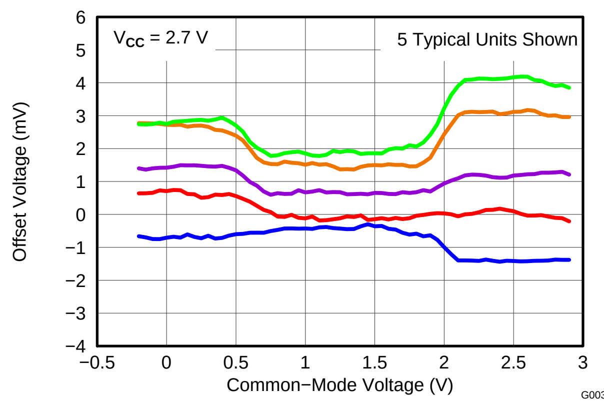


Figure 4.

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

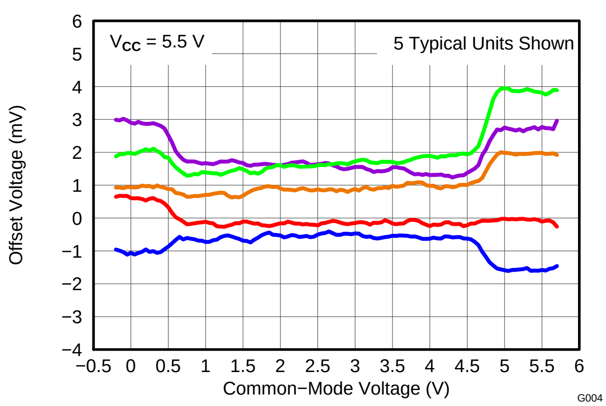


Figure 5.

OFFSET VOLTAGE vs POWER SUPPLY

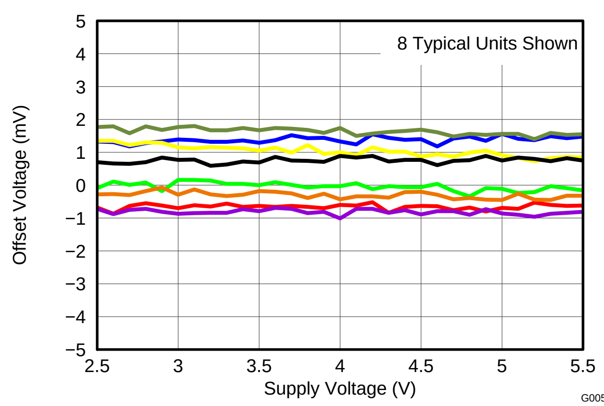


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = +5 V, and input overdrive (V_{OD}) = 20 mV, unless otherwise noted.

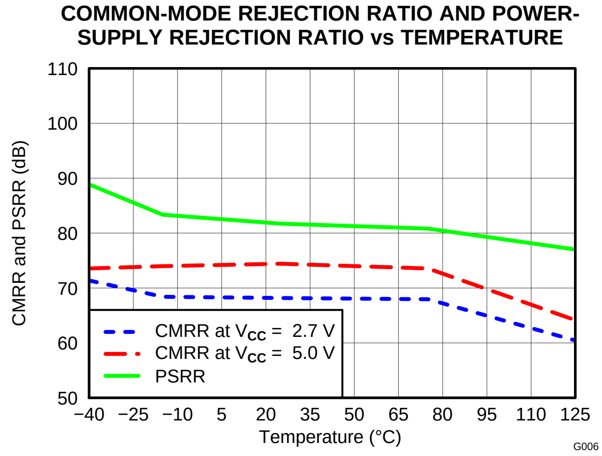


Figure 7.

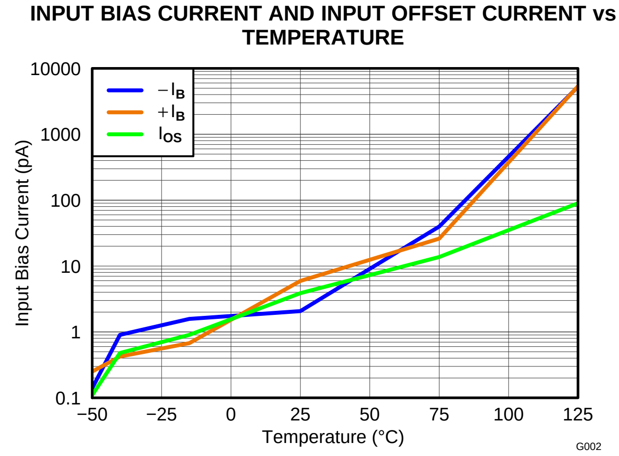


Figure 8.

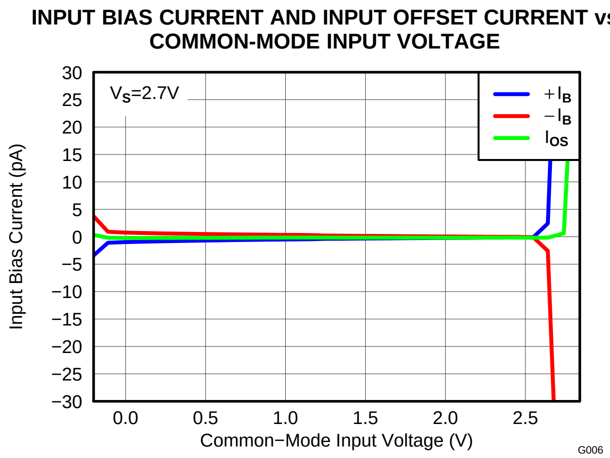


Figure 9.

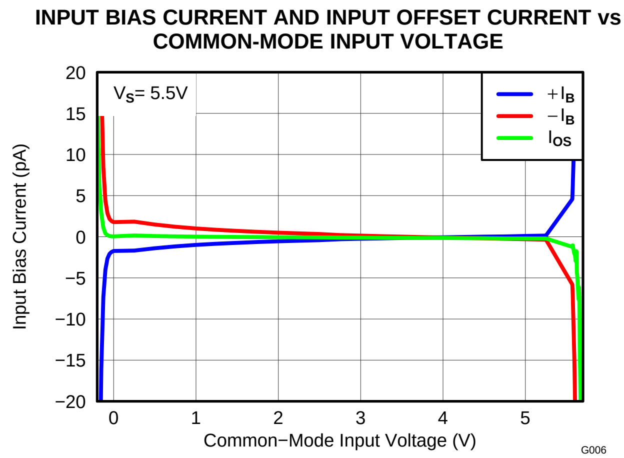


Figure 10.

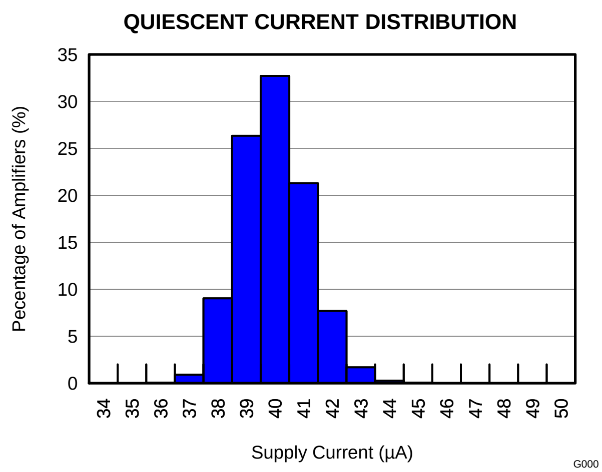


Figure 11.

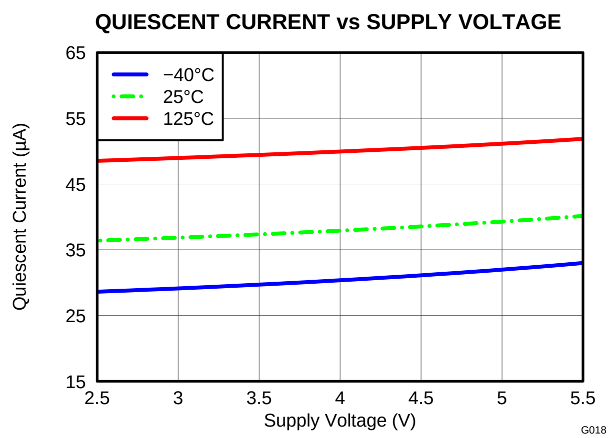


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = +5 V, and input overdrive (V_{OD}) = 20 mV, unless otherwise noted.

QUIESCENT CURRENT vs SWITCHING FREQUENCY

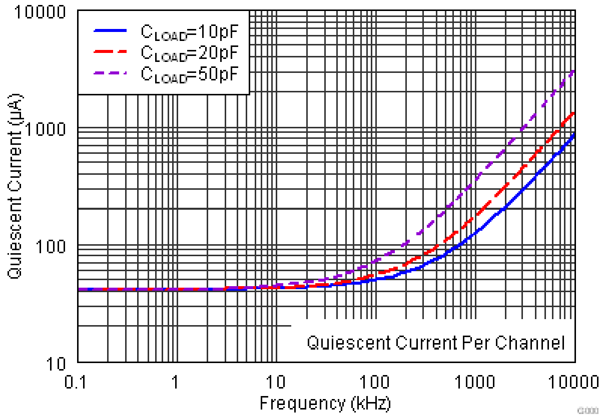


Figure 13.

SHORT-CIRCUIT CURRENT vs TEMPERATURE

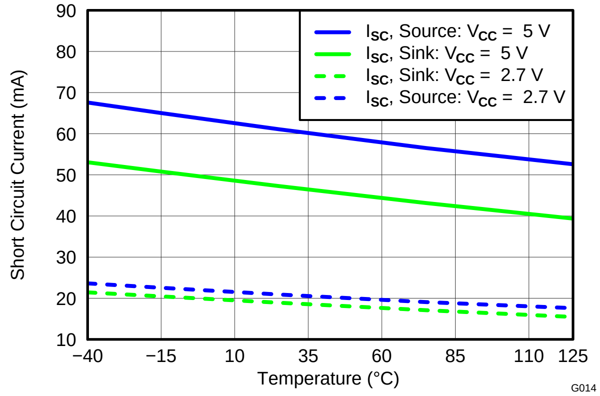


Figure 14.

OUTPUT VOLTAGE vs OUTPUT CURRENT

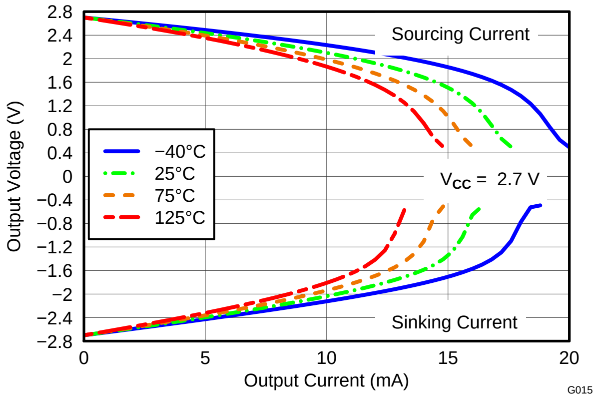


Figure 15.

OUTPUT VOLTAGE vs OUTPUT CURRENT

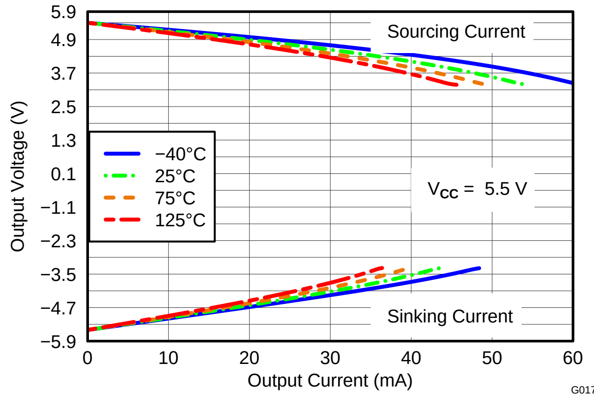


Figure 16.

PROPAGATION DELAY FALLING EDGE

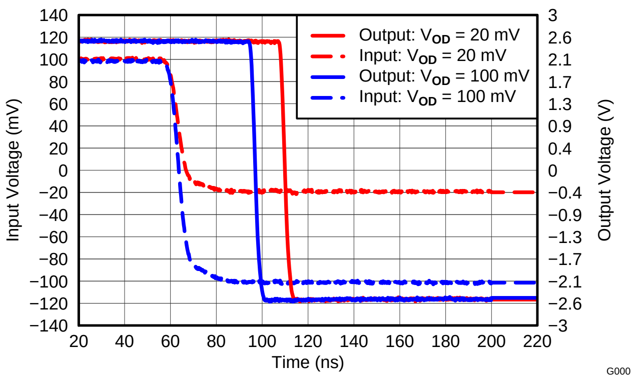


Figure 17.

PROPAGATION DELAY RISING EDGE

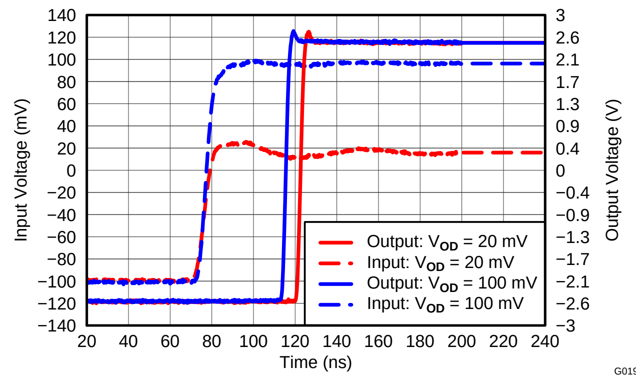


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = +5 V, and input overdrive (V_{OD}) = 20 mV, unless otherwise noted.

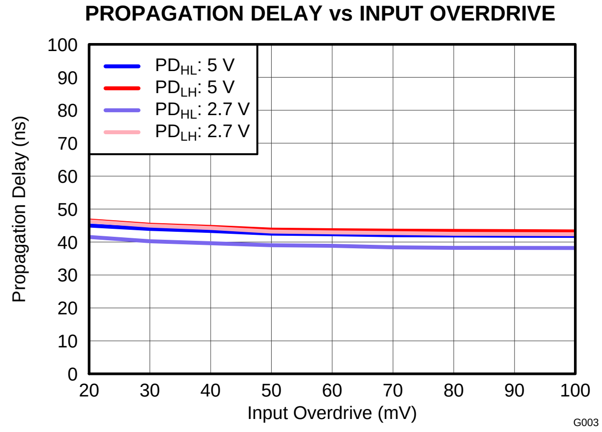


Figure 19.

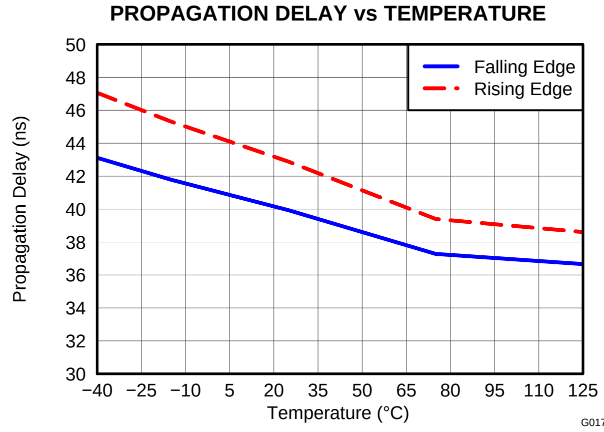


Figure 20.

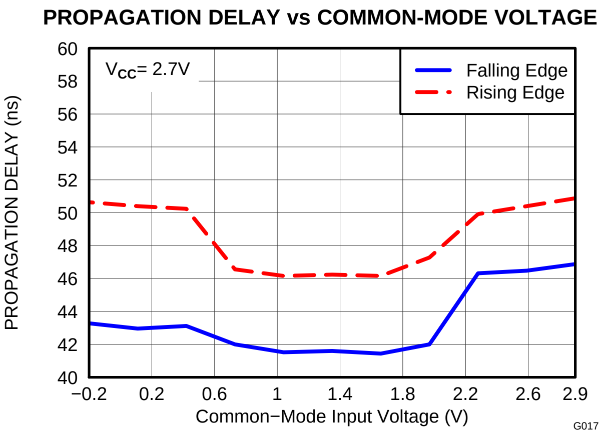


Figure 21.

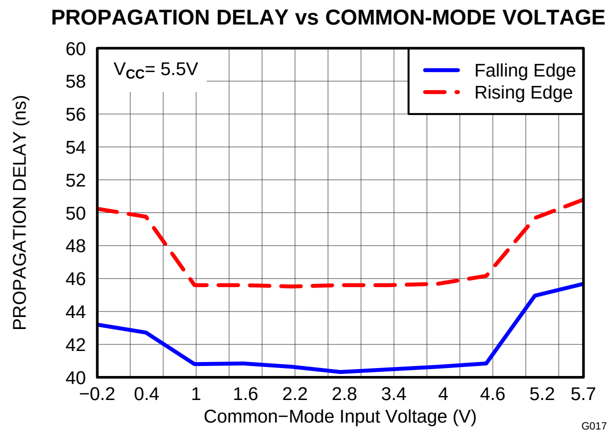


Figure 22.

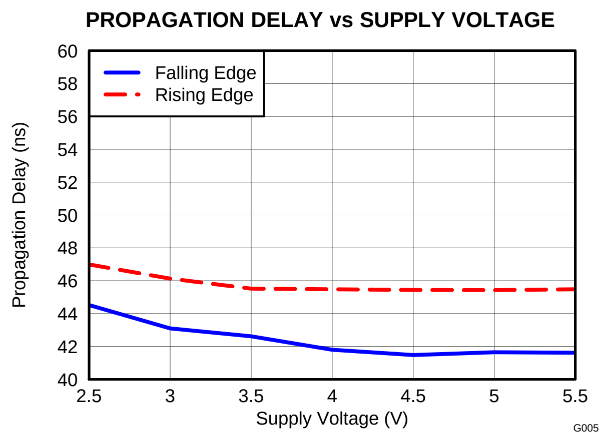


Figure 23.

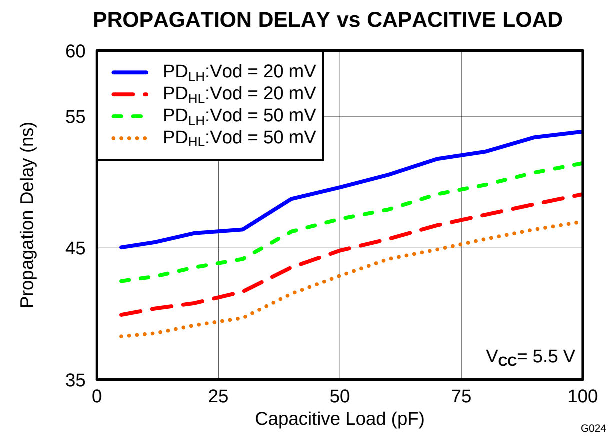


Figure 24.

APPLICATION INFORMATION

The TLV3201 and TLV3202 are single- and dual-supply (respectively), push-pull comparators featuring 40 ns of propagation delay on only 40 µA of supply current. This combination of fast response time and minimal power consumption make the TLV3201 and TLV3202 excellent comparators for portable, battery-powered applications as well as fast-switching threshold detection such as pulse-width modulation (PWM) output monitors and zero-cross detection.

COMPARATOR INPUTS

The TLV3201 and TLV3202 are rail-to-rail input comparators, with an input common-mode range that exceeds the supply rails by 200 mV for both positive and negative supplies. The devices are specified from 2.7 V to 5.5 V, with room temperature operation from 2.5 V to 5.5 V. The TLV3201 and TLV3202 are designed to prevent phase inversion when the input pins exceed the supply voltage. Figure 25 shows the TLV320x response when input voltages exceed the supply, resulting in no phase inversion.

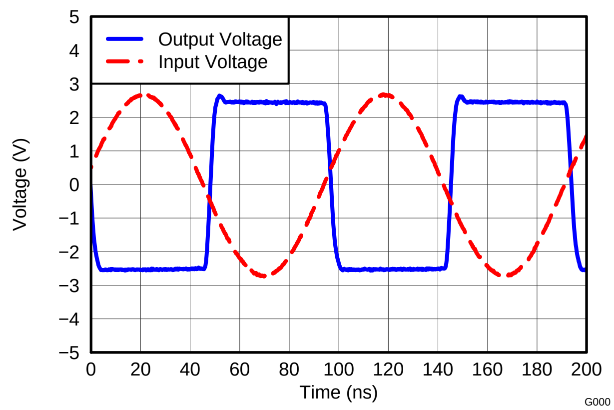


Figure 25. No Phase Inversion: Comparator Response to Input Voltage (Prop Delay Included)

The electrostatic discharge (ESD) protection input structure of two back-to-back diodes and 1-kΩ series resistors are used to limit the differential input voltage applied to the precision input of the comparator by clamping input voltages that exceed V_{CC} beyond the specified operating conditions. If potential overvoltage conditions that exceed absolute maximum ratings are present, the addition of external bypass diodes and resistors is recommended, as shown in Figure 26. Large differential voltages greater than the supply voltage should be avoided to prevent damage to the input stage.

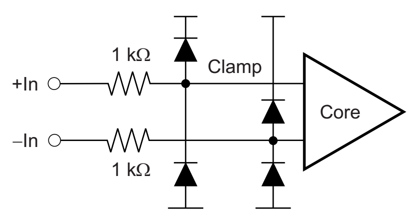


Figure 26. TLV3201 equivalent input structure

EXTERNAL HYSTERESIS

The TLV3201 and TLV3202 have a hysteresis transfer curve (shown in Figure 27) that is a function of the following three components:

- V_{TH}: the actual set voltage or threshold trip voltage
- V_{OS}: the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond in order to change output states.
- V_{HYST}: internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

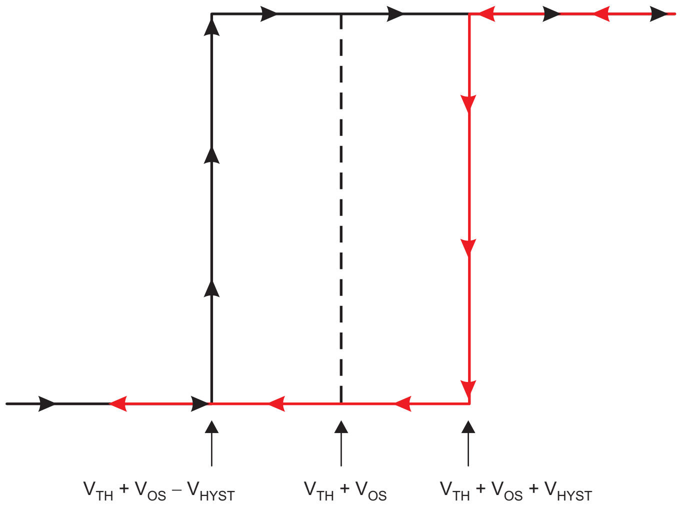


Figure 27. TLV3201 Hysteresis Transfer Curve

Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in Figure 28. When V_{IN} at the inverting input is less than V_A, the output voltage is high (for simplicity assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2. The lower input trip voltage (V_{A1}) is defined by Equation 1:

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When V_{IN} is greater than [$V_A \times (V_{IN} > V_A)$], the output voltage is low, very close to ground. In this case, the three network resistors can be presented as R2 || R3 in series with R1. The upper trip voltage (V_{A2}) is defined by Equation 2:

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

The total hysteresis provided by the network is defined by Equation 3:

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

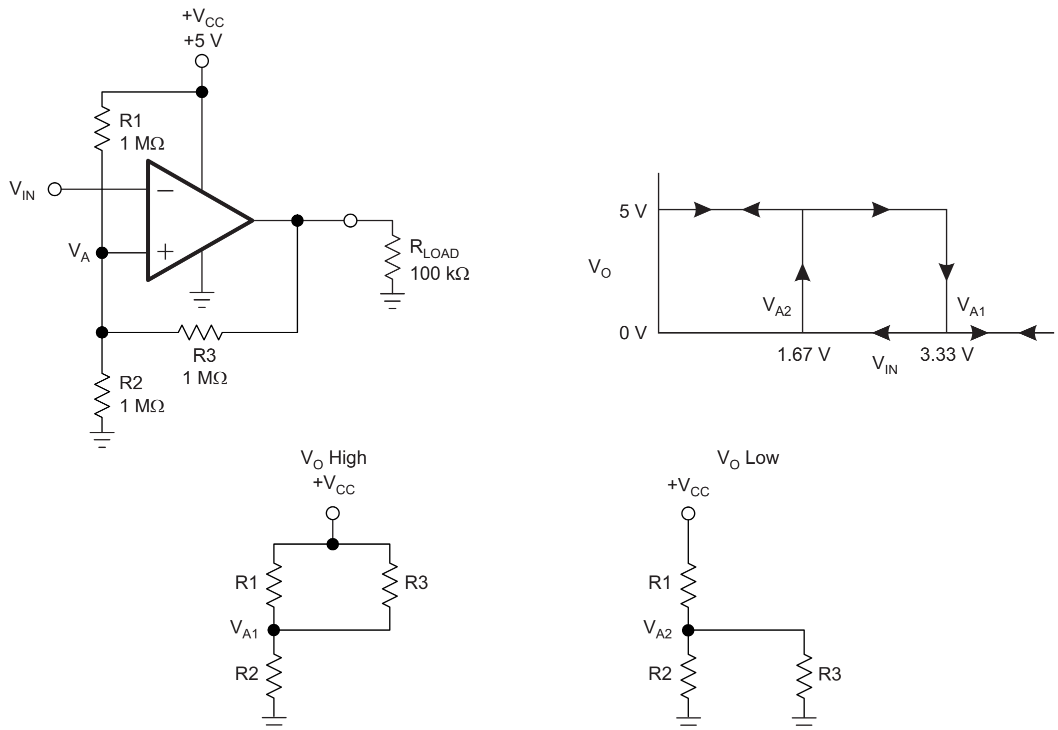


Figure 28. TLV3201 in Inverting Configuration with Hysteresis

Noninverting Comparator with Hysteresis

A noninverting comparator with hysteresis requires a two-resistor network, as shown in Figure 29, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise up to V_{IN1}. V_{IN1} is calculated by Equation 4:

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} \times V_{REF} \quad (4)$$

When V_{IN} is high, the output is also high. In order for the comparator to switch back to a low state, V_{IN} must equal V_{REF} before V_A is again equal to V_{REF}. V_{IN} can be calculated by Equation 5:

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \quad (5)$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as defined by Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \quad (6)$$

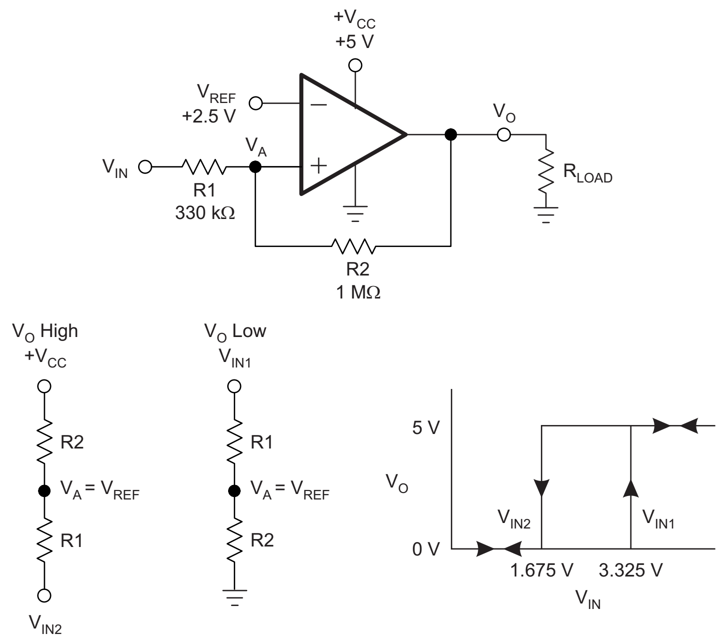


Figure 29. TLV3201 in Noninverting Configuration with Hysteresis

CAPACITIVE LOADS

The TLV3201 and TLV3202 feature a push-pull output. When the output switches, there is a direct path between V_{CC} and ground, causing increased output sinking or sourcing current during the transition. Following the transition the output current decreases and supply current returns to 40 µA, thus maintaining low power consumption. Under reasonable capacitive loads, the TLV3201 and TLV3202 maintain specified propagation delay (see the Typical Characteristics), but excessive capacitive loading under high switching frequencies may increase supply current, propagation delay, or induce decreased slew rate.

CIRCUIT LAYOUT

The TLV3201 and TLV3202 are fast-switching, high-speed comparators and require high-speed layout considerations. For best results, the following layout guidelines should be maintained:

1. Use a printed circuit board (PCB) with a good, unbroken low-inductance ground plane.
2. Place a decoupling capacitor (0.1-μF ceramic, surface-mount capacitor) as close as possible to V_{CC}.
3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
4. Solder the device directly to the PCB rather than using a socket.
5. For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. The topside ground plane runs between the output and inputs.
6. The ground pin ground trace runs under the device up to the bypass capacitor, shielding the inputs from the outputs.

APPLICATIONS CIRCUITS

One of the benefits of ac coupling a single-supply comparator circuit is that it can block dc offsets induced by ground-loop offsets that could potentially produce either a false trip or a common-mode input violation. Figure 30 shows the TLV3201 configured as an ac-coupled comparator.

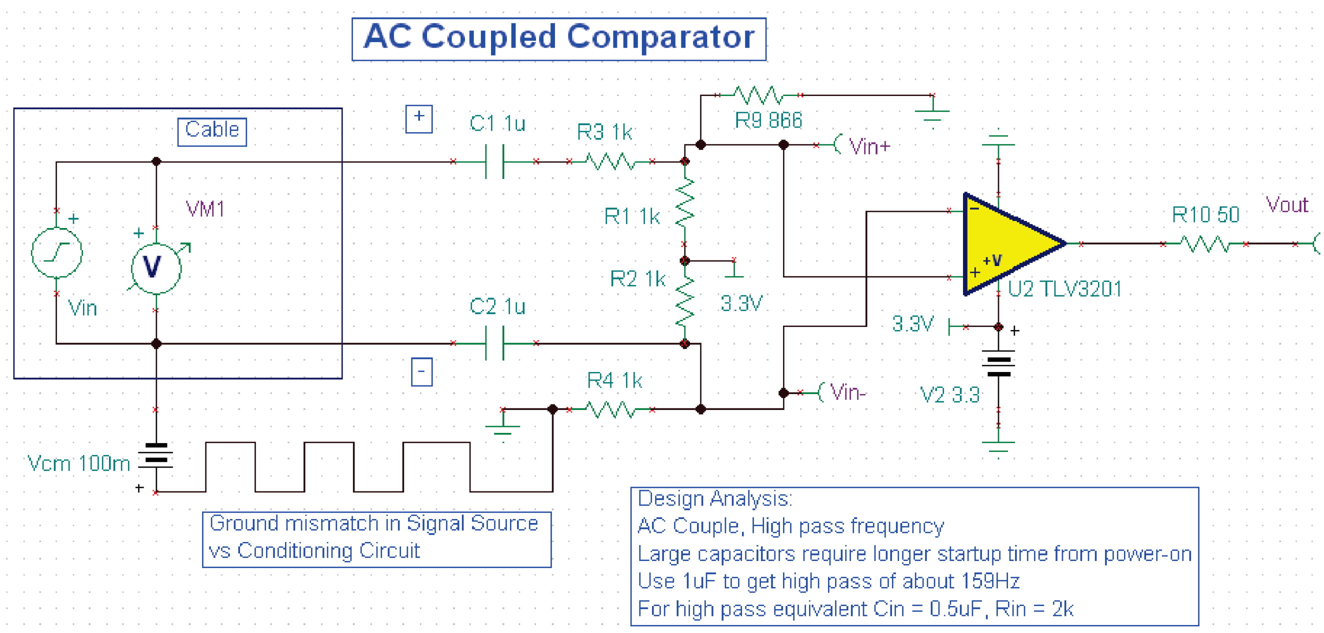


Figure 30. TLV3201 Configured as an AC-Coupled Comparator

Figure 31 shows a single-supply current monitor configured as a difference amplifier with a gain of 50. The OPA320 was chosen for this circuit because of its gain bandwidth (20 MHz), which allows higher speed triggering and monitoring of the current across the shunt resistor followed by the fast response of the TLV3201.

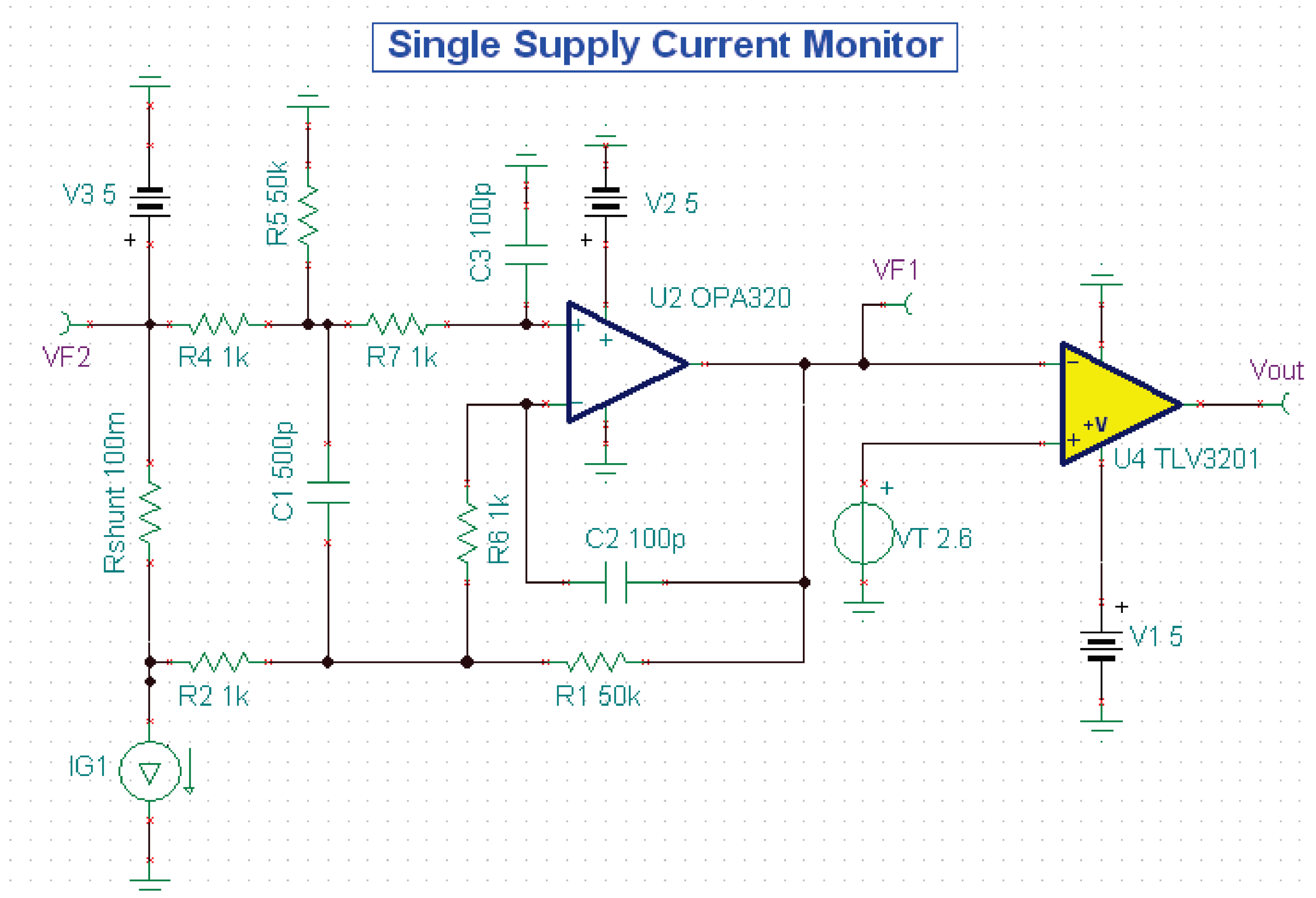


Figure 31. TLV3201 and OPA320 Configured as a Fast-Response Output Current Monitor

Figure 32 shows the TMP20 and TLV3201 designed as a high-speed temperature switch. The TMP20 is an analog output temperature sensor where output voltage decreases with temperature. The comparator output is tripped when the output reaches a critical trip threshold.

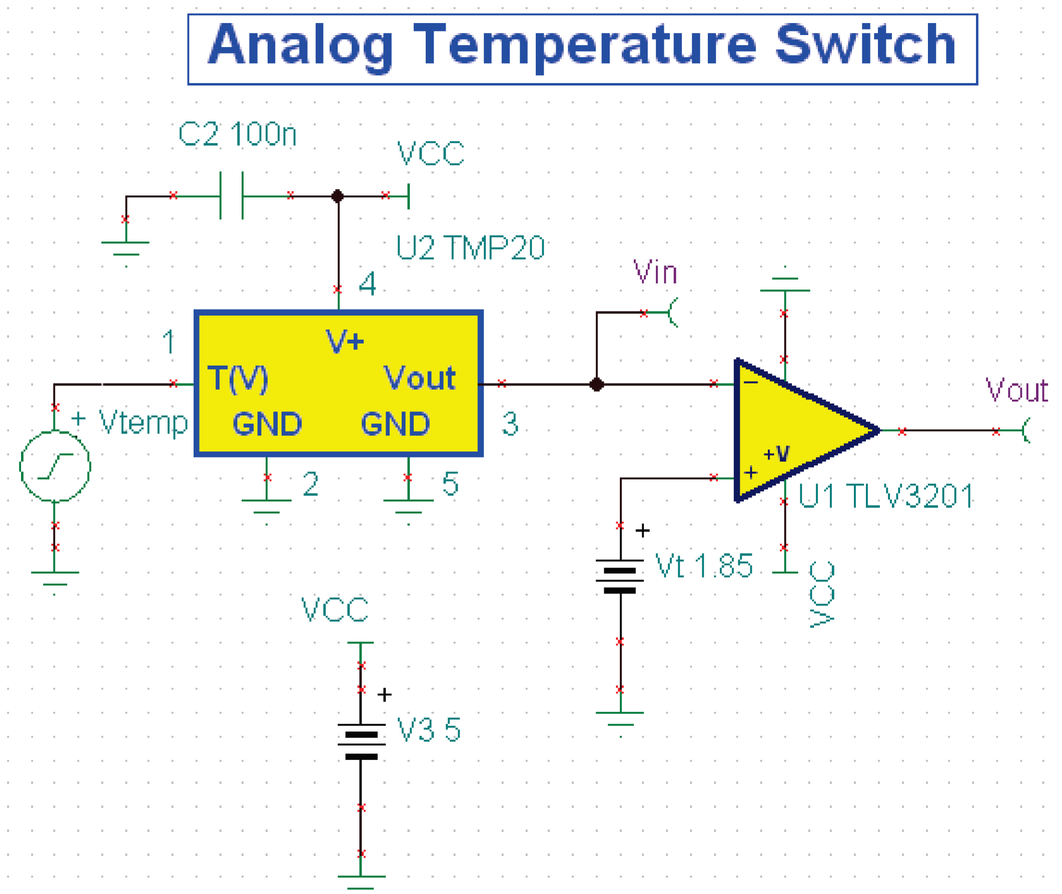


Figure 32. TLV3201 and TMP20 Configured as a Precision Analog Temperature Switch

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2012) to Revision A **Page**

- Changed product status from Production Data to Mixed Status 1
- Added dual channel device 1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLV3201AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAI	Samples
TLV3201AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAI	Samples
TLV3201AIDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SDP	Samples
TLV3201AIDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SDP	Samples
TLV3202AID	ACTIVE	SOIC	D	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL3202	Samples
TLV3202AIDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VUDC	Samples
TLV3202AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VUDC	Samples
TLV3202AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL3202	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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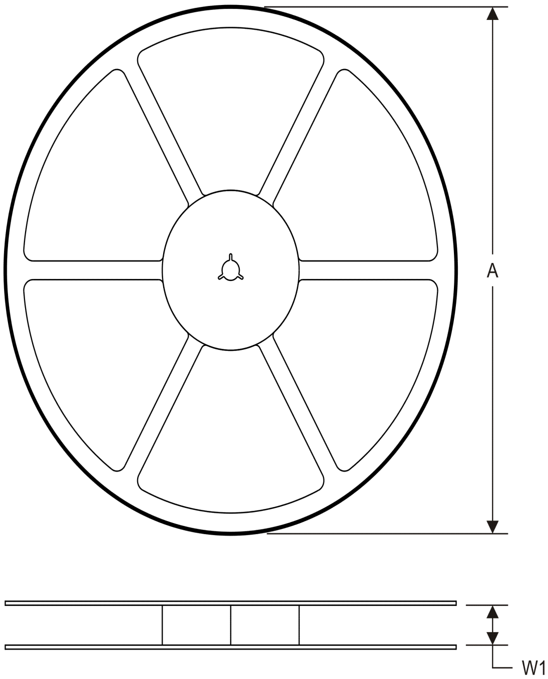
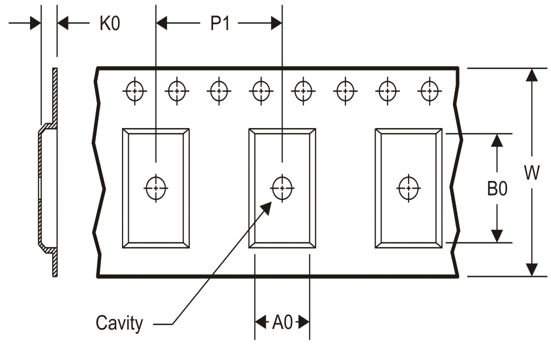
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



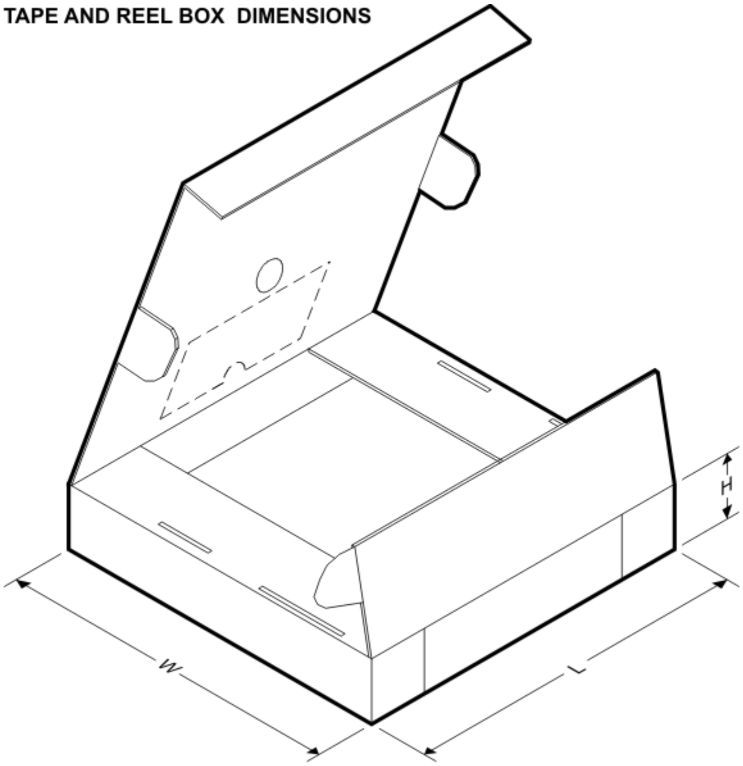
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3201AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV3202AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV3202AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

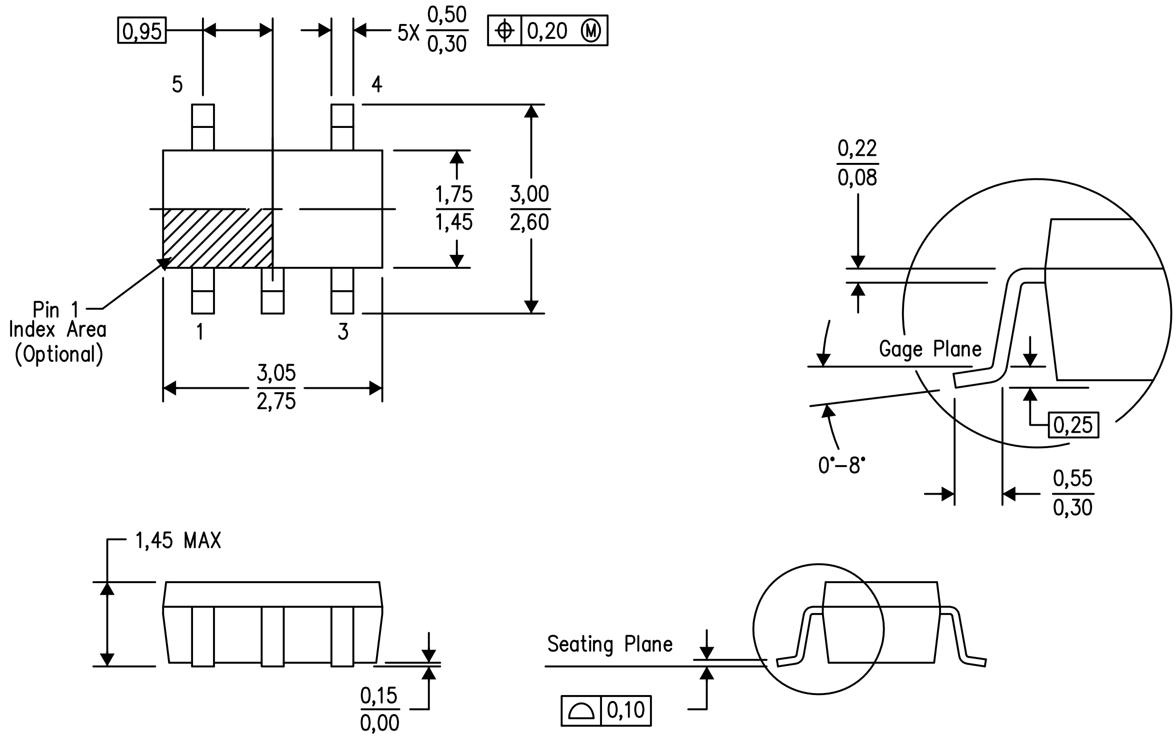
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3201AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV3202AIDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TLV3202AIDR	SOIC	D	8	2500	367.0	367.0	35.0

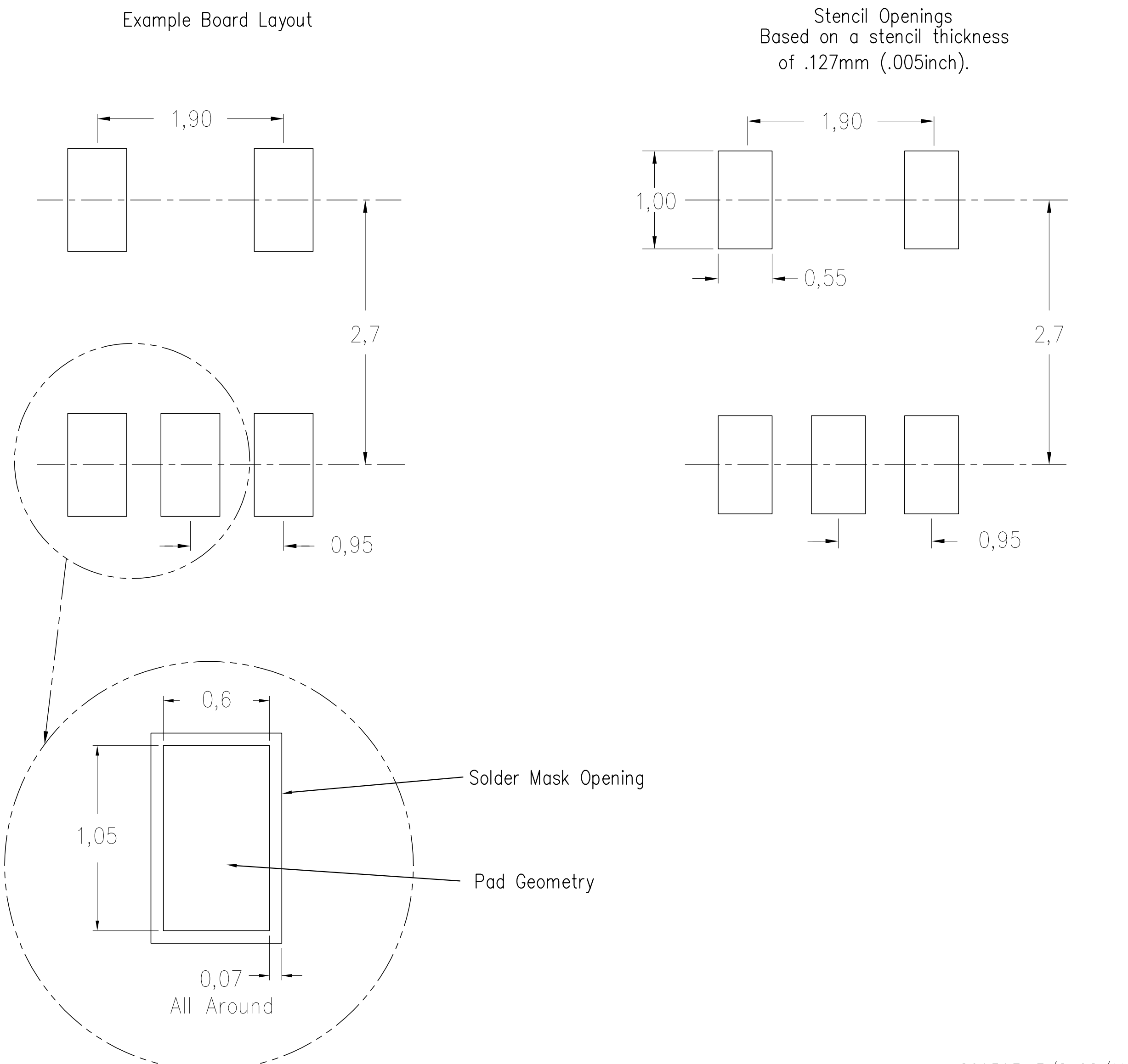
DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/L 08/2013

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.

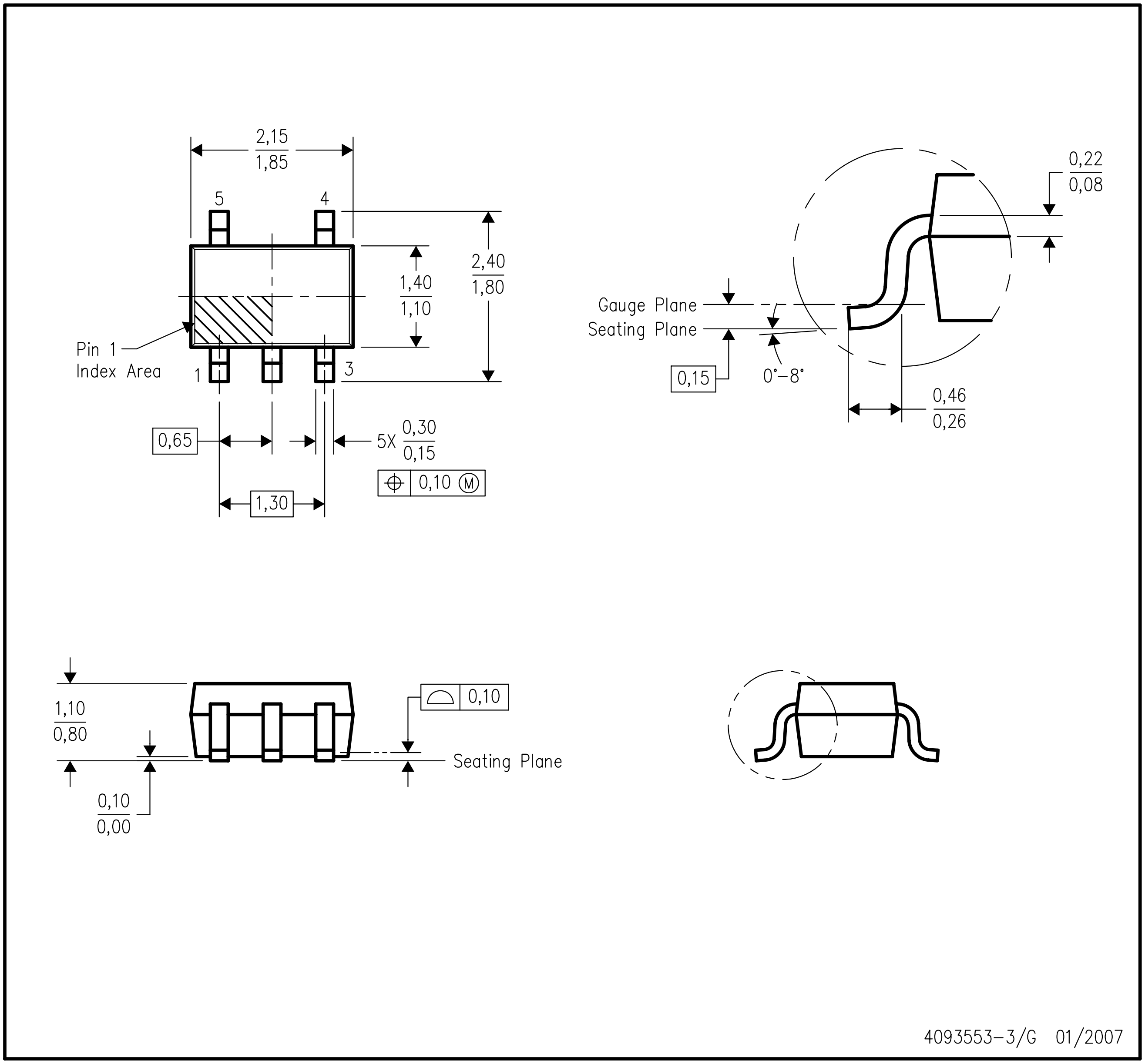
DBV (R-PDSO-G5) PLASTIC SMALL OUTLINE



4209593-3/C 08/11

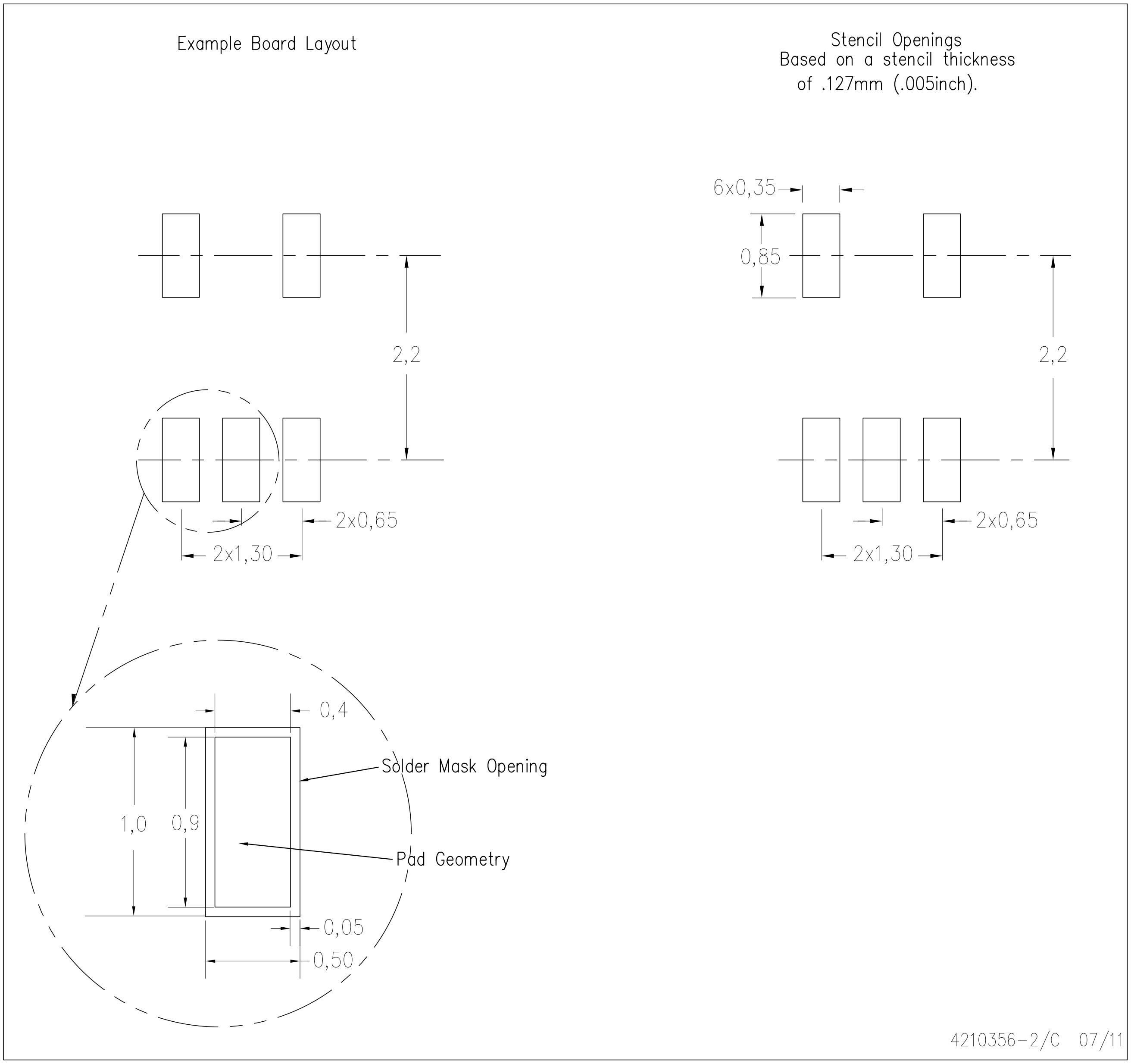
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



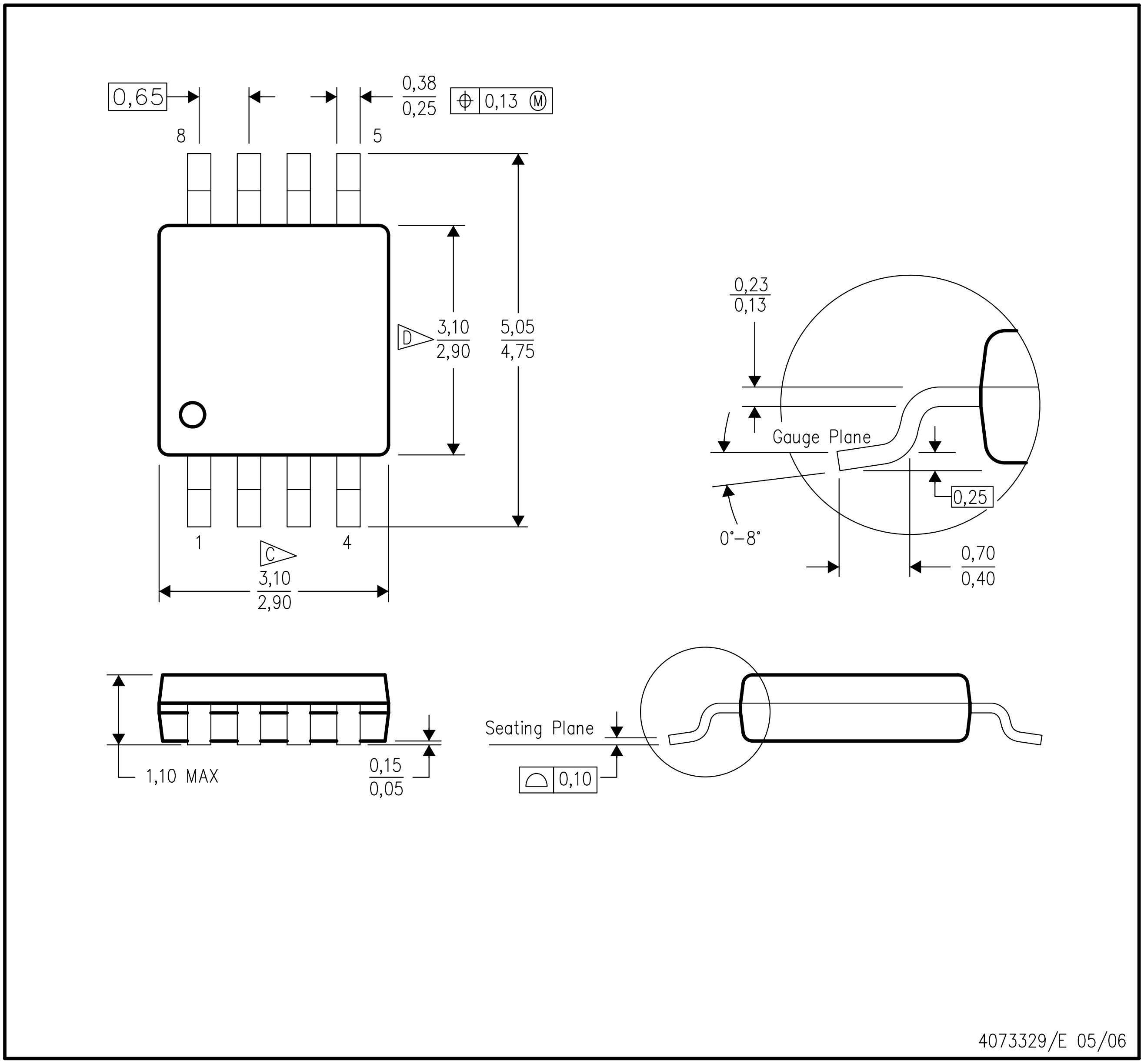
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



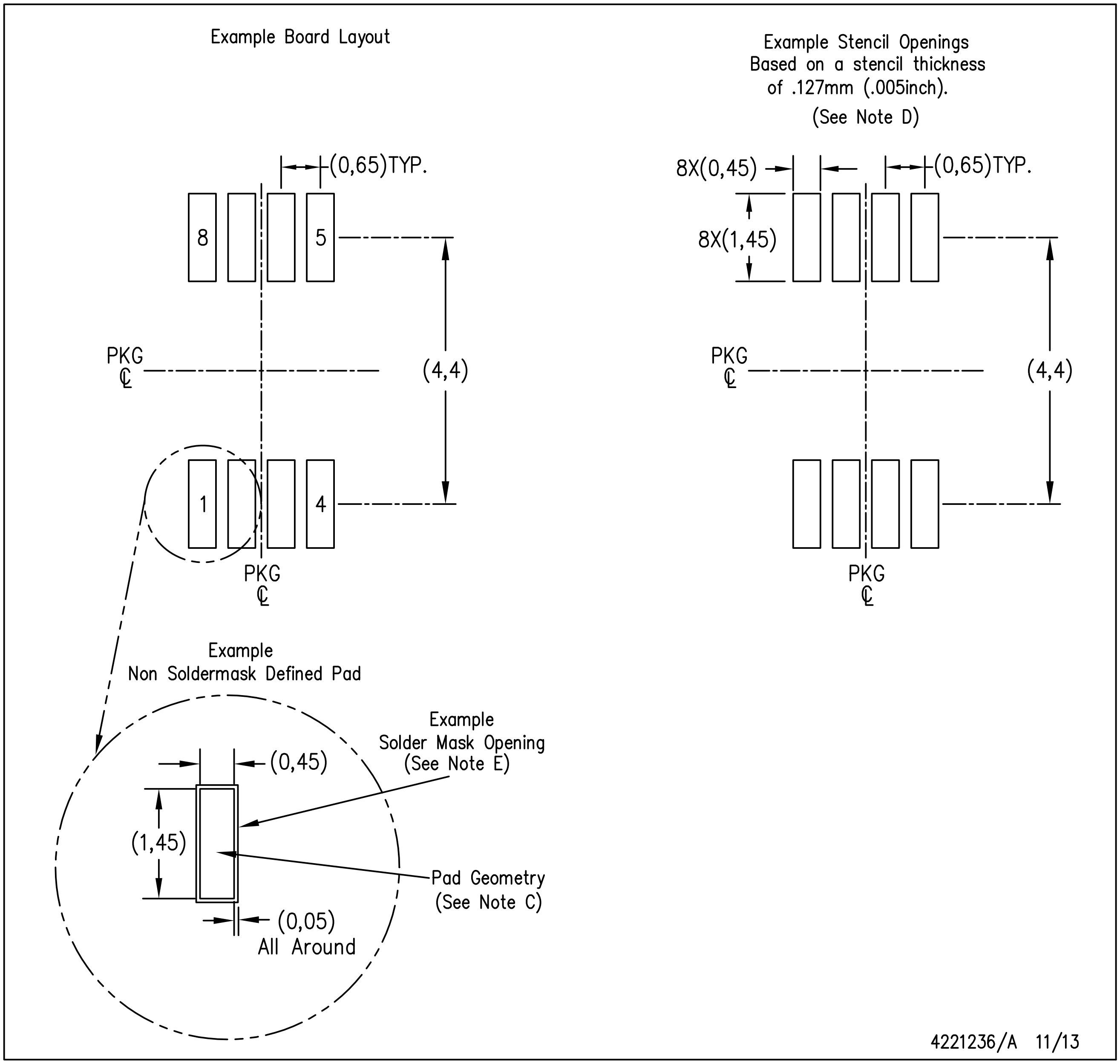
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



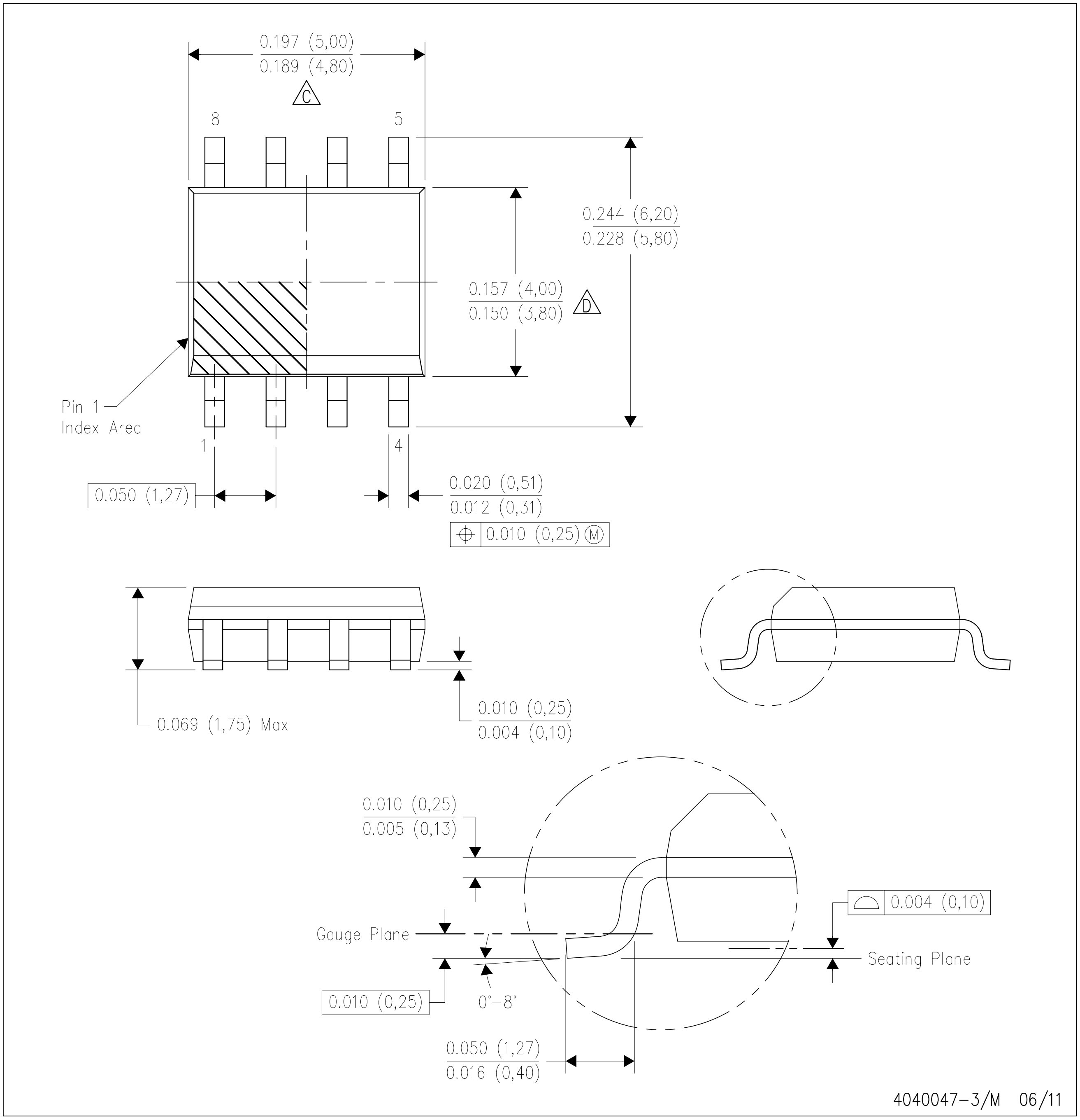
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in inches (millimeters).

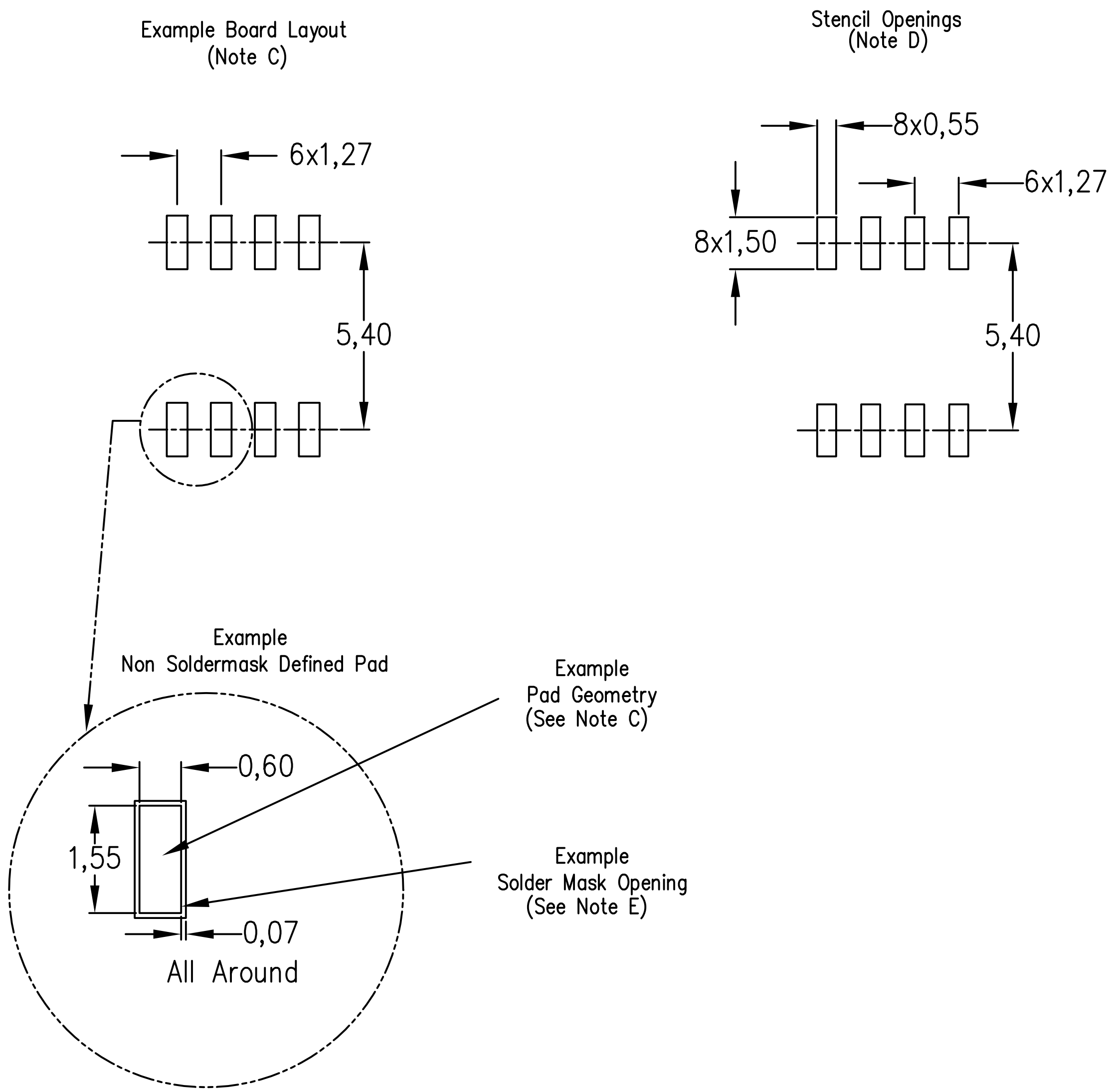
B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



4211283-2/E 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.