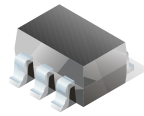


TLV61225

SINGLE CELL HIGH EFFICIENT STEP-UP CONVERTER IN 6 PIN SC-70 PACKAGE

FEATURES

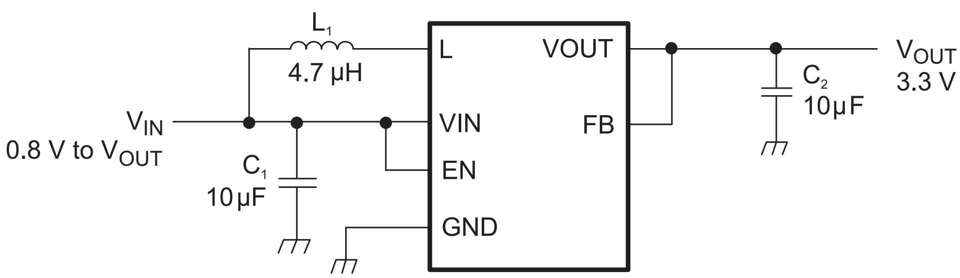
- Up to 94% Efficiency at Typical Operating Conditions
- 5 μA Quiescent Current
- Operating Input Voltage from 0.7 V to 3.3 V
- Pass-Through Function during Shutdown
- More than 40mA Output Current from a 1.2V Input
- Typical Switch Current Rating 400 mA
- Output Overvoltage Protection
- Overtemperature Protection
- Fixed 3.3 V Output Voltage
- Small 6-pin SC-70 Package

APPLICATIONS

- Battery Powered Applications
  - 1 to 2 Cell NiMH or Alkaline
  - 1 cell Li-Primary
- Consumer and Portable Medical Products
- Personal Care Products

DESCRIPTION

The TLV61225 provides a power-supply solution for products powered by either a single-cell or two-cell alkaline or NiMH, or one-cell Li-primary battery. Possible output currents depend on the input-to-output voltage ratio. The boost converter is based on a hysteretic controller topology using synchronous rectification to obtain maximum efficiency at minimal quiescent currents. The output voltage of this device is set internally to a fixed output voltage of 3.3 V. The converter can be switched off by a featured enable pin. While being switched off, battery drain is minimized. The device is offered in a 6-pin SC-70 package (DCK) measuring 2 mm x 2 mm to enable small circuit layout size.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE DEVICE OPTIONS(1)

T_A	OUTPUT VOLTAGE DC/DC	PACKAGE MARKING	PACKAGE	PART NUMBER (2)
–40°C to 85°C	3.3 V	QUL	6-Pin SC-70	TLV61225DCK

(1) Contact the factory to check availability of other fixed output voltage versions.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range(2)	VIN, L, VOUT, EN, FB	–0.3	7.5	V
Temperature range	Operating junction temperature, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	°C
ESD rating	Human Body Model - (HBM)		2	kV
	Machine Model (MM)		200	V
	Charge Device Model - (CDM)		1.5	kV

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

DISSIPATION RATINGS TABLE

PACKAGE	THERMAL RESISTANCE Θ_{JA} (1)	THERMAL RESISTANCE Θ_{JB}	THERMAL RESISTANCE Θ_{JC}	POWER RATING $T_A \le 25°C$	DERATING FACTOR ABOVE $T_A = 25°C$
DCK	225 °C/W	70 °C/W	110 °C/W	444 mW	4.44 mW/°C

(1) Thermal ratings are determined assuming a high K PCB design according to JEDEC standard JESD51-7.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage at VIN	0.7		3.3	V
T_A	Operating free air temperature range	–40		85	°C
T_J	Operating virtual junction temperature range	–40		125	°C

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ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC/DC STAGE							
V_{IN}	Input voltage range			0.7		3.3	V
V_{IN}	Maximum minimum input voltage for startup		$R_{Load} \geq 150\ \Omega$, $T_A = 25°C$		0.7		V
V_{OUT}	TLV61225 output voltage		$V_{IN} < V_{OUT}$	3.13	3.30	3.43	V
I_{LH}	Inductor current ripple				200		mA
I_{SW}	switch current limit		$V_{OUT} = 3.3$ V, $V_{IN} = 1.2$ V	160	400		mA
R_{DSon_HSD}	Rectifying switch on resistance		$V_{OUT} = 3.3$ V		1000		mΩ
R_{DSon_LSD}	Main switch on resistance		$V_{OUT} = 3.3$ V		600		mΩ
	Line regulation		$V_{IN} < V_{OUT}$		0.5 %		
	Load regulation		$V_{IN} < V_{OUT}$		0.5 %		
I_Q	Quiescent current	V_{IN}	$I_O = 0$ mA, $V_{EN} = V_{IN} = 1.2$ V, $V_{OUT} = 3.3$ V		0.5	1	μA
		V_{OUT}			5	10	μA
I_{SD}	Shutdown current	V_{IN}	$V_{EN} = 0$ V, $V_{IN} = 1.2$ V, $V_{OUT} \geq V_{IN}$		0.2	1	μA
I_{LKG_VOUT}	Leakage current into VOUT		$V_{EN} = 0$ V, $V_{IN} = 1.2$ V, $V_{OUT} = 3.3$ V		1		μA
I_{LKG_L}	Leakage current into L		$V_{EN} = 0$ V, $V_{IN} = 1.2$ V, $V_L = 1.2$ V, $V_{OUT} \geq V_{IN}$		0.01	0.7	μA
I_{EN}	EN input current		Clamped on GND or V_{IN} ($V_{IN} < 1.5$ V)		0.005	0.1	μA
CONTROL STAGE							
V_{IL}	maximum EN input low voltage		$V_{IN} \leq 1.5$ V	$0.2 \times V_{IN}$			V
V_{IH}	minimum EN input high voltage		$V_{IN} \leq 1.5$ V			$0.8 \times V_{IN}$	V
V_{IL}	maximum EN input low voltage		$V_{IN} > 1.5$ V		0.4		V
V_{IH}	minimum EN input high voltage		$V_{IN} > 1.5$ V		1.2		V
V_{UVLO}	Undervoltage lockout threshold for turn off		V_{IN} decreasing		500		mV
	Undervoltage lockout hysteresis				50		mV
	Overvoltage protection threshold			5.5		7.5	V
	Overtemperature protection				140		°C
	Overtemperature hysteresis				20		°C

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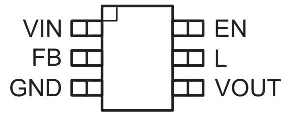
PIN ASSIGNMENTS

DCK PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
EN	6	I	Enable input (1: enabled, 0: disabled). Must be actively tied high or low.
FB	2	I	Output voltage sense input. Must be connected to V_{OUT}.
GND	3		Control / logic and power ground
L	5	I	Connection for Inductor
VIN	1	I	Boost converter input voltage
VOUT	4	O	Boost converter output voltage

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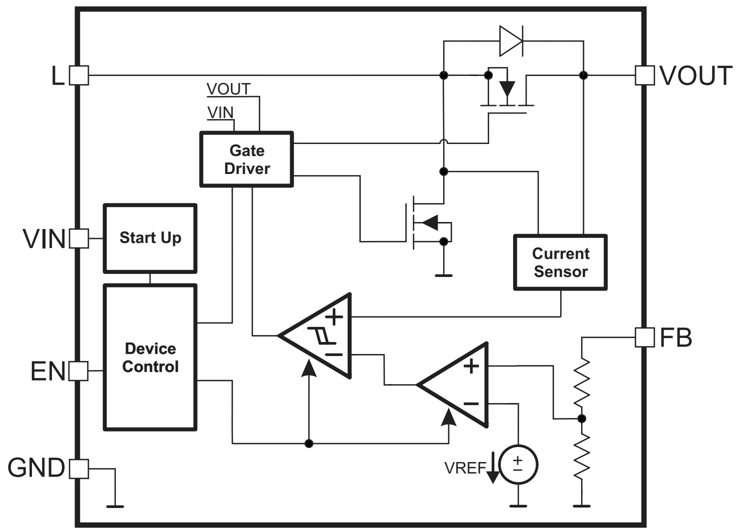
FUNCTIONAL BLOCK DIAGRAM (TLV61225)



PARAMETER MEASUREMENT INFORMATION

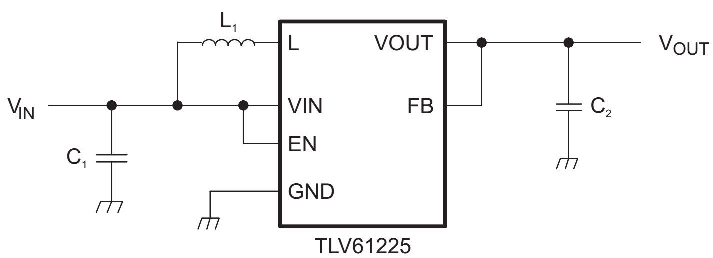


Table 1. List of Components:

COMPONENT REFERENCE	PART NUMBER	MANUFACTURER	VALUE
C_1	GRM188R60J106ME84D	Murata	10 μF, 6.3V
C_2	GRM188R60J106ME84D	Murata	10 μF, 6.3V
L_1	EPL3015-472MLB	Coilcraft	4.7 μH

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Minimum of Maximum Output Current	vs Input Voltage	1
Efficiency	vs Output Current, V_{IN} = [1.2 V; 2.4 V; 3 V]	2
	vs Input Voltage, I_{OUT} = [100 uA; 1 mA; 10 mA; 50 mA]	3
Input Current	vs Input Voltage at No Output Load, Device Enabled	4
Output Voltage	vs Output Current, V_{IN} = [1.2 V; 2.4 V]	5
	vs Input Voltage, Device Disabled, R_{LOAD} = [1 kΩ; 10 kΩ]	6
Waveforms	Output Voltage Ripple V_{IN} = 1.8 V, I_{OUT} = 50mA	7
	Load Transient Response, V_{IN} = 1.2 V, I_{OUT} = 6 mA to 50 mA	8
	Line Transient Response, V_{IN} = 1.8 V to 2.4 V, R_{LOAD} = 100 Ω	9
	Startup after Enable, V_{IN} = 0.7 V, R_{LOAD} = 150 Ω	10

MINIMUM OF MAXIMUM OUTPUT CURRENT vs INPUT VOLTAGE

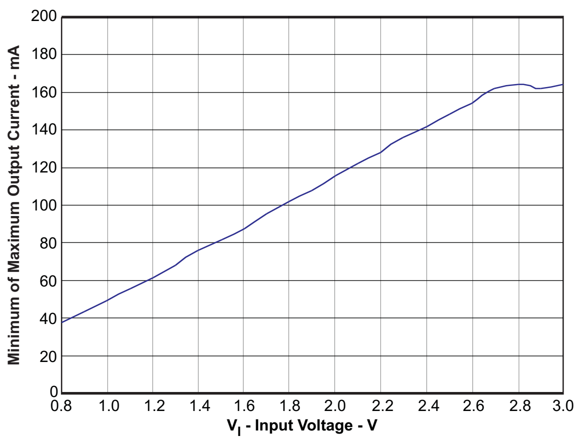


Figure 1.

EFFICIENCY vs OUTPUT CURRENT

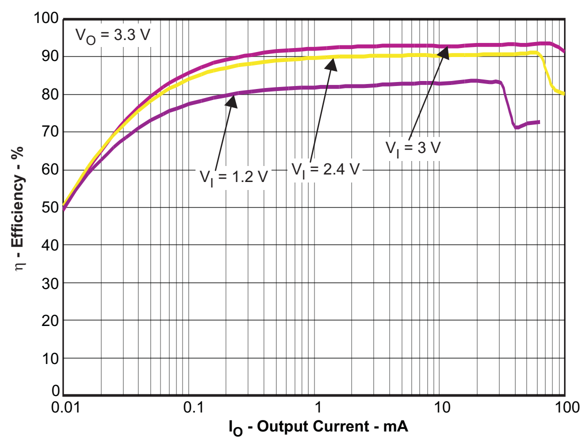


Figure 2.

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EFFICIENCY vs INPUT VOLTAGE

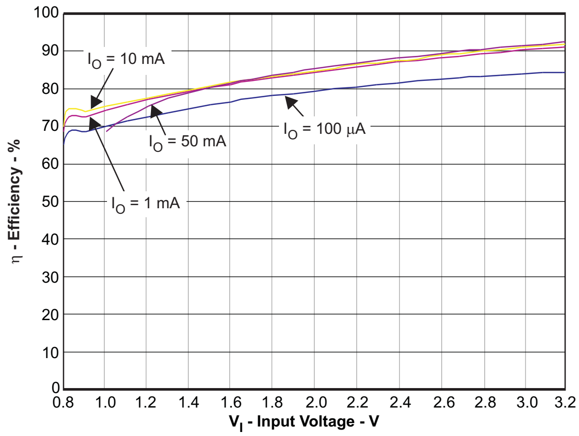

Figure 3.

NO LOAD APPLICATION INPUT CURRENT vs INPUT VOLTAGE

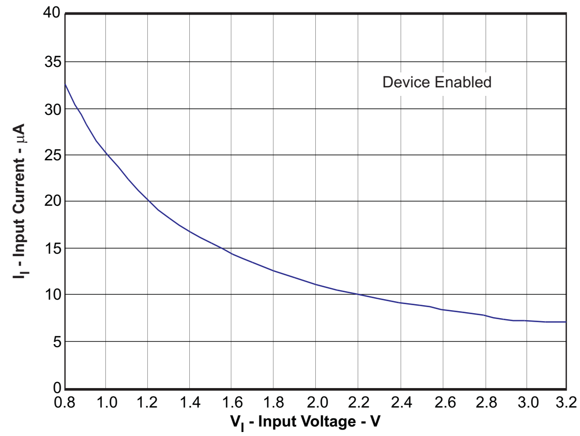

Figure 4.

OUTPUT VOLTAGE vs OUTPUT CURRENT

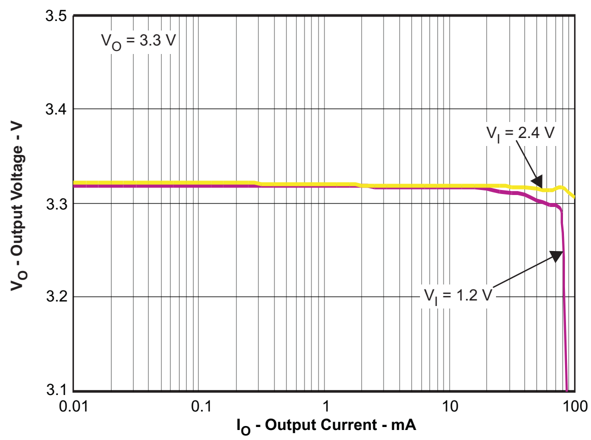

Figure 5.

OUTPUT VOLTAGE vs INPUT VOLTAGE, DEVICE DISABLED

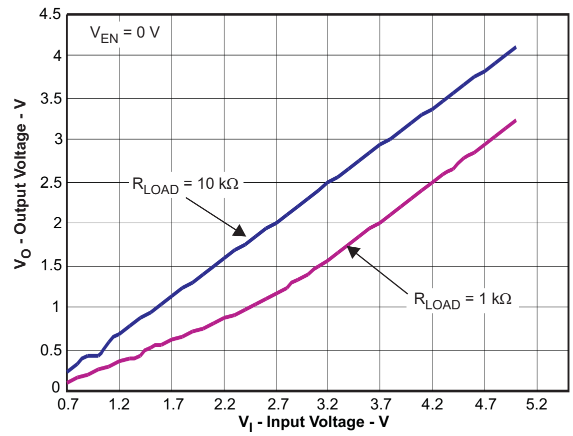

Figure 6.

OUTPUT VOLTAGE RIPPLE

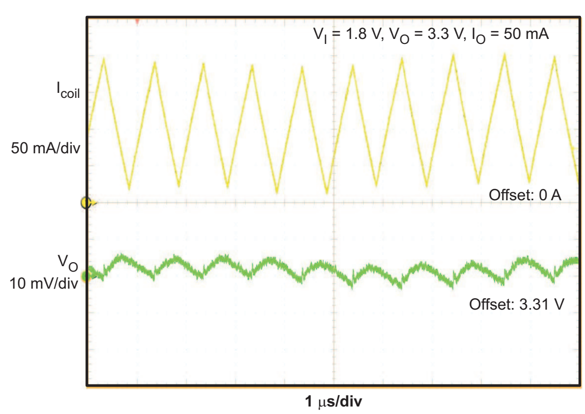

Figure 7.

LOAD TRANSIENT RESPONSE

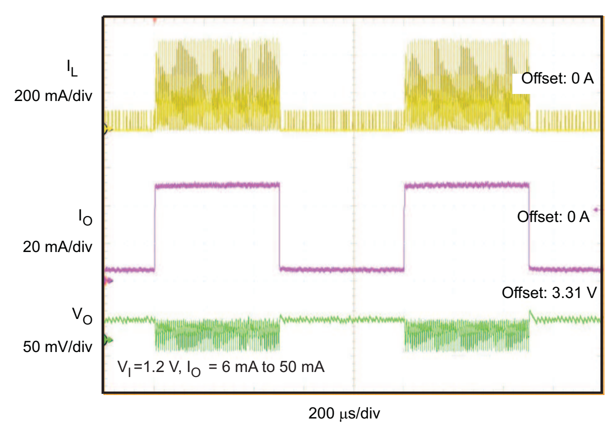

Figure 8.

LINE TRANSIENT RESPONSE

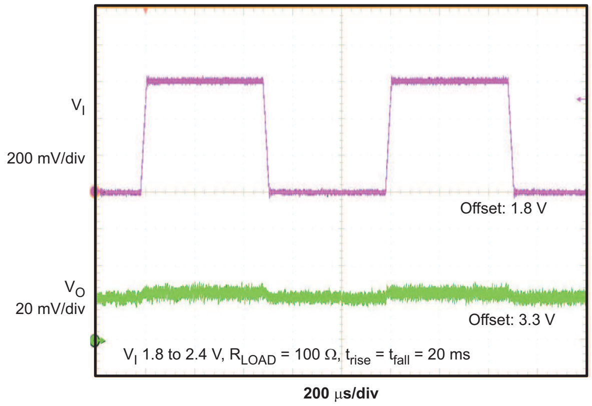

Figure 9.

OUTPUT VOLTAGE
vs
OUTPUT CURRENT AND INPUT VOLTAGE

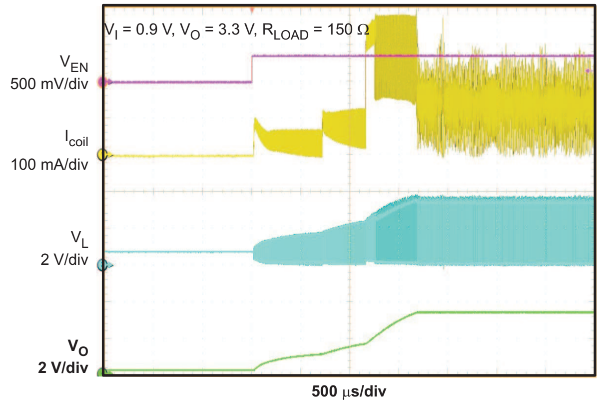

Figure 10.

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DETAILED DESCRIPTION

OPERATION

The TLV61225 is a high performance, high efficient family of switching boost converters. To achieve high efficiency the power stage is implemented as a synchronous boost topology. For the power switching two actively controlled low R_{DSon} power MOSFETs are used.

CONTROLLER CIRCUIT

The device is controlled by a hysteretic current mode controller. This controller regulates the output voltage by keeping the inductor ripple current constant in the range of 200 mA and adjusting the offset of this inductor current depending on the output load. In case the required average input current is lower than the average inductor current defined by this constant ripple the inductor current gets discontinuous to keep the efficiency high at low load conditions.

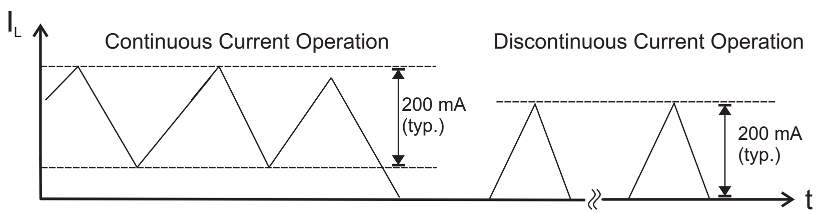

Figure 11. Hysteretic Current Operation

The output voltage V_{OUT} is monitored via the internal feedback network which is connected to the voltage error amplifier. To regulate the output voltage, the voltage error amplifier compares this feedback voltage to the internal voltage reference and adjusts the required offset of the inductor current accordingly.

Device Enable and Shutdown Mode

The device is enabled when EN is set high and shut down when EN is low. During shutdown, the converter stops switching and all internal control circuitry is turned off. In this case the input voltage is connected to the output through the back-gate diode of the rectifying MOSFET. This means that there always will be voltage at the output which can be as high as the input voltage or lower depending on the load.

Startup

After the EN pin is tied high, the device starts to operate. In case the input voltage is not high enough to supply the control circuit properly a startup oscillator starts to operate the switches. During this phase the switching frequency is controlled by the oscillator and the maximum switch current is limited. As soon as the device has built up the output voltage to about 1.8V, high enough for supplying the control circuit, the device switches to its normal hysteretic current mode operation. The startup time depends on input voltage, load current and output capacitance.

Operation at Output Overload

If in normal boost operation the inductor current reaches the internal switch current limit threshold the main switch is turned off to stop further increase of the input current.

In this case the output voltage will decrease since with limited input current it is not possible anymore to provide sufficient power to the output to maintain the programmed output voltage.

If the output voltage drops below the input voltage the backgate diode of the rectifying switch gets forward biased and current starts flowing through it. This diode cannot be turned off, so the current finally is only limited by the remaining DC resistances. As soon as the output load has decreased to a value the converter can supply, the converter resumes normal operation providing the set output voltage.

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Undervoltage Lockout

An implemented undervoltage lockout function (UVLO) stops the operation of the converter if the input voltage drops below the typical undervoltage lockout threshold. This function is implemented in order to prevent malfunctioning of the converter and protect batteries against deep discharge.

Overvoltage Protection

If, for any reason, the output voltage is not fed back properly to the input of the voltage amplifier, control of the output voltage will not work anymore. Therefore overvoltage protection is implemented to avoid the output voltage exceeding critical values for the device and possibly for the system it is supplying. For this protection the TLV61225 output voltage is also monitored internally. In case it reaches the internally programmed threshold the voltage amplifier regulates the output voltage to this value.

Overtemperature Protection

The device has a built-in temperature sensor which monitors the internal IC junction temperature. If the temperature exceeds the programmed threshold (see electrical characteristics table), the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. To prevent unstable operation close to the region of overtemperature threshold, a built-in hysteresis is implemented.

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APPLICATION INFORMATION

DESIGN PROCEDURE

The TLV61225 DC/DC converter is intended for systems powered by a single or dual cell Alkaline or NiMH battery with a typical terminal voltage between 0.7 V and 3.3 V. Additionally, any other voltage source with a typical output voltage between 0.7 V and 3.3 V can be used with the TLV61225.

Programming the Output Voltage

At fixed voltage versions, the output voltage is programmed by an internal resistor divider. The FB pin is used to sense the output voltage. To configure the devices properly, the FB pin needs to be connected directly to VOUT.

Inductor Selection

To make sure that the TLV61225 devices can operate, a suitable inductor must be connected between pin VIN and pin L. Inductor values of 4.7 µH show good performance over the whole input and output voltage range.

Due to the fixed inductor current ripple control the switching frequency is defined by the inductor value. For a given switching frequency, input and output voltage the required inductance can be estimated using Equation 1.

$$L = \frac{1}{f \times 200\ \text{mA}} \times \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT}} \quad (1)$$

Using inductor values higher than 4.7 µH can improve efficiency since higher values cause lower switching frequency and less switching losses. Using inductor values below 2.2 µH is not recommended.

To ensure reliable operation of the TLV61225 under all load conditons it is recommended to use indutors with a current rating of 400mA or higher. This will cover normal operation including current peaks during line and load transients.

The following inductor series from different suppliers have been used with the TLV61225 converter:

Table 2. List of Inductors

VENDOR	INDUCTOR SERIES
Coilcraft	EPL3015
	EPL2010
Murata	LQH3NP
Tajo Yuden	NR3015
Wurth Elektronik	WE-TPC Typ S

Capacitor Selection

Input Capacitor

At least a 10-µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor placed as close as possible to the VIN and GND pins of the IC is recommended.

Output Capacitor

For the output capacitor C_2 , it is recommended to use small ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC. There are no minimum output capacitor ESR requirements for maintaining control loop stability. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, the use of a small ceramic capacitor with an capacitance value in the range of 2.2µF in parallel to the large capacitor is recommended. This small capacitor should be placed as close as possible to the VOUT and GND pins of the IC.

A minimum capacitance value of 4.7 µF should be used, 10 µF are recommended. To calculate the required output capacitance in case an inductor with a value higher than 4.7 µH has been selected Equation 2 can be used.

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$$C_2 \geq \frac{L}{2} \times \frac{\mu F}{\mu H} \tag{2}$$

Layout Considerations

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitor, as well as the inductor should be placed as close as possible to the IC.

To lay out the ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current. Assure that the ground traces are connected close to the device GND pin.

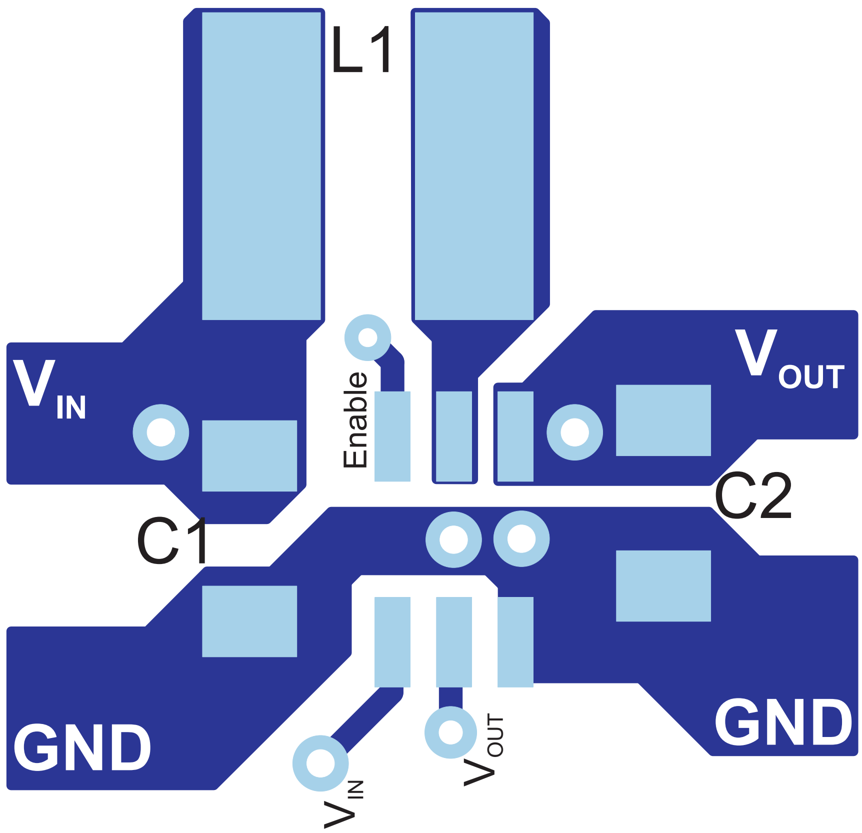

Figure 12. PCB Layout Suggestion

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power-dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

For more details on how to use the thermal parameters in the dissipation ratings table please check the Thermal Characteristics Application Note (SZZA017) and the IC Package Thermal Metrics Application Note (SPRA953).

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLV61225DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TLV61225DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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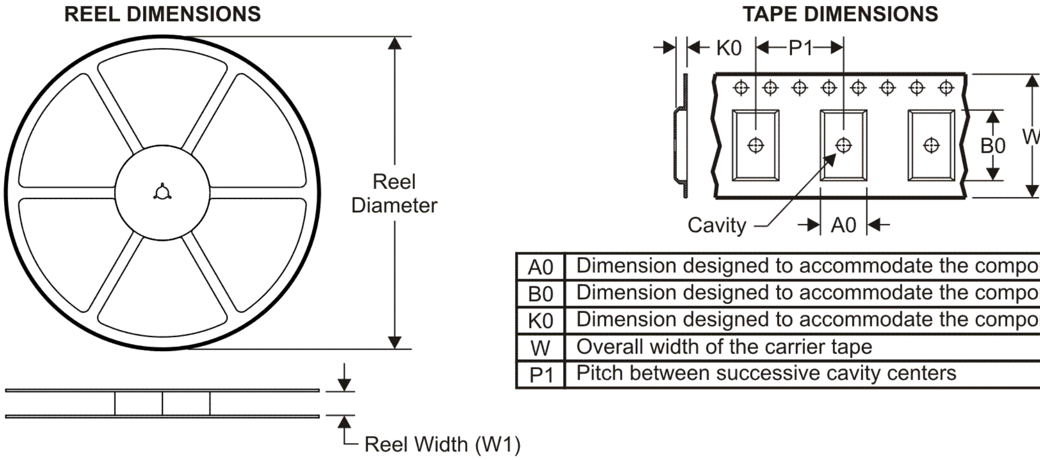
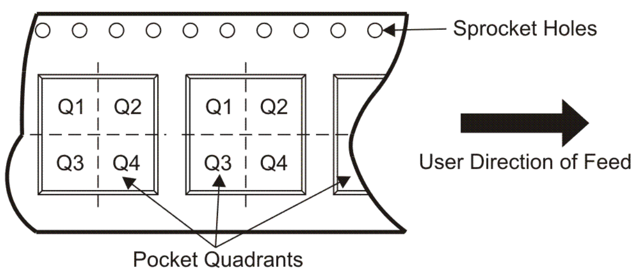
TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

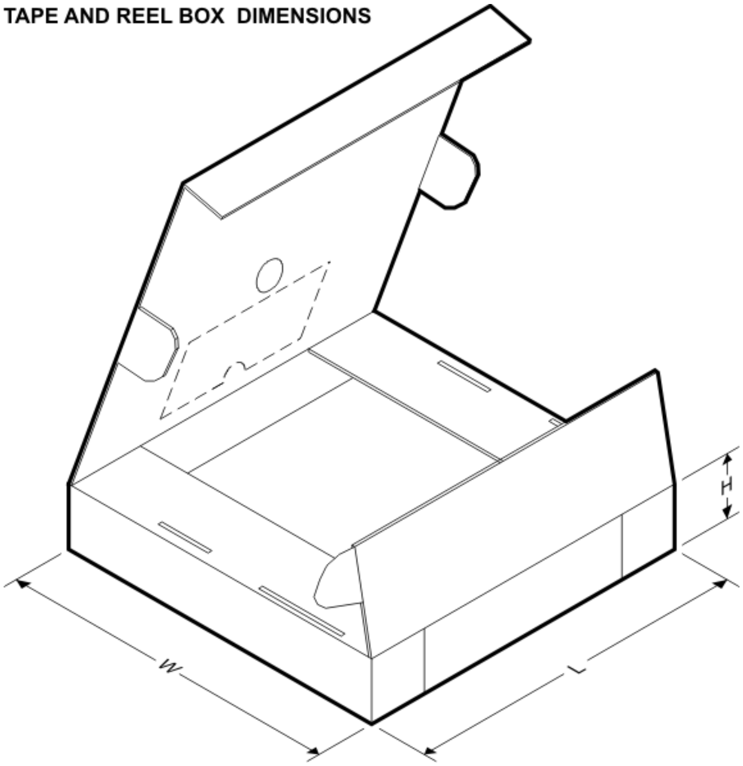
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV61225DCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV61225DCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3

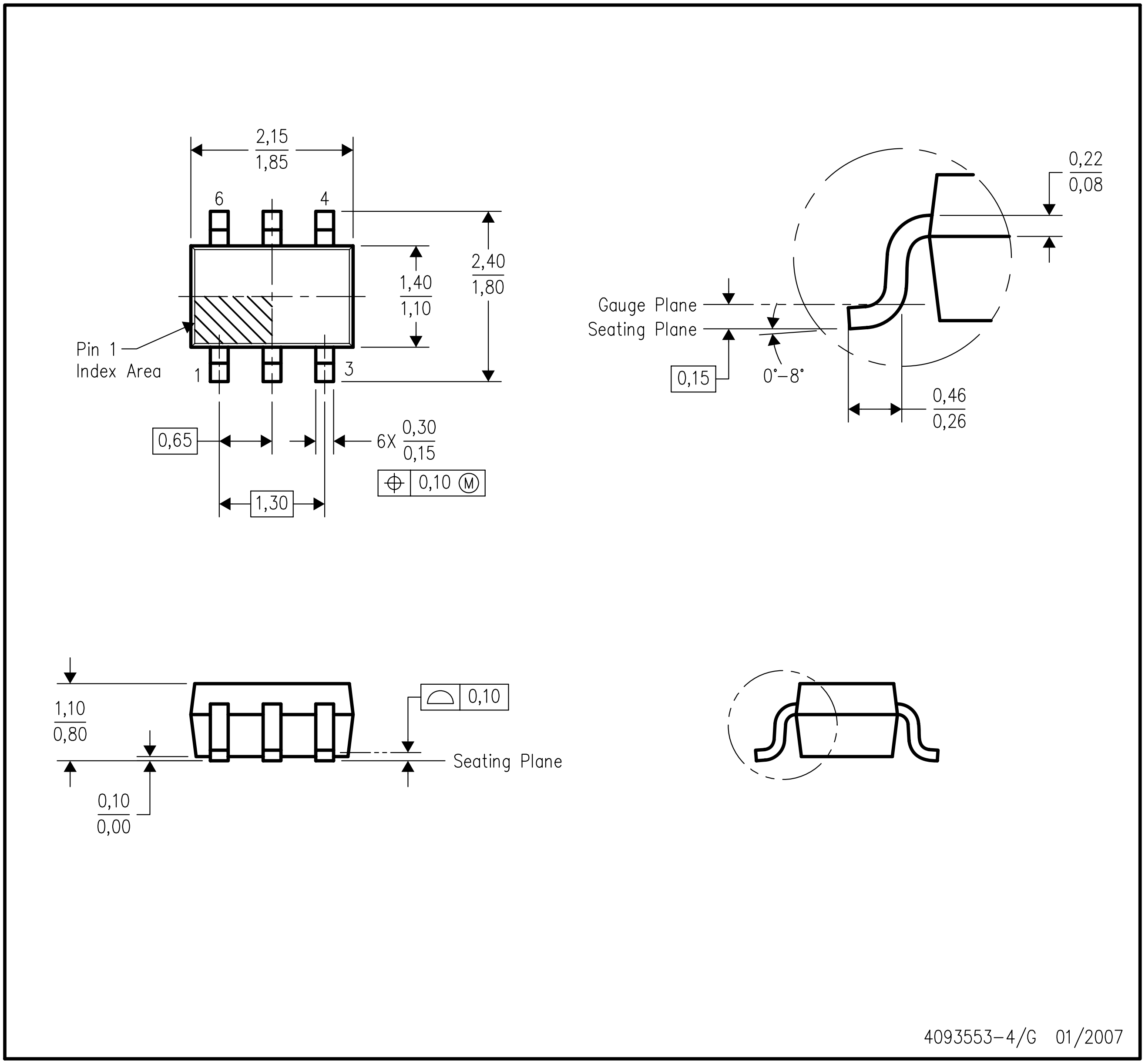
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

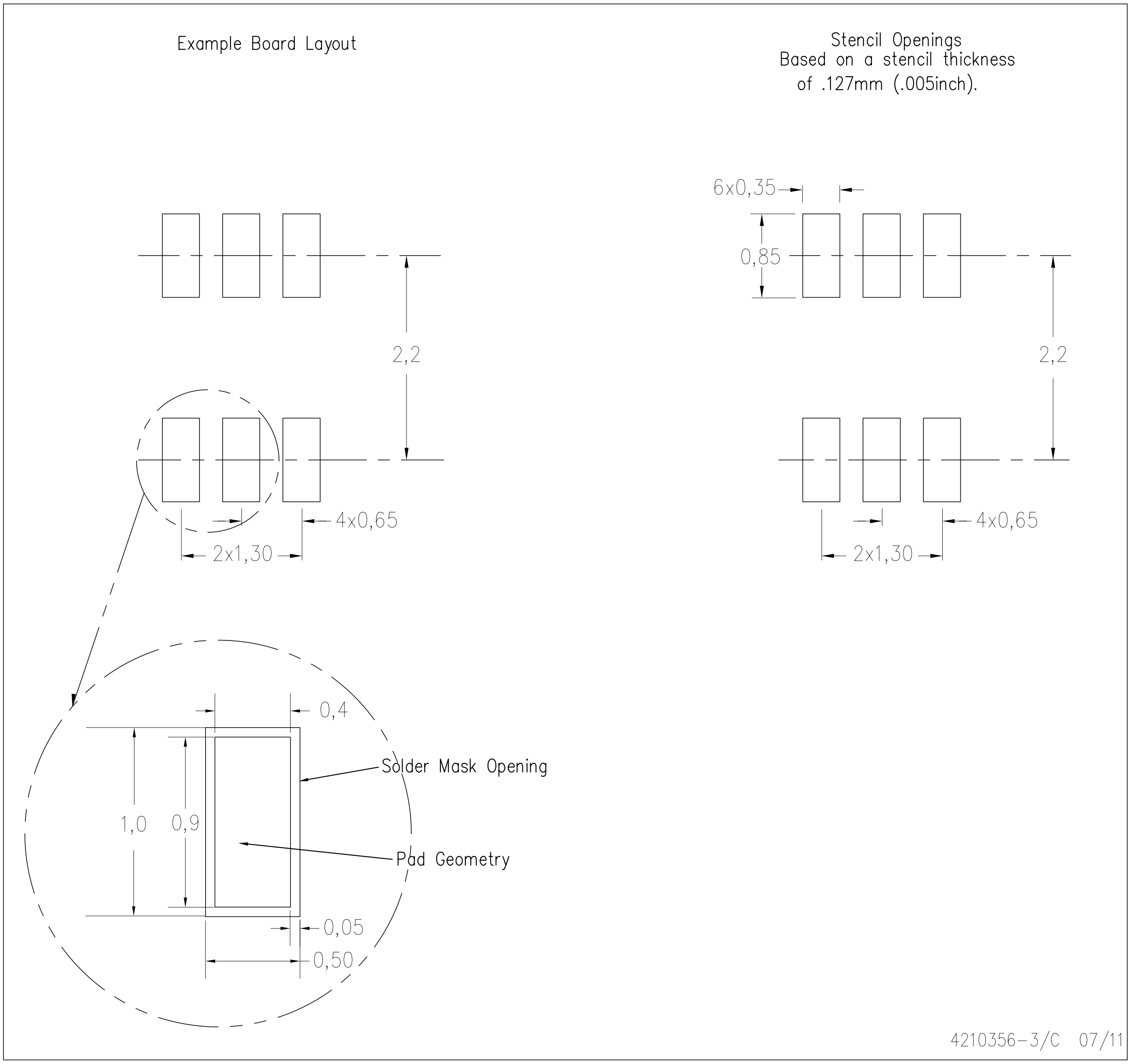
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV61225DCKR	SC70	DCK	6	3000	203.0	203.0	35.0
TLV61225DCKT	SC70	DCK	6	250	203.0	203.0	35.0

DCK (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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