3A High Efficient Synchronous Step Down Converter with DCS™ Control

Check for Samples: TLV62090

FEATURES

- 2.5 V to 5.5 V Input Voltage Range
- DCS™ Control
- 95% Converter Efficiency
- Power Save Mode
- 20 µA Operating Quiescent Current
- 100% Duty Cycle for Lowest Dropout
- 1.4 MHz Typical Switching Frequency
- 0.8 V to V_{IN} Adjustable Output Voltage
- Output Discharge Function
- Adjustable Softstart
- Two Level Short Circuit Protection
- Output Voltage Tracking
- Wide Output Capacitance Selection
- Available in 3x3mm 16 Pin QFN Package

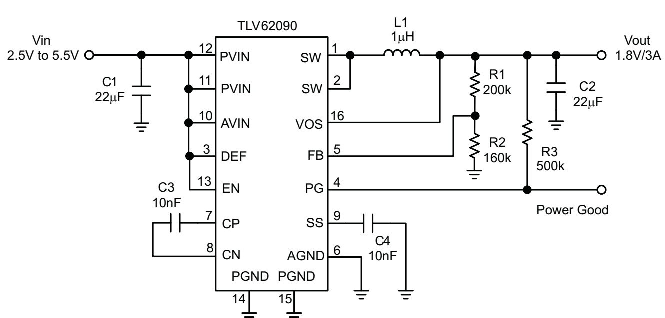
APPLICATIONS

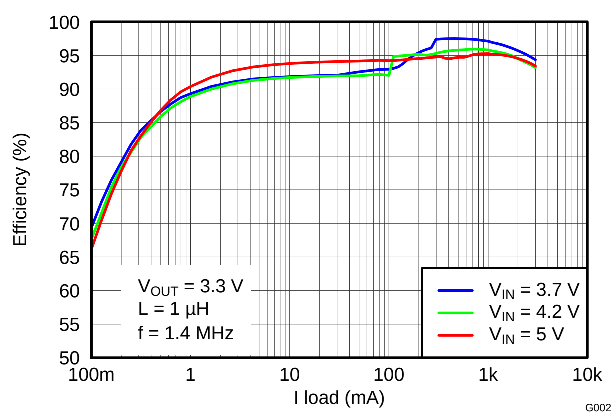
- Distributed Power Supplies
- Notebook, Netbook Computers
- Hard Disk Drivers
- Processor Supply
- Battery Powered Applications

DESCRIPTION

The TLV62090 device is a high frequency synchronous step down converter optimized for small solution size, high efficiency and suitable for battery powered applications. To maximize efficiency, the converter operates in PWM mode with a nominal switching frequency of 1.4 MHz and automatically enters Power Save Mode operation at light load currents. When used in distributed power supplies and point of load regulation, the device allows voltage tracking to other voltage rails and tolerates output capacitors ranging from 10 µF up to 150 µF and beyond. Using the DCS™ Control topology the device achieves excellent load transient performance and accurate output voltage regulation.

The output voltage start-up ramp is controlled by the softstart pin, which allows operation as either a standalone power supply or in tracking configurations. Power sequencing is also possible by configuring the Enable and Power Good pins. In Power Save Mode, the device operates at typically 20 µA quiescent current. Power Save Mode is entered automatically and seamlessly maintaining high efficiency over the entire load current range.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	ORDERING	PACKAGE	PACKAGE MARKING
-40°C to 85°C	TLV62090	RGT	SBV

(1) For detailed ordering information please see the PACKAGE OPTION ADDENDUM section at the end of the datasheet.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Voltage range	PVIN, AVIN, FB, SS, EN, DEF, VOS(2)	–0.3	7	V
	SW, PG	–0.3	V_{IN}+0.3	V
Power Good sink current	PG		1	mA
ESD rating	Human Body Model		2	kV
	Charged Device Model		500	V
Continuous total power dissipation		See the Thermal Table		
Operating junction temperature range, T_J		–40	150	°C
Operating ambient temperature range, T_A		–40	85	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS62090 QFN (16 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	47	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	60	
θ_{JB}	Junction-to-board thermal resistance	20	
ψ_{JT}	Junction-to-top characterization parameter	1.5	
ψ_{JB}	Junction-to-board characterization parameter	20	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	5.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS(1)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range V_{IN}	2.5		5.5	V
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) See the application section for further information

ELECTRICAL CHARACTERISTICS

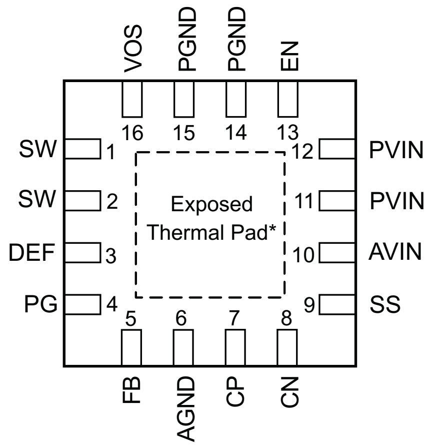
V_{IN} = 3.6V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.5		5.5	V
I_{QIN}	Quiescent current	Not switching, FB = FB +5 %, Into PVIN and AVIN		20		µA
I_{sd}	Shutdown current	Into PVIN and AVIN		0.6	5	µA
UVLO	Undervoltage lockout threshold	V_{IN} falling	2.1	2.2	2.3	V
	Undervoltage lockout hysteresis			200		mV
	Thermal shutdown	Temperature rising		150		ºC
	Thermal shutdown hysteresis			20		ºC
Control SIGNAL EN						
V_H	High level input voltage	V_{IN} = 2.5 V to 6 V	1			V
V_L	Low level input voltage	V_{IN} = 2.5 V to 6 V			0.4	V
I_{lkg}	Input leakage current	EN = GND or V_{IN}		10	100	nA
R_{PD}	Pull down resistance			400		kΩ
Softstart						
I_{SS}	Softstart current		6.3	7.5	8.7	µA
POWER GOOD						
V_{th}	Power good threshold	Output voltage rising		95%		
		Output voltage falling		90%		
V_L	Low level voltage	$I_{(sink)}$ = 1mA			0.4	V
I_{PG}	PG sinking current				1	mA
I_{lkg}	Leakage current	V_{PG} = 3.6V		10	100	nA
POWER SWITCH						
$R_{DS(on)}$	High side FET on-resistance	I_{SW} = 500 mA		50		mΩ
	Low side FET on-resistance	I_{SW} = 500 mA		40		mΩ
I_{LIM}	High side FET switch current limit		3.7	4.6	5.5	A
f_s	Switching frequency	I_{OUT} = 3 A		1.4		MHz
OUTPUT						
V_s	Output voltage range		0.8		V_{IN}	V
R_{od}	Output discharge resistor	EN = GND, V_{OUT} = 1.8 V		200		Ω
V_{FB}	Feedback regulation voltage			0.8		V
V_{FB}	Feedback voltage accuracy(1) (2)	V_{IN} ≥ V_{OUT} + 1 V, TPS62090 adjustable output version				
		I_{OUT} = 1 A, PWM mode	-1.4%		+1.4%	
		I_{OUT} = 0 mA, V_{OUT} ≥ 1.2 V, PFM mode	-1.4%		+3%	
		I_{OUT} = 0 mA, V_{OUT} < 1.2V, PFM mode	-1.4%		+3.7%	
I_{FB}	Feedback input bias current	V_{FB} = 0.8V, TPS62090 adjustable output version		10	100	nA
	Line regulation	V_{OUT} = 1.8 V, PWM operation		0.016		%/V
	Load regulation	V_{OUT} = 1.8 V, PWM operation		0.04		%/A

(1) For output voltages < 1.2 V, use a 2 x 22 µF output capacitance to achieve +3% output voltage accuracy in PFM mode.
(2) Conditions: L = 1 µH, C_{OUT} = 22 µF. For more information, see the Power Save Mode Operation section of this data sheet.

DEVICE INFORMATION

16 PIN 3x3mm QFN
TOP VIEW



NOTE: *The exposed Thermal Pad is connected to AGND.

PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
SW	1, 2	I	Switch pin of the power stage.
DEF	3	I	This pin is used for internal logic and needs to be pulled high. This pin should not be left floating.
PG	4	O	Power good open drain output. This pin is high impedance if the output voltage is within regulation. This pin is pulled low if the output is below its nominal value. The pull up resistor can not be connected to any voltage higher than the input voltage of the device.
FB	5		Feedback pin of the device.
AGND	6		Analog ground.
CP	7		Internal charge pump flying capacitor. Connect a 10 nF capacitor between CP and CN.
CN	8		Internal charge pump flying capacitor. Connect a 10 nF capacitor between CP and CN.
SS	9	I	Soft-start control pin. A capacitor is connected to this pin and sets the softstart time. Leaving this pin floating sets the minimum start-up time.
AVIN	10		Bias supply input voltage pin.
PVIN	11,12		Power supply input voltage pin.
EN	13		Device enable. To enable the device this pin needs to be pulled high. Pulling this pin low disables the device. This pin has an active pull down resistor of typically 400 kΩ.
PGND	14,15		Power ground connection.
VOS	16		Output voltage sense pin. This pin needs to be connected to the output voltage.
Thermal Pad			The exposed thermal pad is connected to AGND.

FUNCTIONAL BLOCK DIAGRAM

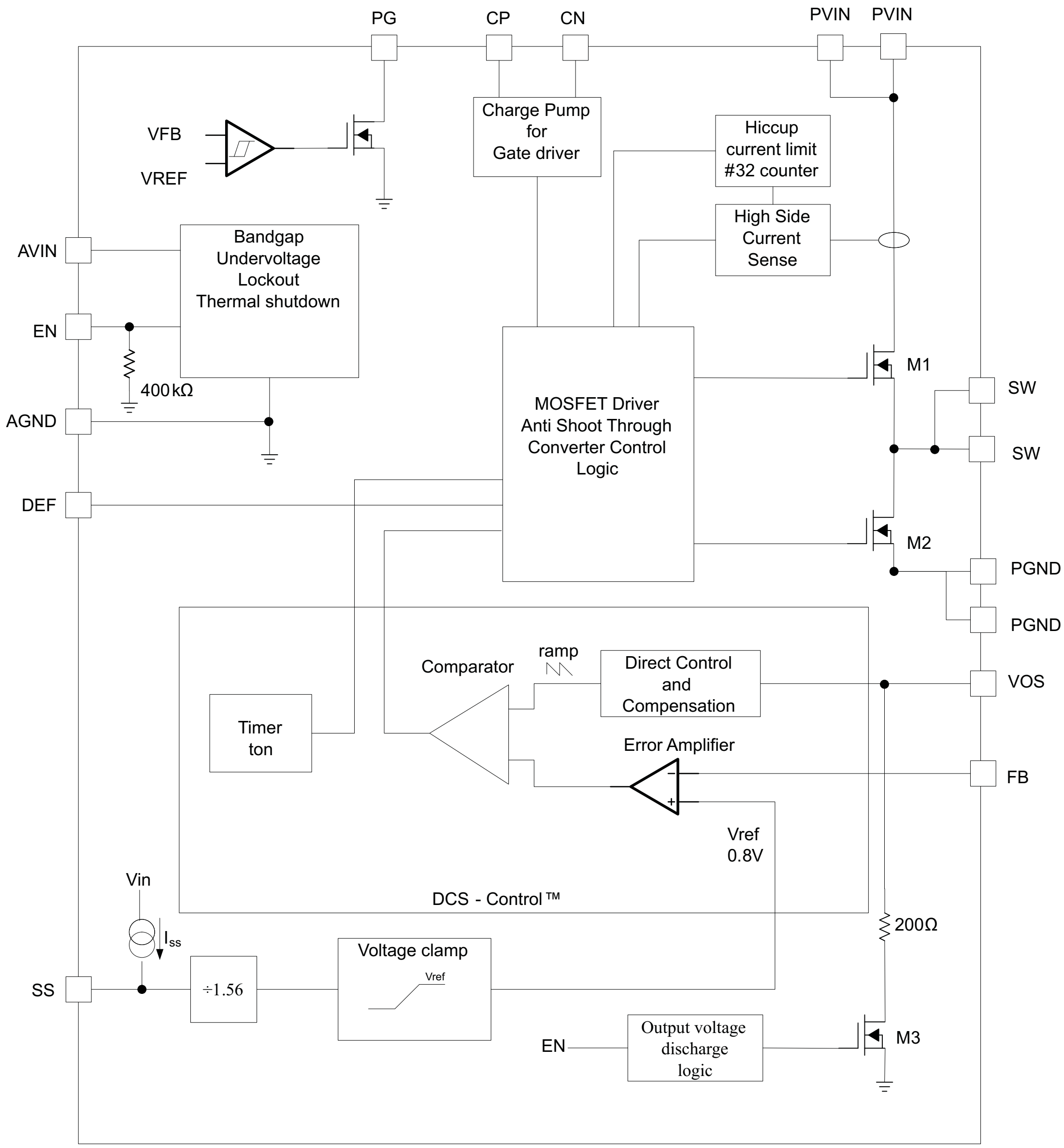


Table 1. List of components

REFERENCE	DESCRIPTION	MANUFACTURER
TLV62090	High efficient step down converter	Texas Instruments
L1	Inductor: 1uH	Coilcraft XFL4020-102
C1	Ceramic capacitor: 22uF	(6.3V, X5R, 0805)
C2	Ceramic capacitor: 22uF	(6.3V, X5R, 0805)
C3, C4	Ceramic capacitor	Standard
R1, R2, R3	Resistor	Standard

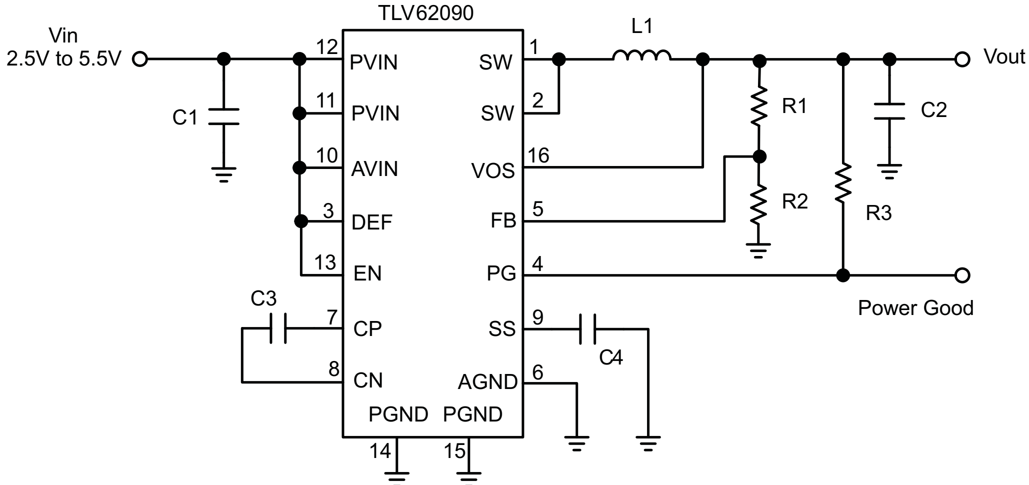


Figure 1. Parametric Measurement Circuit

TYPICAL CHARACTERISTICS

		FIGURE
Efficiency	vs load current (V_O = 3.3 V)	Figure 2
Efficiency	vs load current (V_O = 1.8 V)	Figure 3
Efficiency	vs load current (V_O = 1.05 V)	Figure 4
Output voltage	vs load current (V_O = 1.8 V)	Figure 5
High Side FET on-resistance	vs input voltage	Figure 6
Switching frequency	vs load current (V_O = 1. 8 V)	Figure 7
Switching frequency	vs input voltage (V_O = 1.8 V)	Figure 8
Quiescent current	vs input voltage (V_O = 1.8 V)	Figure 9
PWM operation	V_O = 1.8 V	Figure 10
PFM operation	V_O = 1.8 V	Figure 11
Load sweep	V_O = 1.8 V	Figure 12
Start-up	V_O = 1.8 V, C_{SS} = 10 nF	Figure 13
Shutdown	V_O = 1.8 V	Figure 14
Hiccup short circuit protection	V_O = 1.8 V	Figure 15
Hiccup Short circuit protection	V_O = 1.8 V, recovery after short circuit	Figure 16
Load transient response	V_O = 1.8 V, 300 mA to 2.5 A	Figure 17
Load transient response	V_O = 1.8 V, 300 mA to 2.5 A	Figure 18
Load transient response	V_O = 1.8 V, 20 mA to 1 A	Figure 19

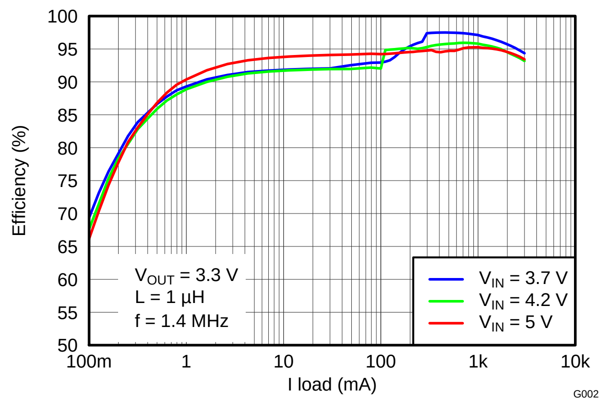


Figure 2. Efficiency vs Load Current

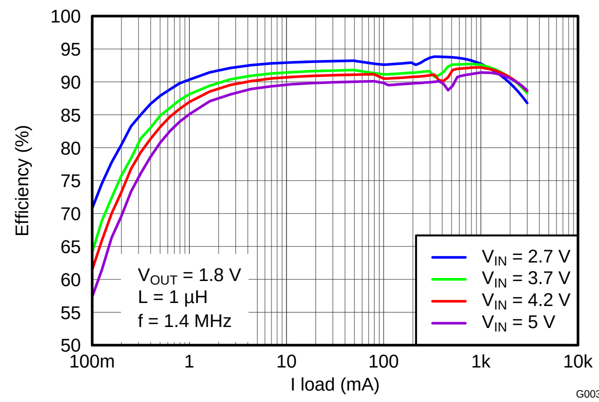


Figure 3. Efficiency vs Load Current

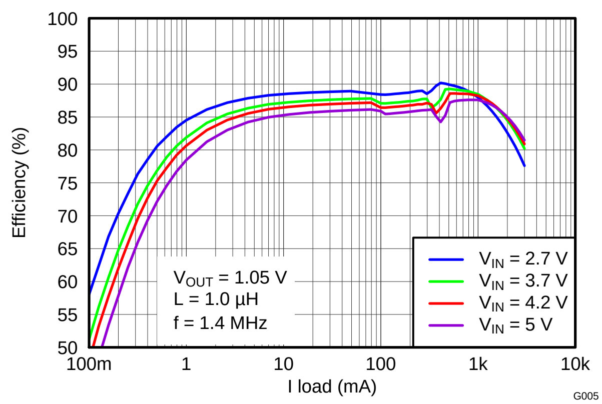


Figure 4. Efficiency vs Load Current

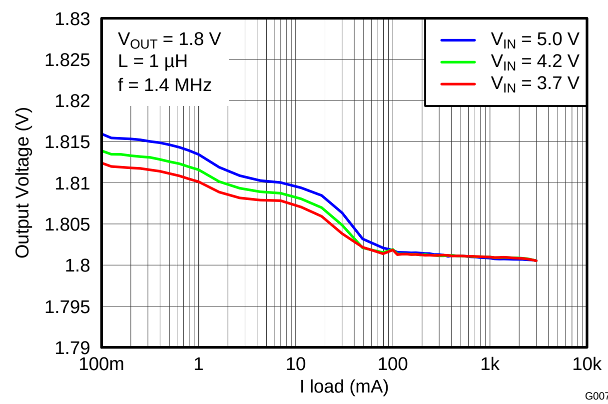


Figure 5. Output Voltage vs Load Current

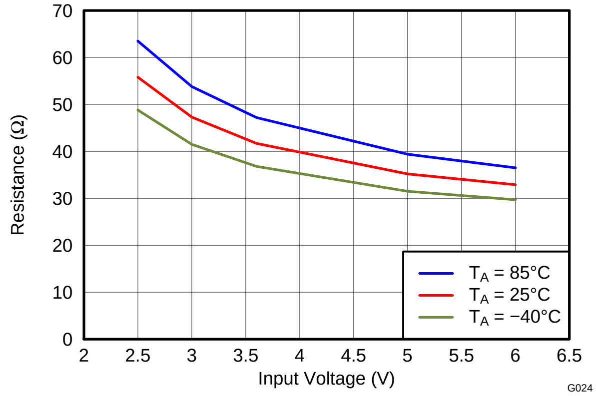


Figure 6. High Side FET On-Resistance vs Input Voltage

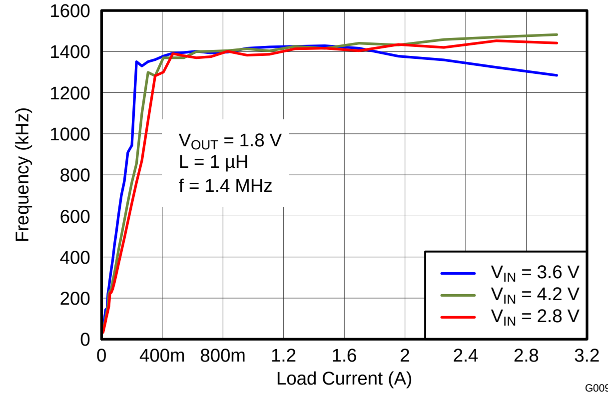


Figure 7. Switching Frequency vs Load Current

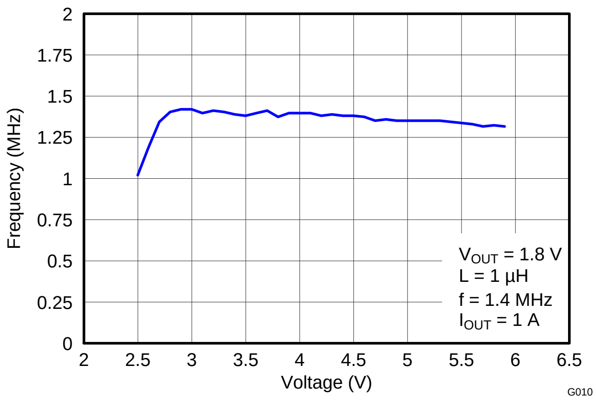


Figure 8. Switching Frequency vs Input Voltage

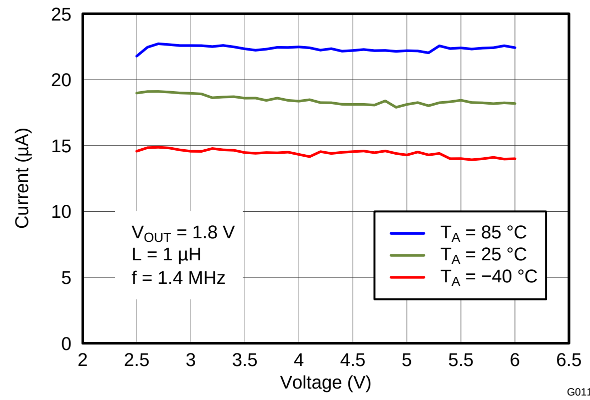


Figure 9. Quiescent Current vs Input Voltage

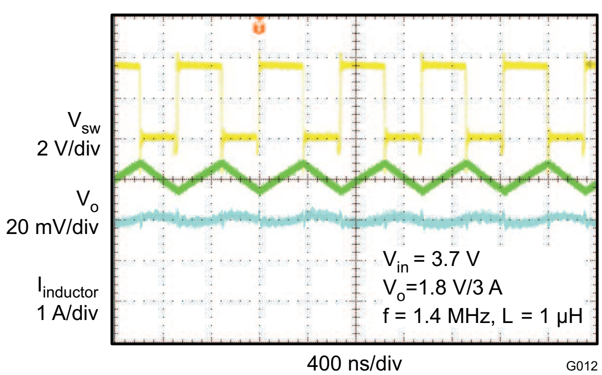


Figure 10. PWM Operation

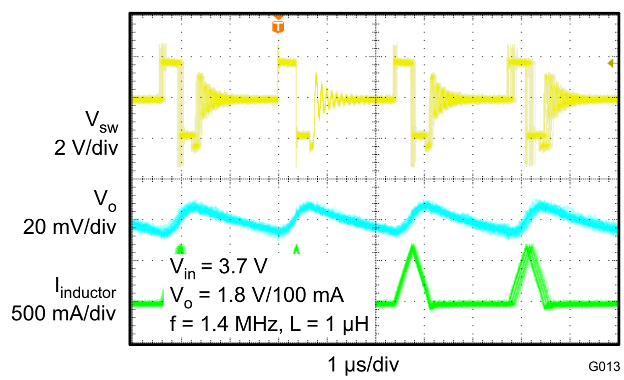


Figure 11. PFM Operation

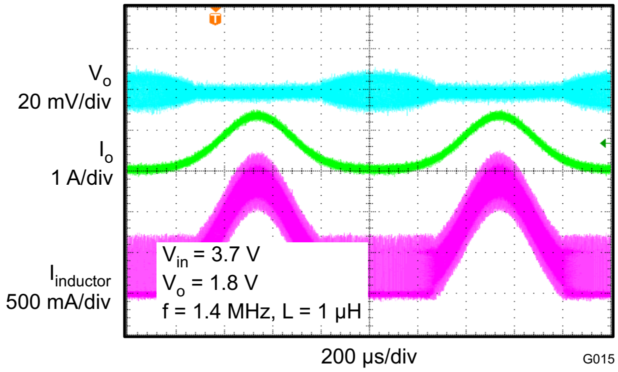


Figure 12. Load Sweep

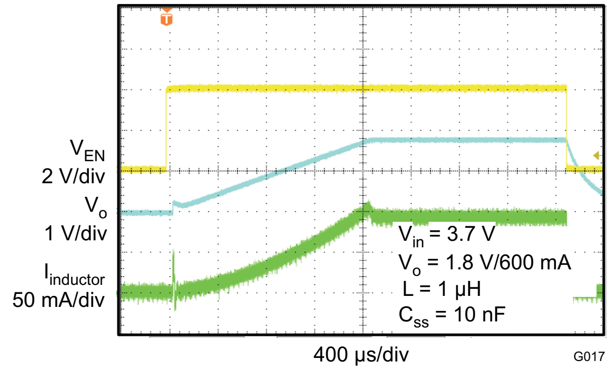


Figure 13. Start-Up

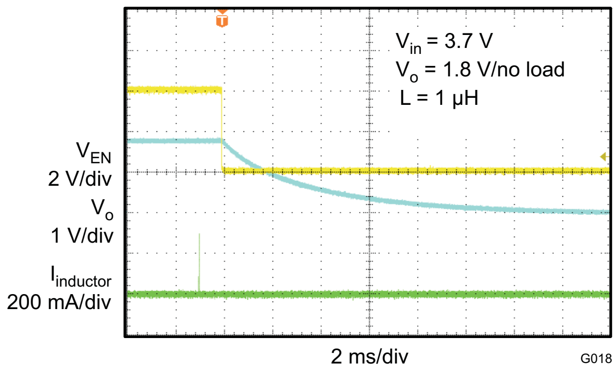


Figure 14. Shutdown

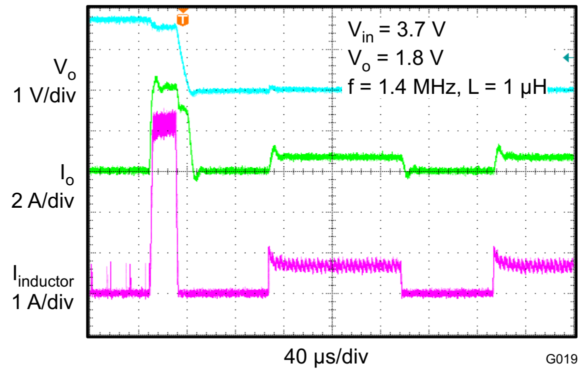


Figure 15. Hiccup Short Circuit Protection

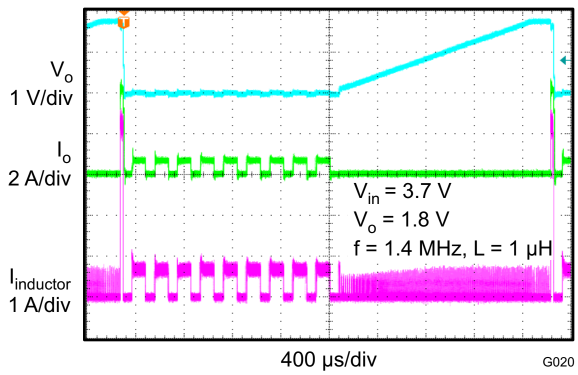


Figure 16. Hiccup Short Circuit Protection

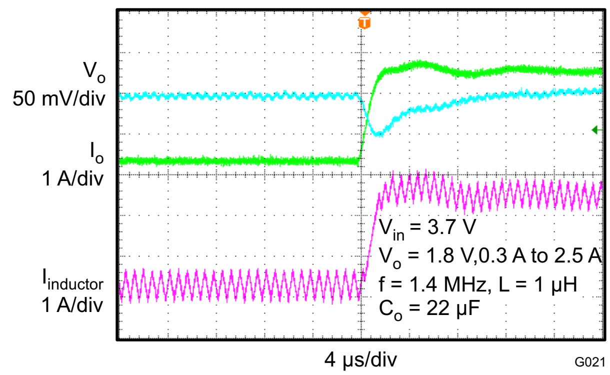


Figure 17. Load Transient Response

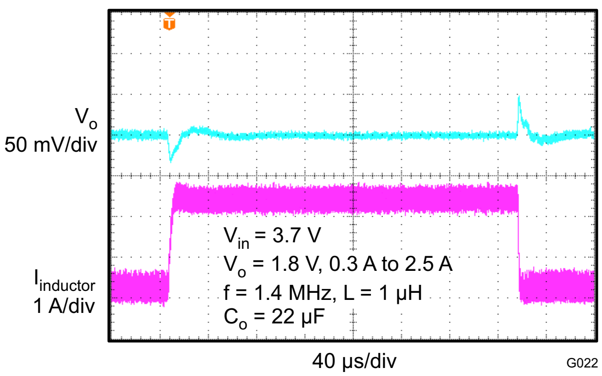


Figure 18. Load Transient Response

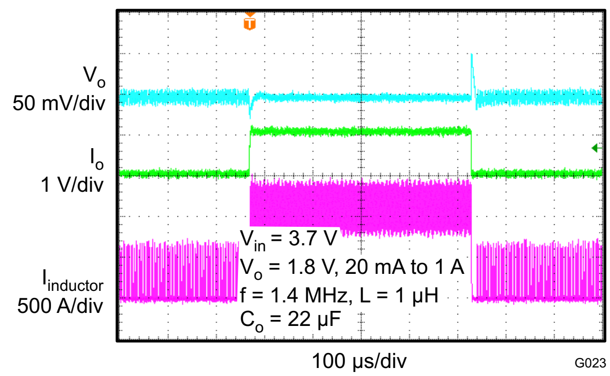


Figure 19. Load Transient Response

DETAILED DESCRIPTION

Operation

The TLV62090 synchronous switched mode converter is based on DCS™ Control (Direct Control with Seamless transition into Power Save Mode). This is an advanced regulation topology that combines the advantages of hysteretic and voltage mode control.

The DCS™ Control topology operates in PWM (Pulse Width Modulation) mode for medium to heavy load conditions and in Power Save Mode at light load currents. In PWM, the converter operates with its nominal switching frequency of 1.4 MHz having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters Power Save Mode, reducing the switching frequency and minimizing the IC quiescent current to achieve high efficiency over the entire load current range. DCS™ Control supports both operation modes (PWM and PFM) using a single building block having a seamless transition from PWM to Power Save Mode without effects on the output voltage. The TLV62090 offers excellent DC voltage regulation and load transient regulation, combined with low output voltage ripple, minimizing interference with RF circuits.

PWM Operation

At medium to heavy load currents, the device operates with pulse width modulation (PWM) at a nominal switching frequency of 1.4 MHz. As the load current decreases, the converter enters the Power Save Mode operation reducing its switching frequency. The device enters Power Save Mode at the boundary to discontinuous conduction mode (DCM).

Power Save Mode Operation

As the load current decreases, the converter enters Power Save Mode operation. During Power Save Mode the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current while maintaining high efficiency. The Power Save Mode is based on a fixed on-time architecture following Equation 1.

$$ton = \frac{V_{OUT}}{V_{IN}} \times 360ns \times 2$$

$$f = \frac{2 \times I_{OUT}}{ton^2 \left(1 + \frac{V_{IN} - V_{OUT}}{V_{OUT}}\right) \times \frac{V_{IN} - V_{OUT}}{L}} \quad (1)$$

In Power Save Mode the output voltage rises slightly above the nominal output voltage in PWM mode, as shown in Figure 5. This effect can be reduced by increasing the output capacitance or the inductor value. This effect can also be reduced by programming the output voltage of the TLV62090 lower than the target value. As an example, if the target output voltage is 3.3 V, then the TLV62090 can be programmed to 3.3V - 0.8%. As a result the output voltage accuracy is now -2.2% to +2.2% instead of -1.4% to 3%. The output voltage accuracy in PFM operation is reflected in the electrical specification table and given for a 22 µF output capacitance.

Low Dropout Operation (100% Duty Cycle)

The device offers low input to output voltage difference by entering 100% duty cycle mode. In this mode the high side MOSFET switch is constantly turned on. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage where the output voltage falls below its nominal regulation value is given by:

$$V_{IN(min)} = V_{OUT(max)} + I_{OUT} \times (R_{DS(on)} + R_L) \quad (2)$$

Where

$R_{DS(on)}$ = High side FET on-resistance

R_L = DC resistance of the inductor

$V_{OUT(max)}$ = nominal output voltage plus maximum output voltage tolerance

Softstart (SS)

To minimize inrush current during start up, the device has an adjustable softstart depending on the capacitor value connected to the SS pin. The device charges the softstart capacitor with a constant current of typically 7.5 µA. The feedback voltage follows this voltage with a fraction of 1.56 until the internal reference voltage of 0.8 V is reached. The softstart operation is completed once the voltage at the softstart capacitor has reached typically 1.25 V. The soft-start time can be calculated using Equation 3. The larger the softstart capacitor the longer the softstart time. The relation between softstart voltage and feedback voltage can be estimated using Equation 4.

$$t_{SS} = C_{SS} \times \frac{1.25V}{7.5\mu A} \quad (3)$$

$$V_{FB} = \frac{V_{SS}}{1.56} \quad (4)$$

This is also the case for the fixed output voltage option having the internal regulation voltage. Leaving the softstart pin floating sets the minimum start-up time.

Start-up Tracking (SS)

The softstart pin can also be used to implement output voltage tracking with other supply rails. The internal reference voltage follows the voltage at the softstart pin with a fraction of 1.56 until the internal reference voltage of 0.8 V is reached. The softstart pin can be used to implement output voltage tracking as shown in Figure 20.

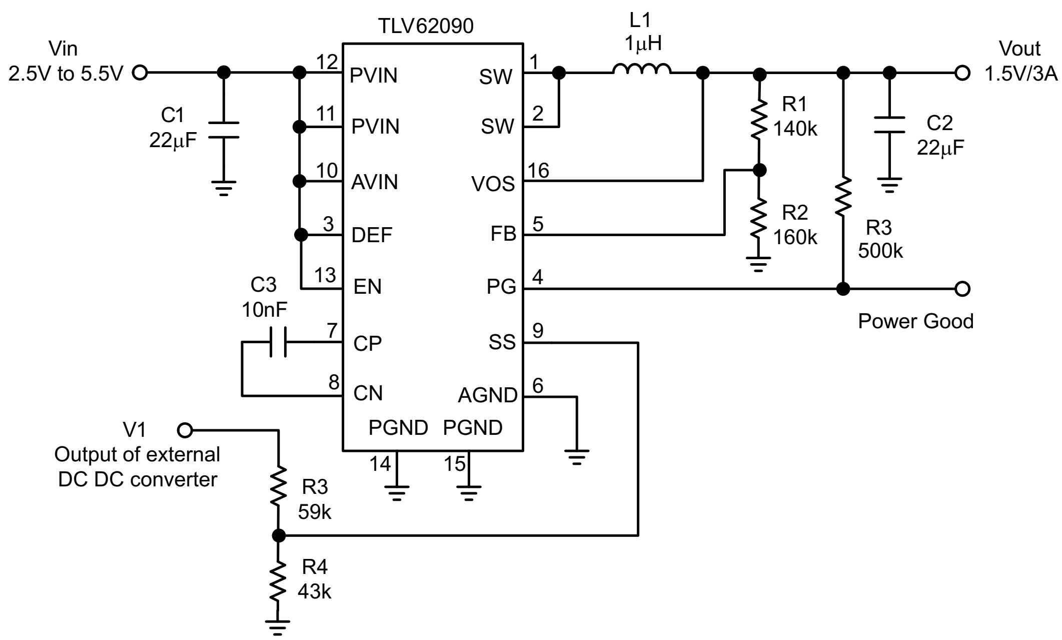


Figure 20. Output Voltage Tracking

In Figure 20, the output V2 tracks the voltage applied to V1. The voltage tracks simultaneously when following conditions are met:

$$\frac{R3}{R4} = \frac{R1}{R2} \times 1.56 \quad (5)$$

As the fraction of R3/R4 becomes larger the voltage V1 ramps up faster than V2, and if it gets smaller then the ramp is slower than V2. R4 needs to be determined first using Equation 6.

$$R4 = \frac{1.25V}{300\mu A} \quad (6)$$

In the calculation of R4, 300 µA current is used to achieve sufficient accuracy by taking into account the typical 7.5 µA soft-start current. After determining R4, R3 can be calculated using Equation 5.

Short Circuit Protection (Hiccup-Mode)

The device is protected against hard short circuits to GND and over-current events. This is implemented by a two level short circuit protection. During start-up and when the output is shorted to GND the switch current limit is reduced to 1/3 of its typical current limit of 4.6 A. Once the output voltage exceeds typically 0.6 V the current limit is released to its nominal value. The full current limit is implemented as a hiccup current limit. Once the internal current limits is triggered 32 times the device stops switching and starts a new start-up sequence after a typical delay time of 66 µS passed by. The device will go through these cycles until the high current condition is released.

Output Discharge Function

To make sure the device starts up under defined conditions, the output gets discharged via the VOS pin with a typical discharge resistor of 200 Ω whenever the device shuts down. This happens when the device is disabled or if thermal shutdown, undervoltage lockout or short circuit hiccup-mode is triggered.

Power Good Output (PG)

The power good output is low when the output voltage is below its nominal value. The power good will become high impedance once the output is within 5% of regulation. The PG pin is an open drain output and is specified to typically sink up to 1 mA. This output requires a pull-up resistor to be monitored properly. The pull-up resistor cannot be connected to any voltage higher than the input voltage of the device.

Undervoltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages, an undervoltage lockout is included. UVLO shuts down the device at input voltages lower than typically 2.2 V with a 200 mV hysteresis.

Thermal Shutdown

The device goes into thermal shutdown once the junction temperature exceeds typically 150°C with a 20°C hysteresis.

APPLICATION INFORMATION

DESIGN PROCEDURE

The first step is the selection of the output filter components. To simplify this process, and Table 2 outline possible inductor and capacitor value combinations.

Table 2. Output Filter Selection

INDUCTOR VALUE [µH][1]	OUTPUT CAPACITOR VALUE [µF][2]				
	10	22	47	100	150
0.47		√	√	√	√
1.0	√	√[3]	√	√	√
2.2	√	√	√	√	√
3.3					

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and –30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and –50%.
(3) Typical application configuration. Other check mark indicates alternative filter combinations

Inductor Selection

The inductor selection is affected by several parameter like inductor ripple current, output voltage ripple, transition point into Power Save Mode, and efficiency. See Table 3 for typical inductors.

Table 3. Inductor Selection

INDUCTOR VALUE	COMPONENT SUPPLIER	SIZE (LxWxH mm)	Isat/DCR
0.6 µH	Coilcraft XAL4012-601	4 x 4 x 2.1	7.1A/9.5 mΩ
1 µH	Coilcraft XAL4020-102	4 x 4 x 2.1	5.9A/13.2 mΩ
1 µH	Coilcraft XFL4020-102	4 x 4 x 2.1	5.1 A/10.8 mΩ
0.47 µH	TOKO DFE252012 R47	2.5 x 2 x 1.2	3.7A/39 mΩ
1 µH	TOKO DFE252012 1R0	2.5 x 2 x 1.2	3.0A/59 mΩ
0.68 µH	TOKO DFE322512 R68	3.2 x 2.5 x 1.2	3.5A/37 mΩ
1 µH	TOKO DFE322512 1R0	3.2 x 2.5 x 1.2	3.1A/45 mΩ

In addition, the inductor has to be rated for the appropriate saturation current and DC resistance (DCR). The inductor needs to be rated for a saturation current as high as the typical switch current limit, of 4.6 A or according to Equation 7 and Equation 8. Equation 7 and Equation 8 calculate the maximum inductor current under static load conditions. The formula takes the converter efficiency into account. The converter efficiency can be taken from the data sheet graph`s or 80% can be used as a conservative approach. The calculation must be done for the maximum input voltage where the peak switch current is highest.

$$I_L = I_{OUT} + \frac{\Delta I_L}{2} \quad (7)$$

$$I_L = I_{OUT} + \frac{\frac{V_{OUT}}{\eta} \times \left(1 - \frac{V_{OUT}}{V_{IN} \times \eta}\right)}{2 \times f \times L} \quad (8)$$

where

f = Converter switching frequency (typical 1.4 MHz)
L = Selected inductor value
η = Estimated converter efficiency (use the number from the efficiency curves or 0.80 as an conservative assumption)
Note: The calculation must be done for the maximum input voltage of the application

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current. A margin of 20% needs to be added to cover for load transients during operation.

Input and Output Capacitor Selection

For best output and input voltage filtering, low ESR ceramic capacitors are recommended. The input capacitor minimizes input voltage ripple, suppresses input voltage spikes and provides a stable system rail for the device. A 22 µF or larger input capacitor is recommended. The output capacitor value can range from 10 µF up to 150 µF and beyond. The recommended typical output capacitor value is 22 µF and can vary over a wide range as outline in the output filter selection table.

Setting the Output Voltage

The output voltage is set by an external resistor divider according to the following equations:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8\ V \times \left(1 + \frac{R1}{R2}\right) \tag{9}$$

$$R2 = \frac{V_{FB}}{I_{FB}} = \frac{0.8\ V}{5\ \mu A} \approx 160\ k\Omega \tag{10}$$

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R2 \times \left(\frac{V_{OUT}}{0.8V} - 1\right) \tag{11}$$

When sizing R2, in order to achieve low quiescent current and acceptable noise sensitivity, use a minimum of 5 µA for the feedback current I_{FB}. Larger currents through R2 improve noise sensitivity and output voltage accuracy.

Layout Guideline

It is recommended to place all components as close as possible to the IC. The VOS connection is noise sensitive and needs to be routed as short and directly to the output terminal of the inductor. The exposed thermal pad of the package, analog ground (pin 6) and power ground (pin 14, 15) should have a single joint connection at the exposed thermal pad of the package. This minimizes switch node jitter. The charge pump capacitor connected to CP and CN should be placed close to the IC to minimize coupling of switching waveforms into other traces and circuits. See the evaluation module User Guide (SLVU670) for an example of component placement, routing and thermal design.

TYPICAL APPLICATIONS

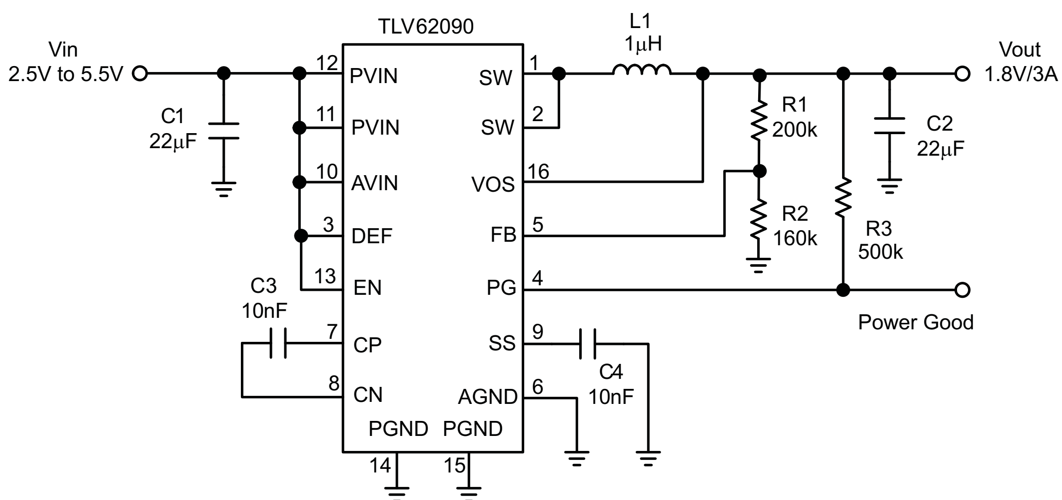


Figure 21. 1.8 V Adjustable Version

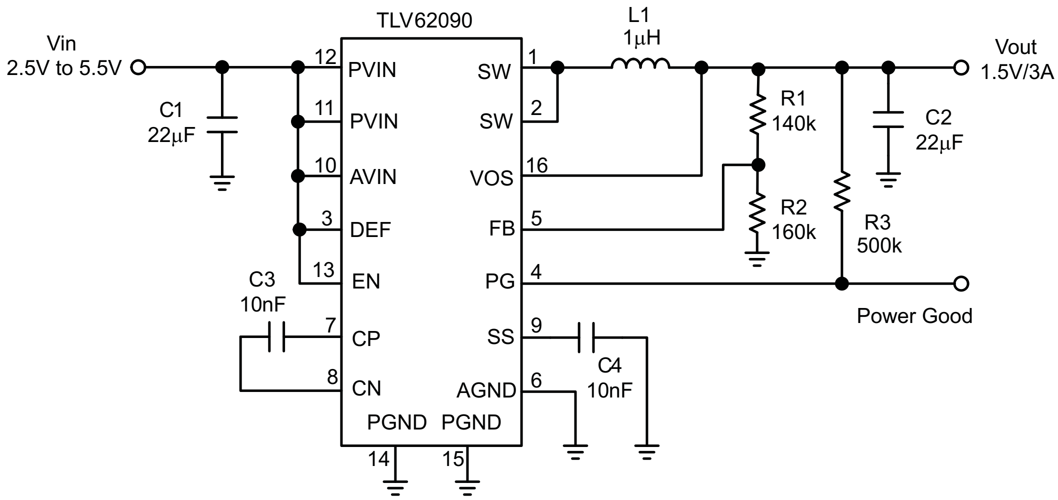


Figure 22. 1.5 V Adjustable Version

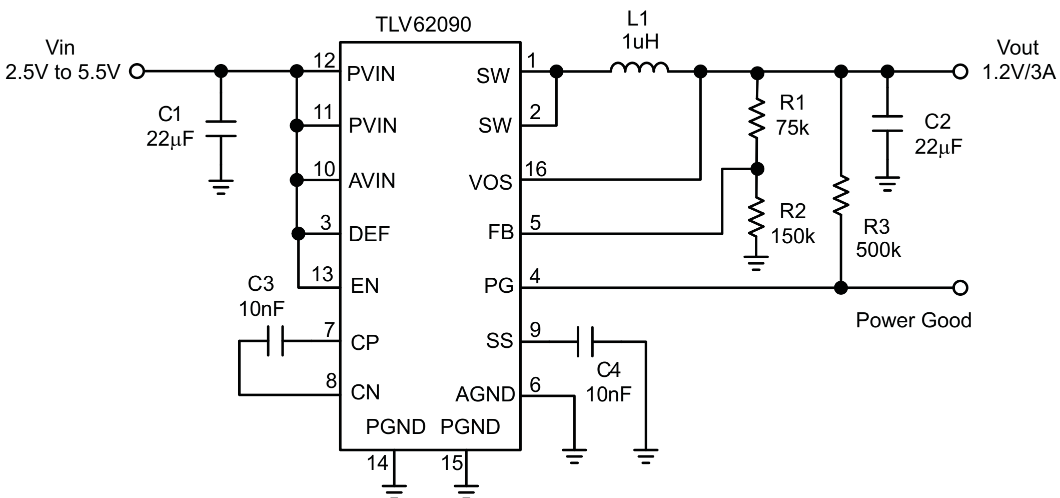


Figure 23. 1.2 V Adjustable Version

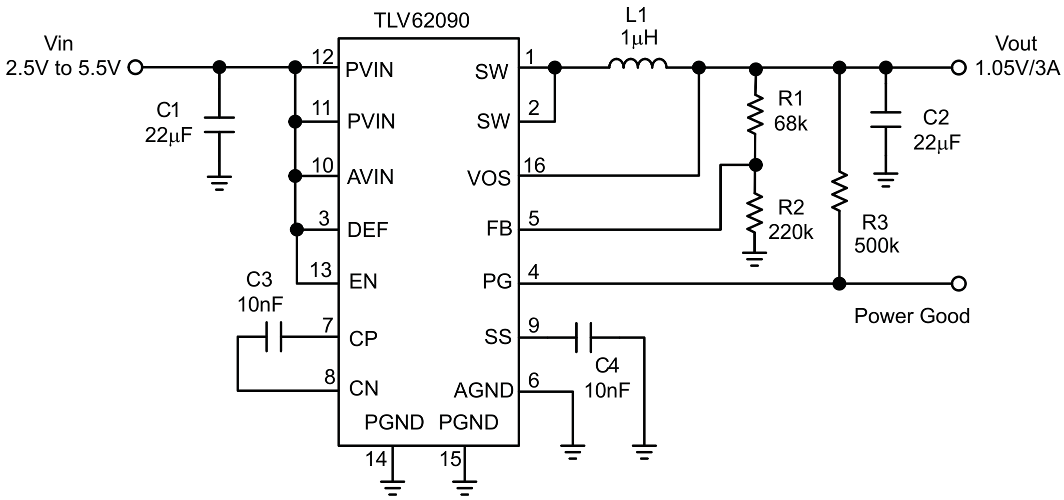


Figure 24. 1.05 V Adjustable Version

REVISION HISTORY

Changes from Original (March 2012) to Revision A	Page
• Changed Vin From: 2.5V to 6V To: 2.5V to 5.5V in Figure 1	6
• Changed Vin From: 2.5V to 6V To: 2.5V to 5.5V in Figure 20	11
• Changed Vin From: 2.5V to 6V To: 2.5V to 5.5V in Figure 21, Figure 22, Figure 23, and Figure 24	14

Changes from Revision A (March 2012) to Revision B	Page
• Changed the Input voltage range MAX value From: 6V To 5.5V	3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLV62090RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBV	Samples
TLV62090RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBV	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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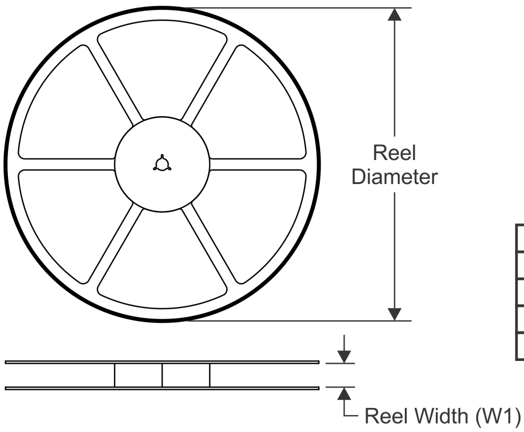
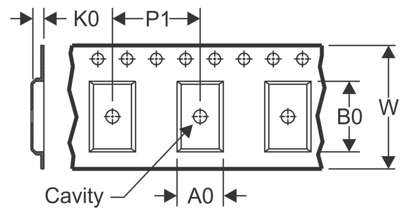
TAPE AND REEL INFORMATION

REEL DIMENSIONS

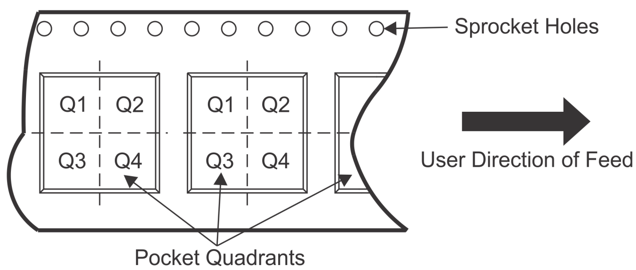


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

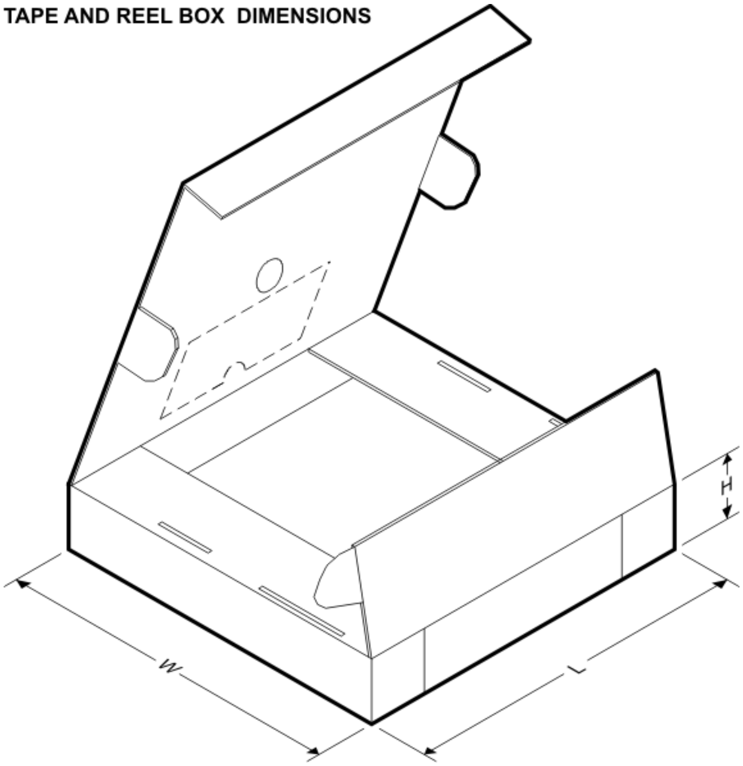
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV62090RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV62090RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

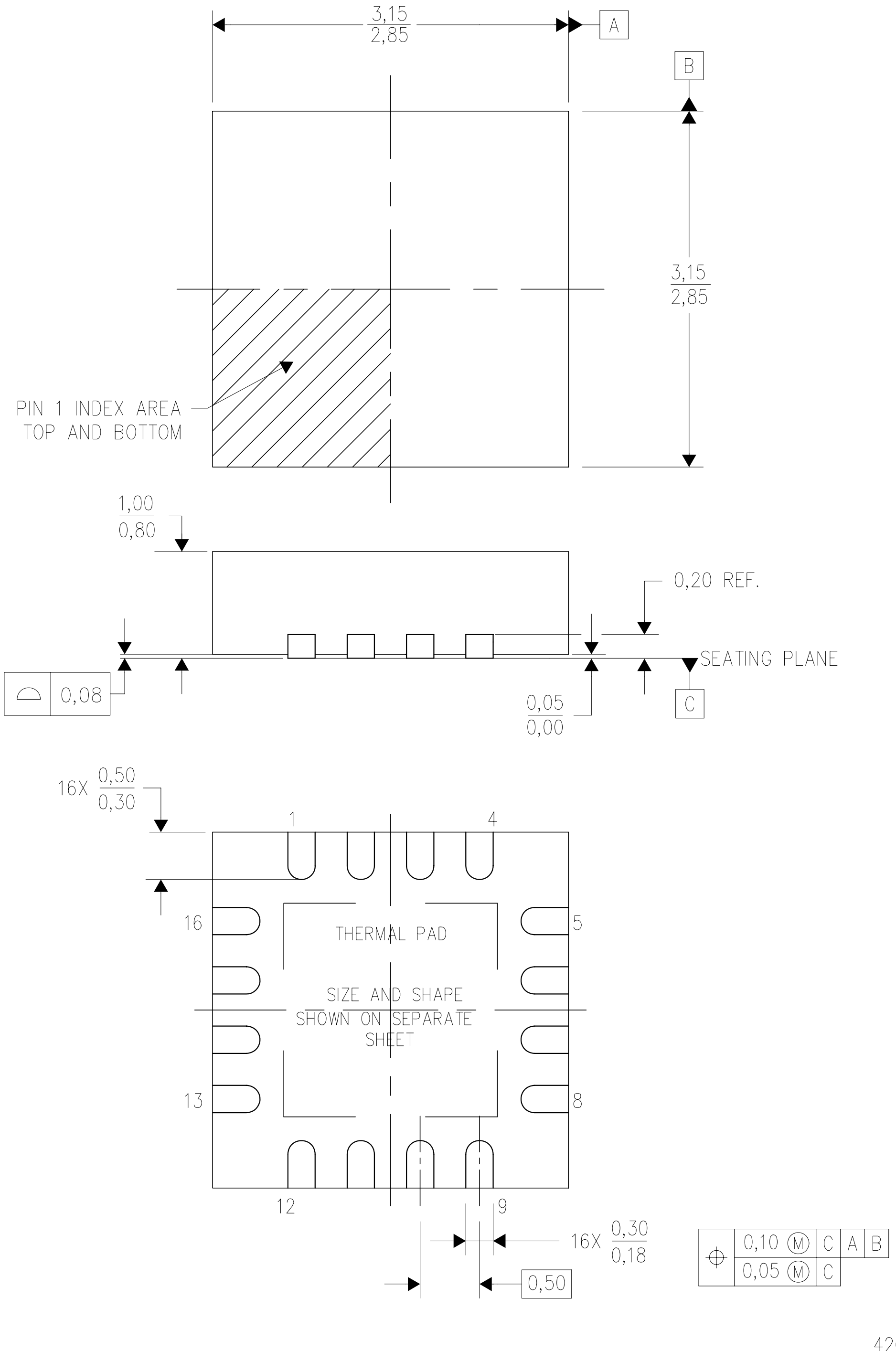
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV62090RGTR	QFN	RGT	16	3000	367.0	367.0	35.0
TLV62090RGTT	QFN	RGT	16	250	210.0	185.0	35.0

RGT (S-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No—leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO—220.

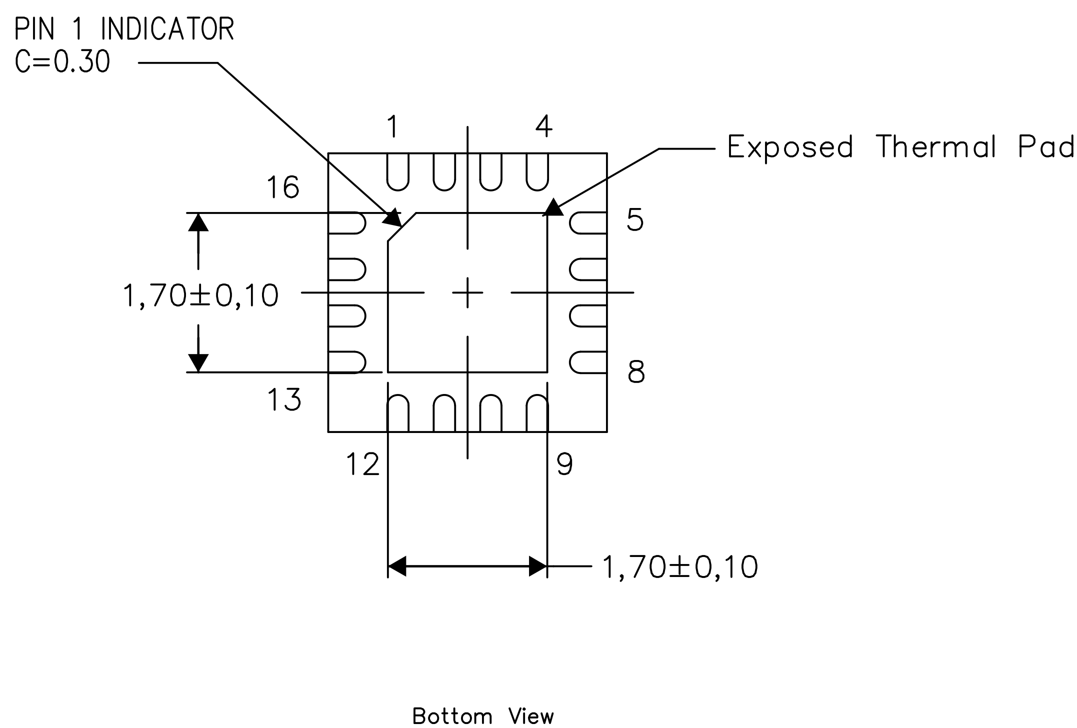
RGT (S-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

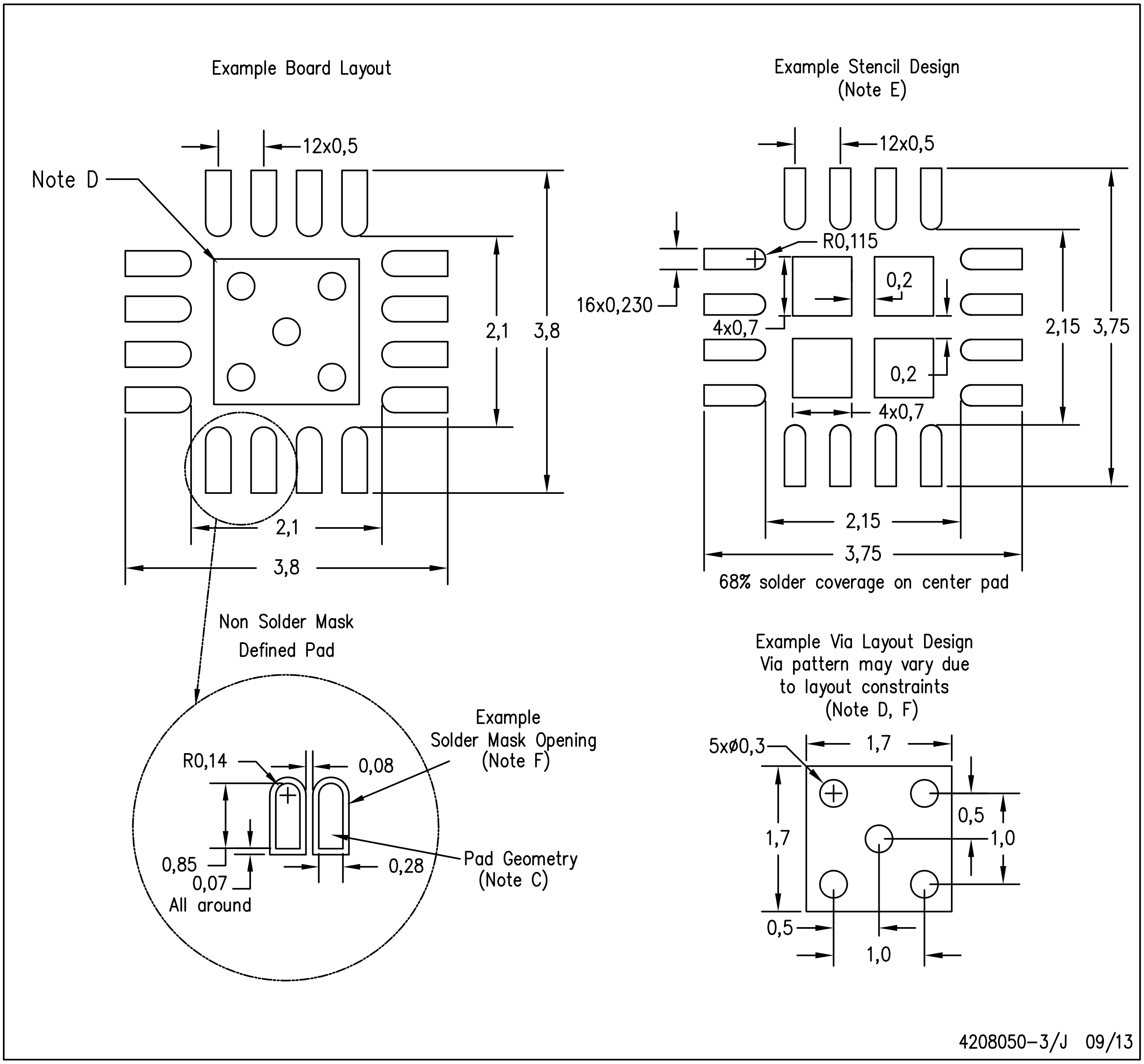


Exposed Thermal Pad Dimensions

4206349-4/U 09/13

NOTE: All linear dimensions are in millimeters

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

IMPORTANT NOTICE

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