200-mA, Low I_Q, Low-Noise, Low-Dropout Regulator in Ultra-Small 0.8-mm x 0.8-mm WCSP

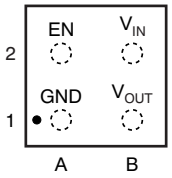
FEATURES

- **Very Low Dropout:**
  - **105 mV at I_{OUT} = 150 mA**
  - **145 mV at I_{OUT} = 200 mA**
- **Accuracy: 0.5% Typical**
- **Low I_Q: 35 µA**
- **Available in Fixed-Output Voltages from 0.7 V to 4.8 V**
- **High PSRR: 70 dB at 1 kHz**
- **Stable with Effective Capacitance of 0.1 µF**
- **Thermal Shutdown and Overcurrent Protection**
- **Available in 0.8-mm x 0.8-mm WCSP**

APPLICATIONS

- **Wireless Handsets**
- **Smart Phones, PDAs**
- **MP3 Players**
- **Zigbee™ Networks**
- **Bluetooth® Devices**
- **Other Li-Ion Operated Hand-Held Products**
- **WLAN and Other PC Add-On Cards**

YFF, YFP PACKAGES
WCSP-4
(TOP VIEW)

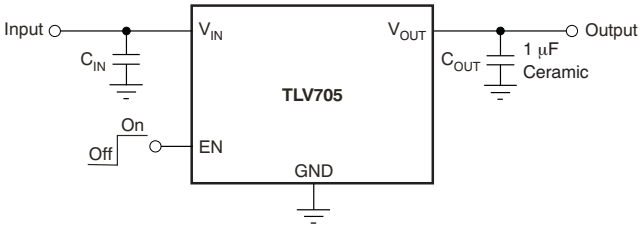


DESCRIPTION

The TLV705 series of low-dropout (LDO) linear regulators are low quiescent current devices with excellent line and load transient performance. Designed for power-sensitive applications, a precision bandgap and error amplifier provides typical accuracy of 0.5%. Low output noise, very high power-supply rejection ratio (PSRR), and low dropout voltage make this series of LDOs ideal for a wide selection of battery-operated hand-held equipment. All devices have a thermal shutdown and current limit for safety.

Furthermore, the TLV705 is stable with an effective output capacitance of only 0.1 µF. This feature enables the use of cost-effective capacitors that have higher bias voltage and temperature derating. The devices regulate to the specified accuracy with zero output load. The TLV705P series also provides an active pull-down circuit to quickly discharge output.

The TLV705 and TLV705P series are both available in a 0.8-mm × 0.8-mm WCSP with two height options that are optimal for hand-held applications.



Typical Application Circuit (Fixed-Voltage Versions)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS(1)

PRODUCT	V_{OUT}
TLV705**xx(x)Pyyyz**	**XX(X)** is nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example 28 = 2.8 V). **P** is optional; devices with ***P*** have an LDO regulator with an active output discharge. **YYY** is Package Designator **Z** is Package Quantity; ***R*** is for Reel (3000 pieces), ***T*** is for Tape (250 pieces)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Specified at T_J = –40°C to +125°C, unless otherwise noted. All voltages are with respect to GND.

		VALUE		UNIT
		MIN	MAX	
Voltage(2)	V_{IN}	–0.3	6	V
	V_{EN}	–0.3	6	V
	V_{OUT}	–0.3	6	V
Maximum output current	I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See Table 2		
Temperature	Operating junction, T_J	–55	+150	°C
	Storage, T_{stg}	–55	+150	°C
Electrostatic Discharge Rating(3)	Human body model (HBM) QSS 009-105 (JESD22-A114A)		2	kV
	Charged device model (CDM) QSS 009-147 (JESD22-C101B.01)		500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)		TLV705 YFF, YFP 4 BALLS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	160	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	80	
θ_{JB}	Junction-to-board thermal resistance	90	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	78	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

At T_J = –40°C to +125°C, V_{IN} = $V_{OUT\ (typ)}$ + 0.5 V or 2 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = 0.9 V, and C_{OUT} = 1 µF, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER		TEST CONDITIONS		TLV705			UNIT
				MIN	TYP	MAX	
V_{IN}	Input voltage range			2		5.5	V
V_{OUT}	Output voltage range			0.7		4.8	V
V_O	DC output accuracy	–40°C ≤ T_J ≤ +125°C	0 mA ≤ I_{OUT} ≤ 200 mA, V_{OUT} ≥ 1 V	–2	±0.5	2	%
			0 mA ≤ I_{OUT} ≤ 200 mA, V_{OUT} < 1 V	–20	±5	20	mV
$\Delta V_O/\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V			0.05	5	mV
$\Delta V_O/\Delta I_{OUT}$	Load regulation	0 mA ≤ I_{OUT} ≤ 200 mA			1		mV
V_{DO}	Dropout voltage(1)	V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 200 mA			145	250	mV
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$, T_J = +25°C		260	400	550	mA
I_{GND}	Ground pin current	I_{OUT} = 0 mA			35	55	µA
		I_{OUT} = 200 mA			315		µA
$I_{SHUTDOWN}$	Shutdown ground pin current	V_{EN} ≤ 0.4 V, 2 V ≤ V_{IN} ≤ 4.5 V			1	1.8	µA
PSRR	Power-supply rejection ratio	V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, f = 10 kHz			80		dB
		V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, f = 1 MHz			55		dB
V_N	Output noise voltage	BW = 100 Hz to 100 kHz, I_{OUT} = 10 mA	V_{IN} = 2.3 V, V_{OUT} = 1.8 V		26.6		μV_{RMS}
			V_{IN} = 3.3 V, V_{OUT} = 2.8 V		26.7		μV_{RMS}
			V_{IN} = 3.8 V, V_{OUT} = 3.3 V		28.2		μV_{RMS}
		BW = 10 Hz to 100 kHz, I_{OUT} = 10 mA	V_{IN} = 2.3 V, V_{OUT} = 1.8 V		30.7		μV_{RMS}
			V_{IN} = 3.3 V, V_{OUT} = 2.8 V		31.3		μV_{RMS}
			V_{IN} = 3.8 V, V_{OUT} = 3.3 V		34.1		μV_{RMS}
t_{STR}	Startup time(2)	C_{OUT} = 1 µF, I_{OUT} = 200 mA			100		µs
V_{HI}	Enable high (enabled)			0.9		V_{IN}	V
V_{LO}	Enable low (disabled)			0		0.4	V
I_{EN}	EN pin current	EN = 5.5 V			0.01		µA
UVLO	Undervoltage lockout	V_{IN} rising			1.9		V
t_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing			+160		°C
		Reset, temperature decreasing			+140		°C
T_J	Operating junction temperature			–40		+125	°C

(1) V_{DO} is measured for devices with $V_{OUT(NOM)}$ = 2.35 V so that V_{IN} = 2.3 V.
(2) Startup time = time from EN assertion to 0.98 × $V_{OUT(NOM)}$.

FUNCTIONAL BLOCK DIAGRAMS

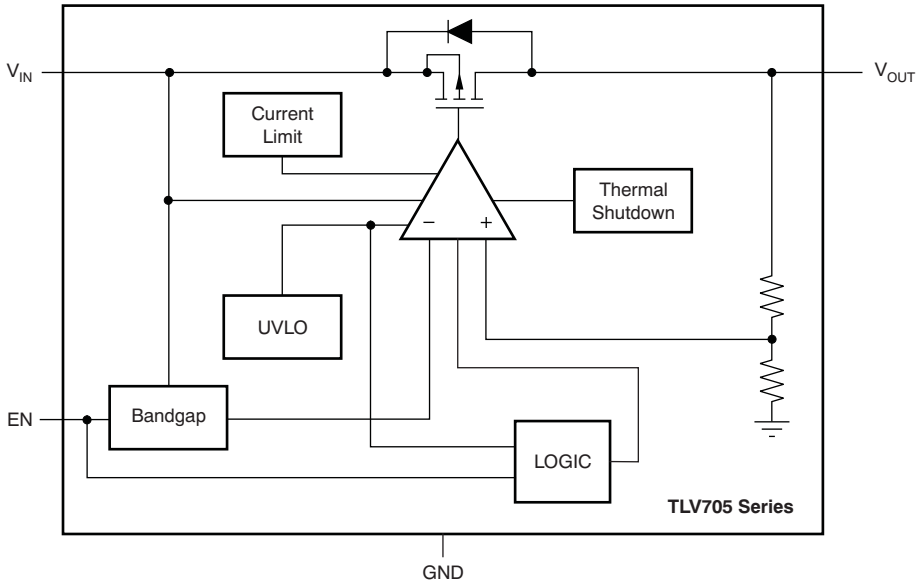


Figure 1. TLV705 Diagram

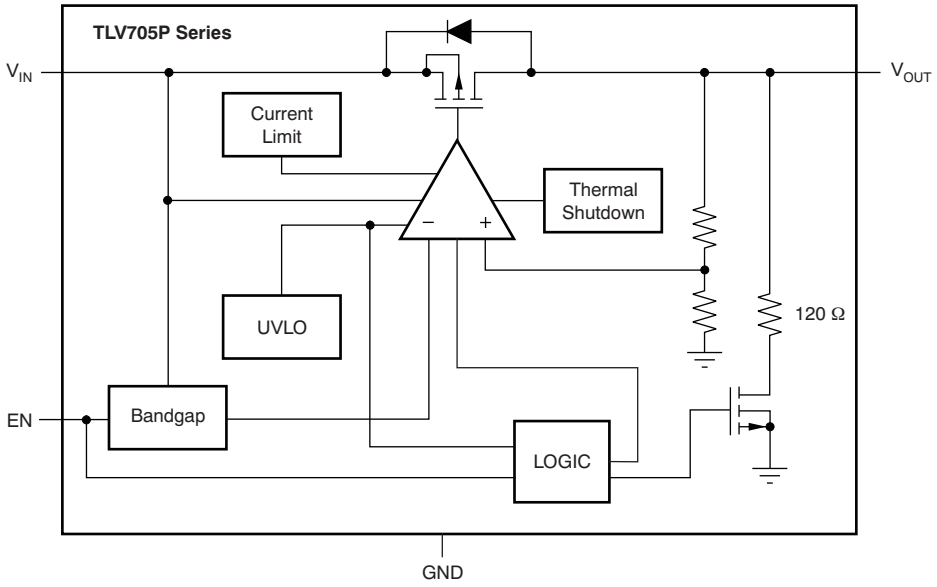


Figure 2. TLV705P Diagram

PIN CONFIGURATION

YFF, YFP PACKAGES
WCSP-4
(TOP VIEW)

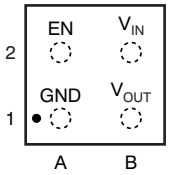


Table 1. Pin Descriptions

TLV705		
NAME	**PIN #**	**DESCRIPTION**
GND	A1	Ground pin
EN	A2	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode, thus reducing operating current to 1 µA, nominal.
V_{OUT}	B1	Regulated output voltage pin. A small 1-µF ceramic capacitor is required to be placed from this pin to ground to assure stability. See the *Input and Output Capacitor Requirements* section for more details.
V_{IN}	B2	Input pin. A small 1-µF ceramic capacitor is recommended to be placed from this pin to ground for good transient performance. See the *Input and Output Capacitor Requirements* section for more details.

TYPICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), I_{OUT} = 10 mA, V_{EN} = 0.9 V, C_{OUT} = 1 µF, and V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2 V, whichever is greater, unless otherwise noted. Typical values are at T_J = +25°C.

LINE REGULATION

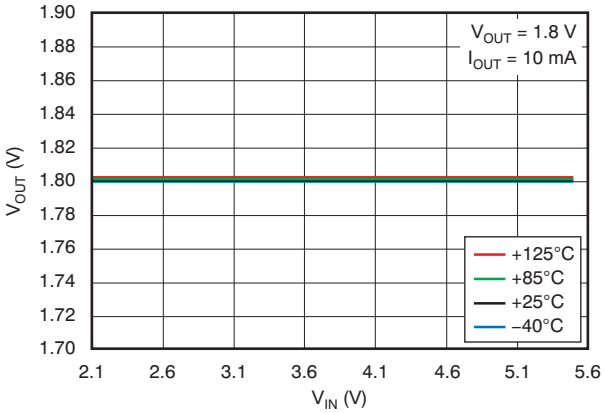


Figure 3.

LINE REGULATION

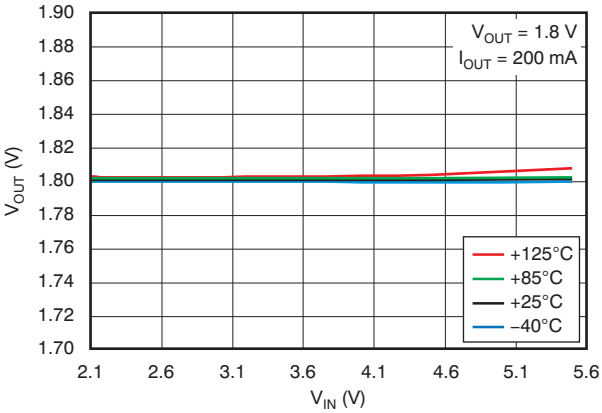


Figure 4.

LOAD REGULATION
(0 mA ≤ I_{OUT} ≤ 200 mA)

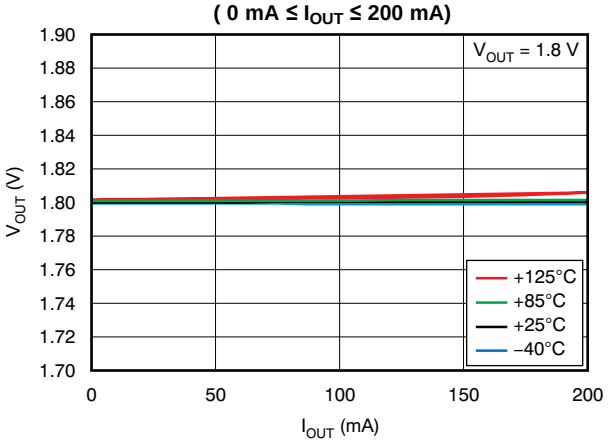


Figure 5.

DROPOUT VOLTAGE vs INPUT VOLTAGE

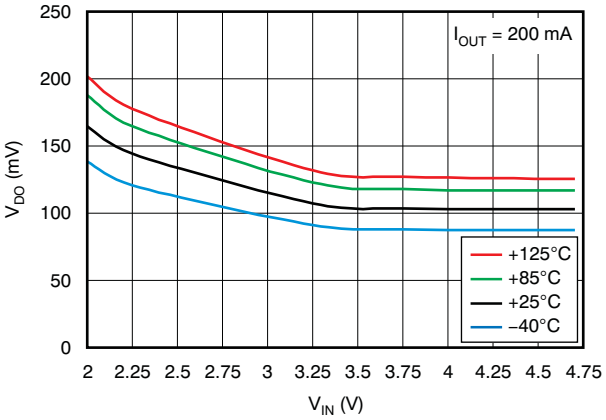


Figure 6.

DROPOUT VOLTAGE vs OUTPUT CURRENT

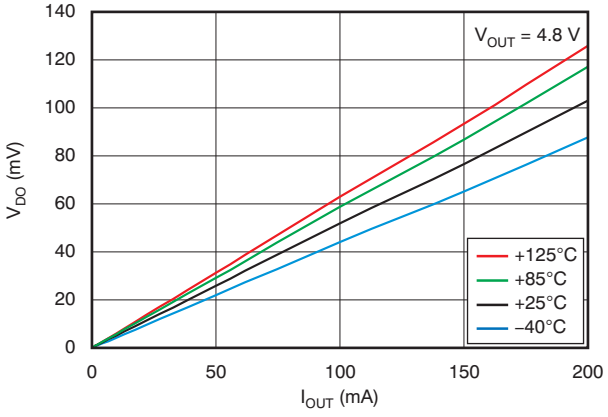


Figure 7.

OUTPUT VOLTAGE vs TEMPERATURE

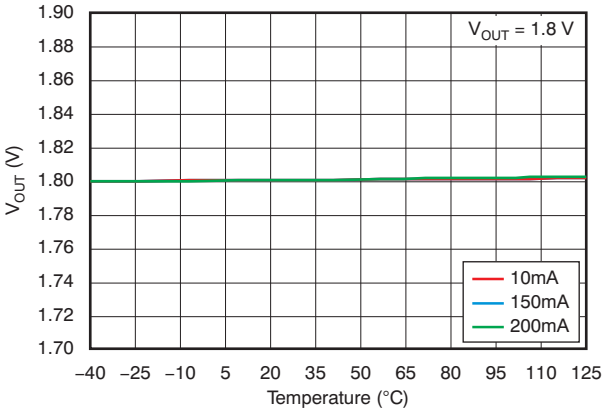


Figure 8.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), I_{OUT} = 10 mA, V_{EN} = 0.9 V, C_{OUT} = 1 µF, and V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2 V, whichever is greater, unless otherwise noted. Typical values are at T_J = +25°C.

GROUND PIN CURRENT vs INPUT VOLTAGE

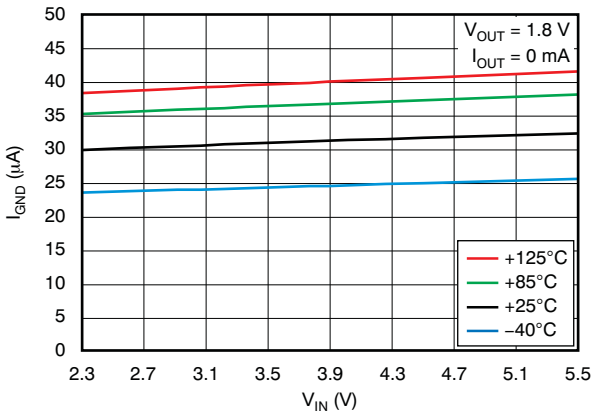


Figure 9.

GROUND PIN CURRENT vs OUTPUT CURRENT

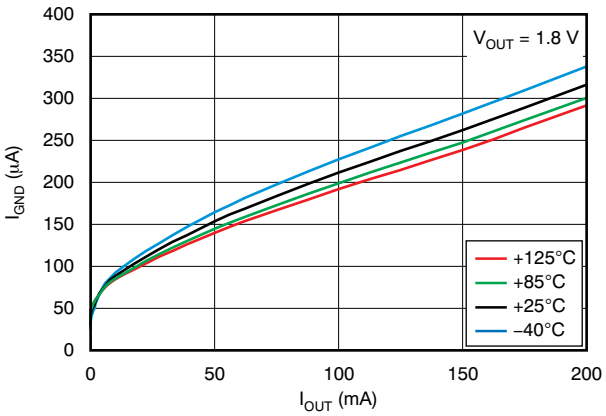


Figure 10.

GROUND PIN CURRENT vs TEMPERATURE

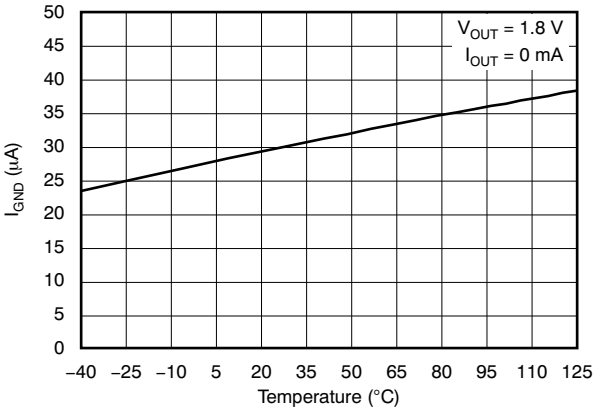


Figure 11.

SHUTDOWN PIN CURRENT vs INPUT VOLTAGE

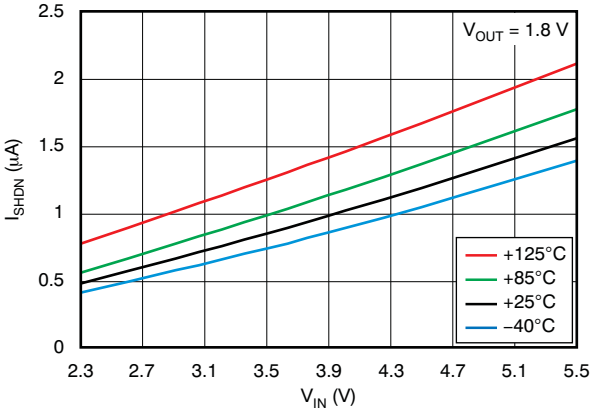


Figure 12.

CURRENT LIMIT vs INPUT VOLTAGE

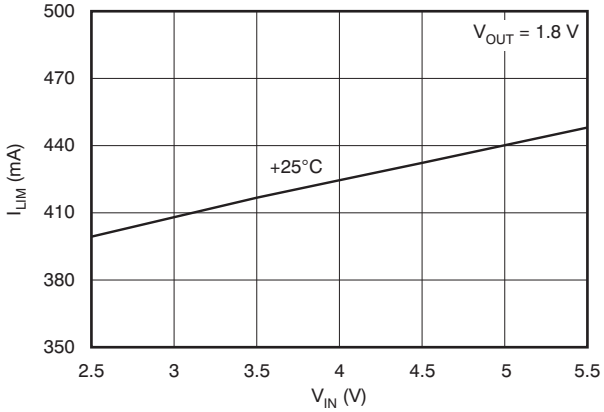


Figure 13.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

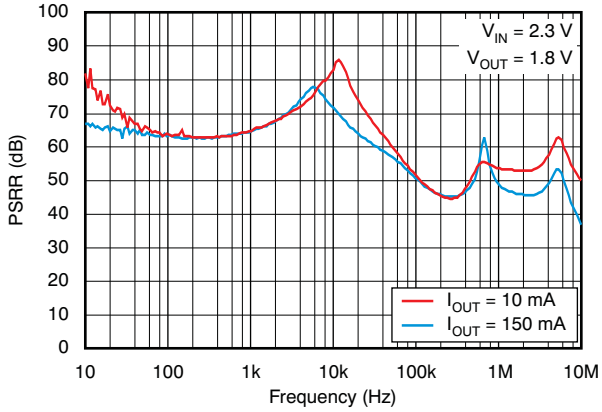


Figure 14.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), I_{OUT} = 10 mA, V_{EN} = 0.9 V, C_{OUT} = 1 µF, and V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2 V, whichever is greater, unless otherwise noted. Typical values are at T_J = +25°C.

POWER-SUPPLY REJECTION RATIO vs INPUT VOLTAGE

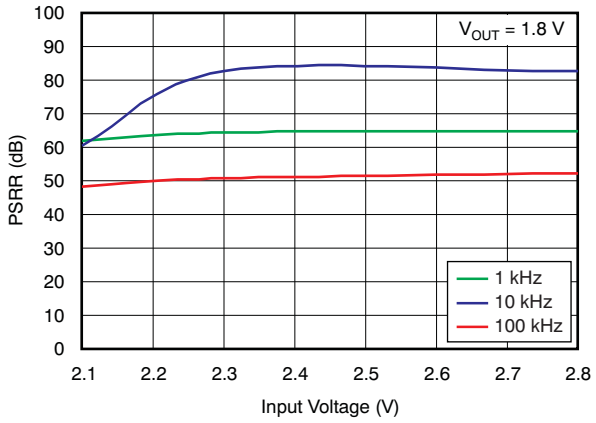


Figure 15.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

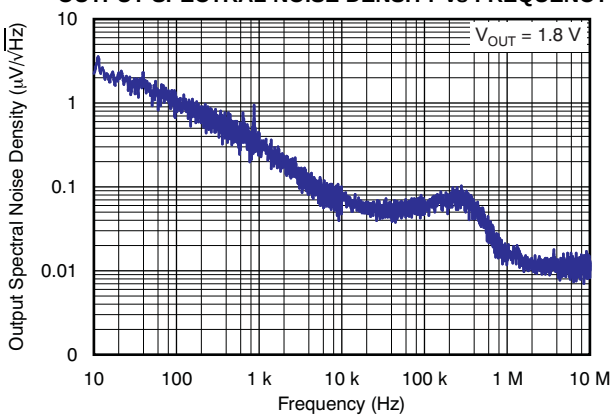


Figure 16.

INTEGRATED NOISE vs OUTPUT VOLTAGE

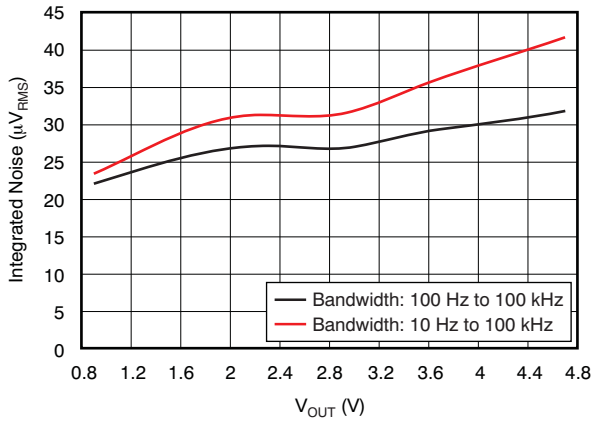


Figure 17.

LOAD TRANSIENT 0

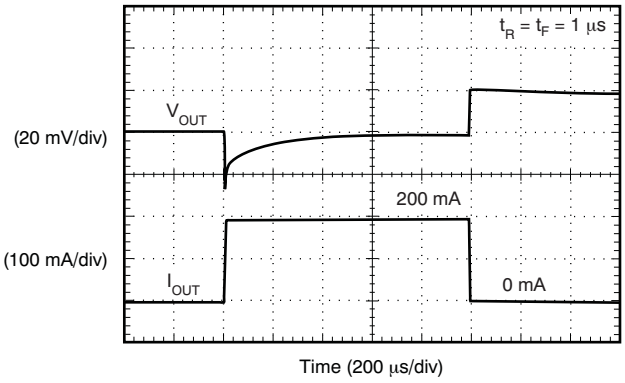


Figure 18.

LOAD TRANSIENT 1

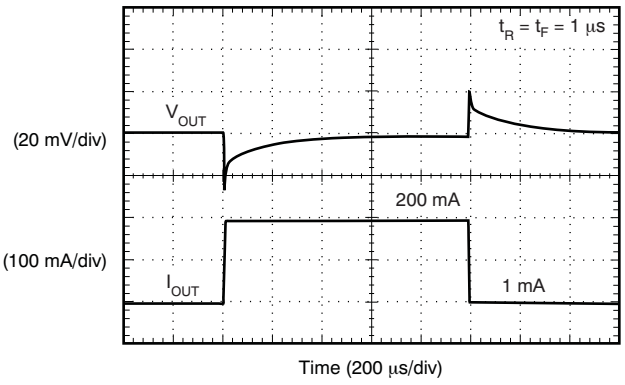


Figure 19.

LOAD TRANSIENT 3

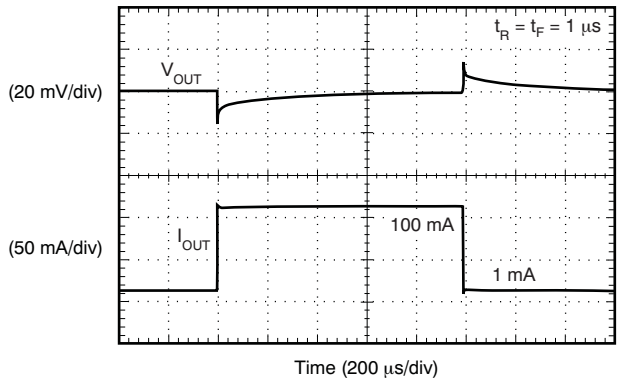


Figure 20.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), I_{OUT} = 10 mA, V_{EN} = 0.9 V, C_{OUT} = 1 µF, and V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2 V, whichever is greater, unless otherwise noted. Typical values are at T_J = +25°C.

SMALL-STEP LINE TRANSIENT (10mA)

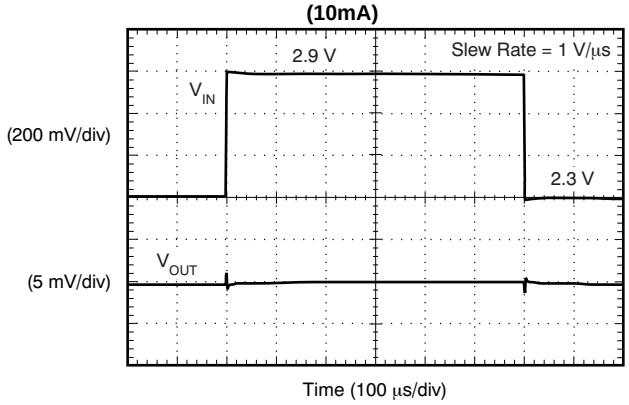


Figure 21.

SMALL-STEP LINE TRANSIENT (200mA)

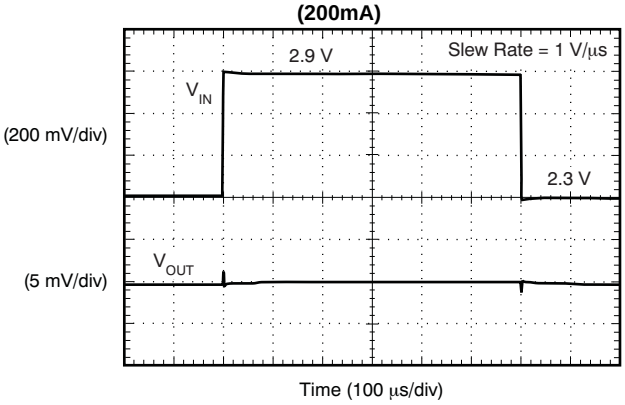


Figure 22.

V_{IN} INRUSH CURRENT

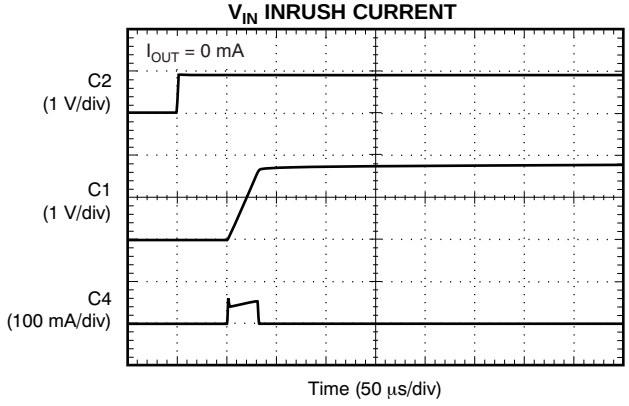


Figure 23.

V_{IN} INRUSH CURRENT

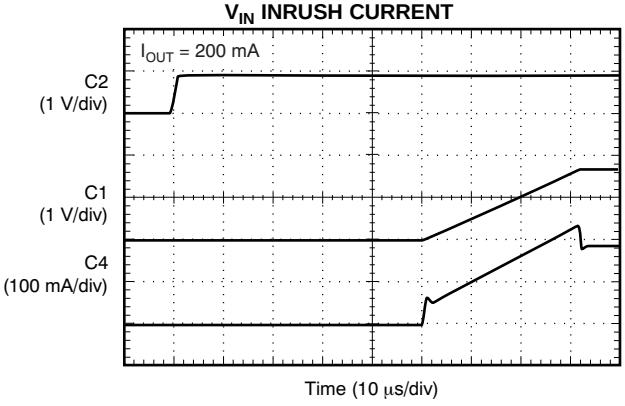


Figure 24.

LINE TRANSIENT (10mA)

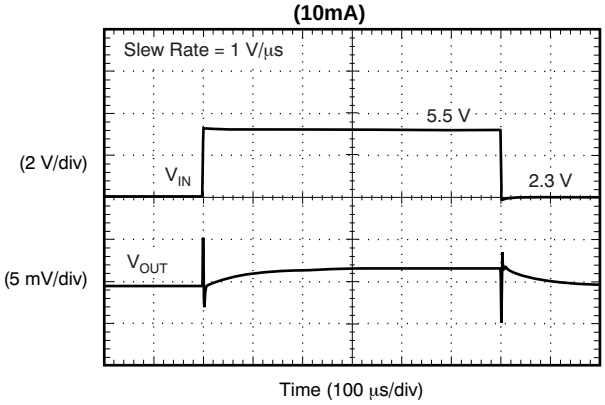


Figure 25.

LINE TRANSIENT (200mA)

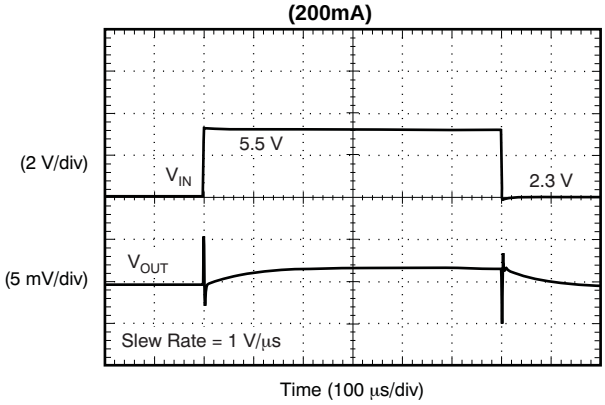


Figure 26.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), I_{OUT} = 10 mA, V_{EN} = 0.9 V, C_{OUT} = 1 µF, and V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2 V, whichever is greater, unless otherwise noted. Typical values are at T_J = +25°C.

POWER-UP/POWER-DOWN

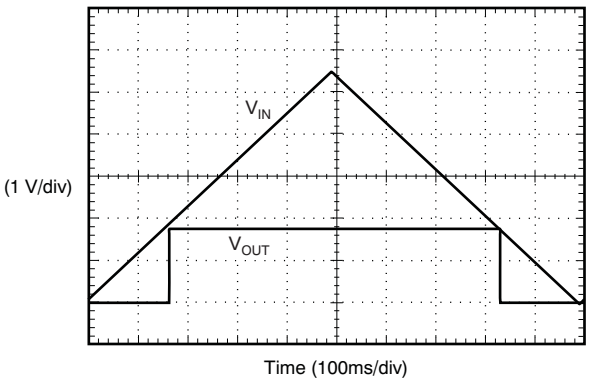


Figure 27.

APPLICATION INFORMATION

The TLV705 and TLV705P series of devices belong to a new family of next-generation value low-dropout (LDO) voltage regulators. They consume low quiescent current and deliver excellent line and load transient performance. This performance, combined with low noise, very good PSRR with little (V_{IN} – V_{OUT}) headroom, makes these devices ideal for RF portable applications. This family of regulators offers sub-bandgap output voltages down to 0.7 V, current limit, and thermal protection, and are specified from –40°C to +125°C. The TLV705P provides an active pull-down circuit to quickly discharge the outputs.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

1-µF X5R- and X7R-type ceramic capacitors are recommended because these components have minimal variation in value and equivalent series resistance (ESR) over temperature. However, the TLV705 series is designed to be stable with an effective capacitance of 0.1 µF or larger at the output. Thus, the device would also be stable with capacitors of other dielectrics as long as the effective capacitance under the operating bias voltage and temperature is greater than 0.1 µF. This effective capacitance refers to the capacitance that the LDO sees under operating bias voltage and temperature conditions (that is, the capacitance after taking the bias voltage and temperature derating into consideration). In addition to allowing the use of lower cost dielectrics, it also enables using smaller footprint capacitors that have higher derating in space-constrained applications.

Note that using a 0.1-µF rating capacitor at the output of the LDO does not ensure stability because the effective capacitance under operating conditions would be less than 0.1 µF. Maximum ESR should be less than 200 mΩ.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1-µF low ESR capacitor across the V_{IN} and GND pins of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2 Ω, a 0.1-µF input capacitor may be necessary to ensure stability.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

Input and output capacitors should be placed as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. High ESR capacitors may degrade PSRR.

INTERNAL CURRENT LIMIT

The internal current limits of the TLV705 series help protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and can be measured as $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The PMOS pass transistor dissipates $[(V_{IN} – V_{OUT}) \times I_{LIMIT}]$ until a thermal shutdown is triggered and the device turns off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown; see the *Thermal Information* section for more details.

The PMOS pass element in the TLV705 has a built-in body diode that conducts current when the voltage at V_{OUT} exceeds the voltage at V_{IN}. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of rated output current is recommended.

SOFT-START

The startup current is given by Equation 1. This equation shows that soft-start current is directly proportional to C_{OUT}.

$$I_{SOFT\text{-}START} = C_{OUT}\ (\mu F) \times 0.06\ (V/\mu s) + I_{LOAD}\ (mA) \quad (1)$$

The output voltage ramp rate is independent of C_{OUT} and the load current, and has a typical value of 0.06 V/µs.

The TLV705 automatically adjusts the soft-start current to supply both the load current and the current to charge C_{OUT}. For example, if I_{LOAD} = 0 mA upon enabling the LDO, then $I_{SOFT\text{-}START}$ = 1 µF × 0.06 V/µs + 0 mA = 60 mA, which is the current that charges the output capacitor. However if I_{LOAD} = 200 mA, then $I_{SOFT\text{-}START}$ = 1 µF × 0.06 V/µs + 200 mA = 260 mA, which is the current required for charging the output capacitor and supplying the load current.

If the output capacitor and load are increased such that the soft-start current exceeds the output current limit, it is clamped at the typical current limit of 400 mA. For example, if C_{OUT} = 10 µF and I_{OUT} = 200 mA, then 10 µF × 0.06 V/µs + 200 mA = 800 mA is not supplied. Instead, it is clamped at 400 mA.

SHUTDOWN

The enable pin (EN) is active high. The device is enabled when the EN pin goes above 0.9 V. This relatively lower value of voltage required to turn the LDO on can be used to power the device with the GPIO of recent processors with a GPIO voltage lower than traditional microcontrollers. The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, EN can be connected to the V_{IN} pin. The TLV705P version has internal active pull-down circuitry that discharges the output with a time constant of:

$$\tau = (120 \times R_L)/(120 + R_L) \times C_{OUT}$$

Where:

R_L = load resistance, C_{OUT} = output capacitor (2)

DROPOUT VOLTAGE

The TLV705 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} approximately scales with the output current because the PMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in Figure 15 in the Typical Characteristics.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude, but increases the duration of the transient response.

UNDERVOLTAGE LOCK-OUT (UVLO)

The TLV705 uses an undervoltage lockout (UVLO) circuit to keep the output shut off until the internal circuitry is operating properly.

THERMAL INFORMATION

Thermal protection disables the output when the junction temperature rises to approximately +165°C, allowing the device to cool. When the junction temperature cools to approximately +145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C, maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TLV705 is been designed to protect against overload conditions. It is not intended to replace proper heatsinking. Continuously running the TLV705 into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low and high-K boards are given in the Thermal Information table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Refer to Table 2 for thermal performance on the TLV705 evaluation module (EVM). The EVM is a two-layer board with two ounces of copper per side. Dimensions and layout of the board are illustrated in Figure 28 and Figure 29, respectively.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 3:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (3)$$

Table 2. Power Dissipation Ratings(1)

BOARD	PACKAGE	$R_{\theta J}$	$T_A \leq 25°C$ POWER RATING	$T_A = +70°C$ POWER RATING	$T_A = +85°C$ POWER RATING
High-K	YFF, YFP	140 °C/W	714 mW	392 mW	285 mW

(1) Thermal resistance as measured on the evaluation module (EVM).

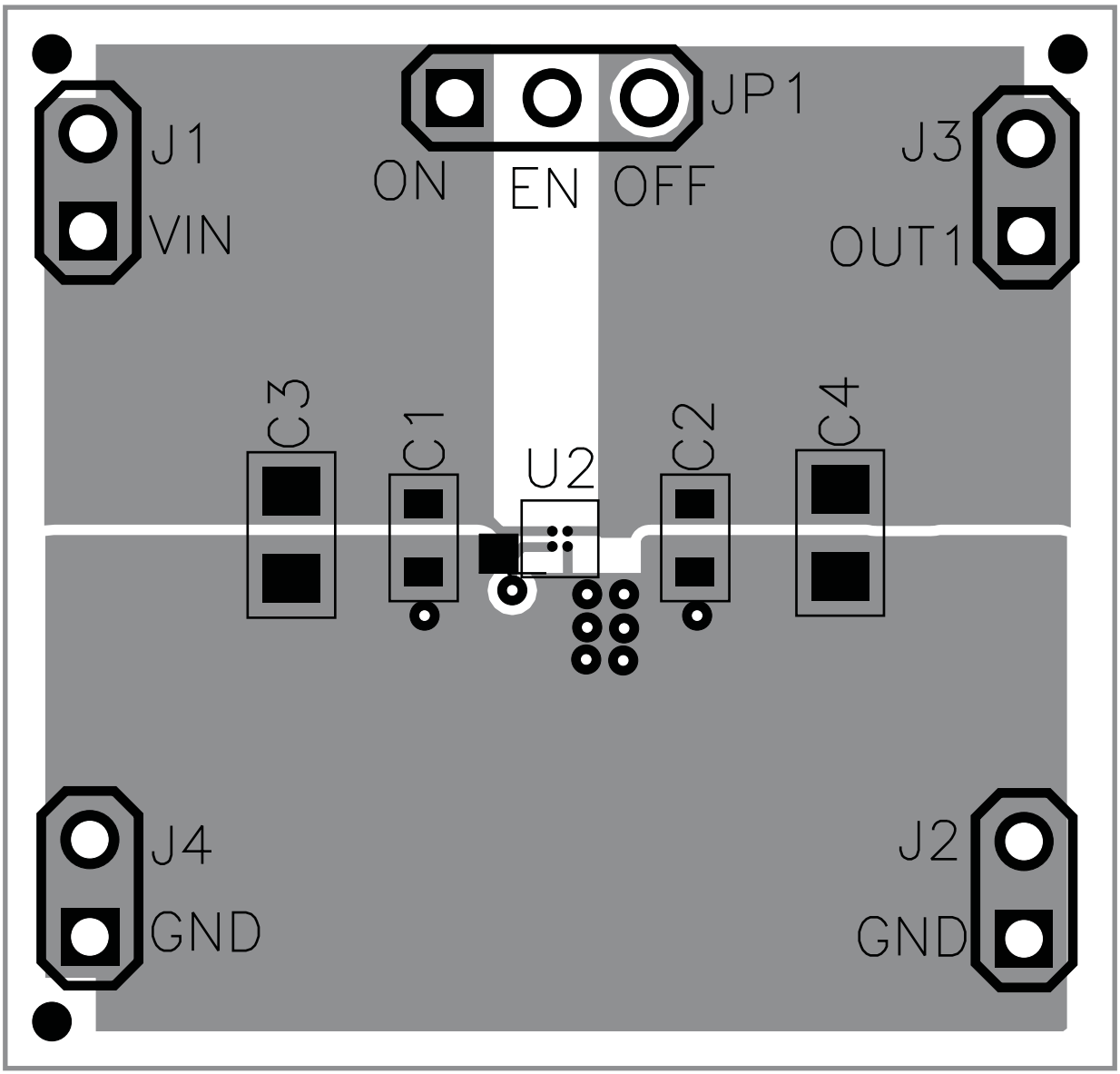


Figure 28. Silkscreen, Top Layer

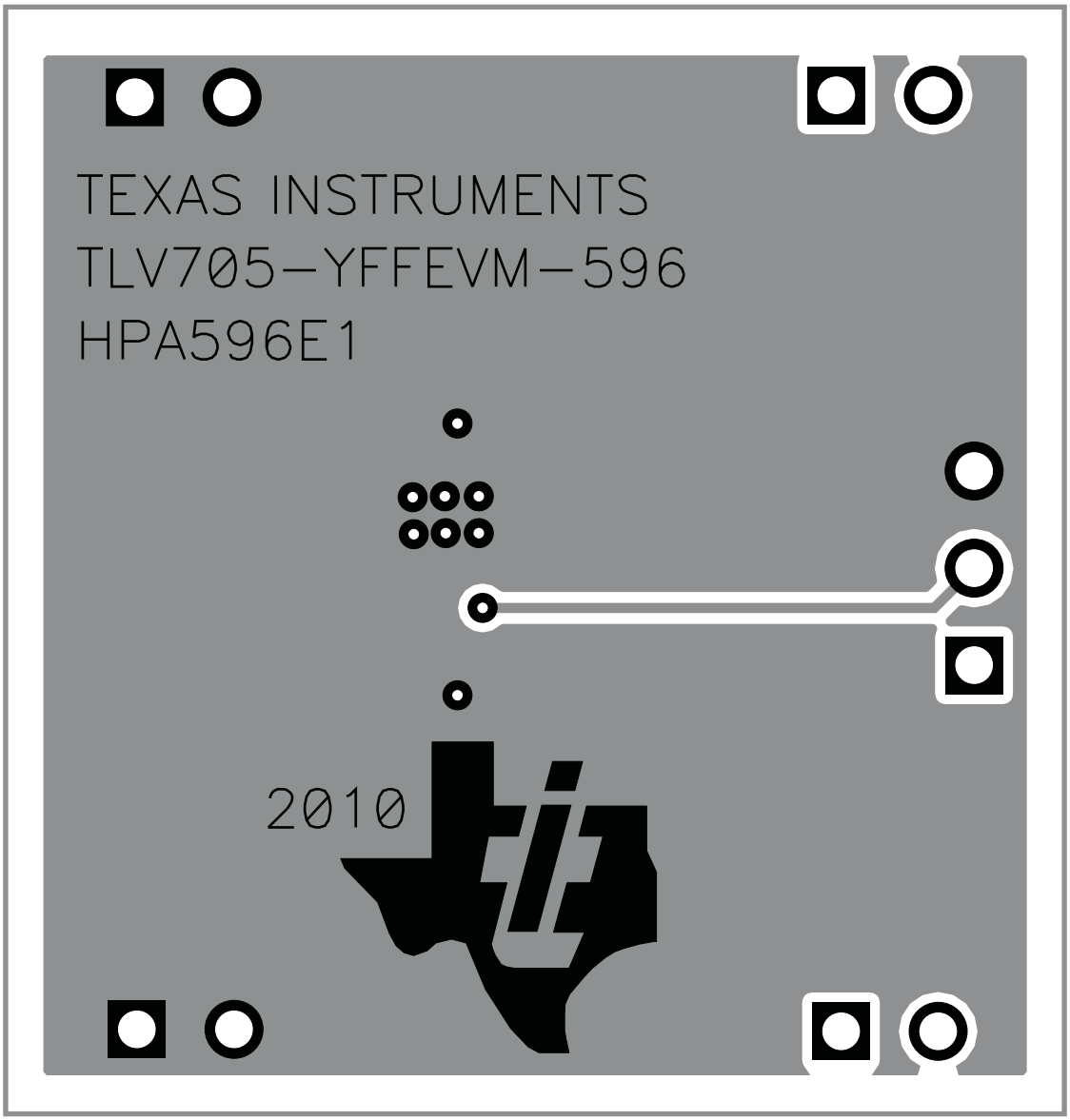


Figure 29. Silkscreen, Bottom Layer

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2011) to Revision C **Page**

- Deleted last Features bullet 1

Changes from Revision A (August 2011) to Revision B **Page**

- Added last Features bullet 1
- Changed front page pin out drawing 1
- Changed last sentence of Description section 1
- Added YFP package to Thermal Information table 2
- Added YFP to title of pin out drawing 5
- Added YFP to Package column of Table 2 13
- Added *Mechanical Packages* section (removed June 2013; packages are now automatically appended) 15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLV70512YFPR	ACTIVE	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	BU	Samples
TLV70512YFPT	ACTIVE	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	BU	Samples
TLV70515YFPR	ACTIVE	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	BV	Samples
TLV70515YFPT	ACTIVE	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	BV	Samples
TLV705185YFPR	ACTIVE	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	YS	Samples
TLV705185YFPT	ACTIVE	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	YS	Samples
TLV70518YFPR	ACTIVE	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	WT	Samples
TLV70518YFPT	ACTIVE	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	WT	Samples
TLV70525YFPR	ACTIVE	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	YB	Samples
TLV70525YFPT	ACTIVE	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	YB	Samples
TLV705285YFPR	ACTIVE	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	BW	Samples
TLV705285YFPT	ACTIVE	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	BW	Samples
TLV70528YFPR	ACTIVE	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	WU	Samples
TLV70528YFPT	ACTIVE	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	WU	Samples
TLV70530YFPR	ACTIVE	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	XA	Samples
TLV70530YFPT	ACTIVE	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	XA	Samples
TLV70533YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	US	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLV70533YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	US	Samples
TLV70533YFPR	ACTIVE	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	VV	Samples
TLV70533YFPT	ACTIVE	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	VV	Samples
TLV70534YFPR	ACTIVE	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	B4	Samples
TLV70534YFPT	ACTIVE	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	B4	Samples
TLV70536YFPR	ACTIVE	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	BX	Samples
TLV70536YFPT	ACTIVE	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	BX	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

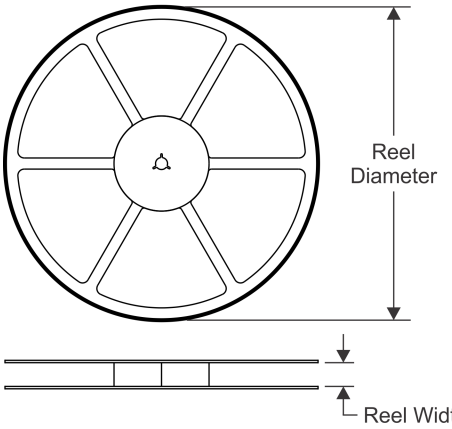
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

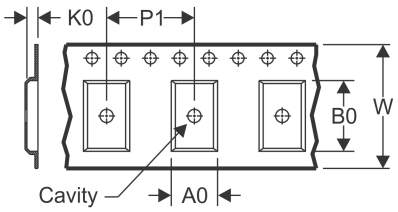
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

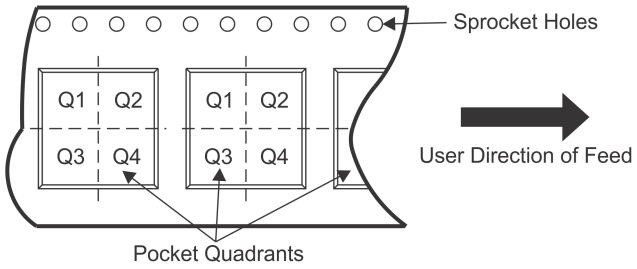


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

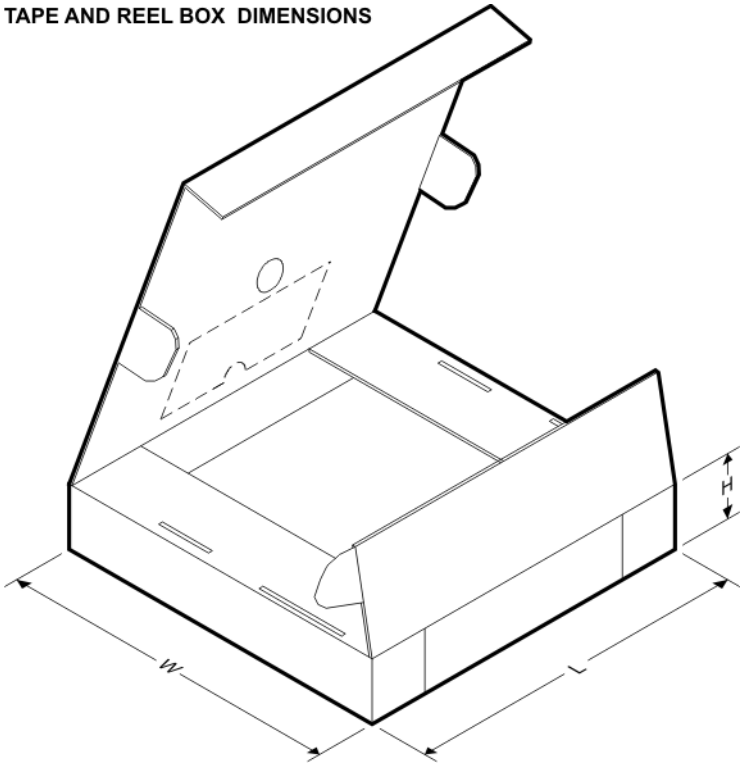


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70512YFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TLV70512YFPT	DSBGA	YFP	4	250	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TLV70515YFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TLV70515YFPT	DSBGA	YFP	4	250	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TLV705185YFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TLV705185YFPT	DSBGA	YFP	4	250	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TLV70518YFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TLV70518YFPT	DSBGA	YFP	4	250	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TLV70525YFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TLV70525YFPT	DSBGA	YFP	4	250	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TLV705285YFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TLV705285YFPT	DSBGA	YFP	4	250	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TLV70528YFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TLV70528YFPT	DSBGA	YFP	4	250	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TLV70530YFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TLV70530YFPT	DSBGA	YFP	4	250	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TLV70533YFFR	DSBGA	YFF	4	3000	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
TLV70533YFFT	DSBGA	YFF	4	250	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70533YFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TLV70533YFPT	DSBGA	YFP	4	250	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TLV70534YFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TLV70534YFPT	DSBGA	YFP	4	250	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TLV70536YFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TLV70536YFPT	DSBGA	YFP	4	250	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

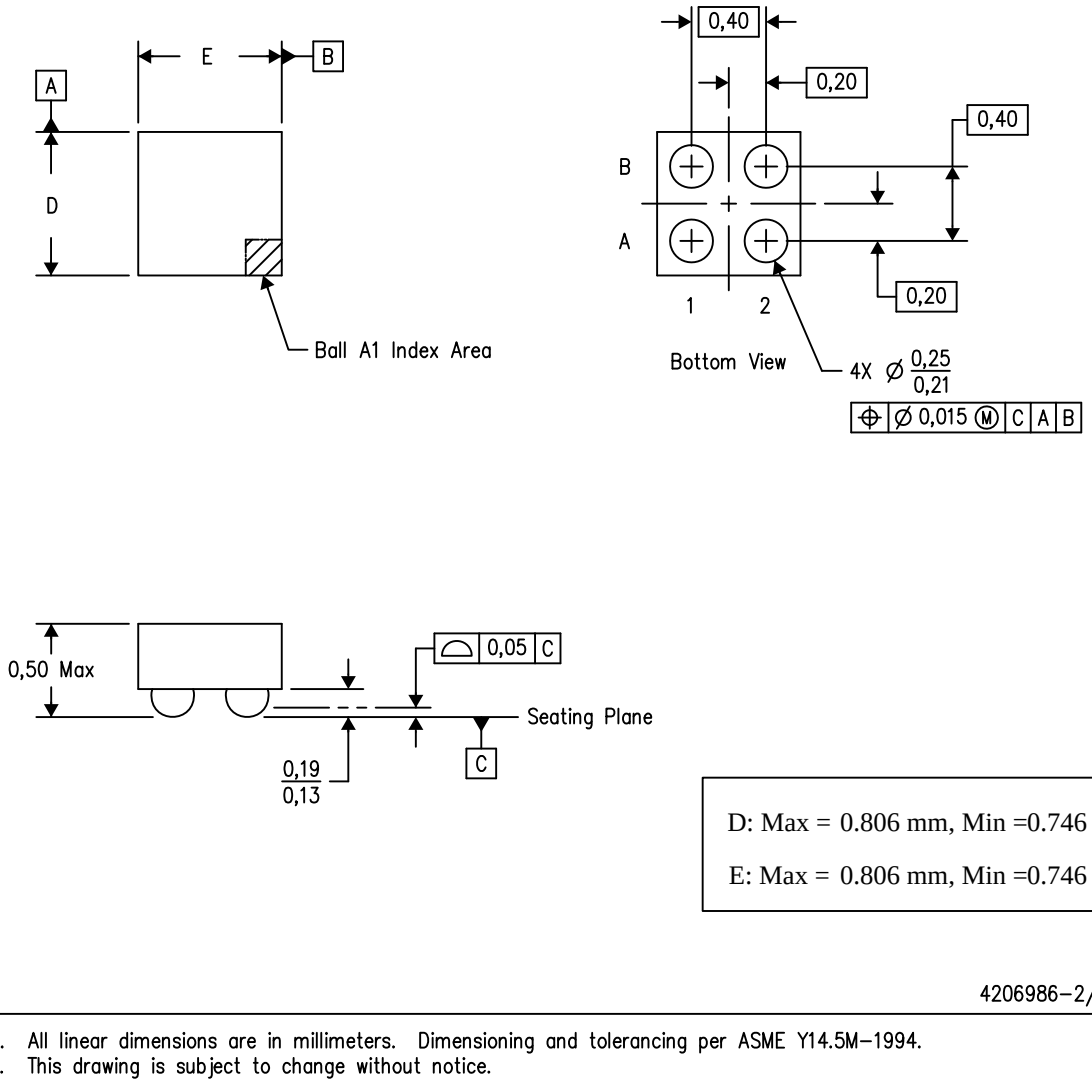


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70512YFPR	DSBGA	YFP	4	3000	182.0	182.0	17.0
TLV70512YFPT	DSBGA	YFP	4	250	182.0	182.0	17.0
TLV70515YFPR	DSBGA	YFP	4	3000	182.0	182.0	17.0
TLV70515YFPT	DSBGA	YFP	4	250	182.0	182.0	17.0
TLV705185YFPR	DSBGA	YFP	4	3000	182.0	182.0	17.0
TLV705185YFPT	DSBGA	YFP	4	250	182.0	182.0	17.0
TLV70518YFPR	DSBGA	YFP	4	3000	182.0	182.0	17.0
TLV70518YFPT	DSBGA	YFP	4	250	182.0	182.0	17.0
TLV70525YFPR	DSBGA	YFP	4	3000	182.0	182.0	17.0
TLV70525YFPT	DSBGA	YFP	4	250	182.0	182.0	17.0
TLV705285YFPR	DSBGA	YFP	4	3000	182.0	182.0	17.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV705285YFPT	DSBGA	YFP	4	250	182.0	182.0	17.0
TLV70528YFPR	DSBGA	YFP	4	3000	182.0	182.0	17.0
TLV70528YFPT	DSBGA	YFP	4	250	182.0	182.0	17.0
TLV70530YFPR	DSBGA	YFP	4	3000	182.0	182.0	17.0
TLV70530YFPT	DSBGA	YFP	4	250	182.0	182.0	17.0
TLV70533YFFR	DSBGA	YFF	4	3000	210.0	185.0	35.0
TLV70533YFFT	DSBGA	YFF	4	250	210.0	185.0	35.0
TLV70533YFPR	DSBGA	YFP	4	3000	182.0	182.0	17.0
TLV70533YFPT	DSBGA	YFP	4	250	182.0	182.0	17.0
TLV70534YFPR	DSBGA	YFP	4	3000	182.0	182.0	17.0
TLV70534YFPT	DSBGA	YFP	4	250	182.0	182.0	17.0
TLV70536YFPR	DSBGA	YFP	4	3000	182.0	182.0	17.0
TLV70536YFPT	DSBGA	YFP	4	250	182.0	182.0	17.0

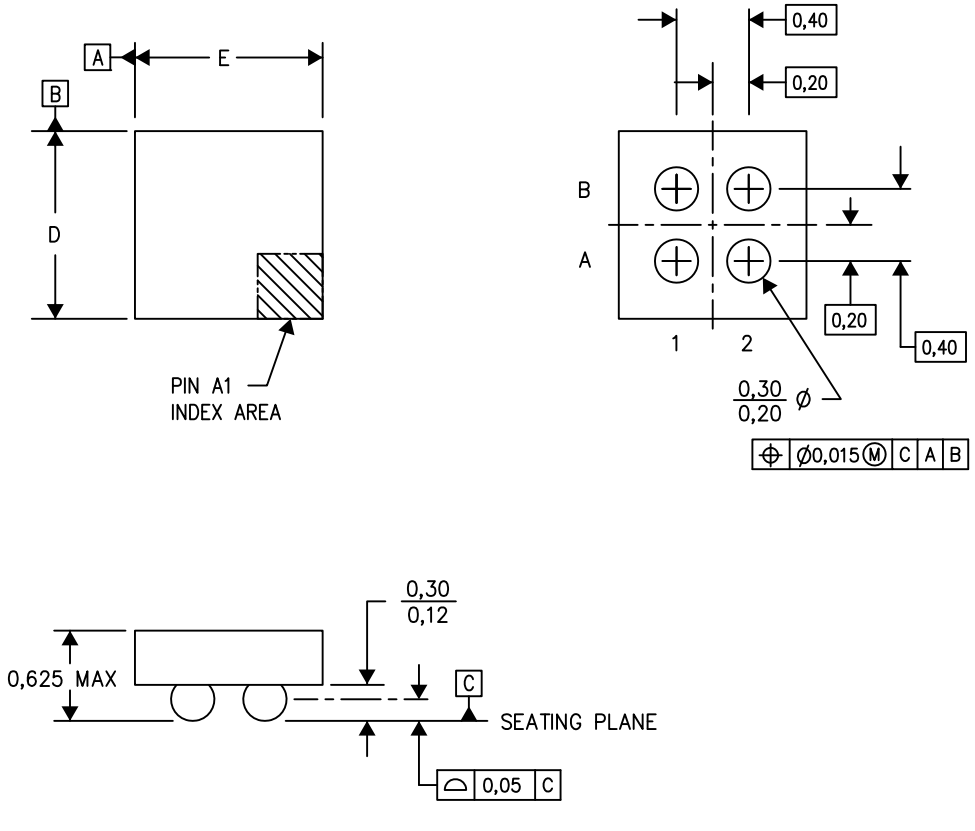
YFP (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments

YFF (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY



D: Max = 0.806 mm, Min =0.746 mm

E: Max = 0.806 mm, Min =0.746 mm

4207625–2/AN 07/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

PowerPAD is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265