150-mA, Low-Dropout Regulator with Foldback Current Limit for Portable Devices

Check for Samples: TLV717xx, TLV717xxP

FEATURES

- **Very Low Dropout: 215 mV at 150 mA**
- **Accuracy: 0.5% (typical)**
- **Low I_Q: 35 µA**
- **Available in Fixed-Output Voltages: 1.2 V to 5.0 V(1)**
- **High PSRR:**
  - **70 dB at 1 kHz**
  - **50 dB at 1 MHz**
- **Stable with Effective Output Capacitance: 0.1 µF(2)**
- **Foldback Current Limit**
- **Package: 1-mm × 1-mm DQN**

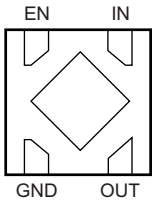
(1) See the Package Option Addendum at the end of this document for a complete list of available voltage options.

(2) See the *Input and Output Capacitor Requirements* section in the *Application Information* for more details.

APPLICATIONS

- **Wireless Handsets, Smart Phones, PDAs**
- **MP3 Players**
- **Other Hand-Held Products**

TLV717xx
1-mm x 1-mm DQN
(Bottom View)



DESCRIPTION

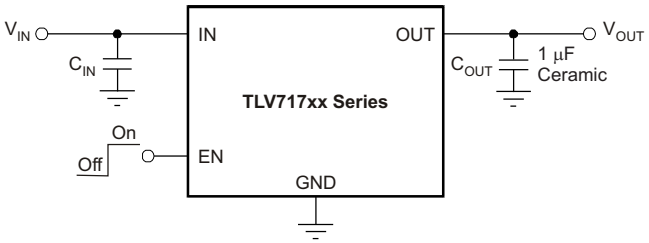
The TLV717xx series of low-dropout (LDO) linear regulators are low quiescent current LDOs with excellent line and load transient performance and are designed for power-sensitive applications. These devices provide a typical accuracy of 0.5%.

The TLV717xx series offer current foldback that throttles down the output current with a decrease in load resistance. The typical value at which current foldback initiates is 350 mA; the typical value of the output short current limit value is 40 mA.

Furthermore, these devices are stable with an effective output capacitance of only 0.1 µF. This feature enables the use of cost-effective capacitors that have higher bias voltages and temperature derating. The devices regulate to specified accuracy with no output load.

The TLV717xx series is available in a 1-mm × 1-mm DQN package that makes them ideal for hand-held applications. The TLV717xxP provides an active pull-down circuit to quickly discharge output loads.

Typical Application Circuit



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}
TLV717**xx(x)Pyyyz**	**XX(X)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 475 = 4.75 V). **P** is optional; devices with P have an LDO regulator with an active output discharge. **YYY** is the package designator. **Z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

At T_J = –25°C, unless otherwise noted. All voltages are with respect to GND.

		VALUE		UNIT
		MIN	MAX	
Voltage	Input range, V_{IN}	–0.3	6.0	V
	Enable range, V_{EN}	–0.3	V_{IN} + 0.3	V
	Output range, V_{OUT}	–0.3	6.0	V
Current	Maximum output, I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation, P_{DISS}		See Thermal Information table		
Temperature	Junction range, T_J	–55	+150	°C
	Storage junction range, T_{stg}	–55	+150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM)		2000	V
	Charged device model (CDM)		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TLV717xx TLV717xxP	UNITS
		DQN	
		4 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	393.3	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	140.3	
θ_{JB}	Junction-to-board thermal resistance	330	
ψ_{JT}	Junction-to-top characterization parameter	6.5	
ψ_{JB}	Junction-to-board characterization parameter	329	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	147.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

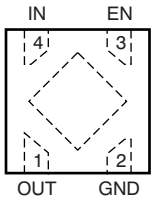
ELECTRICAL CHARACTERISTICS

At operating temperature range (T_A = –40°C to +85°C), T_A = +25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.7 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF, unless otherwise noted.

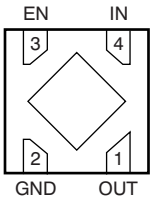
PARAMETER		TEST CONDITIONS		TLV717			UNIT
				MIN	TYP	MAX	
V_{IN}	Input voltage range			1.7		5.5	V
V_{OUT}	Output voltage range			1.2		5.0	V
I_{OUT}	Output current			150			mA
	DC output accuracy	T_A = +25°C			0.5		%
		V_{OUT} ≥ 1.2 V, –40°C ≤ T_A ≤ +85°C		–1.5		+1.5	%
		V_{OUT} ≤ 1.2 V				25	mV
$\Delta V_O/V_{IN}$	Line regulation	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V			1	5	mV
$\Delta V_O/I_{OUT}$	Load regulation	0 mA ≤ I_{OUT} ≤ 150 mA			10	20	mV
V_{DO}	Dropout voltage	V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 150 mA	1.2 V ≤ V_{OUT} < 1.5 V		330	500	mV
			1.5 V ≤ V_{OUT} < 1.8 V		330	450	mV
			1.8 V ≤ V_{OUT} ≤ 5.0 V		215	350	mV
I_{GND}	Ground pin current	I_{OUT} = 0 mA			35	55	µA
I_{SHDN}	Shutdown current	V_{EN} ≤ 0.4 V, 2.0 V ≤ V_{IN} ≤ 4.5 V			0.1	0.5	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 30 mA	f = 10 Hz		70		dB
			f = 100 Hz		70		dB
			f = 1 kHz		65		dB
			f = 10 kHz		60		dB
			f = 100 kHz		43		dB
V_{NOISE}	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA			55		μV_{RMS}
t_{STR}	Startup time	C_{OUT} = 1.0 µF, I_{OUT} = 150 mA			100		µs
I_{SC}	Short current limit	V_{IN} = min ($V_{OUT(NOM)}$ + 1 V, 5.5 V), V_{OUT} = 0 V			40		mA
V_{HI}	Enable high (enabled)			0.9		V_{IN}	V
V_{LO}	Enable low (disabled)			0		0.4	V
I_{EN}	EN pin current	EN = 5.5 V			0.01		µA
$R_{PULLDOWN}$	Pull-down resistor (TLV717xxP only)				120		Ω
UVLO	Undervoltage lockout	V_{IN} rising			1.6		V

PIN CONFIGURATION

DQN PACKAGE
1-mm × 1-mm TBD
(Top View)



DQN PACKAGE
1-mm × 1-mm TBD
(Bottom View)



PIN DESCRIPTIONS

PIN		DESCRIPTION
NAME	NO.	
EN	3	Enable pin. Driving EN over 1.2 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
GND	2	Ground pin
IN	4	Input pin. A small capacitor is recommended from this pin to ground to assure stability. See the *Input and Output Capacitor Requirements* section in the *Application Information* for more details.
OUT	1	Regulated output voltage pin. A small 1-µF ceramic capacitor is recommended from this pin to ground to assure stability. See the *Input and Output Capacitor Requirements* section in the *Application Information* for more details.
Thermal pad	—	It is recommended to connect this pin to GND for improved thermal performance.

FUNCTIONAL BLOCK DIAGRAMS

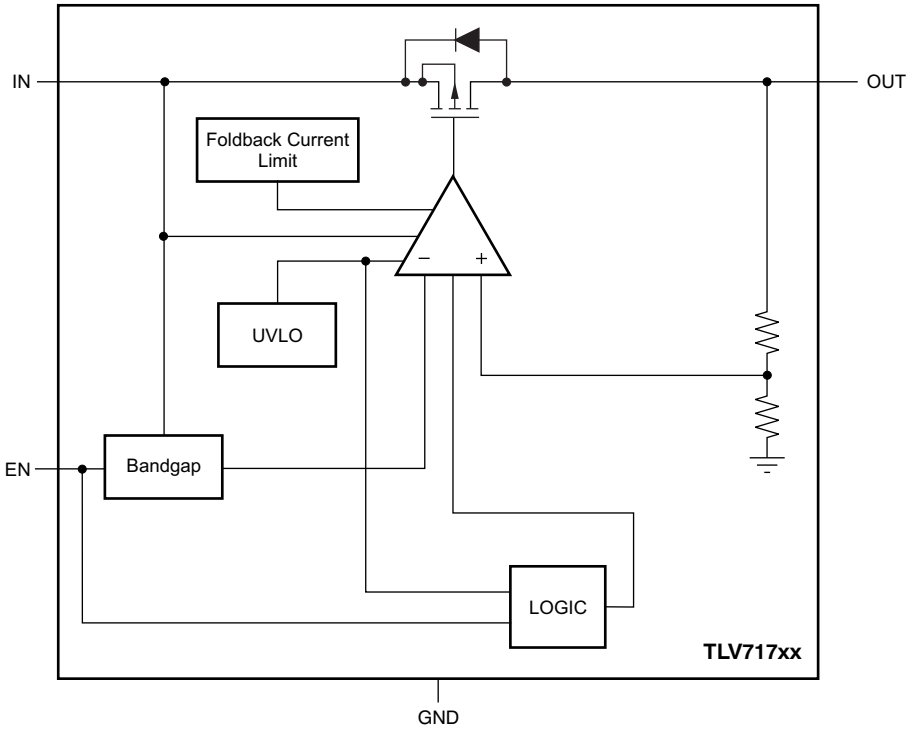


Figure 1. TLV717xx Block Diagram

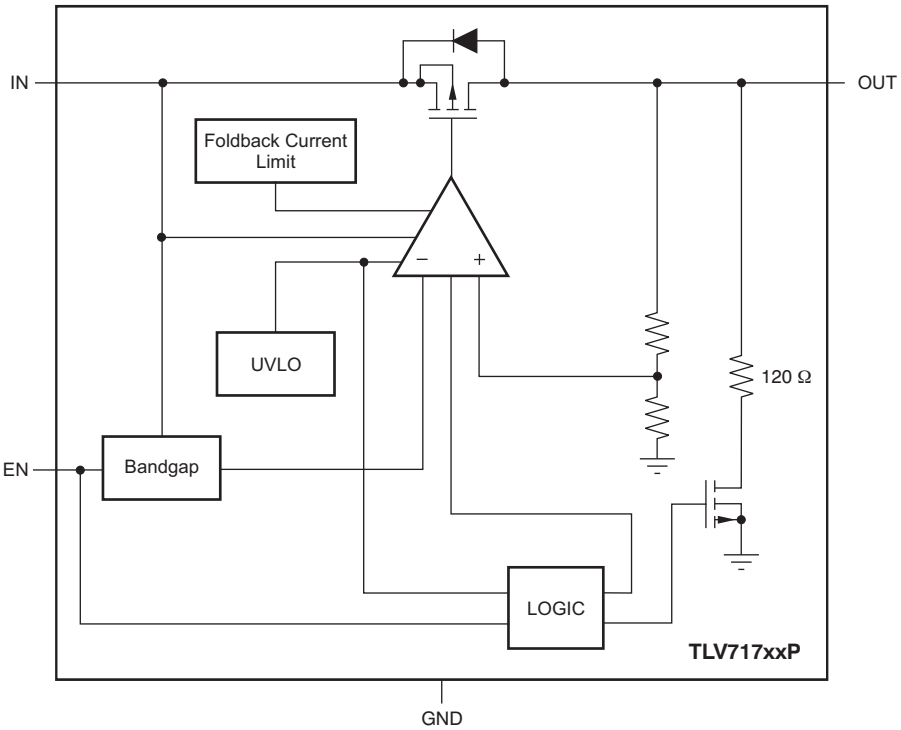


Figure 2. TLV717xxP Block Diagram

TYPICAL CHARACTERISTICS

At operating temperature range (T_A = –40°C to +85°C), T_A = +25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.7 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF, unless otherwise noted.

LOAD REGULATION

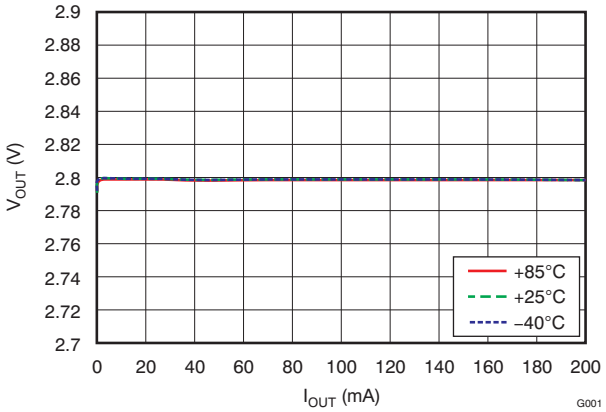


Figure 3.

LINE REGULATION

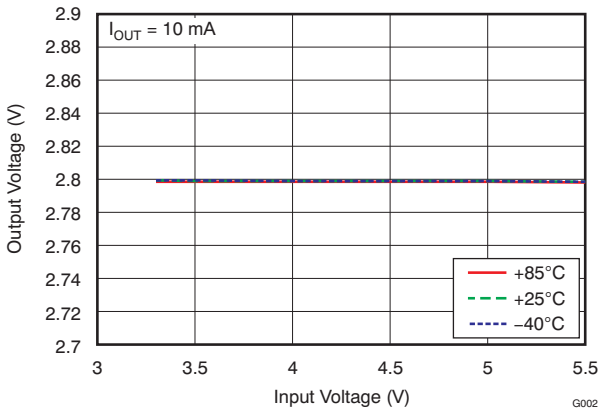


Figure 4.

LINE REGULATION

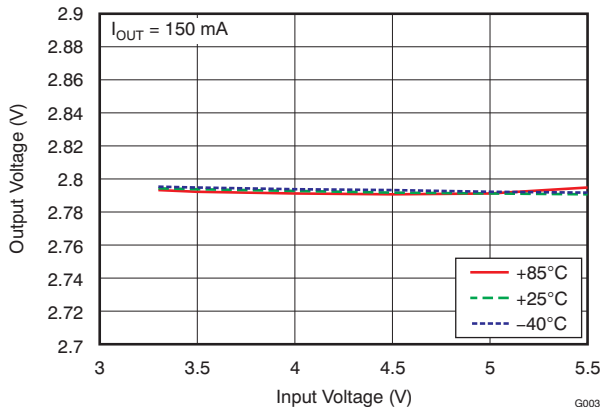


Figure 5.

DROPOUT VOLTAGE vs FIXED OUTPUT VOLTAGE VERSIONS

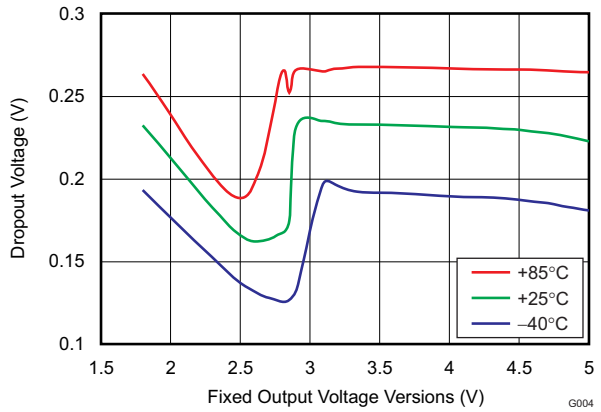


Figure 6.

DROPOUT VOLTAGE vs OUTPUT CURRENT

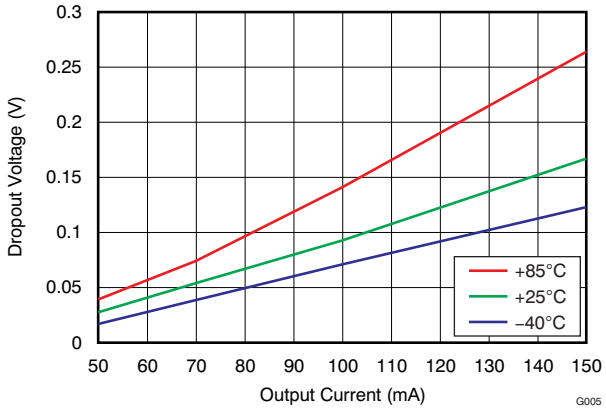


Figure 7.

OUTPUT VOLTAGE vs TEMPERATURE

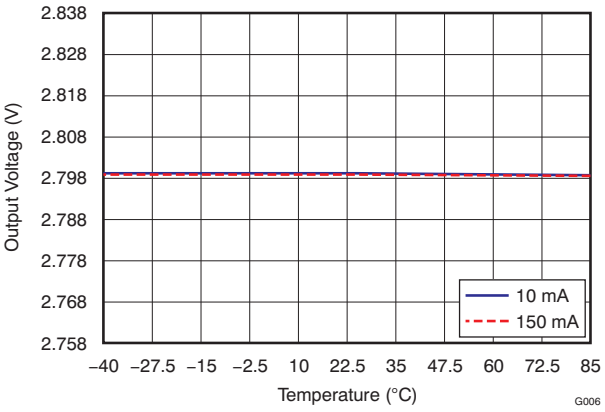


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At operating temperature range (T_A = –40°C to +85°C), T_A = +25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.7 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF, unless otherwise noted.

GROUND PIN CURRENT vs INPUT VOLTAGE

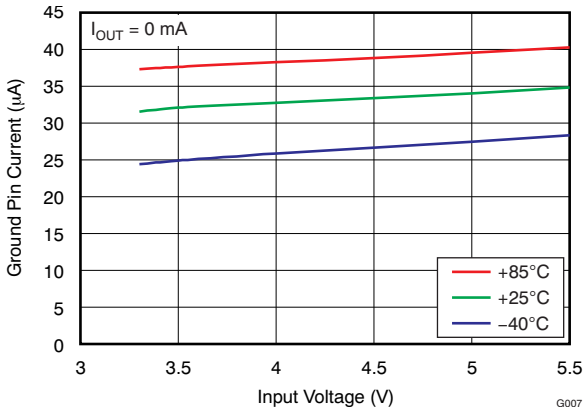


Figure 9.

GROUND PIN CURRENT vs OUTPUT CURRENT

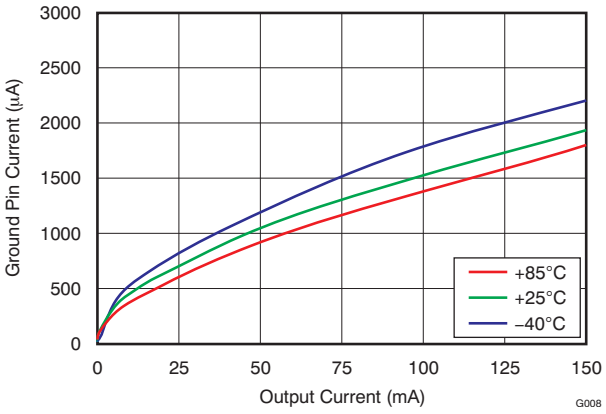


Figure 10.

GROUND PIN CURRENT vs TEMPERATURE

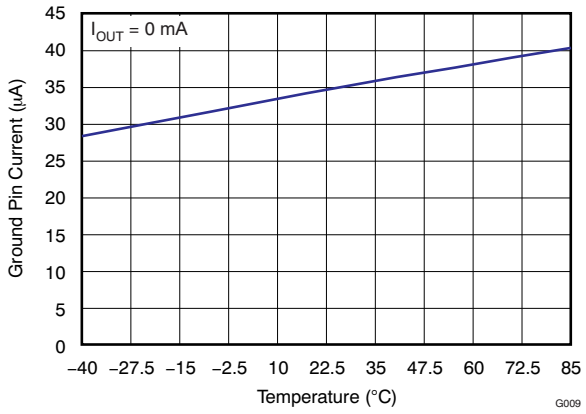


Figure 11.

OUTPUT VOLTAGE vs OUTPUT CURRENT

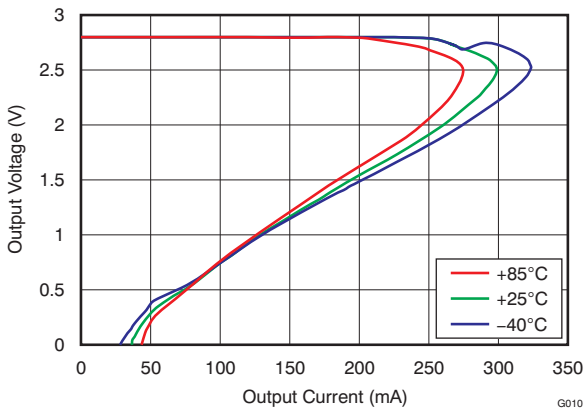


Figure 12.

TLV71728
PSRR vs FREQUENCY

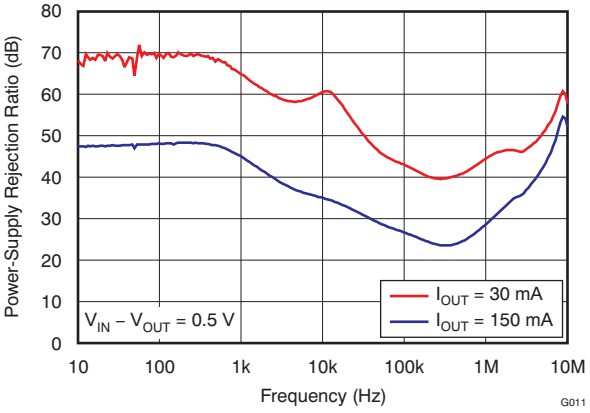


Figure 13.

TLV71728
PSRR vs FREQUENCY

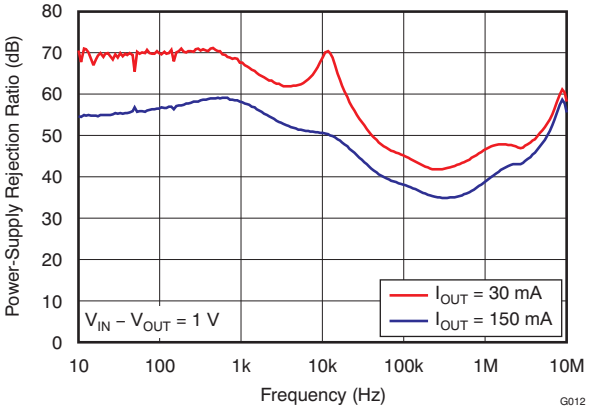


Figure 14.

TYPICAL CHARACTERISTICS (continued)

At operating temperature range (T_A = –40°C to +85°C), T_A = +25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.7 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF, unless otherwise noted.

PSRR vs INPUT VOLTAGE

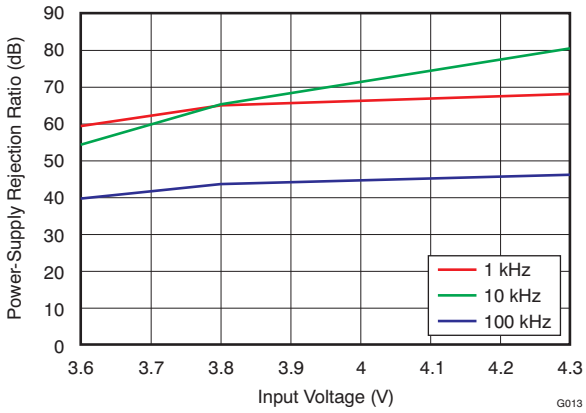


Figure 15.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

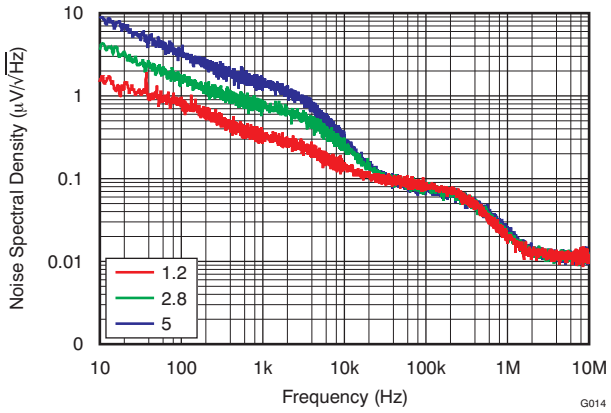


Figure 16.

APPLICATION INFORMATION

The TLV717xx belongs to a new family of next-generation value low-dropout (LDO) regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise, very good PSRR with little (V_{IN} – V_{OUT}) headroom, make this family of devices ideal for RF portable applications.

This family of regulators offers current foldback. Device operating junction temperature is –40°C to +125°C.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. The TLV717xx is designed to be stable with an effective capacitance of 0.1 µF or larger at the output, though a 1-µF ceramic capacitor is recommended for typical applications. Thus, the device is stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1 µF. This effective capacitance refers to the capacitance that the LDO detects under operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of cheaper dielectrics, this capability of being stable with 0.1-µF effective capacitance also enables the use of smaller footprint capacitors that have higher derating in size- and space-constrained applications. Note that using a 0.1-µF rated capacitor at the LDO output does not ensure stability because the effective capacitance under the specified operating conditions would be less than 0.1 µF. Maximum ESR should be less than 200 mΩ.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1.0-µF, low ESR capacitor across the IN and GND pins of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast, rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2 Ω, a 0.1-µF input capacitor may be necessary to ensure stability.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

Input and output capacitors should be placed as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the device GND pin. In addition, the output capacitor ground connection should be connected directly to the device GND pin. High ESR capacitors may degrade PSRR performance.

INTERNAL CURRENT LIMIT

The TLV717xx has an internal foldback current limit that helps to protect the regulator during fault conditions. The current supplied by the device is gradually throttled down as the output voltage decreases. When the output is shorted, the LDO supplies a typical current of 40 mA. Output voltage is not regulated when the device is in current limit, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The advantage of foldback current limit is that the I_{LIMIT} value is less than the fixed current limit. Therefore, the power that the PMOS pass transistor dissipates [(V_{IN} – V_{OUT}) × I_{LIMIT}] is much less.

The TLV717xx PMOS pass element has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

SHUTDOWN

The enable pin (EN) is active high. The device is enabled when the voltage at the EN pin goes above 0.9 V. This relatively lower voltage value required to turn the LDO on can be exploited to power the LDO with a GPIO of recent processors whose GPIO logic 1 voltage level is lower than traditional microcontrollers. The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, EN can be connected to the IN pin.

DROPOUT VOLTAGE

The TLV717xx uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout. As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude but increases the duration of the transient response.

UNDERVOLTAGE LOCKOUT (UVLO)

The TLV717xx uses an undervoltage lockout circuit (UVLO = 1.6 V) to keep the output shut off until the internal circuitry operates properly.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to ambient air. Performance data for JEDEC-low and high-K boards are given in the Thermal Information table. Using heavier copper increases the effectiveness in removing heat from the device. The addition, plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 1.

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (1)$$

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2011) to Revision A	Page
• Changed document status from Product Preview to Production Data	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLV71712PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UX	Samples
TLV71712PDQNR3	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UX	Samples
TLV71712PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UX	Samples
TLV71713PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VC	Samples
TLV71713PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VC	Samples
TLV71715PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UY	Samples
TLV71715PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UY	Samples
TLV717185PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VN	Samples
TLV717185PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VN	Samples
TLV71718PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UZ	Samples
TLV71718PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UZ	Samples
TLV71721PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AR	Samples
TLV71721PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AR	Samples
TLV71725PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VA	Samples
TLV71725PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VA	Samples
TLV71727PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AS	Samples
TLV71727PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AS	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLV717285PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VE	Samples
TLV717285PQNR	PREVIEW	X2SON	DQN	5	3000	TBD	Call TI	Call TI	-40 to 85		
TLV71728PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VD	Samples
TLV71728PDQNR3	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VD	Samples
TLV71728PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VD	Samples
TLV71729PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VI	Samples
TLV71729PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VI	Samples
TLV71730PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VF	Samples
TLV71730PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VF	Samples
TLV71733PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VG	Samples
TLV71733PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VG	Samples
TLV71736PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VH	Samples
TLV71736PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

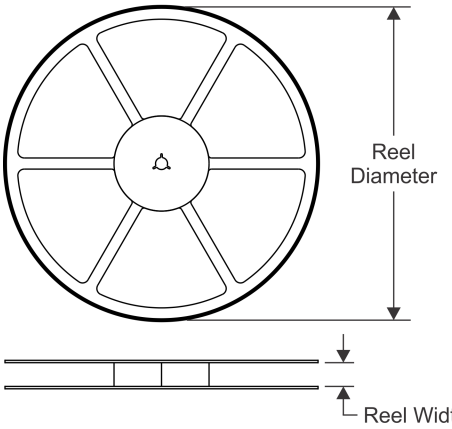
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

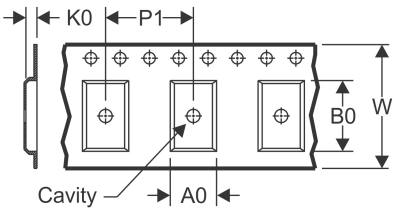
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

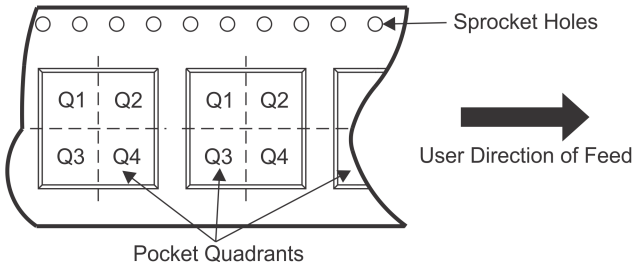


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

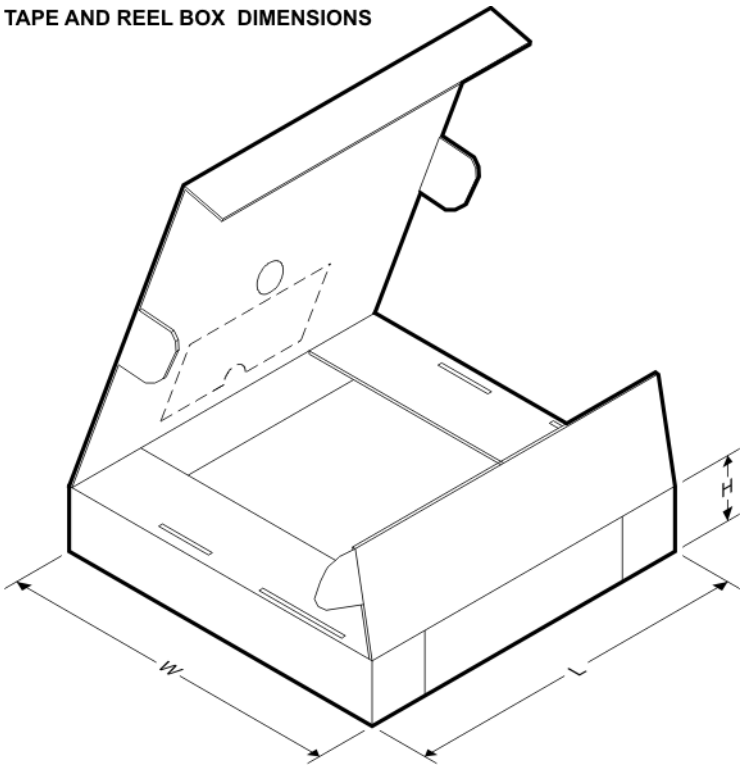


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV71712PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71712PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71712PDQNR3	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	2.0	8.0	Q3
TLV71712PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71712PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71713PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71713PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71713PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71713PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71715PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71715PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71715PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71715PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV717185PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV717185PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV717185PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV717185PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71718PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV71718PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71718PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71718PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71721PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71721PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71721PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71721PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71725PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71725PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71725PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71725PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71727PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71727PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71727PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71727PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV717285PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV717285PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71728PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71728PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71728PDQNR3	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	2.0	8.0	Q3
TLV71728PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71728PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71729PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71729PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71729PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71729PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71730PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71730PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71730PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71730PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71733PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71733PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71733PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71733PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71736PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71736PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71736PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71736PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

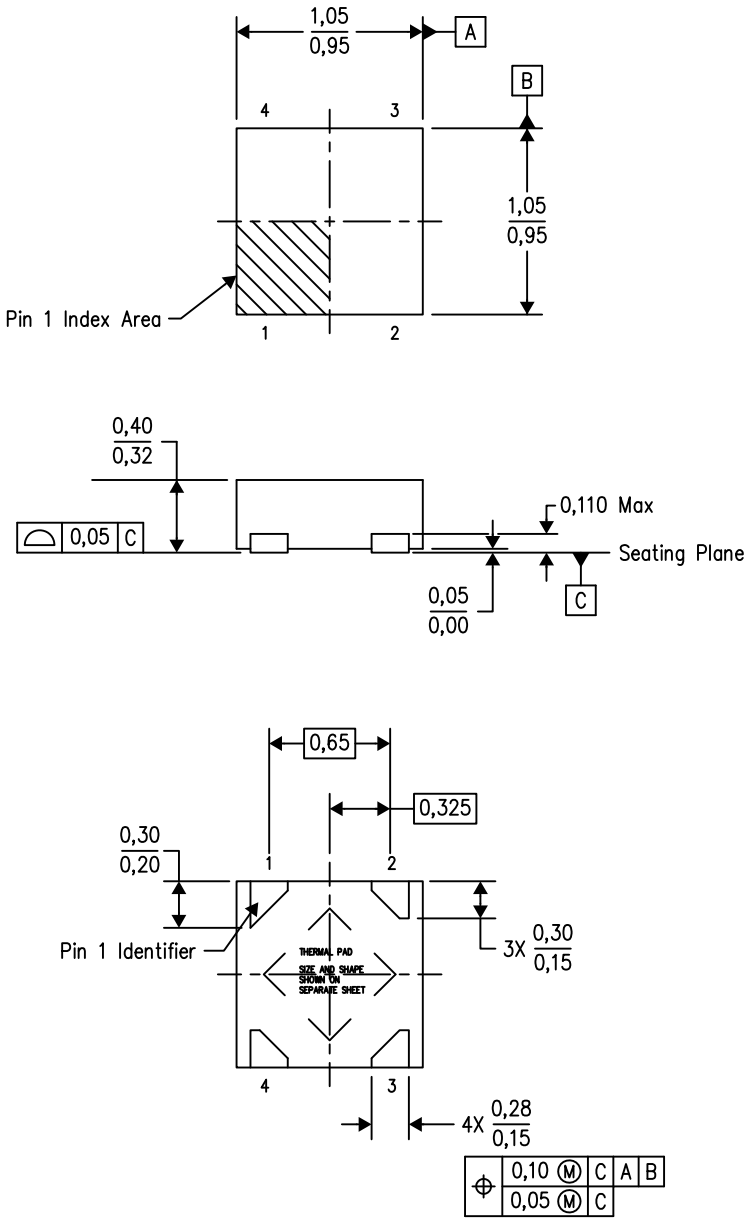


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV71712PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV71712PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV71712PDQNR3	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV71712PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV71712PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV71713PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV71713PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV71713PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV71713PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV71715PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV71715PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV71715PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV71715PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV717185PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV717185PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV717185PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV717185PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV71718PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV71718PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV71718PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV71718PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV71721PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV71721PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV71721PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV71721PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV71725PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV71725PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV71725PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV71725PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV71727PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV71727PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV71727PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV71727PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV717285PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV717285PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV71728PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV71728PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV71728PDQNR3	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV71728PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV71728PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV71729PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV71729PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV71729PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV71729PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV71730PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV71730PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV71730PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV71730PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV71733PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV71733PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV71733PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV71733PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV71736PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV71736PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV71736PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV71736PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0

DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD



4210367/D 09/2012

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

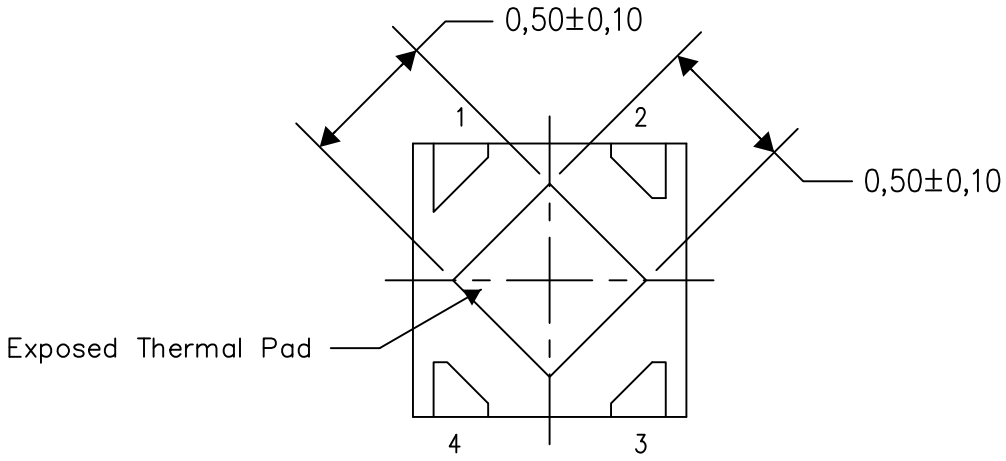
DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



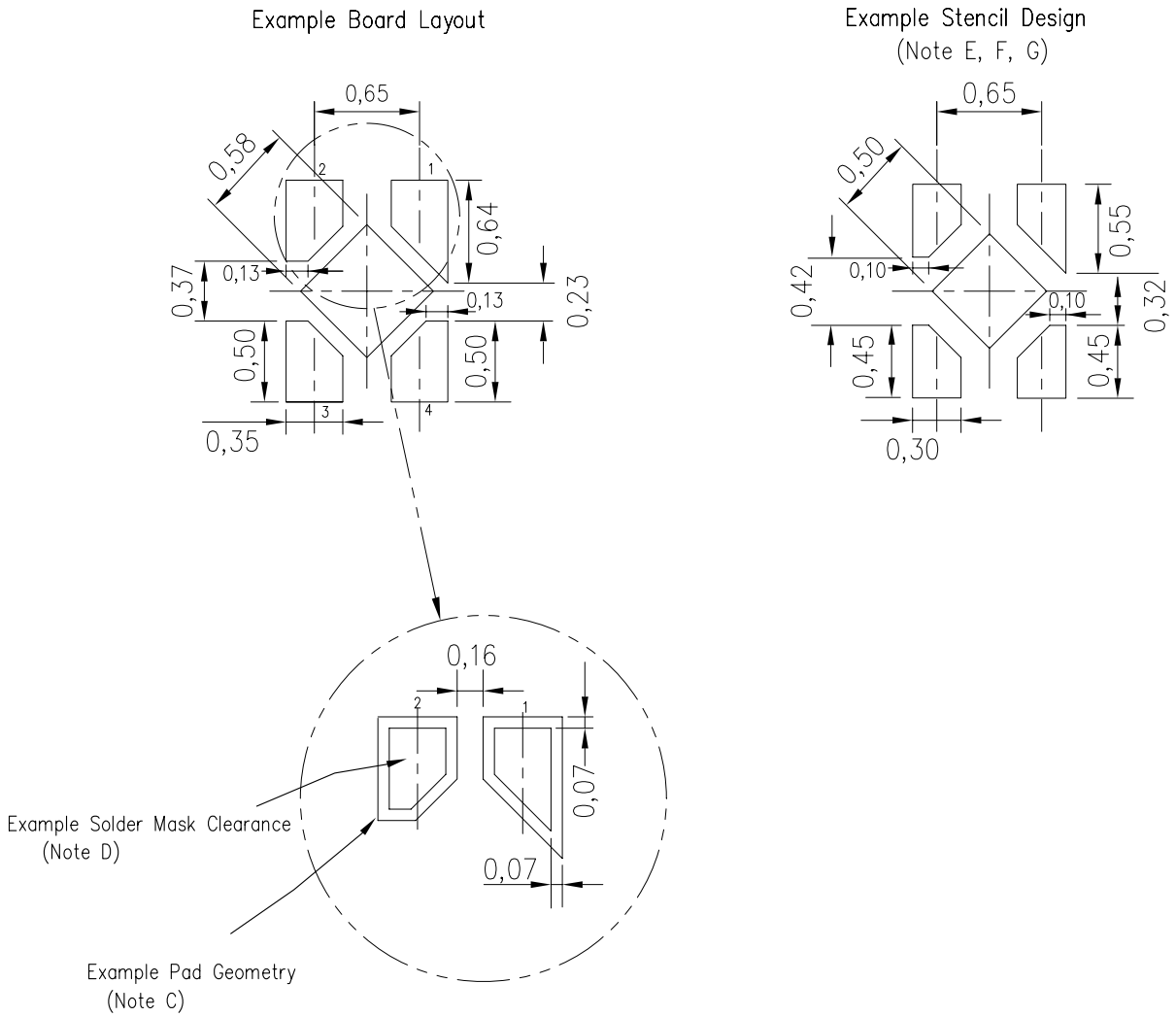
Bottom View

Exposed Thermal Pad Dimensions

4210393–2/E 04/12

NOTE: All linear dimensions are in millimeters

DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

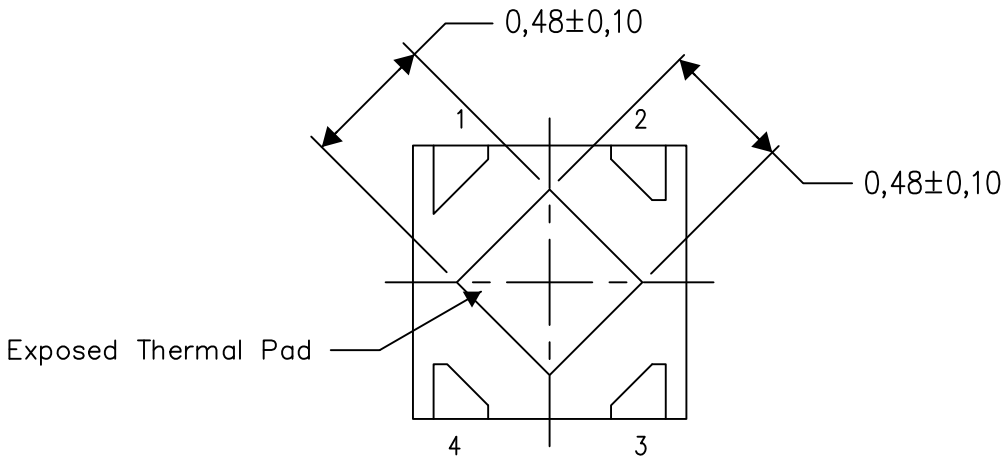
DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



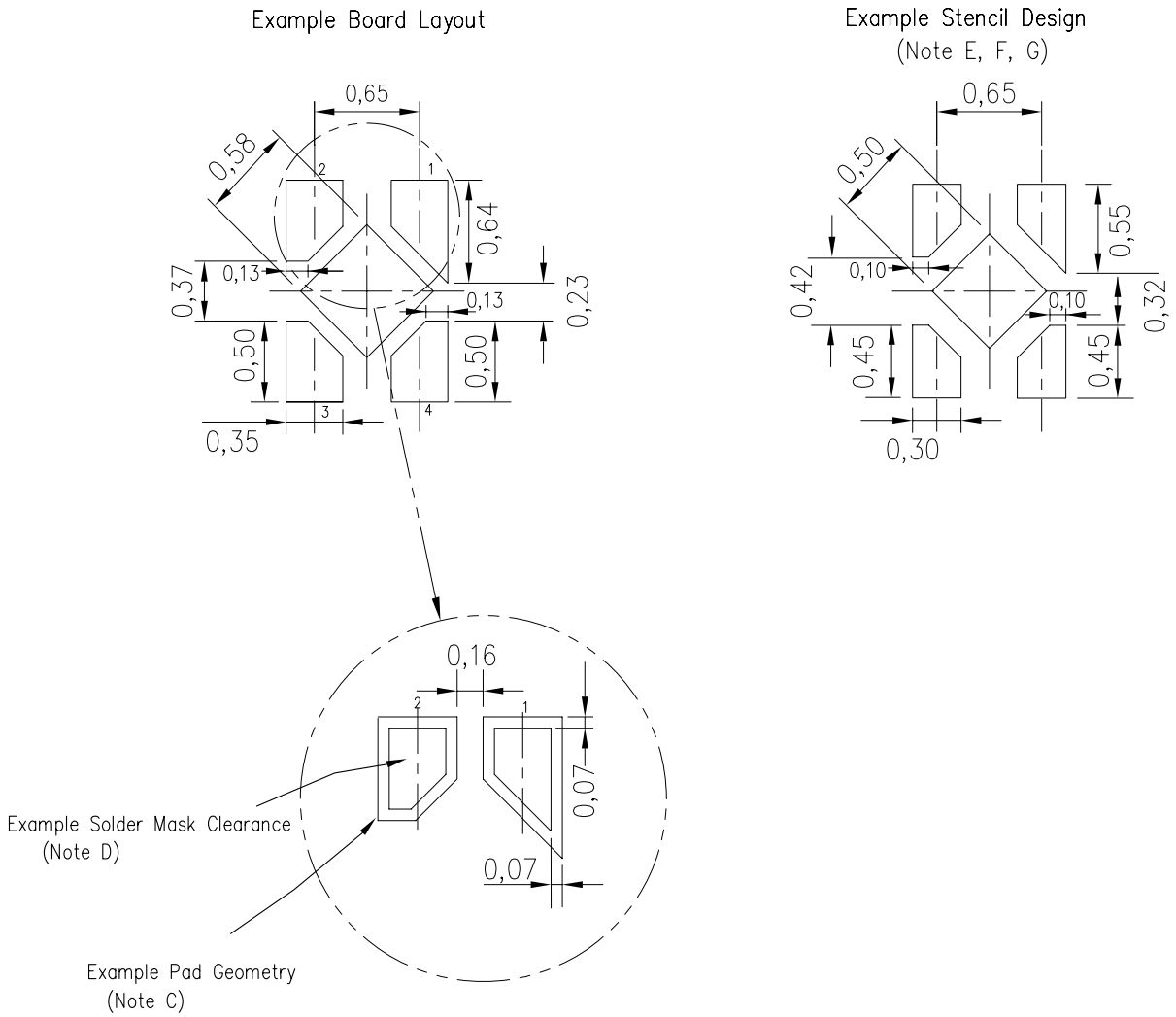
Bottom View

Exposed Thermal Pad Dimensions

4210393–3/E 04/12

NOTE: All linear dimensions are in millimeters

DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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