DIGITAL TEMPERATURE SENSOR WITH I²C INTERFACE

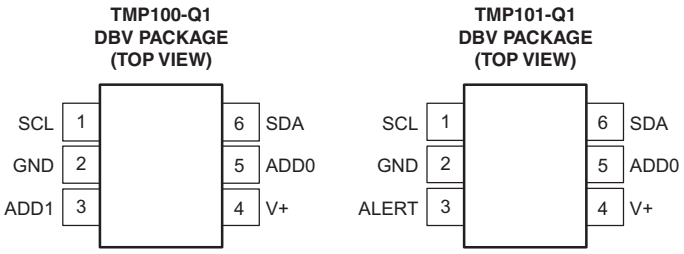
Check for Samples: TMP100-Q1, TMP101-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Digital Output: I²C Serial 2-Wire**
- **Resolution: 9- to 12-Bits, User-Selectable**
- **Accuracy: ±2.0°C from −25°C to 85°C (max)**
  ±3.0°C from −40°C to 125°C (max)
- **Low Quiescent Current: 45 µA, 0.1 µA Standby**
- **Wide Supply Range: 2.7 V to 5.5 V**
- **Tiny SOT23-6 Package**

APPLICATIONS

- **Power-Supply Temperature Monitoring**
- **Computer Peripheral Thermal Protection**
- **Battery Management**
- **Thermostat Controls**
- **Electromechanical Device Temperature**



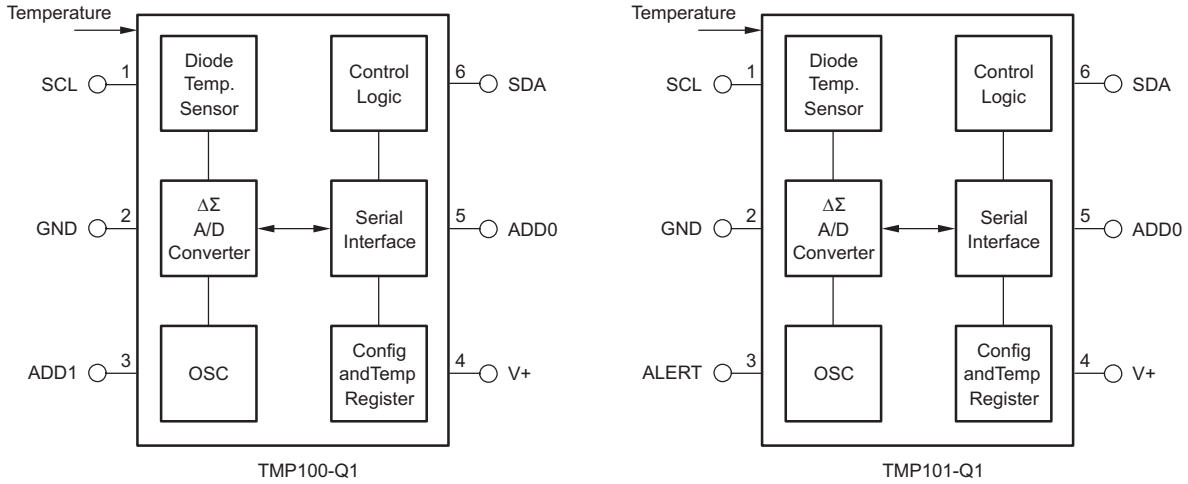
DESCRIPTION

The TMP100-Q1-Q1 and TMP101-Q1 are two-wire, serial output temperature sensors available in SOT23-6 packages. Requiring no external components, the TMP100-Q1-Q1 and TMP101-Q1 are capable of reading temperatures with a resolution of 0.0625°C.

The TMP100-Q1-Q1 and TMP101-Q1 feature SMBus and I²C interface compatibility, with the TMP100-Q1 allowing up to eight devices on one bus. The TMP101-Q1 offers SMBus alert function with up to three devices per bus.

The TMP100-Q1 and TMP101-Q1 are ideal for extended temperature measurement in a variety of communication, computer, consumer, environmental, industrial, and instrumentation applications.

The TMP100-Q1 and TMP101-Q1 are specified for operation over a temperature range of −40°C to 125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOT23-6 - DBV	Reel of 2000	TMP100NAQDBVRQ1	PREVIEW
			TMP101NAQDBVRQ1	DUGQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Power supply			7.5	V
V_I	Input voltage range(2)		–0.5	7.5	V
T_A	Operating temperature range		–40	125	°C
T_{stg}	Storage temperature range		–65	150	°C
$T_{J\ max}$	Junction temperature			150	°C
	ESD rating	Human Body Model		2000	V
		Machine Model		200	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input voltage rating applies to all TMP100-Q1 and TMP101-Q1 input voltages.

ELECTRICAL CHARACTERISTICS

at T_A = −40°C to 125°C and V_+ = 2.7 V to 5.5 V, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Temperature Input					
Range		−40		125	°C
Accuracy (temperature error)	−25°C to 85°C		±0.5	±2.0	°C
	−40°C to 125°C		±1.0	±3.0	
Resolution	Selectable		±0.0625		°C
Digital Input/Output					
High-level input logic, V_{IH}		0.7(V+)		6.0	V
Low-level input logic, V_{IL}		−0.5		0.3(V+)	V
Input current, I_{IN}	0 V ≤ V_{IN} ≤ 6 V			1	µA
V_{OL} SDA output logic level	I_{OL} = 3mA	0	0.15	0.4	V
V_{OL} ALERT output logic level	I_{OL} = 4mA	0	0.15	0.4	V
Resolution	Selectable		9 to 12		Bits
Conversion time	9-Bit		40	75	ms
	10-Bit		80	150	
	11-Bit		160	300	
	12-Bit		320	600	

ELECTRICAL CHARACTERISTICS (continued)

at T_A = −40°C to 125°C and V_+ = 2.7 V to 5.5 V, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Conversion rate	9-Bit		25		s/s
	10-Bit		12		
	11-Bit		6		
	12-Bit		3		
Power Supply					
Operating range		2.7		5.5	V
Quiescent current, I_Q	Serial bus inactive		45	75	µA
	Serial bus active, SCL frequency = 400 kHz		70		
	Serial bus active, SCL frequency = 3.4 MHz		150		
Shutdown Current, I_{SD}	Serial bus inactive		0.1	1	µA
	Serial bus active, SCL frequency = 400 kHz		20		
	Serial bus active, SCL frequency = 3.4 MHz		100		
Temperature Range					
Specified range		−40		125	°C
Storage range		−60		150	°C
Thermal resistance, θJ_A	SOT23-6 surface-mount		200		°C/W

TYPICAL CHARACTERISTICS

at T_A = 25°C and V_+ = 5.0 V, unless otherwise noted.

QUIESCENT CURRENT vs TEMPERATURE

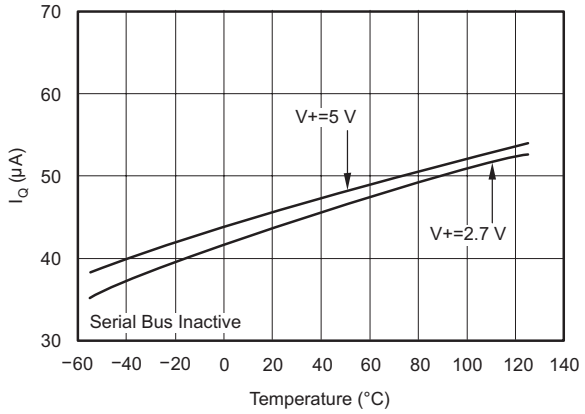


Figure 1.

SHUTDOWN CURRENT vs TEMPERATURE

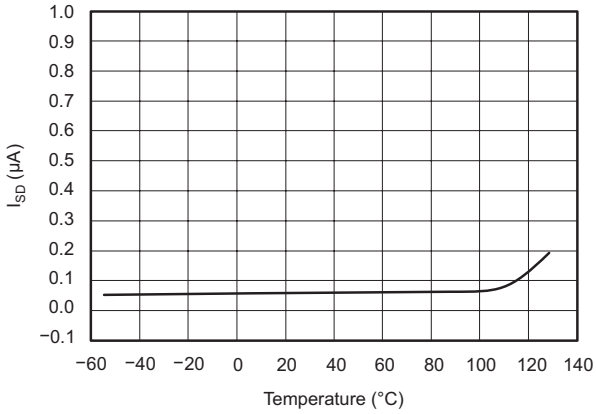


Figure 2.

CONVERSION TIME vs TEMPERATURE

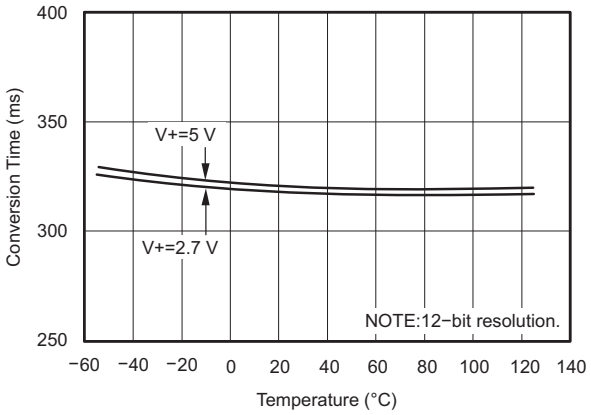


Figure 3.

TEMPERATURE ACCURACY vs TEMPERATURE

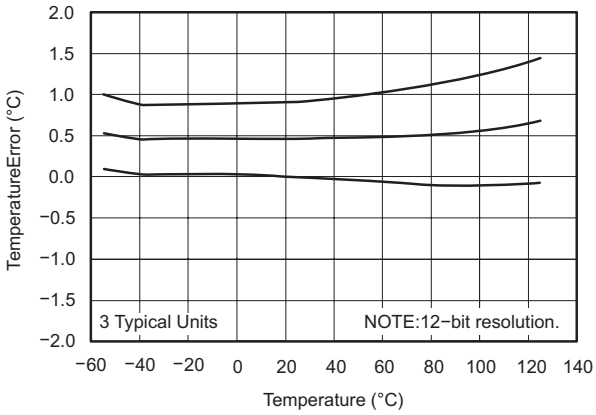


Figure 4.

QUIESCENT CURRENT WITH BUS ACTIVITY vs TEMPERATURE

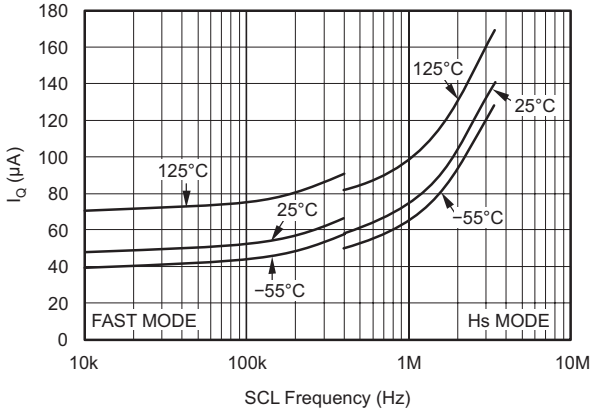


Figure 5.

APPLICATION INFORMATION

The TMP100-Q1 and TMP101-Q1 are digital temperature sensors optimal for thermal management and thermal protection applications. The TMP100-Q1 and TMP101-Q1 are I^2C and SMBus interface-compatible and are specified over a temperature range of −40°C to 125°C.

The TMP100-Q1 and TMP101-Q1 require no external components for operation except for pull-up resistors on SCL, SDA, and ALERT, although a 0.1µF bypass capacitor is recommended, as shown in Figure 6 and Figure 72.

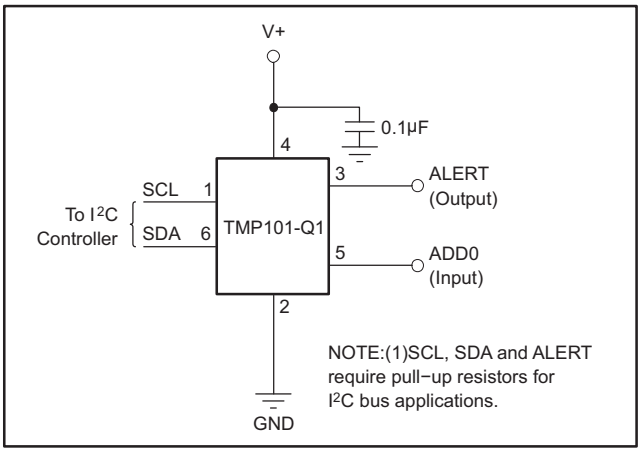


Figure 6. Typical Connections of the TMP101-Q1

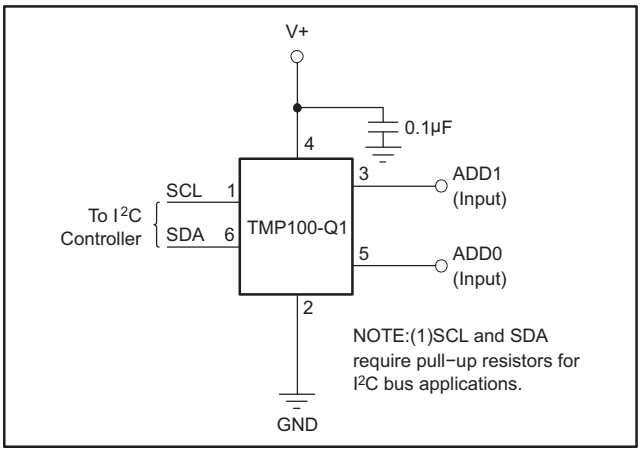


Figure 7. Typical Connections of the TMP100-Q1

The die flag of the lead frame is connected to pin 2. The sensing device of the TMP100-Q1 and TMP101-Q1 is the chip itself. Thermal paths run through the package leads as well as the plastic package. The lower thermal resistance of metal causes the leads to provide the primary thermal path. The GND pin of the TMP100-Q1 or TMP101-Q1 is directly connected to the metal lead frame, and is the best choice for thermal input.

To maintain the accuracy in applications requiring air or surface temperature measurement, care should be taken to isolate the package and leads from ambient air temperature. A thermally-conductive adhesive will assist in achieving accurate surface temperature measurement.

POINTER REGISTER

Figure 8 shows the internal register structure of the TMP100-Q1 and TMP101-Q1. The 8-bit Pointer Register of the TMP100-Q1 and TMP101-Q1 is used to address a given data register. The Pointer Register uses the two LSBs to identify which of the data registers should respond to a read or write command. Table 1 identifies the bits of the Pointer Register byte. Table 2 describes the pointer address of the registers available in the TMP100-Q1 and TMP101-Q1. Power-up Reset value of P1/P0 is 00.

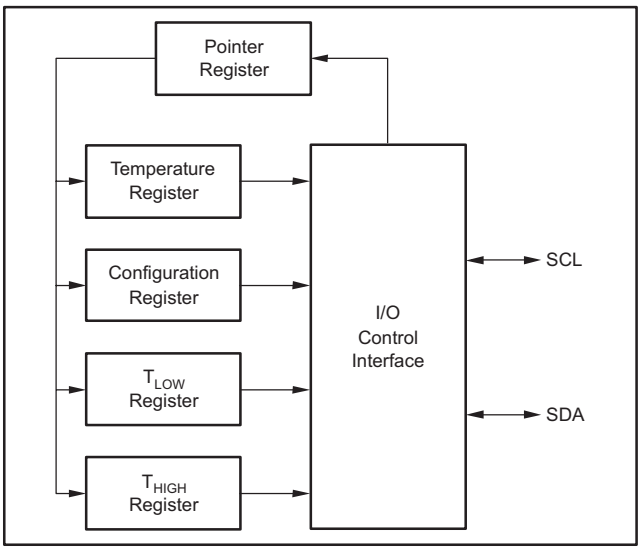


Figure 8. Internal Register Structure of the TMP100-Q1 and TMP101-Q1

Table 1. Pointer Register Type

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register Bits	

Table 2. Pointer Addresses of the TMP100-Q1 and TMP101-Q1 Registers

P1	P0	REGISTER
0	0	Temperature Register (READ Only)
0	1	Configuration Register (READ/WRITE)
1	0	T_{LOW} Register (READ/WRITE)
1	1	T_{HIGH} Register (READ/WRITE)

TEMPERATURE REGISTER

The Temperature Register of the TMP100-Q1 or TMP101-Q1 is a 12-bit read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data and are described in Table 3 and Table 4. The first 12 bits are used to indicate temperature with all remaining bits equal to zero. Data format for temperature is summarized in Table 5. Following power-up or reset, the Temperature Register will read 0°C until the first conversion is complete.

Table 3. Byte 1 of Temperature Register

D7	D6	D5	D4	D3	D2	D1	D0
T11	T10	T9	T8	T7	T6	T5	T4

Table 4. Byte 2 of Temperature Register

D7	D6	D5	D4	D3	D2	D1	D0
T3	T2	T1	T0	0	0	0	0

Table 5. Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
128	0111 1111 1111	7FF
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0.0	0000 0000 0000	000
−0.25	1111 1111 1100	FFC
−25	1110 0111 0000	E70
−55	1100 1001 0000	C90
−128	1000 0000 0000	800

The user can obtain 9, 10, 11, or 12 bits of resolution by addressing the Configuration Register and setting the resolution bits accordingly. For 9-, 10-, or 11-bit resolution, the most significant bits in the Temperature Register are used with the unused LSBs set to zero.

CONFIGURATION REGISTER

The Configuration Register is an 8-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read/write operations are performed MSB first. The format of the Configuration Register for the TMP100-Q1 and TMP101-Q1 is shown in Table 6, followed by a breakdown of the register bits. The power-up/reset value of the Configuration Register is all bits equal to 0. The OS/ALERT bit will read as 1 after power-up/reset.

Table 6. Configuration Register Format

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	OS/ ALERT	R1	R0	F1	F0	POL	TM	SD

SHUTDOWN MODE (SD)

The Shutdown Mode of the TMP100-Q1 and TMP101-Q1 allows the user to save maximum power by shutting down all device circuitry other than the serial interface, which reduces current consumption to less than 1μA. For the TMP100-Q1 and TMP101-Q1, Shutdown Mode is enabled when the SD bit is 1. The device will shutdown once the current conversion is completed. For SD equal to 0, the device will maintain continuous conversion.

THERMOSTAT MODE (TM)

The Thermostat Mode bit of the TMP101-Q1 indicates to the device whether to operate in Comparator Mode (TM = 0) or Interrupt Mode (TM = 1). For more information on comparator and interrupt modes, see the HIGH and LOW Limit Registers section.

POLARITY (POL)

The Polarity Bit of the TMP101-Q1 allows the user to adjust the polarity of the ALERT pin output. If POL = 0, the ALERT pin will be active LOW, as shown in Figure 9. For POL = 1 the ALERT pin will be active HIGH, and the state of the ALERT pin is inverted.

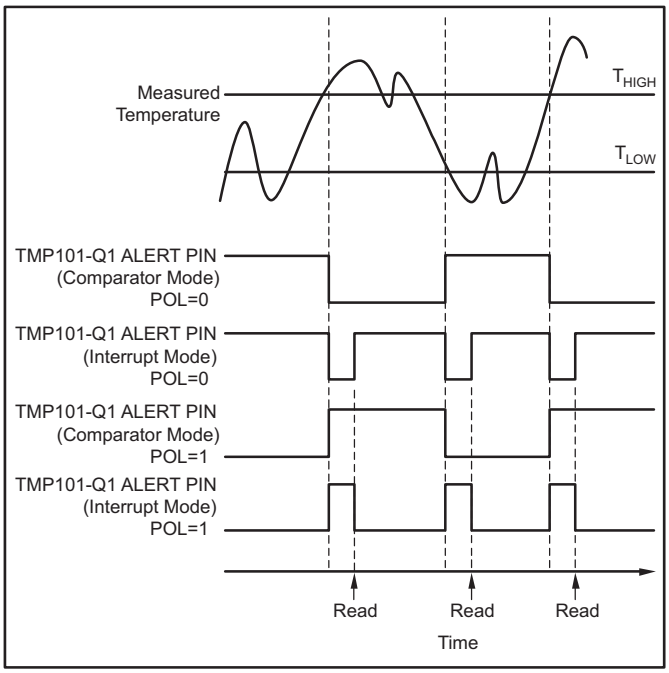


Figure 9. Output Transfer Function Diagrams

FAULT QUEUE (F1/F0)

A fault condition occurs when the measured temperature exceeds the user-defined limits set in the T_{HIGH} and T_{LOW} Registers. Additionally, the number of fault conditions required to generate an alert may be programmed using the Fault Queue. The Fault Queue is provided to prevent a false alert due to environmental noise. The Fault Queue requires consecutive fault measurements in order to trigger the alert function. If the temperature falls below T_{LOW}, prior to reaching the number of programmed consecutive faults limit, the count is reset to 0. Table 7 defines the number of measured faults that may be programmed to trigger an alert condition in the device.

Table 7. Fault Settings of the TMP100-Q1 and TMP101-Q1

F1	F0	CONSECUTIVE FAULTS
0	0	1
0	1	2
1	0	4
1	1	6

CONVERTER RESOLUTION (R1/R0)

The Converter Resolution Bits control the resolution of the internal Analog-to-Digital (A/D) converter. This allows the user to maximize efficiency by programming for higher resolution or faster conversion time. Table 8 identifies the Resolution Bits and relationship between resolution and conversion time.

Table 8. Resolution of the TMP100-Q1 and TMP101-Q1

R1	R0	RESOLUTION	CONVERSION TIME (typical)
0	0	9 Bits (0.5°C)	40 ms
0	1	10 Bits (0.25°C)	80 ms
1	0	11 Bits (0.125°C)	160 ms
1	1	12 Bits (0.0625°C)	320 ms

OS/ALERT (OS)

The TMP100-Q1 and TMP101-Q1 feature a One-Shot Temperature Measurement Mode. When the device is in Shutdown Mode, writing a 1 to the OS/ALERT bit will start a single temperature conversion. The device will return to the shutdown state at the completion of the single conversion. This is useful to reduce power consumption in the TMP100-Q1 and TMP101-Q1 when continuous monitoring of temperature is not required.

Reading the OS/ALERT bit will provide information about the Comparator Mode status. The state of the POL bit will invert the polarity of data returned from the OS/ALERT bit. For POL = 0, the OS/ALERT will read as 1 until the temperature equals or exceeds T_{HIGH} for the programmed number of consecutive faults, causing the OS/ALERT bit to read as 0. The OS/ALERT bit will continue to read as 0 until the temperature falls below T_{LOW} for the programmed number of consecutive faults when it will again read as 1. The status of the TM bit does not affect the status of the OS/ALERT bit.

HIGH AND LOW LIMIT REGISTERS

In Comparator Mode (TM = 0), the ALERT pin of the TMP101-Q1 becomes active when the temperature equals or exceeds the value in T_{HIGH} and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin will remain active until the temperature falls below the indicated T_{LOW} value for the same number of faults.

In Interrupt Mode (TM = 1) the ALERT Pin becomes active when the temperature equals or exceeds T_{HIGH} for a consecutive number of fault conditions. The ALERT pin remains active until a read operation of any register occurs or the device successfully responds to the SMBus Alert Response Address. The ALERT pin will also be cleared if the device is placed in Shutdown Mode. Once the ALERT pin is cleared, it will only become active again by the temperature falling below T_{LOW}. When the temperature falls below T_{LOW}, the ALERT pin will become active and remain active until cleared by a read operation of any register or a successful response to the SMBus Alert Response Address. Once the ALERT pin is cleared, the above cycle will repeat with the ALERT pin becoming active when the temperature equals or exceeds T_{HIGH}. The ALERT pin can also be cleared by resetting the device with the General Call Reset command. This will also clear the state of the internal registers in the device returning the device to Comparator Mode (TM = 0).

Both operational modes are represented in . Table 9 and Table 10 describe the format for the T_{HIGH} and T_{LOW} registers. Power-up Reset values for T_{HIGH} and T_{LOW} are: T_{HIGH} = 80°C and T_{LOW} = 75°C. The format of the data for T_{HIGH} and T_{LOW} is the same as for the Temperature Register.

Table 9. Bytes 1 and 2 of T_{HIGH} Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	H11	H10	H9	H8	H7	H6	H5	H4
BYTE	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
2	H3	H2	H1	H0	0	0	0	0

Table 10. Bytes 1 and 2 of T_{LOW} Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	L11	L10	L9	L8	L7	L6	L5	L4
BYTE	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
2	L3	L2	L1	L0	0	0	0	0

All 12 bits for the Temperature, T_{HIGH}, and T_{LOW} registers are used in the comparisons for the ALERT function for all converter resolutions. The three LSBs in T_{HIGH} and T_{LOW} can affect the ALERT output even if the converter is configured for 9-bit resolution.

SERIAL INTERFACE

The TMP100-Q1 and TMP101-Q1 operate only as slave devices on the I^2C bus and SMBus. Connections to the bus are made via the open-drain I/O lines SDA and SCL. The TMP100-Q1 and TMP101-Q1 support the transmission protocol for fast (up to 400 kHz) and high-speed (up to 3.4 MHz) modes. All data bytes are transmitted most significant bit first.

SERIAL BUS ADDRESS

To program the TMP100-Q1 and TMP101-Q1, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation. The TMP100-Q1 features two address pins to allow up to eight devices to be addressed on a single I^2C interface. Table 11 describes the pin logic levels used to properly connect up to eight devices. Float indicates the pin is left unconnected. The state of pins ADD0 and ADD1 is sampled on the first I^2C bus communication and should be set prior to any activity on the interface.

Table 11. Address Pins and Slave Addresses for the TMP100-Q1

ADD1	ADD0	SLAVE ADDRESS
0	0	1001000
0	Float	1001001
0	1	1001010
1	0	1001100
1	Float	1001101
1	1	1001110
Float	0	1001011
Float	1	1001111

The TMP101-Q1 features one address pin and an ALERT pin, allowing up to three devices to be connected per bus. Pin logic levels are described in Table 12. The address pins of the TMP100-Q1 and TMP101-Q1 are read after reset or in response to an I^2C address acquire request. Following reading, the state of the address pins is latched to minimize power dissipation associated with detection.

The TMP101-Q1 features one address pin and an ALERT pin, allowing up to three devices to be connected per bus. Pin logic levels are described in Table 12. The address pins of the TMP100-Q1 and TMP101-Q1 are read after reset or in response to an I^2C address acquire request. Following reading, the state of the address pins is latched to minimize power dissipation associated with detection.

Table 12. Address Pins and Slave Addresses for the TMP101-Q1

ADD0	SLAVE ADDRESS
0	1001000
Float	1001001
1	1001010

BUS OVERVIEW

The device that initiates the transfer is called a master, and the devices controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions

To address a specific device, a START condition is initiated, indicated by pulling the data-line (SDA) from a HIGH to LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge Bit. During data transfer SDA must remain stable while SCL is HIGH, as any change in SDA while SCL is HIGH will be interpreted as a control signal.

Once all data have been transferred, the master generates a STOP condition indicated by pulling SDA from LOW to HIGH, while SCL is HIGH.

WRITING/READING TO THE TMP100-Q1 AND TMP101-Q1

Accessing a particular register on the TMP100-Q1 and TMP101-Q1 is accomplished by writing the appropriate value to the Pointer Register. The value for the Pointer Register is the first byte transferred after the I^2C slave address byte with the R/W bit LOW. Every write operation to the TMP100-Q1 and TMP101-Q1 requires a value for the Pointer Register. (Refer to Figure 11.)

When reading from the TMP100-Q1 and TMP101-Q1, the last value stored in the Pointer Register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer Register. This is accomplished by issuing an I^2C slave address byte with the R/W bit LOW, followed by the Pointer Register Byte. No additional data are required. The master can then generate a START condition and send the I^2C slave address byte with the R/W bit HIGH to initiate the read command. See Figure 12 for details of this sequence. If repeated reads from the same register are desired, it is not necessary to continually send the Pointer Register bytes as the TMP100-Q1 and TMP101-Q1 will remember the Pointer Register value until it is changed by the next write operation.

SLAVE MODE OPERATIONS

The TMP100-Q1 and TMP101-Q1 can operate as slave receivers or slave transmitters.

Slave Receiver Mode

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit LOW. The TMP100-Q1 or TMP101-Q1 then acknowledges reception of a valid address. The next byte transmitted by the master is the Pointer Register. The TMP100-Q1 or TMP101-Q1 then acknowledges reception of the Pointer Register byte. The next byte or bytes are written to the register addressed by the Pointer Register. The TMP100-Q1 and TMP101-Q1 will acknowledge reception of each data byte. The master may terminate data transfer by generating a START or STOP condition.

Slave Transmitter Mode

The first byte is transmitted by the master and is the slave address, with the R/$\overline{W}$ bit HIGH. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the Pointer Register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master may terminate data transfer by generating a Not-Acknowledge on reception of any data byte, or generating a START or STOP condition.

SMBus ALERT FUNCTION

The TMP101-Q1 supports the SMBus Alert function. When the TMP101-Q1 is operating in Interrupt Mode (TM = 1), the ALERT pin of the TMP101-Q1 may be connected as an SMBus Alert signal. When a master senses that an ALERT condition is present on the ALERT line, the master sends an SMBus Alert command (00011001) on the bus. If the ALERT pin of the TMP101-Q1 is active, the TMP101-Q1 will acknowledge the SMBus Alert command and respond by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte will indicate if the temperature exceeding T_{HIGH} or falling below T_{LOW} caused the ALERT condition. For POL = 0, this bit will be LOW if the temperature is greater than or equal to T_{HIGH}. This bit will be HIGH if the temperature is less than T_{LOW}. The polarity of this bit will be inverted if POL = 1. Refer to Figure 13 for details of this sequence.

If multiple devices on the bus respond to the SMBus Alert command, arbitration during the slave address portion of the SMBus alert command will determine which device will clear its ALERT status. If the TMP101-Q1 wins the arbitration, its ALERT pin will become inactive at the completion of the SMBus Alert command. If the TMP101-Q1 loses the arbitration, its ALERT pin will remain active.

The TMP100-Q1 will also respond to the SMBus ALERT command if its TM bit is set to 1. Since it does not have an ALERT pin, the master needs to periodically poll the device by issuing an SMBus Alert command. If the TMP100-Q1 has generated an ALERT, it will acknowledge the SMBus Alert command and return its slave address in the next byte.

GENERAL CALL

The TMP100-Q1 and TMP101-Q1 respond to the I^2C General Call address (0000000) if the eighth bit is 0. The device will acknowledge the General Call address and respond to commands in the second byte. If the second byte is 00000100, the TMP100-Q1 and TMP101-Q1 will latch the status of their address pins, but will not reset. If the second byte is 00000110, the TMP100-Q1 and TMP101-Q1 will latch the status of their address pins and reset their internal registers.

POR (POWER-ON RESET)

The TMP100-Q1 and TMP101-Q1 both have on-chip power-on reset circuits that reset the device to default settings when the device is powered on. This circuit activates when the power supply is less than 0.3 V for more than 100 ms. If the TMP100-Q1 and TMP101-Q1 are powered down by removing supply voltage from the device, but the supply voltage is not assured to be less than 0.3 V, it is recommended to issue a General Call reset command on the I^2C interface bus to ensure that the TMP100-Q1 and TMP101-Q1 are completely reset.

HIGH-SPEED MODE

In order for the I^2C bus to operate at frequencies above 400kHz, the master device must issue an Hs-mode master code (00001XXX) as the first byte after a START condition to switch the bus to high-speed operation. The TMP100-Q1 and TMP101-Q1 will not acknowledge this byte as required by the I^2C specification, but will switch their input filters on SDA and SCL and their output filters on SDA to operate in Hs-mode, allowing transfers at up to 3.4 MHz. After the Hs-mode master code has been issued, the master will transmit an I^2C slave address to initiate a data transfer operation. The bus will continue to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP100-Q1 and TMP101-Q1 will switch their input and output filters back to fast-mode operation.

TIMING DIAGRAMS

The TMP100-Q1 and TMP101-Q1 are I^2C and SMBus compatible. Figure 10, Figure 11, Figure 12, and Figure 13 describe the various operations on the TMP100-Q1 and TMP101-Q1. Bus definitions are given below. Parameters for Figure 5 are defined in Table 13.

Bus Idle: Both SDA and SCL lines remain HIGH.

Start Data Transfer: A change in the state of the SDA line, from HIGH to LOW, while the SCL line is HIGH, defines a START condition. Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from LOW to HIGH while the SCL line is HIGH defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a Not-Acknowledge on the last byte that has been transmitted by the slave.

Table 13. Timing Diagram Definitions

PARAMETER			FAST MODE		HIGH-SPEED MODE		UNITS
			MIN	MAX	MIN	MAX	
$f_{(SCLK)}$	SCLK operating frequency			0.4		3.4	MHz
$t_{(BUF)}$	Bus free time between STOP and START conditions		600		160		ns
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.		600		160		ns
$t_{(SUSTA)}$	Repeated START condition setup time		600		160		ns
$t_{(SUSTO)}$	STOP condition setup time		600		160		ns
$t_{(HDDAT)}$	Data HOLD time		0		0		ns
t(SUDAT)	Data setup time		100		10		ns
$t_{(LOW)}$	SCLK clock LOW period		1300		160		ns
$t_{(HIGH)}$	SCLK clock HIGH period		600		60		ns
t_F	Clock/data fall time			300		160	ns
t_R	Clock/data rise time			300		160	ns
		for SCLK ≤ 100 kHz		1000			

I²C TIMING DIAGRAMS

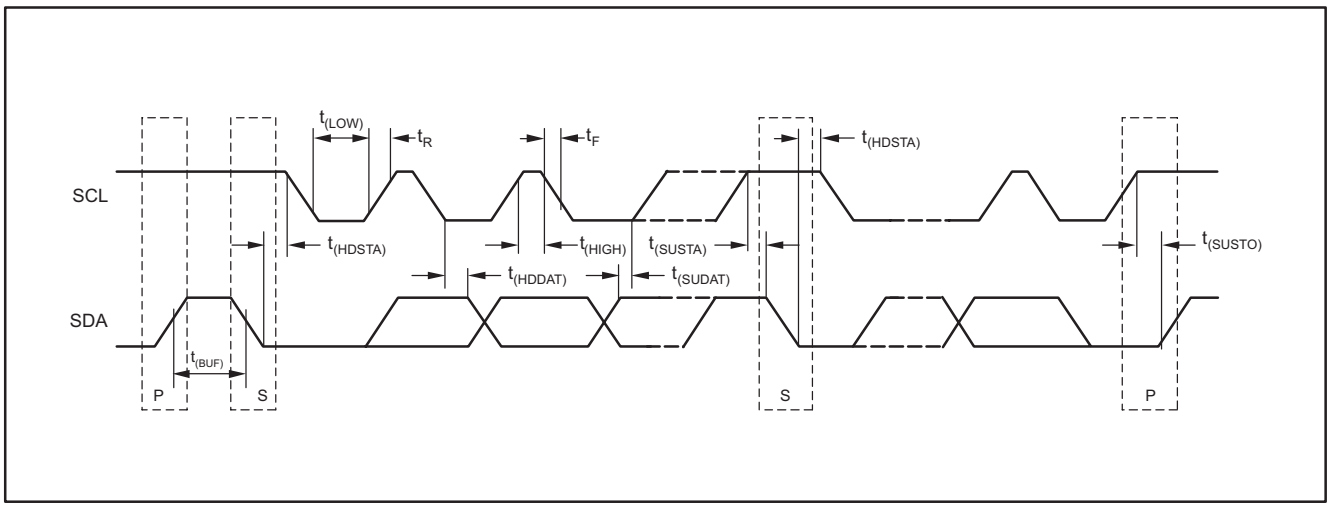


Figure 10. I²C Timing Diagram

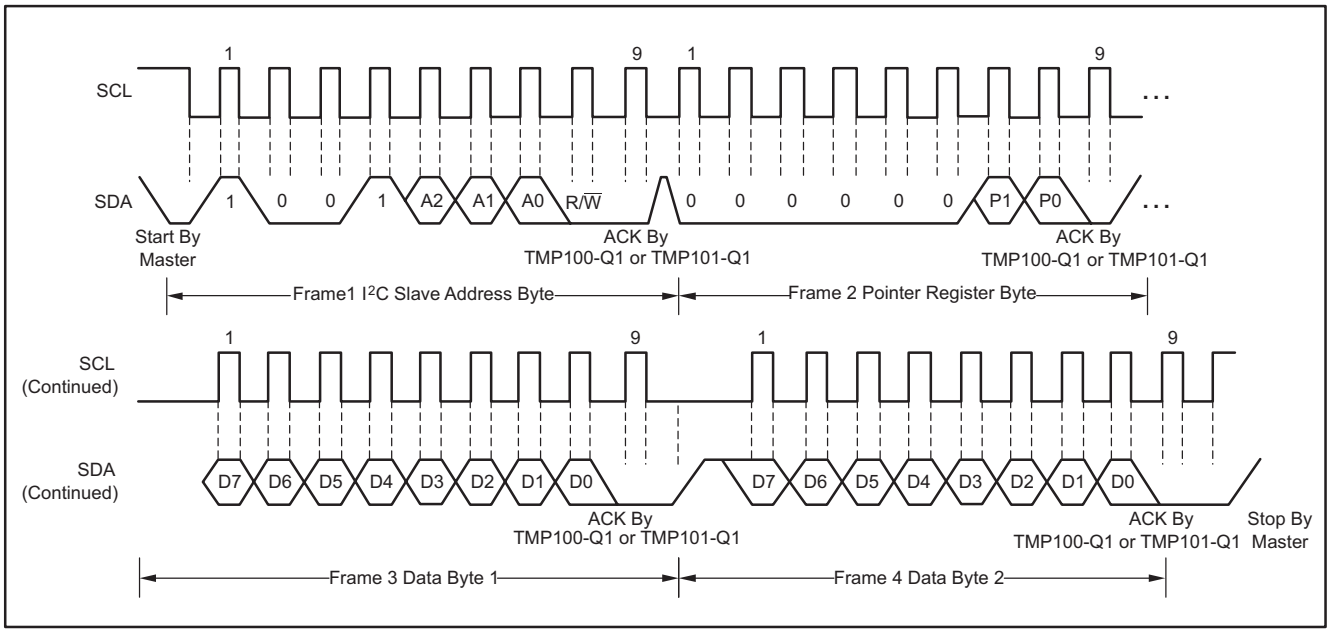


Figure 11. I²C Timing Diagram for Write Word Format

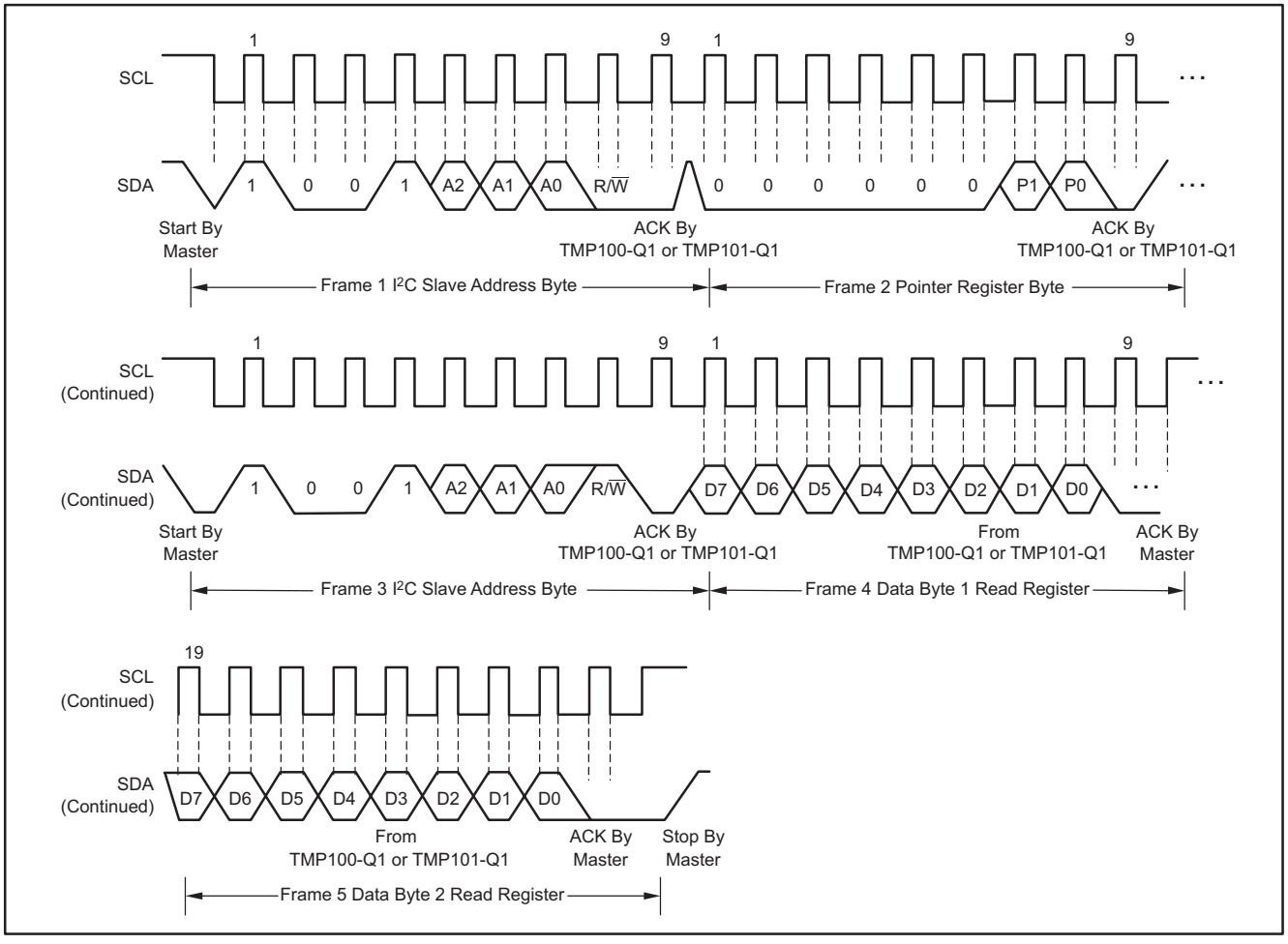


Figure 12. I²C Timing Diagram for Read Word Format

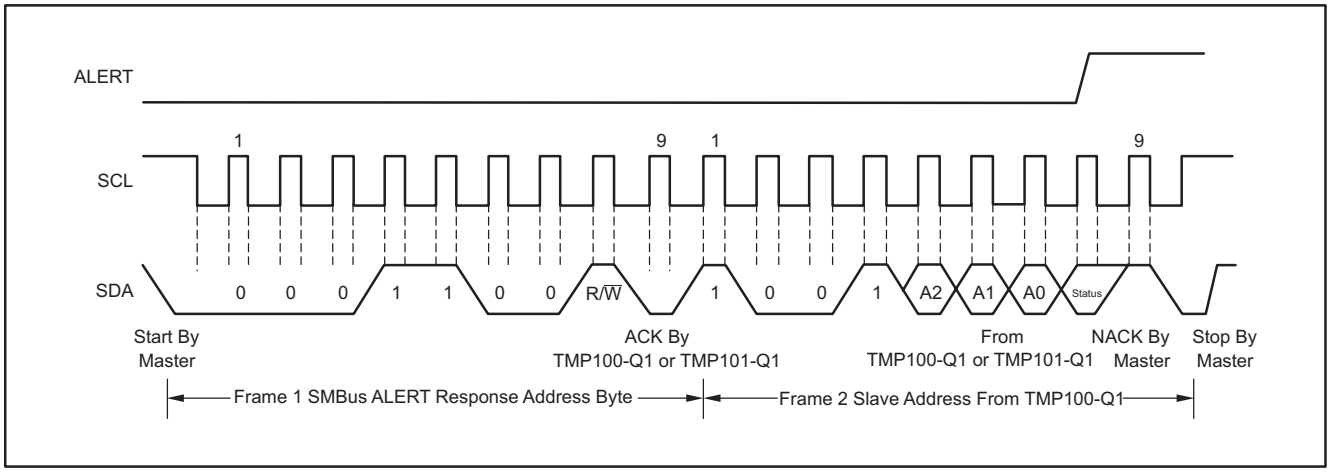


Figure 13. Timing Diagram for SMBus ALERT

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TMP101NAQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	DUGQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

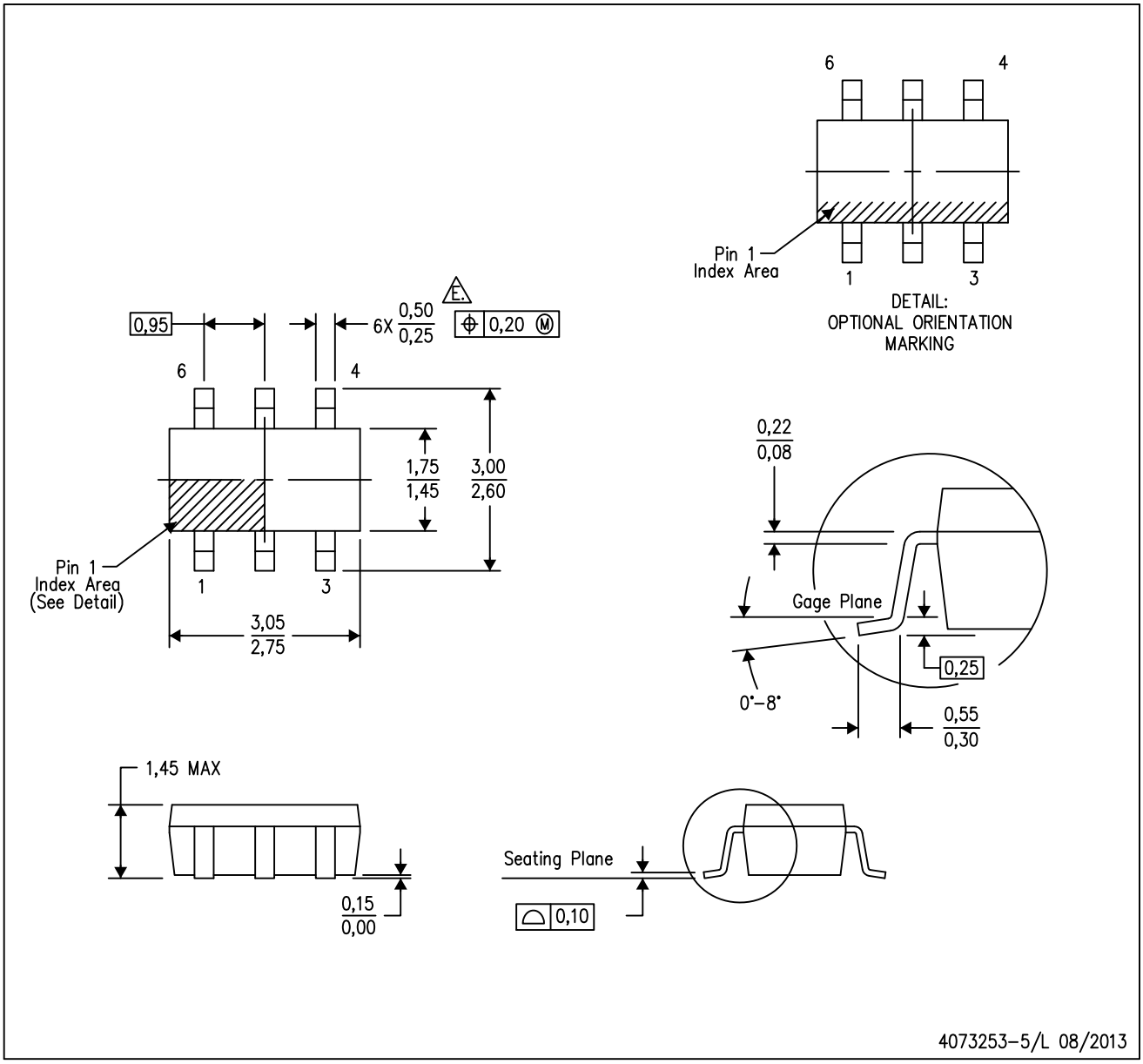
OTHER QUALIFIED VERSIONS OF TMP101-Q1 :

- Catalog: TMP101

NOTE: Qualified Version Definitions:

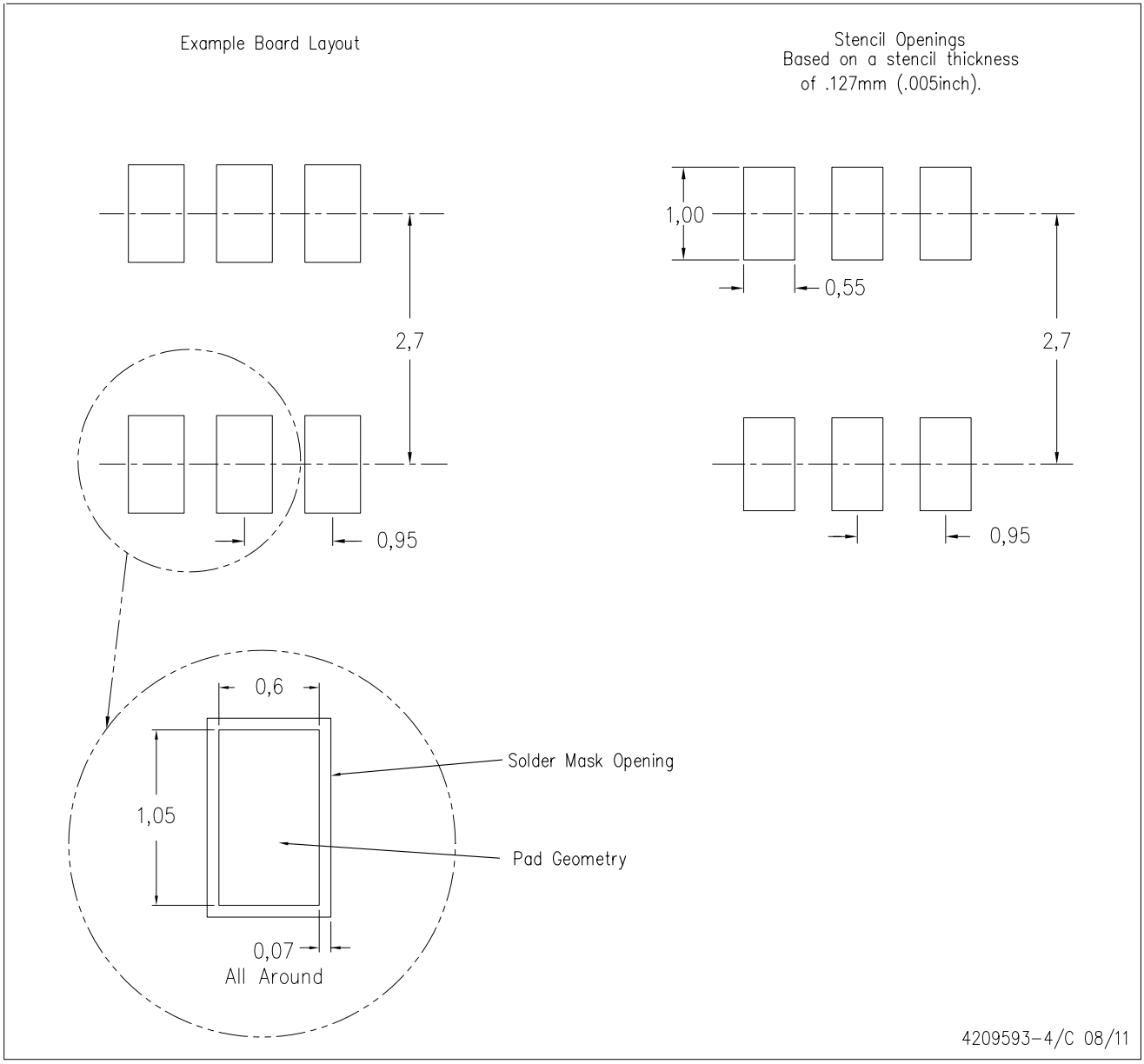
- Catalog - TI's standard catalog product

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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