138-mW DIRECTPATH™ STEREO HEADPHONE AMPLIFIER

Check for Samples: TPA6133A2

FEATURES

- **DirectPath™ Ground-Referenced Outputs**
  - **Eliminates Output DC Blocking Capacitors**
  - **Reduces Board Area**
  - **Reduces Component Height and Cost**
  - **Full Bass Response Without Attenuation**
- **Power Supply Voltage Range: 2.5 V to 5.5 V**
- **High Power Supply Rejection Ratio (>100 dB PSRR)**
- **Differential Inputs for Maximum Noise Rejection (69 dB CMRR)**
- **High-Impedance Outputs When Disabled**
- **Advanced Pop and Click Suppression Circuitry**
- **GPIO Control for Shutdown**
- **20 Pin, 4 mm x 4 mm QFN Package**

APPLICATIONS

- **Mobile Phones**
- **Audio Headsets**
- **Notebook Computers**
- **High Fidelity Applications**

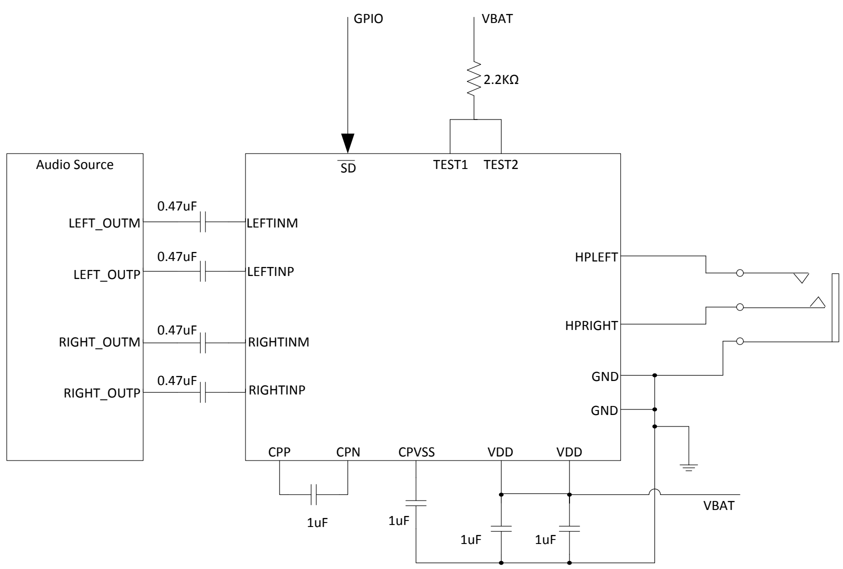
DESCRIPTION

The TPA6133A2 is a stereo DirectPath™ headphone amplifier with GPIO control. The TPA6133A2 has minimal quiescent current consumption, with a typical I_{DD} of 4.2 mA, making it optimal for portable applications. The GPIO control allows the device to be put in a low power shutdown mode.

The TPA6133A2 is a high fidelity amplifier with an SNR of 93 dB. A PSRR greater than 100 dB enables direct-to-battery connections without compromising the listening experience. The output noise of 12 μVrms (typical *A-weighted*) provides a minimal noise background during periods of silence. Configurable differential inputs and high CMRR allow for maximum noise rejection in the noisy environment of a mobile device.

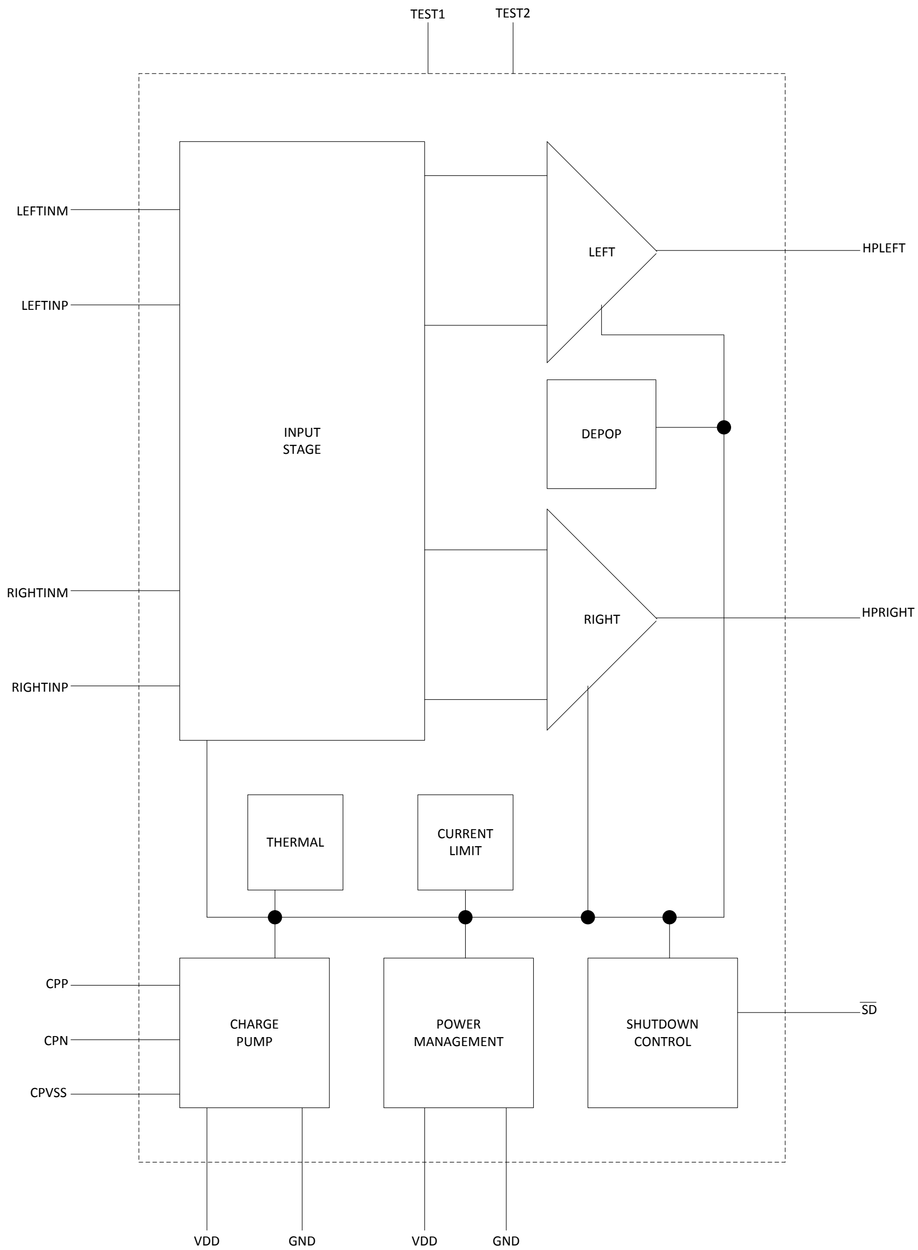
TPA6133A2 is available in a 4 by 4 mm QFN package.

SIMPLIFIED APPLICATION DIAGRAM



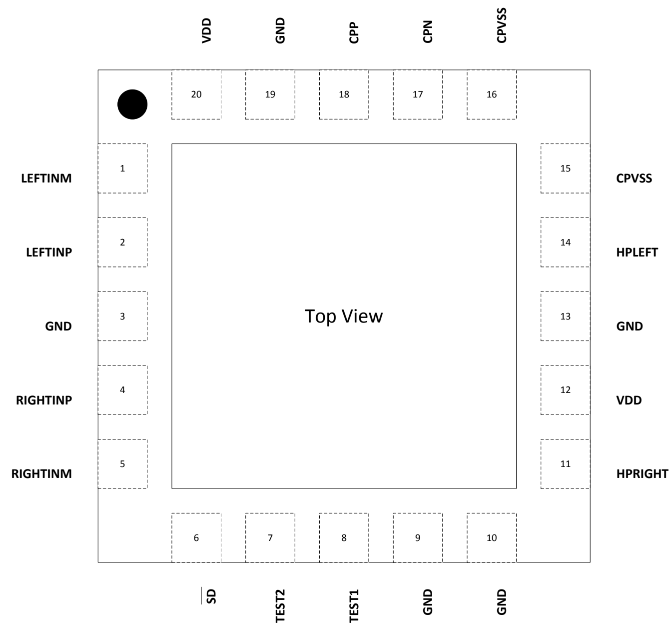
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



Headphone channels and the charge pump are activated by toggling the $\overline{SD}$ pin to logic 1. The charge pump generates a negative supply voltage for the output amplifiers. This allows a 0 V bias at the outputs, eliminating the need for bulky output capacitors. The thermal block detects faults and shuts down the device before damage occurs. The current limit block prevents the output current from getting high enough to damage the device. The De-Pop block eliminates audible pops during power-up, power-down, and amplifier enable and disable events.

RJT PACKAGE
(Top VIEW)



Top View QFN Package (RTJ)

PIN FUNCTIONS

PIN		INPUT, OUTPUT, POWER	DESCRIPTION
NAME	PIN QFN		
V_{DD}	20	P	Charge pump voltage supply. V_{DD} must be connected to the common V_{DD} voltage supply. Decouple to GND (pin 19) with its own 1 µF capacitor.
GND	19	P	Charge pump ground. GND must be connected to common supply GND. It is recommended that this pin be decoupled to the V_{DD} of the charge pump pin (pin 20 on the QFN).
CPP	18	P	Charge pump flying capacitor positive terminal. Connect one side of the flying capacitor to CPP.
CPN	17	P	Charge pump flying capacitor negative terminal. Connect one side of the flying capacitor to CPN.
LEFTINM	1	I	Left channel negative differential input. Impedance must be matched to LEFTINP. Connect the left input to LEFTINM when using single-ended inputs.
LEFTINP	2	I	Left channel positive differential input. Impedance must be matched to LEFTINM. AC ground LEFTINP near signal source while maintaining matched impedance to LEFTINM when using single-ended inputs.
CPVSS	15, 16	P	Negative supply generated by the charge pump. Decouple to pin 19 or a GND plane. Use a 1 µF capacitor.
HPLEFT	14	O	Headphone left channel output. Connect to left terminal of headphone jack.
RIGHTINM	5	I	Right channel negative differential input. Impedance must be matched to RIGHTINP. Connect the right input to RIGHTINM when using single-ended inputs.
RIGHTINP	4	I	Right channel positive differential input. Impedance must be matched to RIGHTINM. AC ground RIGHTINP near signal source while maintaining matched impedance to RIGHTINM when using single-ended inputs.
GND	3, 9, 10, 13	P	Analog ground. Must be connected to common supply GND. It is recommended that this pin be used to decouple V_{DD} for analog. Use pin 13 to decouple pin 12 on the QFN package.
V_{DD}	12	P	Analog V_{DD}. V_{DD} must be connected to common V_{DD} supply. Decouple with its own 1-µF capacitor to analog ground (pin 13).
$\overline{SD}$	6	I	Shutdown. Active low logic. 5V tolerant input.

PIN FUNCTIONS (continued)

PIN		INPUT, OUTPUT, POWER	DESCRIPTION
NAME	PIN QFN		
TEST2	7	I	Factory test pins. Pull up to VDD supply. See Applications Diagram.
TEST1	8	I	Factory test pins. Pull up to VDD supply. See Applications Diagram.
HPRIGHT	11	O	Headphone light channel output. Connect to the right terminal of the headphone jack.
Thermal pad	Die Pad	P	Solder the thermal pad on the bottom of the QFN package to the GND plane of the PCB. It is required for mechanical stability and will enhance thermal performance.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range, T_A = 25°C (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_{DD}		–0.3	6	V
Input voltage	RIGHTINx, LEFTINx	CPVSS-0.2 V to minimum of (3.6 V, VDD+0.2 V)		
	$\overline{SD}$, TEST1, TEST2	–0.3	7	V
Output continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range, T_A		–40	85	°C
Operating junction temperature range, T_J		–40	150	°C
Storage temperature range, T_{stg}		–65	150	°C
ESD Protection	HBM		3	kV
Minimum Load Impedance			12.8 Ω	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS TABLE

PACKAGE	T_A ≤ 25°C POWER RATING	DERATING FACTOR(1) (2)	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
RTJ	4100 mW	41 mW/°C	2250 mW	1640 mW

(1) Derating factor measured with JEDEC High K board: 1S2P - One signal layer and two plane layers.
(2) See JEDEC Standard 51-3 for Low-K board, JEDEC Standard 51-7 for High-K board, and JEDEC Standard 51-12 for using package thermal information. Please see JEDEC document page for downloadable copies: http://www.jedec.org/download/default.cfm.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES(1)	PART NUMBER	SYMBOL
–40°C to 85°C	20-pin, 4 mm × 4 mm QFN	TPA6133A2RTJ(2)	SIZ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) The RTJ package is only available taped and reeled. To order, add the suffix “R” to the end of the part number for a reel of 3000, or add the suffix “T” to the end of the part number for a reel of 250 (that is, TPA6133A2RTJR).

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
	Supply voltage, V_{DD}		2.5	5.5	V
V_{IH}	High-level input voltage	TEST1, TEST2, $\overline{SD}$	1.3		V
V_{IL}	Low-level input voltage	$\overline{SD}$		0.35	V
T_A	Operating free-air temperature		–40	85	°C

ELECTRICAL CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Output offset voltage	V_{DD} = 2.5 V to 5.5 V, inputs grounded			135	400	µV
PSRR	DC Power supply rejection ratio	V_{DD} = 2.5 V to 5.5 V, inputs grounded			–101	-85	dB
CMRR	Common mode rejection ratio	V_{DD} = 2.5 V to 5.5 V			–69		dB
$\lvert I_{IH} \rvert$	High-level input current	V_{DD} = 5.5 V, V_I = V_{DD}	TEST1, TEST2			1	µA
			$\overline{SD}$			10	
$\lvert I_{IL} \rvert$	Low-level input current	V_{DD} = 5.5 V, V_I = 0 V	$\overline{SD}$			1	µA
I_{DD}	Supply current	V_{DD} = 2.5 V to 5.5 V, $\overline{SD}$ = V_{DD}			4.2	6	mA
		Shutdown mode, V_{DD} = 2.5V to 5.5 V, $\overline{SD}$ = 0 V			0.08	1	µA

OPERATING CHARACTERISTICS

V_{DD} = 3.6 V , T_A = 25°C, R_L = 16 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	Stereo, Outputs out of phase, THD = 1%, f = 1 kHz, Gain = +4 dB	V_{DD} = 2.5V		63		mW
			V_{DD} = 3.6V		133		
			V_{DD} = 5V		142		
THD+N	Total harmonic distortion plus noise	P_O = 35 mW	f = 100 Hz		0.0096%		
			f = 1 kHz		0.007%		
			f = 20 kHz		0.0021%		
k_{SVR}	Supply ripple rejection ratio	200 mV_{pp} ripple, f = 217 Hz			-94.3	-85	dB
		200 mV_{pp} ripple, f = 1 kHz			-92		
		200 mV_{pp} ripple, f = 20 kHz			-77.1		
A_v	Channel DC Gain	$\overline{SD}$ = V_{DD}			1.597		V/V
ΔA_v	Gain matching				0.1		%
	Slew rate				0.4		V/µs
V_n	Noise output voltage	V_{DD} = 3.6V, A-weighted, Gain = +4 dB			12		μV_{RMS}
f_{osc}	Charge pump switching frequency			300	381	500	kHz
	Start-up time from shutdown				4.8		ms
	Differential input impedance				36.6		kΩ
SNR	Signal-to-noise ratio	P_o = 35 mW			93		dB
	Thermal shutdown	Threshold			180		°C
		Hysteresis			35		°C
Z_O	HW Shutdown HP output impedance	$\overline{SD}$ = 0 V, measured output to ground.			112		Ω
C_O	Output capacitance				80		pF

Table of Graphs

		FIGURE
Total harmonic distortion + noise	versus Output power	1–4
Total harmonic distortion + noise	versus Frequency	5–12
Supply voltage rejection ratio	versus Frequency	13-14
Common mode rejection ratio	versus Frequency	15-16
Crosstalk	versus Frequency	17-18

TYPICAL CHARACTERISTICS

$C_{(PUMP,\ DECOUPLE,\ ,BYPASS,\ CPVSS)}$ = 1 µF, C_I = 2.2µF.

All THD + N graphs taken with outputs out of phase (unless otherwise noted).

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

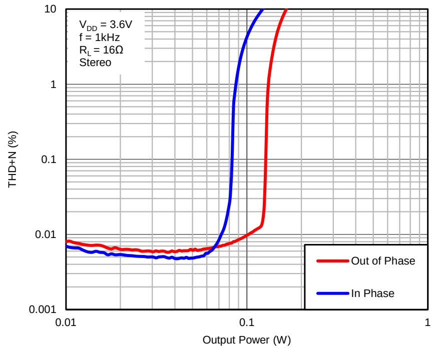


Figure 1.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

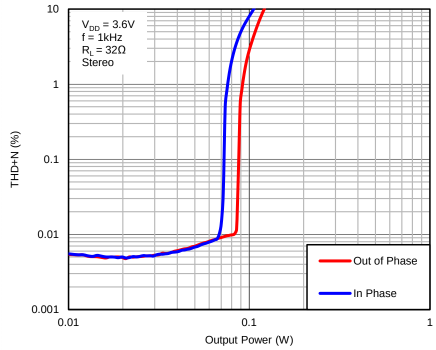


Figure 2.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

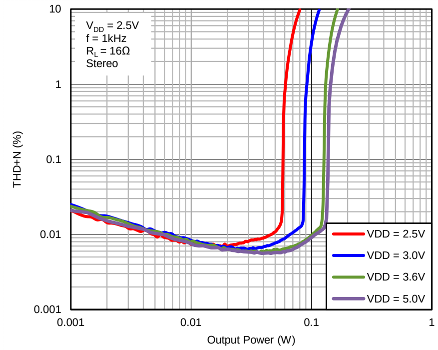


Figure 3.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

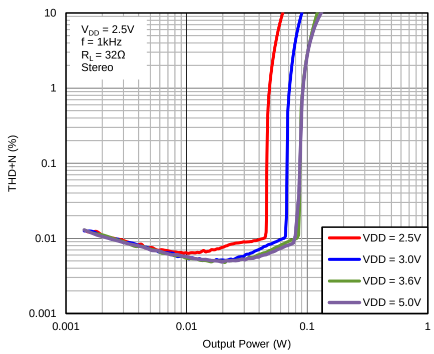


Figure 4.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

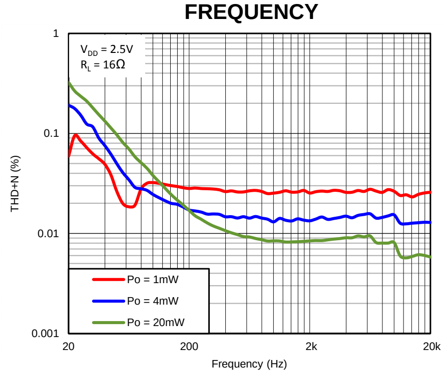


Figure 5.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

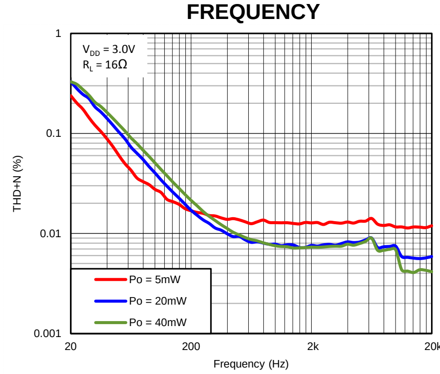


Figure 6.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

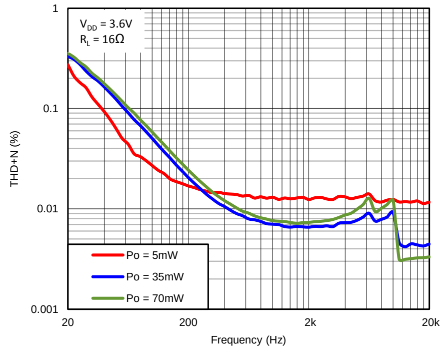


Figure 7.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

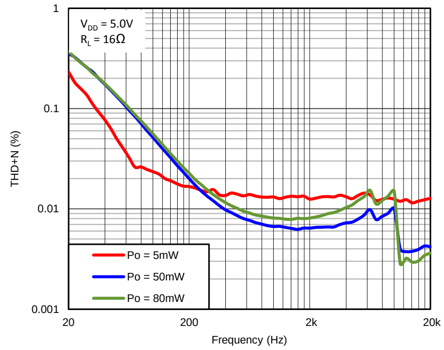


Figure 8.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

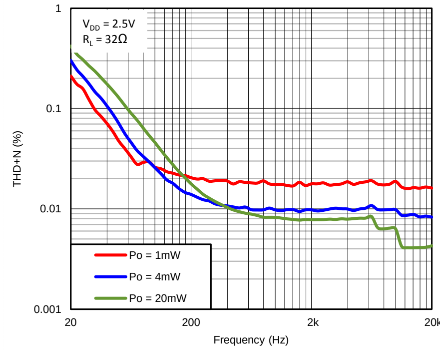


Figure 9.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

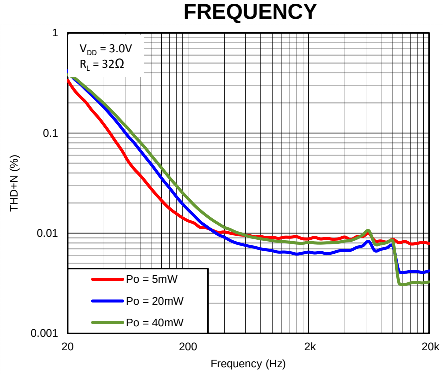


Figure 10.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

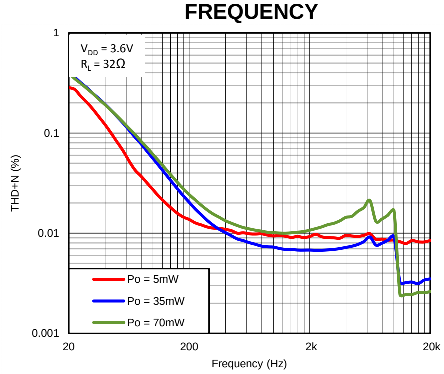


Figure 11.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

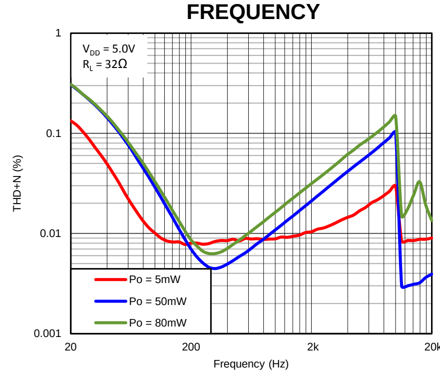


Figure 12.

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

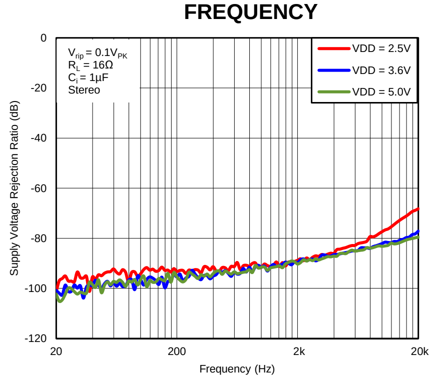


Figure 13.

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

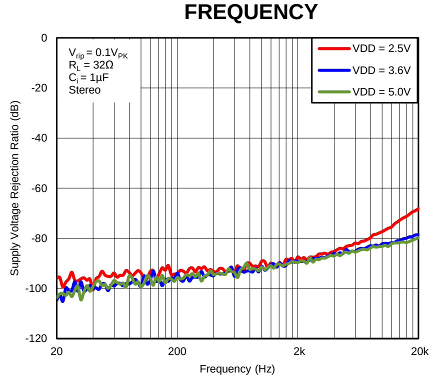


Figure 14.

COMMON MODE REJECTION RATIO vs FREQUENCY

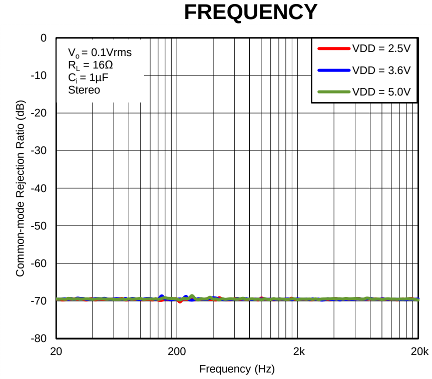


Figure 15.

COMMON MODE REJECTION RATIO vs FREQUENCY

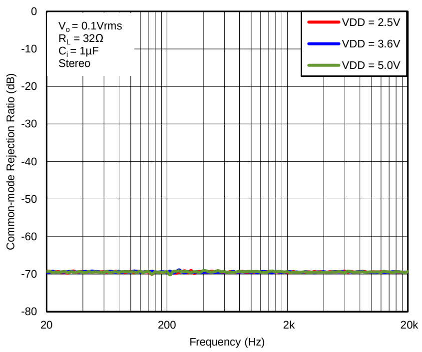


Figure 16.

CROSSTALK vs FREQUENCY

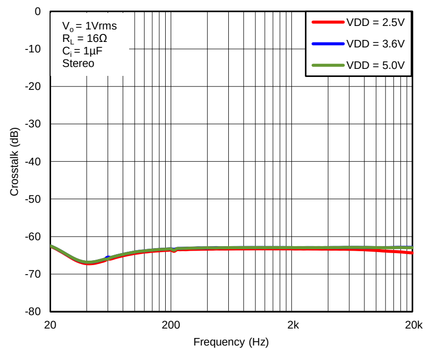


Figure 17.

CROSSTALK vs FREQUENCY

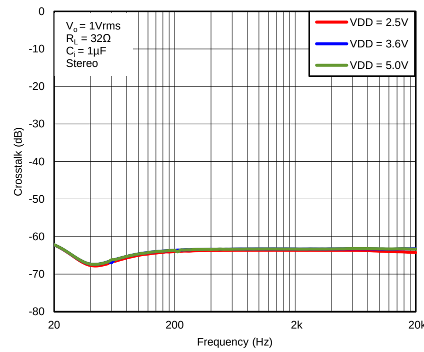
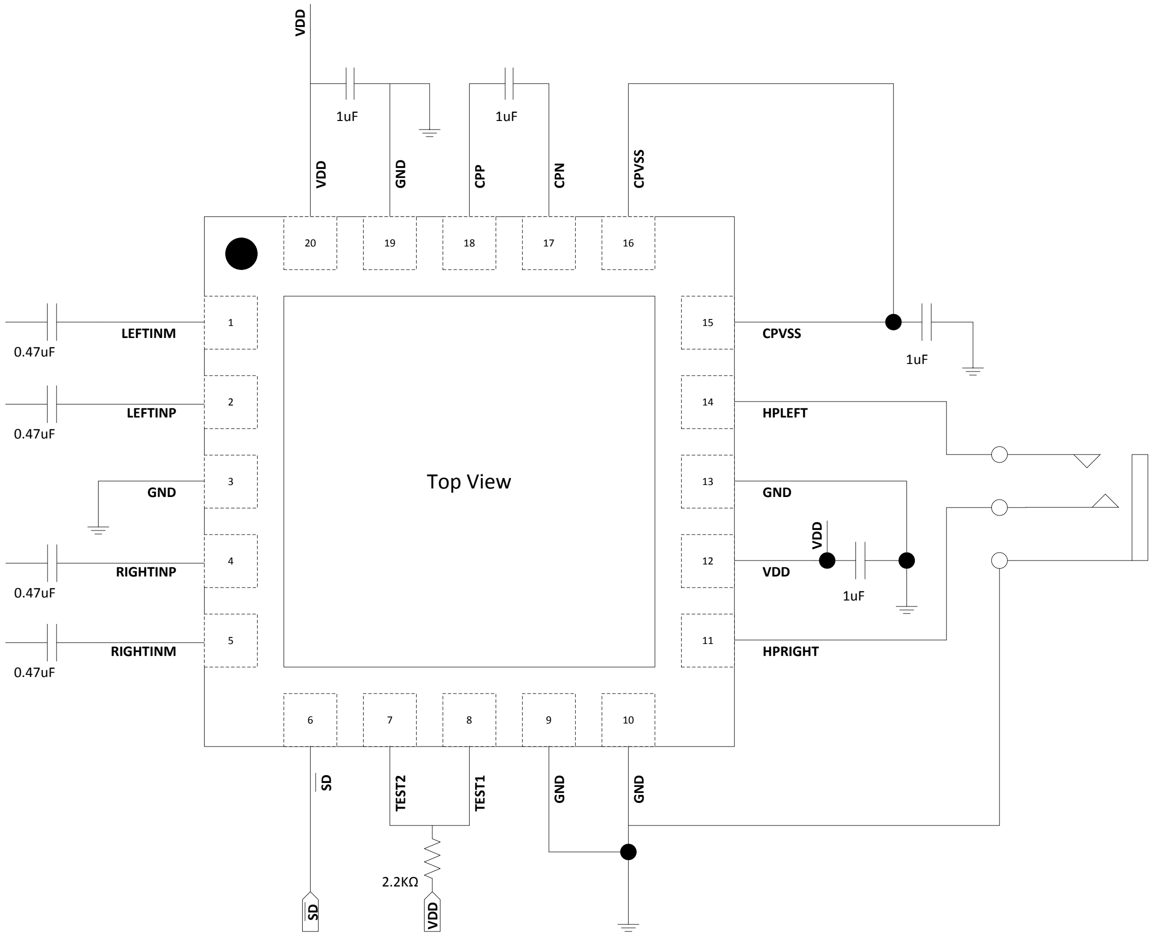


Figure 18.

APPLICATION INFORMATION

SIMPLIFIED APPLICATIONS CIRCUIT



Headphone Amplifiers

Single-supply headphone amplifiers typically require dc-blocking capacitors. The capacitors are required because most headphone amplifiers have a dc bias on the outputs pin. If the dc bias is not removed, the output signal is severely clipped, and large amounts of dc current rush through the headphones, potentially damaging them. The top drawing in Figure 19 illustrates the conventional headphone amplifier connection to the headphone jack and output signal.

DC blocking capacitors are often large in value. The headphone speakers (typical resistive values of 16 Ω or 32 Ω) combine with the dc blocking capacitors to form a high-pass filter. Equation 1 shows the relationship between the load impedance (R_L), the capacitor (C_O), and the cutoff frequency (f_C).

$$f_c = \frac{1}{2\pi R_L C_O} \quad (1)$$

C_O can be determined using Equation 2, where the load impedance and the cutoff frequency are known.

$$C_O = \frac{1}{2\pi R_L f_c} \quad (2)$$

If f_c is low, the capacitor must then have a large value because the load resistance is small. Large capacitance values require large package sizes. Large package sizes consume PCB area, stand high above the PCB, increase cost of assembly, and can reduce the fidelity of the audio output signal.

Two different headphone amplifier applications are available that allow for the removal of the output dc blocking capacitors. The Capless amplifier architecture is implemented in the same manner as the conventional amplifier with the exception of the headphone jack shield pin. This amplifier provides a reference voltage, which is connected to the headphone jack shield pin. This is the voltage on which the audio output signals are centered. This voltage reference is half of the amplifier power supply to allow symmetrical swing of the output voltages. Do not connect the shield to any GND reference or large currents will result. The scenario can happen if, for example, an accessory other than a floating GND headphone is plugged into the headphone connector. See the second block diagram and waveform in Figure 19.

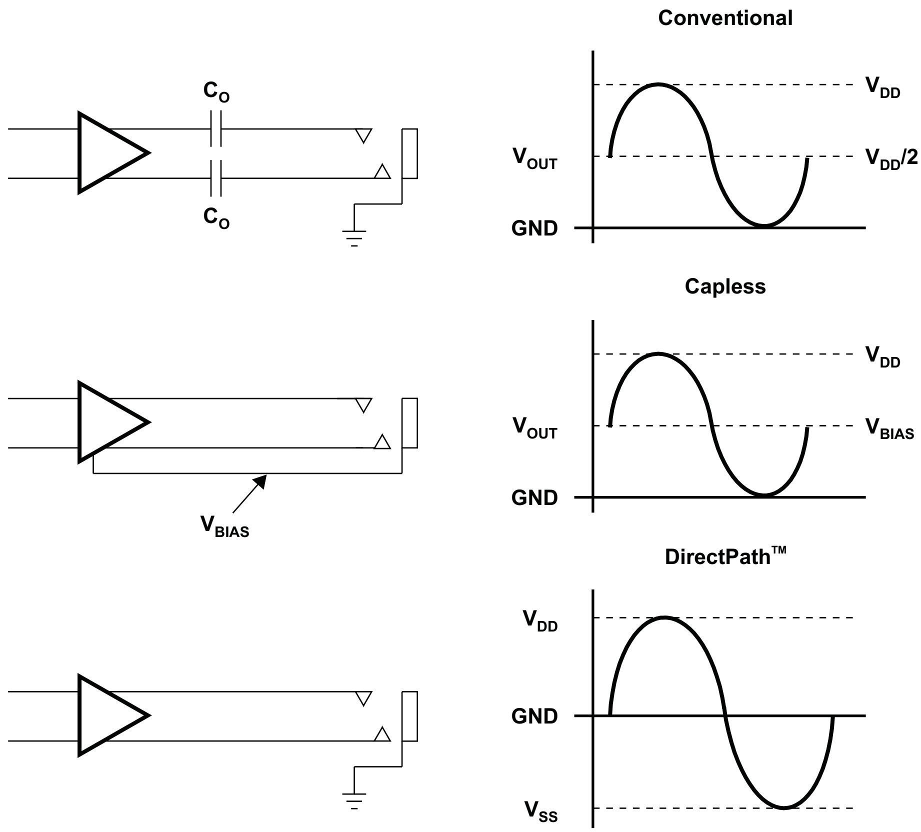


Figure 19. Amplifier Applications

The DirectPath™ amplifier architecture operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail. Combining the user provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split supply mode. The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. The DirectPath™ amplifier requires no output dc blocking capacitors, and does not place any voltage on the sleeve. The bottom block diagram and waveform of Figure 19 illustrate the ground-referenced headphone architecture. This is the architecture of the TPA6133A2.

Input-Blocking Capacitors

DC input-blocking capacitors block the dc portion of the audio source, and allow the inputs to properly bias. Maximum performance is achieved when the inputs of the TPA6133A2 are properly biased. Performance issues such as pop are optimized with proper input capacitors.

The dc input-blocking capacitors may be removed provided the inputs are connected differentially and within the input common mode range of the amplifier, the audio signal does not exceed ±3 V, and pop performance is sufficient.

C_{IN} is a theoretical capacitor used for mathematical calculations only. Its value is the series combination of the dc input-blocking capacitors, $C_{(DCINPUT-BLOCKING)}$. Use Equation 3 to determine the value of $C_{(DCINPUT-BLOCKING)}$. For example, if C_{IN} is equal to 0.22 µF, then $C_{(DCINPUT-BLOCKING)}$ is equal to about 0.47 µF.

$$C_{IN} = \frac{1}{2} C_{(DCINPUT-BLOCKING)} \tag{3}$$

The two $C_{(DCINPUT-BLOCKING)}$ capacitors form a high-pass filter with the input impedance of the TPA6133A2. Use Equation 3 to calculate C_{IN}, then calculate the cutoff frequency using C_{IN} and the differential input impedance of the TPA6133A2, R_{IN}, using Equation 4. Note that the differential input impedance changes with gain. See for input impedance values. The frequency and/or capacitance can be determined when one of the two values are given.

$$fc_{IN} = \frac{1}{2\pi R_{IN} C_{IN}} \quad \text{or} \quad C_{IN} = \frac{1}{2\pi fc_{IN} R_{IN}} \tag{4}$$

If a high pass filter with a -3 dB point of no more than 20 Hz is desired over all gain settings, the minimum impedance would be used in the above equation. shows this to be 37 kΩ. The capacitor value by the above equation would be 0.215 µF. However, this is C_{IN}, and the desired value is for $C_{(DCINPUT-BLOCKING)}$. Multiplying C_{IN} by 2 yields 0.43 µF, which is close to the standard capacitor value of 0.47 µF. Place 0.47 µF capacitors at each input terminal of the TPA6133A2 to complete the filter.

Charge Pump Flying Capacitor and CPVSS Capacitor

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The CP_{VSS} capacitor must be at least equal to the flying capacitor in order to allow maximum charge transfer. Low ESR capacitors are an ideal selection, and a value of 1 µF is typical.

Decoupling Capacitors

The TPA6133A2 is a DirectPath™ headphone amplifier that requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. Use good low equivalent-series-resistance (ESR) ceramic capacitors, typically 1.0 µF. Find the smallest package possible, and place as close as possible to the device V_{DD} lead. Placing the decoupling capacitors close to the TPA6133A2 is important for the performance of the amplifier. Use a 10 µF or greater capacitor near the TPA6133A2 to filter lower frequency noise signals. The high PSRR of the TPA6133A2 will make the 10 µF capacitor unnecessary in most applications.

Layout Recommendations

Exposed Pad On TPA6133A2RTJ Package

Solder the exposed metal pad on the TPA6133A2RTJ QFN package to the a pad on the PCB. *The pad on the PCB may be grounded or may be allowed to float (not be connected to ground or power).* If the pad is grounded, it must be connected to the same ground as the GND pins (3, 9, 10, 13, and 19). See the layout and mechanical drawings at the end of the datasheet for proper sizing. Soldering the thermal pad improves mechanical reliability, improves grounding of the device, and enhances thermal conductivity of the package.

GND Connections

The GND pin for charge pump should be decoupled to the charge pump V_{DD} pin, and the GND pin adjacent to the Analog V_{DD} pin should be separately decoupled to each other.

Modes of Operation

The TPA6133A2 supports two modes of operation. When the $\overline{SD}$ pin is driven to logic 0, the device is in low power mode where the charge pump is powered down, the headphone channel is disabled and the outputs are weakly pulled to ground. When the $\overline{SD}$ pin is driven to logic 1, the device enters an active mode with charge pump powered up and headphone channel enabled with channel gain of +4dB. The transition from inactive to active and active to inactive states is done softly to avoid audible artifacts.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA6133A2RTJR	ACTIVE	QFN	RTJ	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SIZ	Samples
TPA6133A2RTJT	ACTIVE	QFN	RTJ	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SIZ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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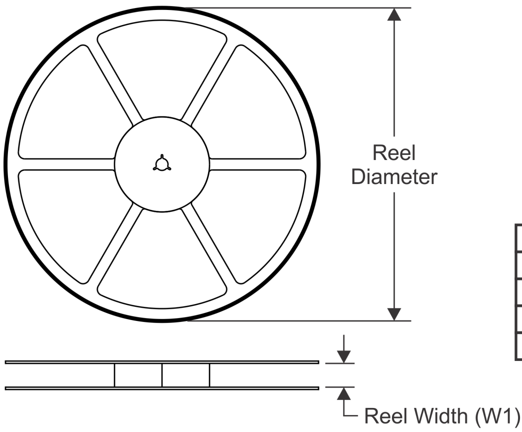
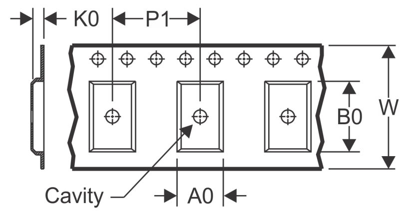
TAPE AND REEL INFORMATION

REEL DIMENSIONS

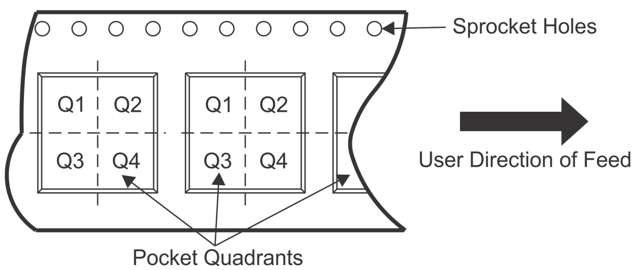


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

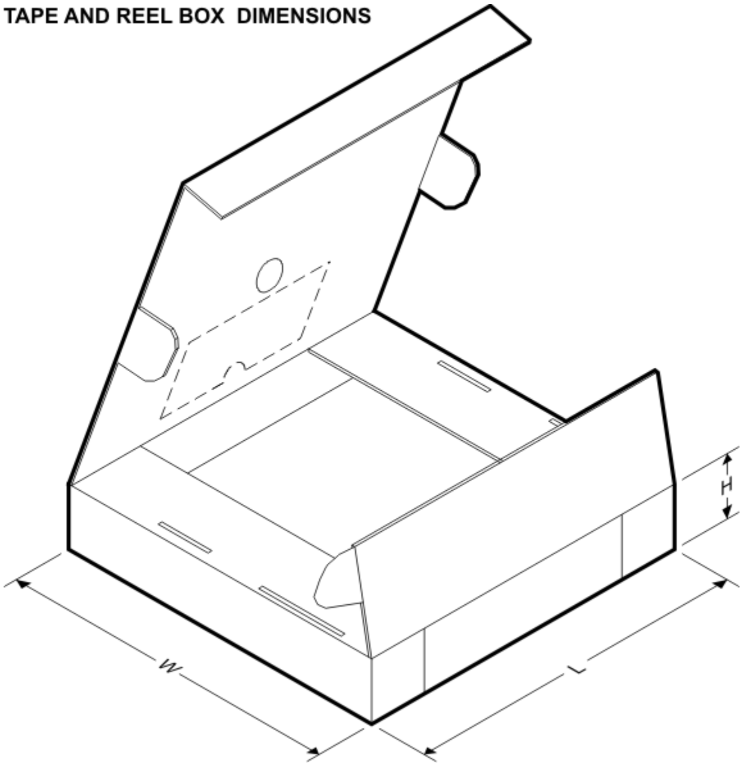
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6133A2RTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPA6133A2RTJT	QFN	RTJ	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

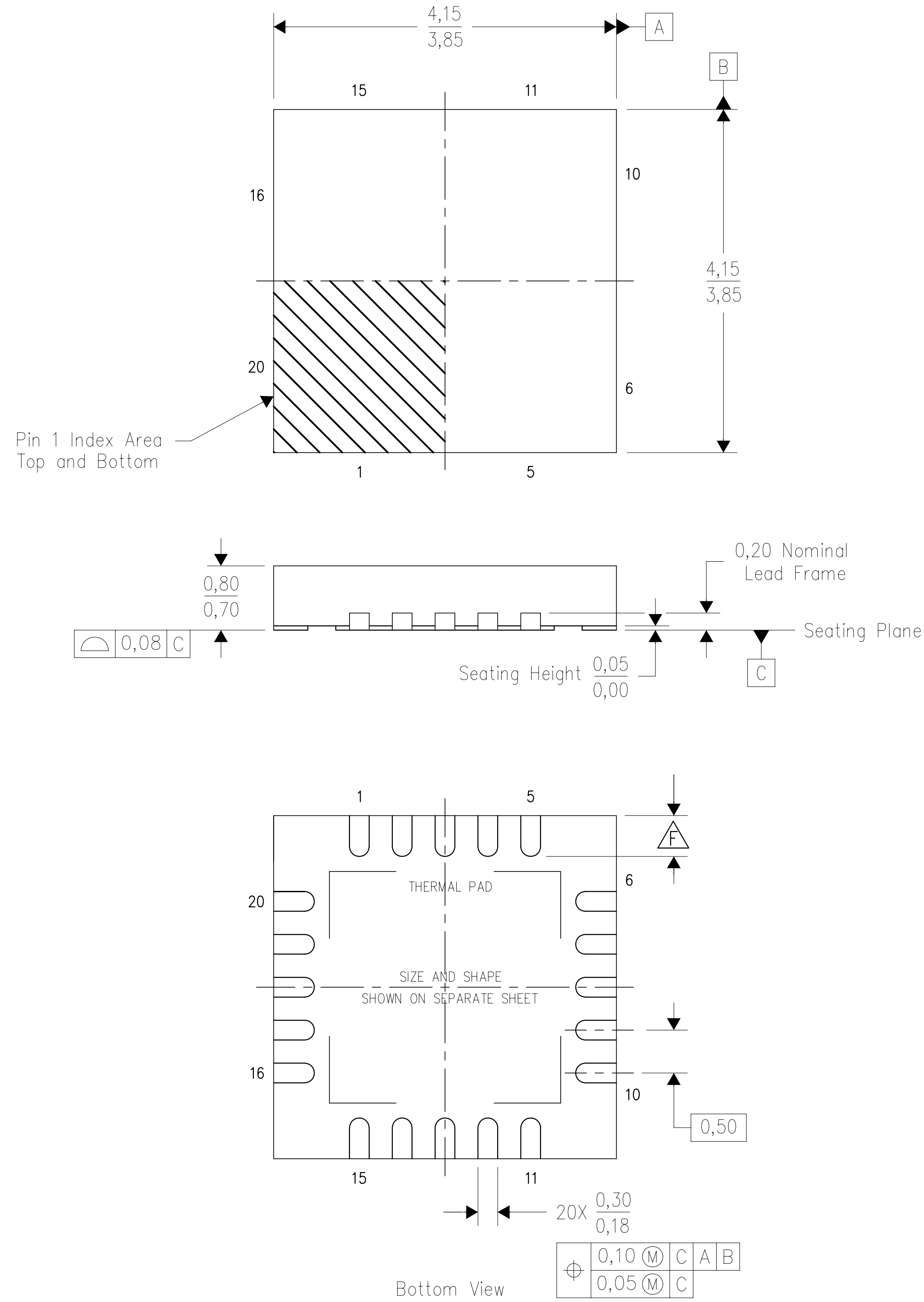
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6133A2RTJR	QFN	RTJ	20	3000	367.0	367.0	35.0
TPA6133A2RTJT	QFN	RTJ	20	250	210.0	185.0	35.0

RTJ (S-PWQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD



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NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

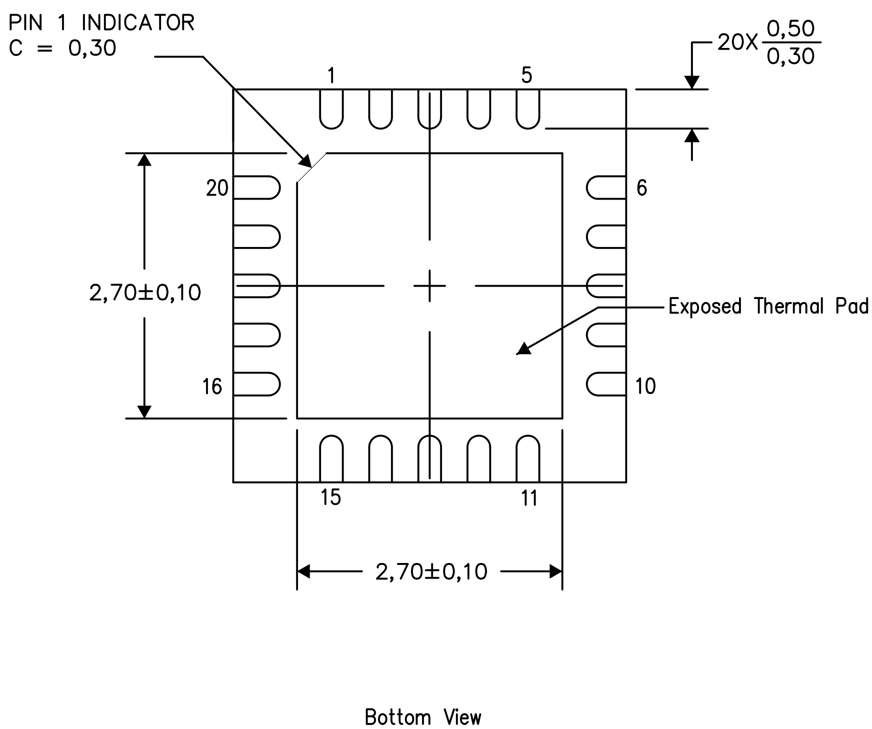
RTJ (S-PWQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

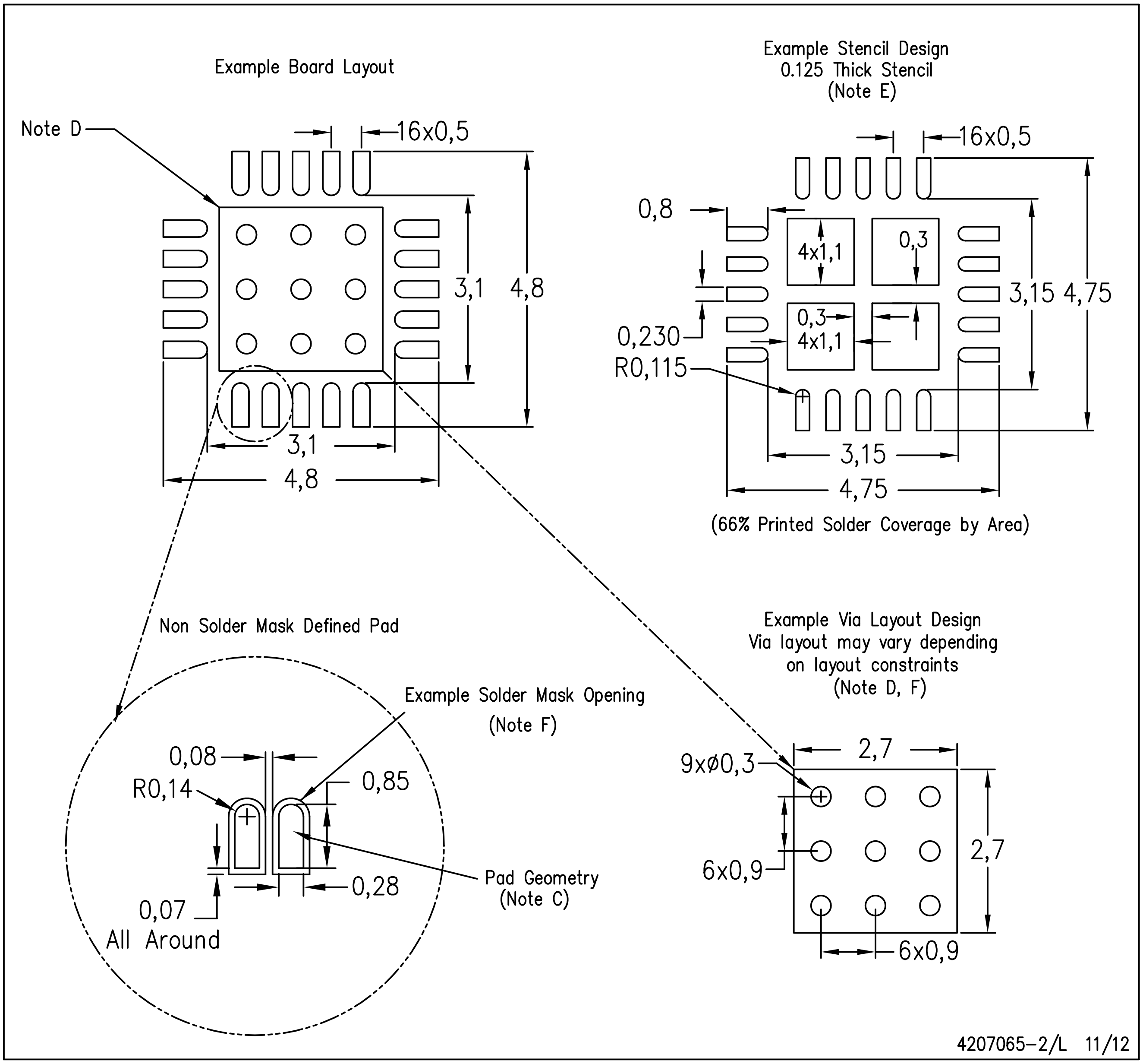


Exposed Thermal Pad Dimensions

4206256-2/R 11/12

NOTE: All linear dimensions are in millimeters

RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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