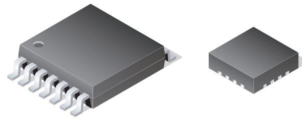


DirectPath™ 25-mW Headphone Amplifier With Programmable-Fixed Gain

Check for Samples: TPA6139A2

FEATURES

- **DirectPath™**
  - **Eliminates Pop/Clicks**
  - **Eliminates Output DC-Blocking Capacitors**
  - **3 V to 3.6 V Supply voltage**
- **Low Noise and THD**
  - **SNR > 105 dB at –1x Gain**
  - **Typical Vn < 15 μVms 20-20kHz at –1x Gain**
  - **THD+N < 0.003% at 10kΩ Load and –1x Gain**
- **25 mW into 600 Ω Load**
- **2 Vrms Output Voltage into 5kΩ Load**
- **Single Ended Input and Output**
- **Programmable Gain Select Reduces Component Count**
  - **13x Gain Values**
- **Active Mute With More Than 80dB Attenuation**
- **Short Circuit and Thermal Protection**
- **±8kV HBM ESD Protected Outputs**

APPLICATIONS

- **PDP / LCD TV**
- **Blu-ray Disc™, DVD Players**
- **Mini/Micro Combo Systems**
- **Soundcards**

DESCRIPTION

The TPA6139A2PW is a 25mW Pop-Free stereo Head Phone driver designed to reduce component count, board space and cost. It is ideal for single supply electronics where size and cost are critical design parameters.

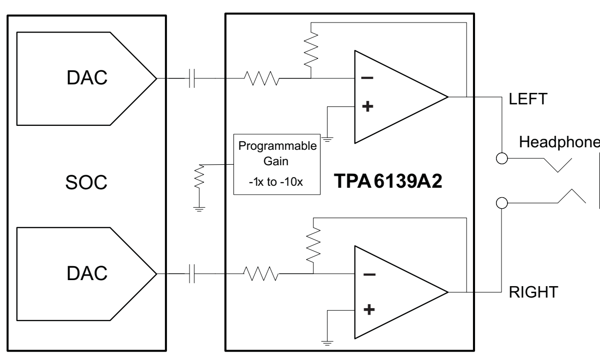
The TPA6139A2 does not require a power supply greater than 3.3V to generate its 25mW, nor does it require a split rail power supply.

Designed using TI's patented DIRECTPATH™ technology which integrates a charge pump to generate a negative supply rail that provides a clean, pop-free ground biased output. The TPA6139A2 is capable of driving 25mW into 32Ω and 2Vms into a 600Ω load. DIRECTPATH also allows the removal of the costly output DC-blocking capacitors.

The device has fixed gain single ended inputs with a gain select pin. Using a single resistor on this pin, the designer can choose from 13 internal programmable gain settings to match the line driver with the Codec output level. It also reduces the component count and board space.

Headphone outputs have ±8kV HBM ESD protection enabling a simple ESD protection circuit. The TPA6139A2 has built-in active mute control with more that 80dB attenuation for pop-free mute on/off control.

The TPA6139A2 is available in a 14-pin TSSOP and a 16-pin QFN. For a pin compatible 2vrms line driver see DRV612.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

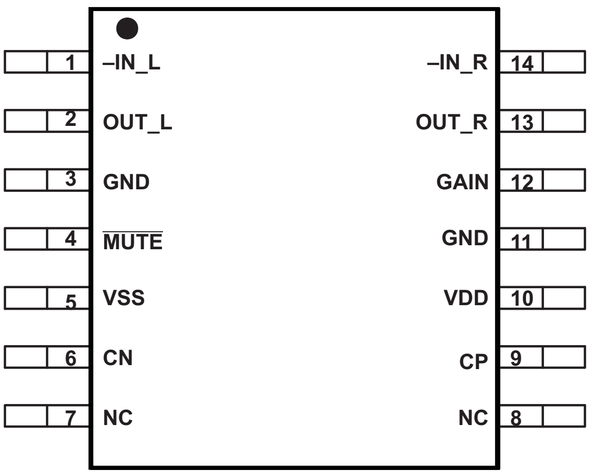
GENERAL INFORMATION

PIN ASSIGNMENT

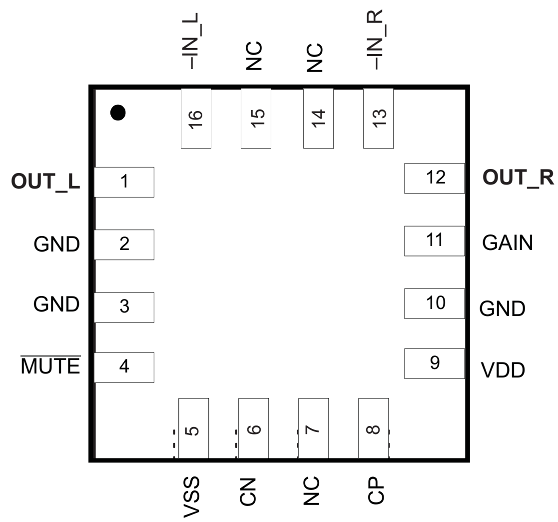
The TPA6139A2 is available in the:

- 14-pin TSSOP package (PW) or
- 16-pin QFN package (RGT)

PW PACKAGE
TSSOP
(TOP VIEW)



RGT PACKAGE
QFN
(TOP VIEW)

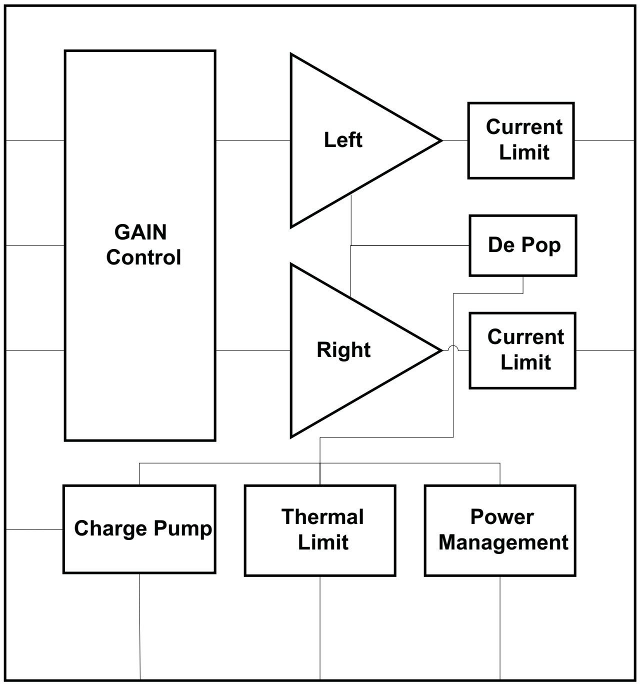


PIN FUNCTIONS

PIN			FUNCTION(1)	DESCRIPTION
NAME	PW NO.	RGT NO.		
-IN_L	1	16	I	Negative input, left channel
OUT_L	2	1	O	Output, left channel
GND	3, 11	2, 3, 10	P	Ground
MUTE	4	4	I	MUTE, active low
VSS	5	5	O	Change Pump negative supply voltage
CN	6	6	I/O	Charge Pump flying capacitor negative connection
NC	7, 8	7. 14, 15		No internal connection
CP	9	8	I/O	Charge Pump flying capacitor positive connection
VDD	10	9	P	Supply voltage, connect to positive supply
GAIN	12	11	I	Gain set programming pin; connect a resistor to ground. See Table 1 for recommended resistor values
OUT_R	13	12	O	Output, right channel
-IN_R	14	13	I	Negative input, right channel

(1) I = input, O = output, P = power

SYSTEM BLOCK DIAGRAM



ORDERING INFORMATION(1)

T_A	PACKAGE	DESCRIPTION
–40°C to 85°C	TPA6139A2PW	14-pin TSSOP
–40°C to 85°C	TPA6139A2RGT	16-pin QFN

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

THERMAL INFORMATION

THERMAL METRIC(1)		TPA6139A2 PW (14-Pin)	TPA6139A2 RGT (16-Pin)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	130	52	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	49	71	
θ_{JB}	Junction-to-board thermal resistance	63	26	
ψ_{JT}	Junction-to-top characterization parameter	3.6	3.0	
ψ_{JB}	Junction-to-board characterization parameter	62	26	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	9.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
VDD to GND		–0.3 to 4	V
Input voltage, V_I		VSS–0.3 to VDD+0.3	V
$\overline{MUTE}$ to GND		–0.3 to VDD+0.3	V
Maximum operating junction temperature range, T_J		–40 to 150	°C
Storage temperature		–40 to 150	°C
Lead temperature		260	°C
ESD Protection – HBM	OUT_L, OUT_R	8	kV
	All other pins	2	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range unless otherwise noted

			MIN	NOM	MAX	UNIT
VDD	Supply voltage	DC supply voltage	3.0	3.3	3.6	V
R_L				5		kΩ
V_{IL}	Low-level input voltage	$\overline{MUTE}$	38	40	43	%PVDD
V_{IH}	High-level input voltage	$\overline{MUTE}$	57	60	66	%PVDD
T_A	Free-air temperature		–40	25	85	°C

ELECTRICAL CHARACTERISTICS

VDD = 3.3V, R_{Load} = 32Ω, T_A = 25°C, Charge pump: C_{CP} = 1.0 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OS}\|$	Output offset voltage	VDD = 3.3 V, input ac-coupled		0.5	1	mV
PSRR	Power-supply rejection ratio		70	80		dB
V_{OH}	High-level output voltage	VDD = 3.3 V	3.1			V
V_{OL}	Low-level output voltage	VDD = 3.3 V			–3.05	V
Vuvp_on	PVDD, under voltage detection				2.8	V
Vuvp_hysteresis	PVDD, under voltage detection, hysteresis			200		mV
Fcp	Charge pump switching frequency			350		kHz
$\|I_{IH}\|$	High-level input current, $\overline{\text{MUTE}}$	VDD = 3.3 V, V_{IH} = VDD			1	µA
$\|I_{IL}\|$	Low-level input current, $\overline{\text{MUTE}}$	VDD = 3.3 V, V_{IL} = 0 V			1	µA
I (VDD)	Supply current, no load	VDD, $\overline{\text{MUTE}}$ = 3.3 V		25		mA
	Supply current, MUTED	VDD = 3.3 V, $\overline{\text{MUTE}}$ = GND		25		mA
Tsd	Thermal shutdown			150		°C
	Thermal shutdown hysteresis			15		°C
P_O	Output Power, outputs in phase	THD+N = 1%, f = 1kHz, 32Ω load		25		mW
V_O	Output Voltage, outputs in phase	THD+N = 1%, f = 1kHz, 32Ω load		0.9		V_{rms}
		THD+N = 1%, f = 1kHz, 600Ω load		2.0		
THD+N	Total Harmonic distortion plus noise	f = 1kHz, 32Ω load, Po= 25mW, -1x gain		0.03%		
THD+N	Total Harmonic distortion plus noise	f = 1kHz, 10kΩload, Vo=2 Vrms, -1x gain		0.005%		
ΔA_V	Gain matching	Between left and right channels		0.25		dB
Z_O	Output impedance when muted	$\overline{\text{MUTE}}$ = GND			1	Ω
	Input to output attenuation when muted	$\overline{\text{MUTE}}$ = GND		80		dB
SNR	Signal to noise ratio	A-weighted, AES17 filter, 1Vrms ref 32Ω load, -1x gain		99		dB
	Signal to noise ratio	A-weighted, AES17 filter, 2Vrms ref 600Ω load, -1x gain		105		dB
V_n	Noise voltage	A-weighted, AES17 filter, Gain=-2x		12		µV
	Slew rate			4.5		V/µs
Gbw	Unity Gain bandwidth			8		MHz
Crosstalk	Channel to channel	f = 1kHz, Rload = 32Ω, Po= 25mW		–85		dB
Vincm_pos	Positive Common mode input voltage			+2.0		V
Vincm_neg	Negative Common mode input voltage			–2.0		V
I_{lim}	Output current limit			60		mA

PROGRAMMABLE GAIN SETTINGS

V_{DD} = 3.3 V, R_{load} = 32 kΩ, T_A = 25°C, Charge pump:= C_{CP} 1 µF, C_{IN} = 1.0 µF, 1 x gain select (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	TPA6139A2			UNIT
			MIN	TYP	MAX	
R_Tol	Gain programming resistor tolerance				2%	
ΔA_V	Gain matching	Between left and right channels		0.25		dB
	Gain step tolerance			0.10		dB
	Gain steps	Gain resistor 2% tolerance 249k or higher 82k0 49k2 35k1 27k3 20k5 15k4 11k5 9k09 7k50 6k19 5k11 3k90		 –2.0 –1.0 –1.5 –2.3 –2.5 –3.0 –3.5 –4.0 –5.0 –5.6 –6.4 –8.3 –10.0		V/V
	Input impedance	Gain resistor 2% tolerance 249k or higher 82k0 49k2 35k1 27k3 20k5 15k4 11k5 9k09 7k50 6k19 5k11 3k90		 37 55 44 33 31 28 24 22 18 17 15 12 10.0		kΩ

(1) If pin 12, GAIN, is left floating an internal pull-up sets the gain to –2.0x
Gain setting is latched during power-up

TYPICAL CHARACTERISTICS, LINE DRIVER

V_{DD} = 3.3 V, T_A = 25°C, R_L = 2.5 kΩ, C_{PUMP} = $C_{(VSS)}$ = 10 µF, Gain Step = –2V/V (unless otherwise noted)

THD+N vs OUTPUT VOLTAGE
3.3 V, 100 kΩ, 1 kHz

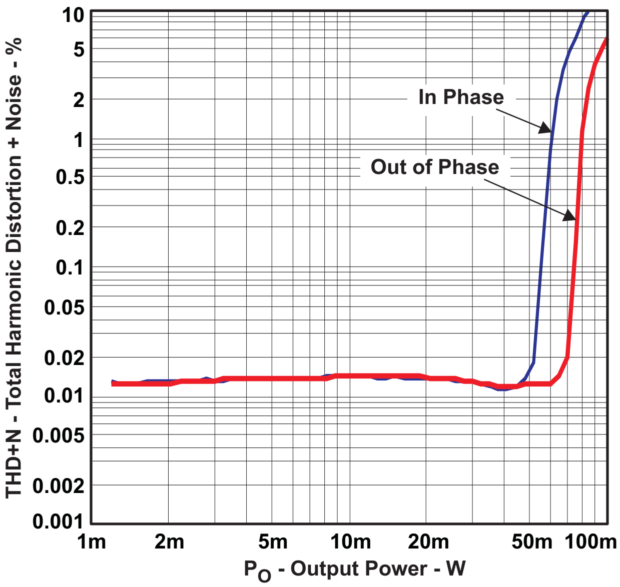


Figure 1.

THD+N vs OUTPUT VOLTAGE
3.3 V, 600 Ω load, 1 kHz

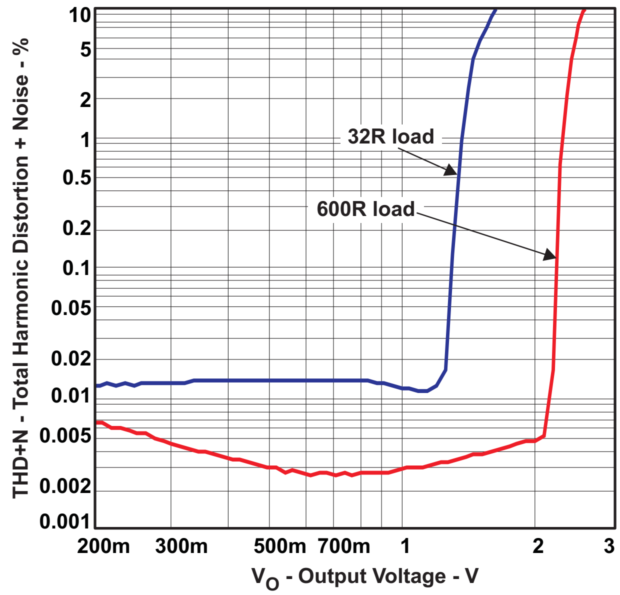


Figure 2.

CHANNEL SEPARATION
3.3 V, 5 kΩ load, 2 Vrms, Blue L to R, Red R to L

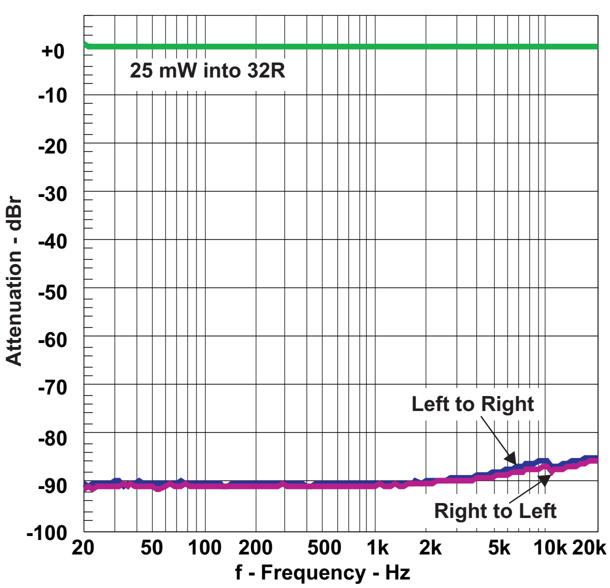


Figure 3.

FFT

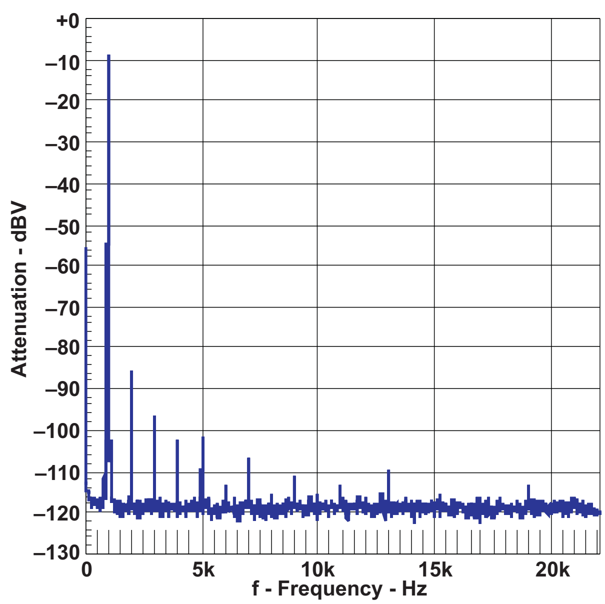


Figure 4.

TYPICAL CHARACTERISTICS, LINE DRIVER (continued)

V_{DD} = 3.3 V, T_A = 25°C, R_L = 2.5 kΩ, C_{PUMP} = $C_{(VSS)}$ = 10 µF, Gain Step = –2V/V (unless otherwise noted)

Gain vs FREQUENCY

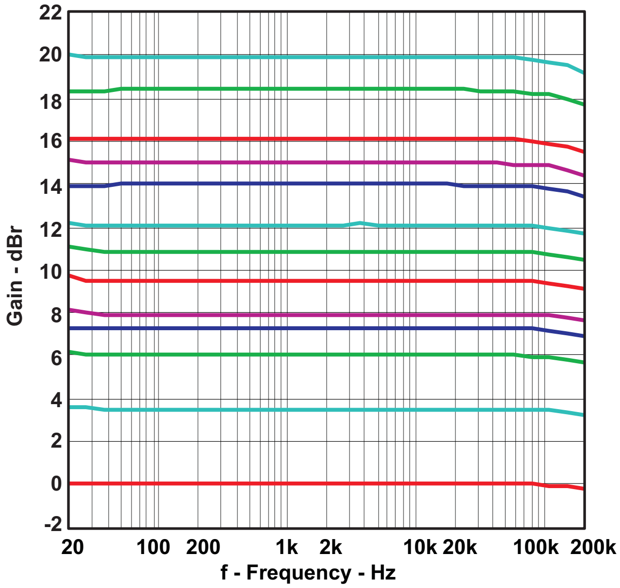


Figure 5.

TOTAL HARMONIC DISTORTION vs FREQUENCY

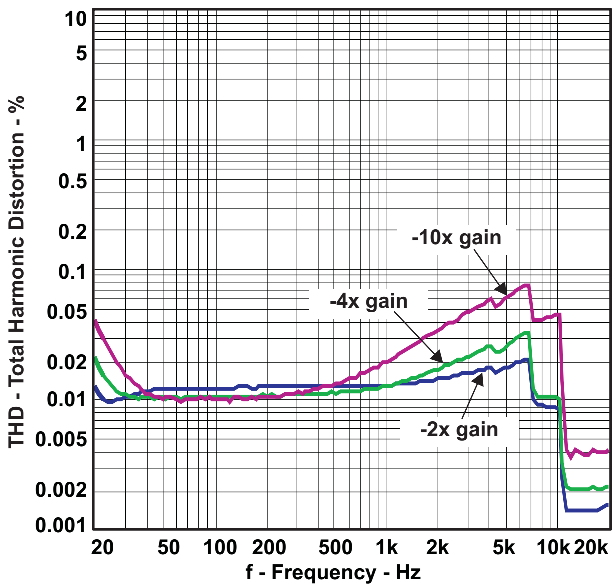


Figure 6.

MUTE TO UN-MUTE

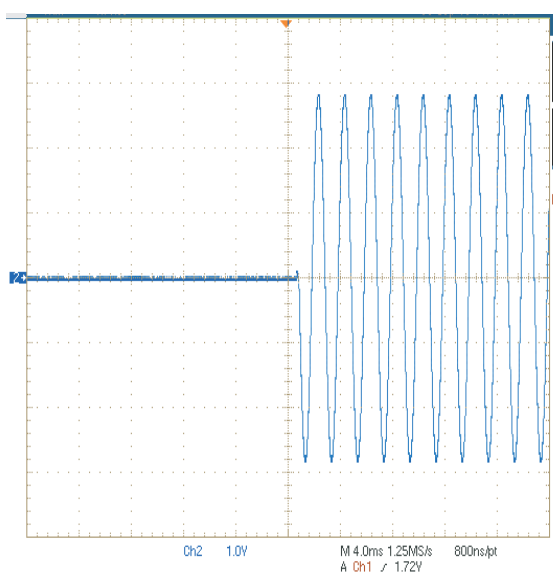


Figure 7.

UN-MUTE TO MUTE

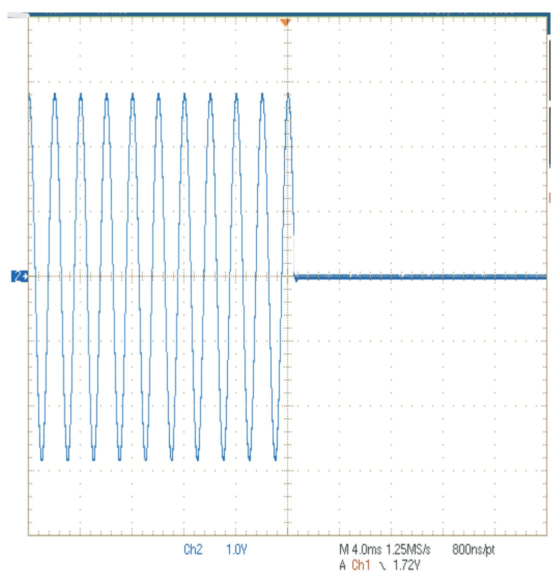


Figure 8.

APPLICATION INFORMATION

LINE DRIVER AMPLIFIERS

Single-supply line-driver amplifiers typically require dc-blocking capacitors. The top drawing in Figure 9 illustrates the conventional line-driver amplifier connection to the load and output signal.

DC blocking capacitors are often large in value, and a mute circuit is needed during power up to minimize click and pop. The output capacitor and mute circuit consume PCB area and increase cost of assembly, and can reduce the fidelity of the audio output signal.

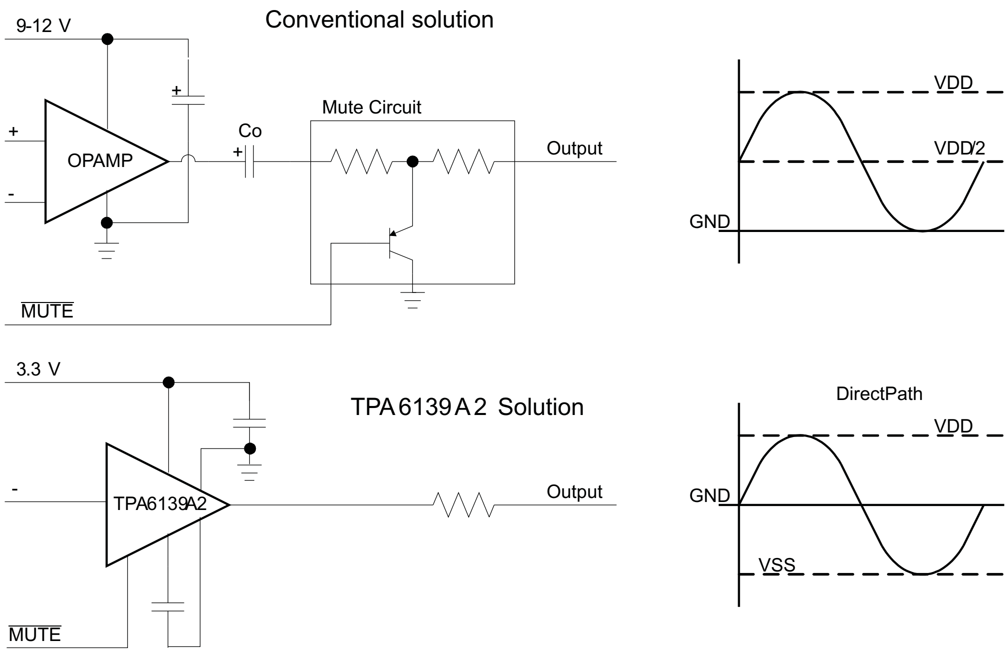


Figure 9. Conventional and DirectPath Line Driver

The DirectPath™ amplifier architecture operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail.

Combining the user-provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split supply mode.

The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. Combining this with the built-in click and pop reduction circuit, the DirectPath™ amplifier requires no output dc blocking capacitors.

The bottom block diagram and waveform of Figure 9 illustrate the ground-referenced line-driver architecture. This is the architecture of the TPA6139A2.

COMPONENT SELECTION

Charge Pump

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The VSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low ESR capacitors are an ideal selection, and a value of 1μF is typical. Capacitor values that are smaller than 1μF cannot be recommended as it limits the negative voltage swing in low impedance loads.

Decoupling Capacitors

The TPA6139A2 is a DirectPath™ amplifier that requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1μF, placed as close as possible to the device VDD leads works best. Placing this decoupling capacitor close to the TPA6139A2 is important for the performance of the amplifier. For filtering lower frequency noise signals, a 10-μF or greater capacitor placed near the audio power amplifier also helps, but it is not required in most applications because of the high PSRR of this device.

Gain-Setting

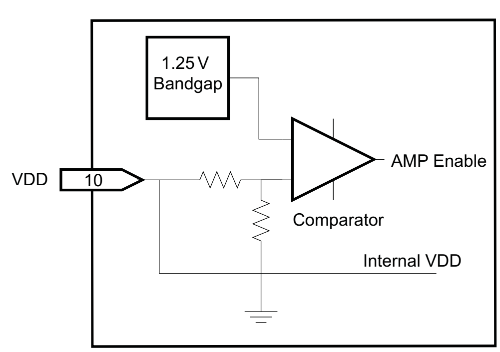
The gain setting is programmed with the GAIN pin individually for line driver and headphone section. Gain setting is latched when the $\overline{\text{MUTE}}$ pin is set high. Table 1 lists the gain settings. The default gain with the gain-set pin left open is –2x.

Table 1. Gain Settings

Gain_set RESISTOR	GAIN	GAIN (dB)	INPUT RESISTANCE
No connect	–2.0x	6.0	37k
82k0	–1.0x	0.0	55k
49k2	–1.5x	3.5	44k
35k1	–2.3x	7.2	33k
27k3	–2.5x	8.0	31k
20k5	–3.0x	9.5	28k
15k4	–3.5x	10.9	24k
11k5	–4.0x	12.0	22k
9k09	–5.0x	14.0	18k
7k50	–5.6x	15.0	17k
6k19	–6.4x	16.1	15k
5k11	–8.3x	18.4	12k
3k90	–10x	20.0	10k

Internal Under Voltage Detection

The TPA6139A2 contains an internal precision band gap reference voltage and a comparator used to monitor the supply voltage, VDD. The internal VDD monitor is set at 2.8V with 200mV hysteresis.



Input-Blocking Capacitors

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the TPA6139A2. These capacitors block the dc portion of the audio source and allow the TPA6139A2 inputs to be properly biased to provide maximum performance. The input blocking capacitors also limit the DC gain to 1, limiting the DC-offset voltage at the output.

These capacitors form a high-pass filter with the input resistor, R_{IN}. The cutoff frequency is calculated using Equation 1. For this calculation, the capacitance used is the input-blocking capacitor and the resistance is the input resistor chosen from Table 1. Then the frequency and/or capacitance can be determined when one of the two values is given.

$$fc_{IN} = \frac{1}{2\pi R_{IN} C_{IN}} \quad \text{or} \quad C_{IN} = \frac{1}{2\pi fc_{IN} R_{IN}} \qquad (1)$$

For a fixed cutoff frequency of 2Hz the size of the input capacitance is shown in the table below with the capacitors rounded up to nearest E6 values. For 20Hz cutoff simply divide the capacitor values with 10; e.g., for 1x gain, 150nF is needed.

Table 2. Input Capacitor for Different Gain and Cutoff

Gain_set RESISTOR	GAIN	Gain (dB)	INPUT RESISTANCE	2 Hz Cutoff
249k	–2.0x	6.0	37k	2.2 µF
82k0	–1.0x	0.0	55k	1.5 µF
49k2	–1.5x	3.5	44k	2.2 µF
35k1	–2.3x	7.2	33k	3.3 µF
27k3	–2.5x	8.0	31k	3.3 µF
20k5	–3.0x	9.5	28k	3.3 µF
15k4	–3.5x	10.9	24k	3.3 µF
11k5	–4.0x	12.0	22k	4.7 µF
9k09	–5.0x	14.0	18k	4.7 µF
7k50	–5.6x	15.0	17k	4.7 µF
6k19	–6.4x	16.1	15k	6.8 µF
5k11	–8.3x	18.4	12k	6.8 µF
3k90	–10x	20.0	10k	10 µF

Pop-Free Power Up

Pop-free power up is ensured by keeping the $\overline{\text{MUTE}}$ low during power supply ramp up and down. The pin should be kept low until the input AC-coupling capacitors are fully charged before asserting the $\overline{\text{MUTE}}$ pin high to pre-charge the ac-coupling; and, pop-less power-up is achieved. Figure 10 illustrates the preferred sequence.

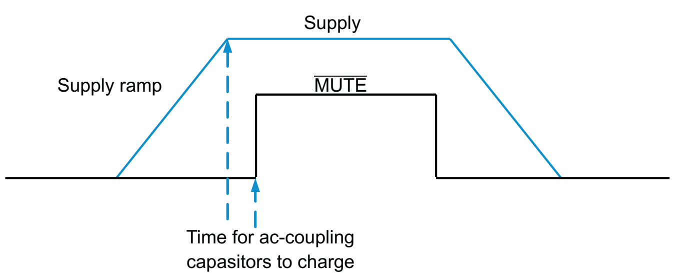


Figure 10. Power-Up Sequence

CAPACITIVE LOAD

The TPA6139A2 has the ability to drive a high capacitive load up to 220 pF directly. Higher capacitive loads can be accepted by adding a series resistor of 47 Ω or larger for the line driver output.

LAYOUT RECOMMENDATIONS

A proposed layout for the TPA6139A2 can be seen in the TPA6139A2EVM User's Guide (SLOU248), and the Gerber files can be downloaded from http://focus.ti.com/docs/toolsw/folders/print/TPA6139A2evm.html. To access this information, open the TPA6139A2 product folder and look in the Tools and Software folder.

Ground traces are recommended to be routed as a star ground to minimize hum interference. VDD, VSS decoupling capacitors and the charge pump capacitors should be connected with short traces.

PIN COMPATIBLE WITH THE DRV612

The TPA6139A2 stereo Headphone amplifier is pin compatible with the DRV612 . A single PCB layout can therefore be used with stuffing options for different board configurations.

APPLICATION CIRCUIT

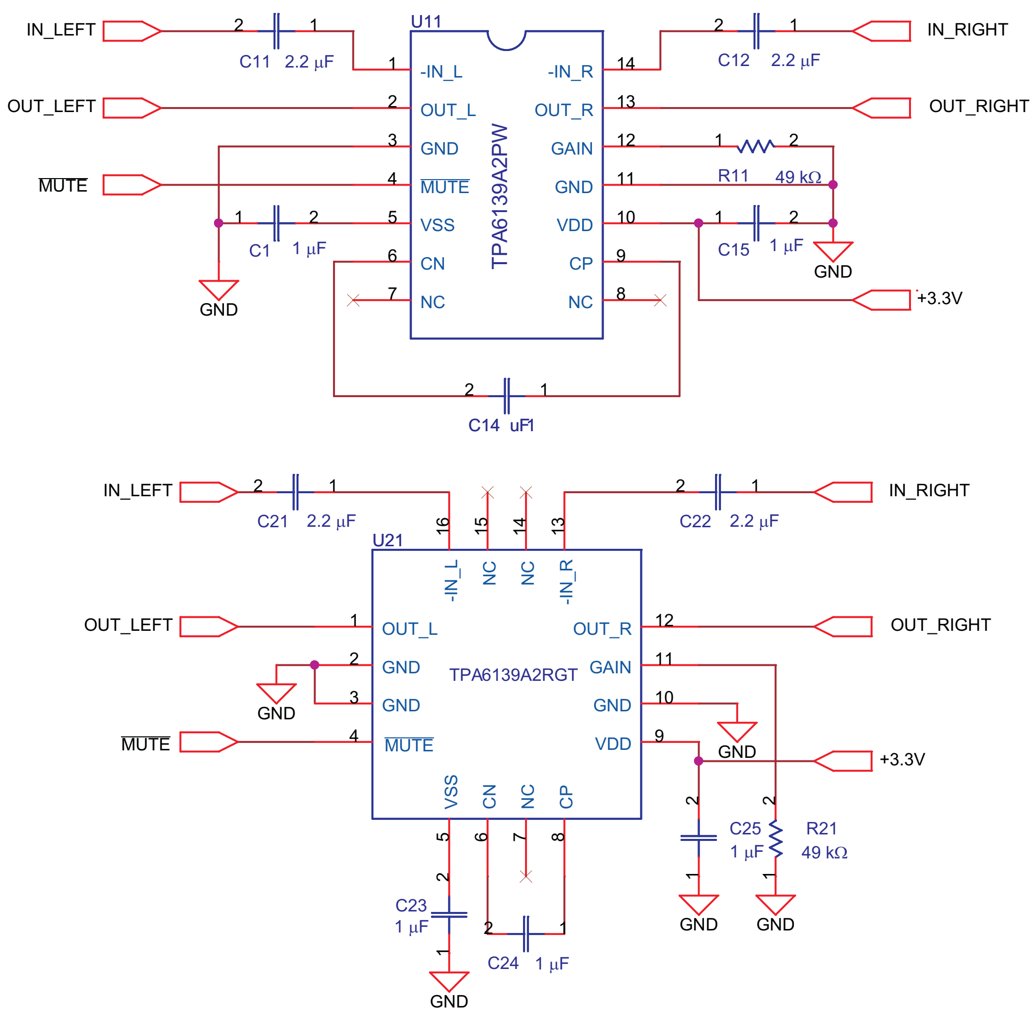


Figure 11. Single Ended Input and Output, Gain Set to –1.5x

REVISION HISTORY

NOTE: Page numbers in current version may differ from previous versions.

Changes from Original (January 2011) to Revision A	Page
• Changed "2.5-mW" to "25-mW" in Title line and added revision A - May 2011 pub date to Header infomation	1
• Changed pin assignment figures to match package outline drawings	2
• Changed conditions statement from "R_{IN} = 10 kΩ, R_{fb} = 20 kΩ" to "Step = –2V/V" for TYP CHARA, LINE DRIVER section	7
• Changed conditions statement from "R_{IN} = 10 kΩ, R_{fb} = 20 kΩ" to "Step = –2V/V" for TYP CHARA, LINE DRIVER section	8

Changes from Revision A (May 2011) to Revision B	Page
• Changed the RGT package From: Preview To: Production	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPA6139A2PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA6139	Samples
TPA6139A2PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA6139	Samples
TPA6139A2RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	T6139	Samples
TPA6139A2RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	T6139	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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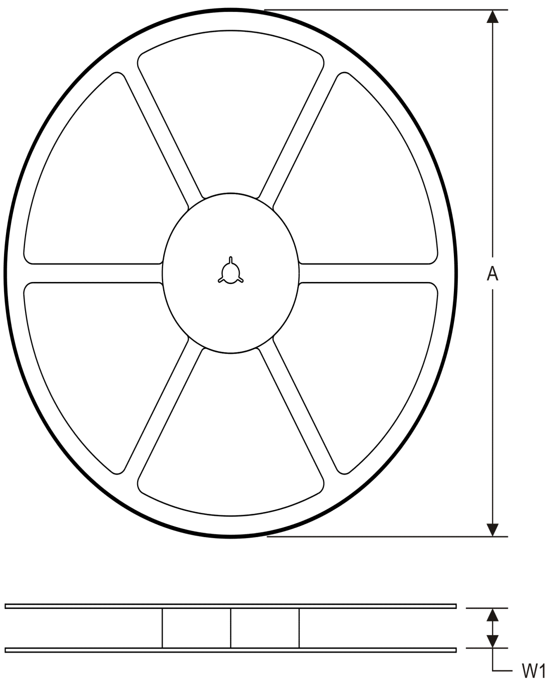
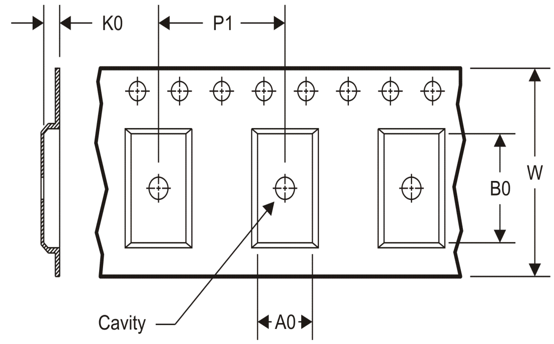
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





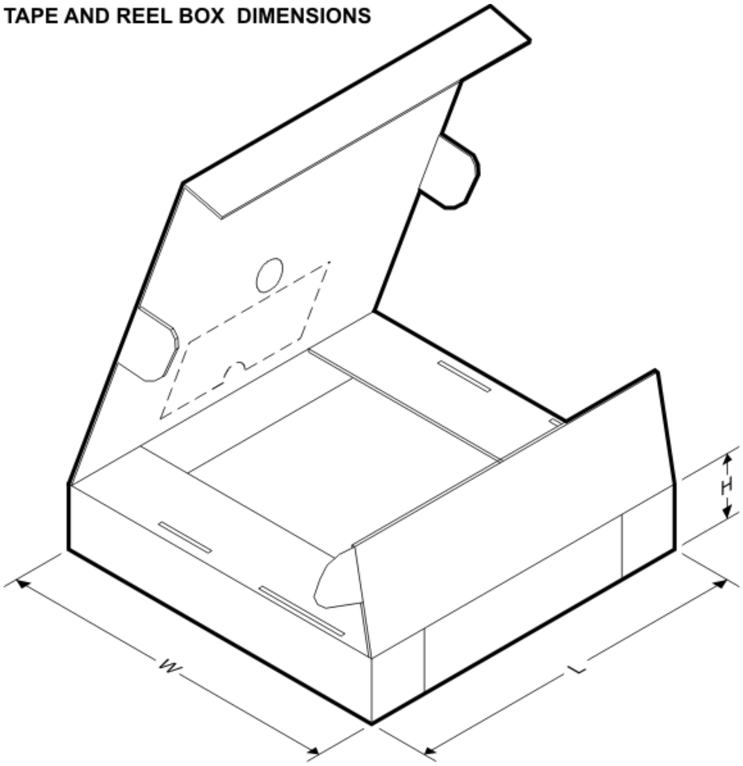
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6139A2PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPA6139A2RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPA6139A2RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

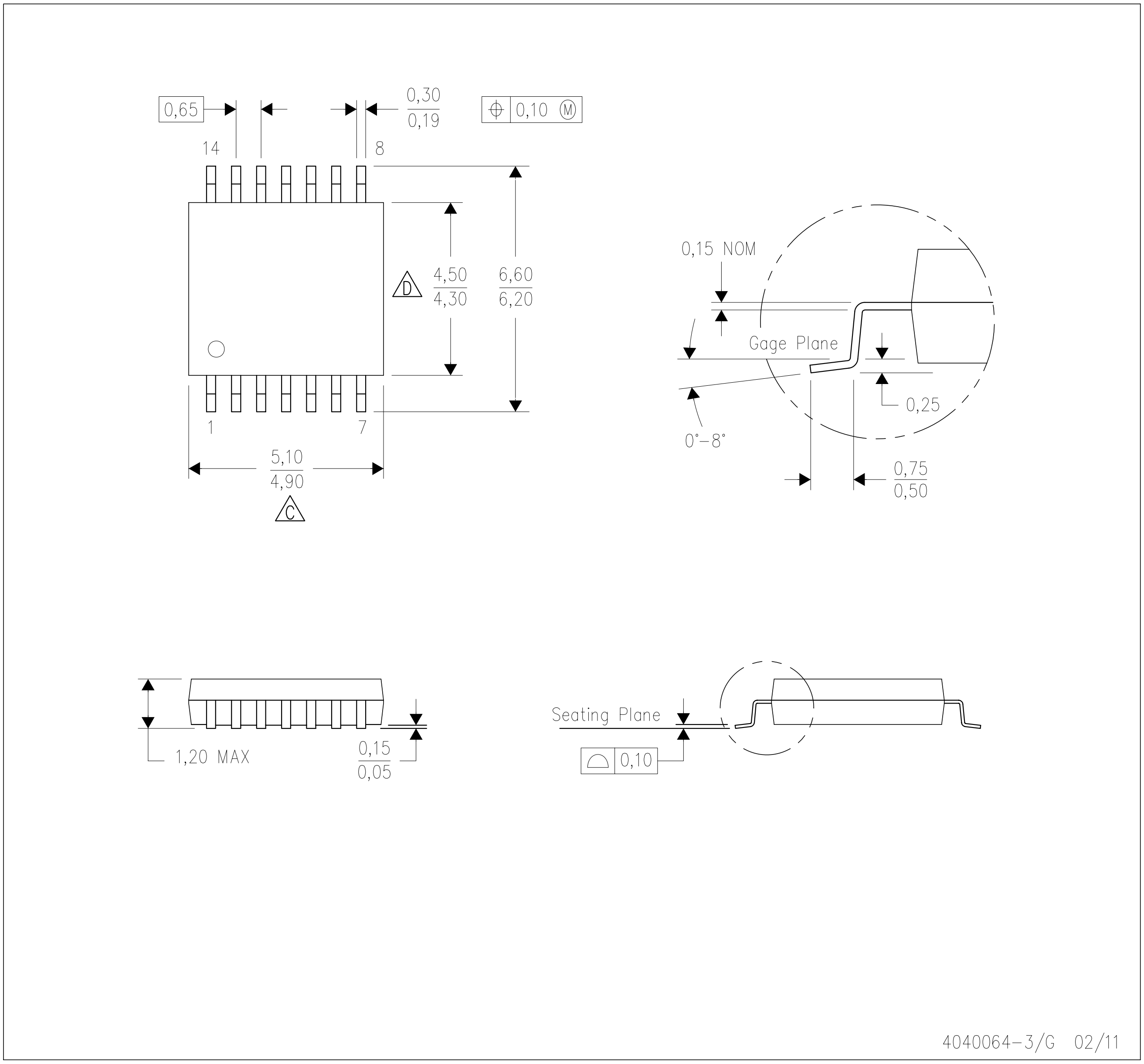
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

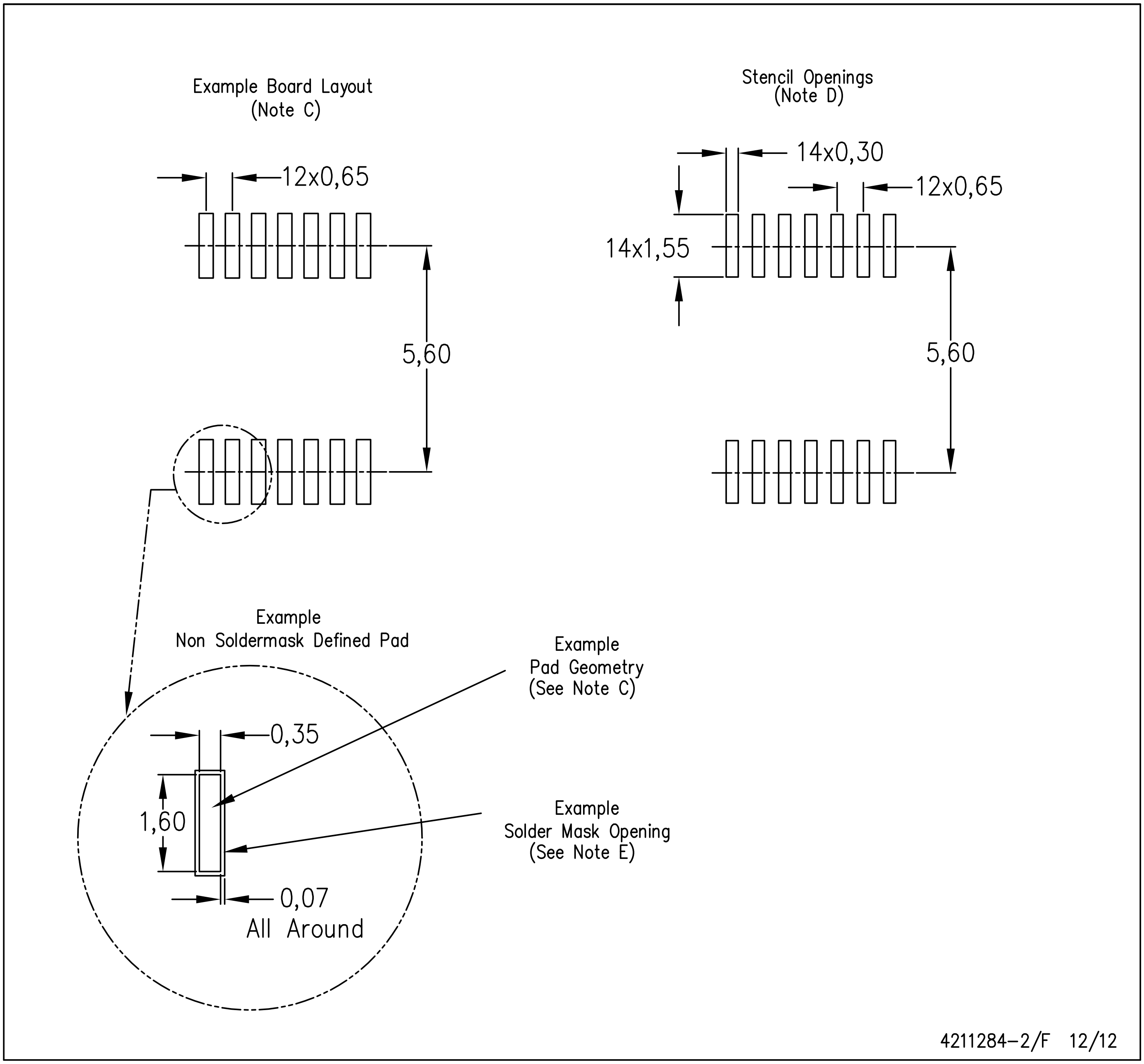
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6139A2PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TPA6139A2RGTR	QFN	RGT	16	3000	367.0	367.0	35.0
TPA6139A2RGTT	QFN	RGT	16	250	210.0	185.0	35.0

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



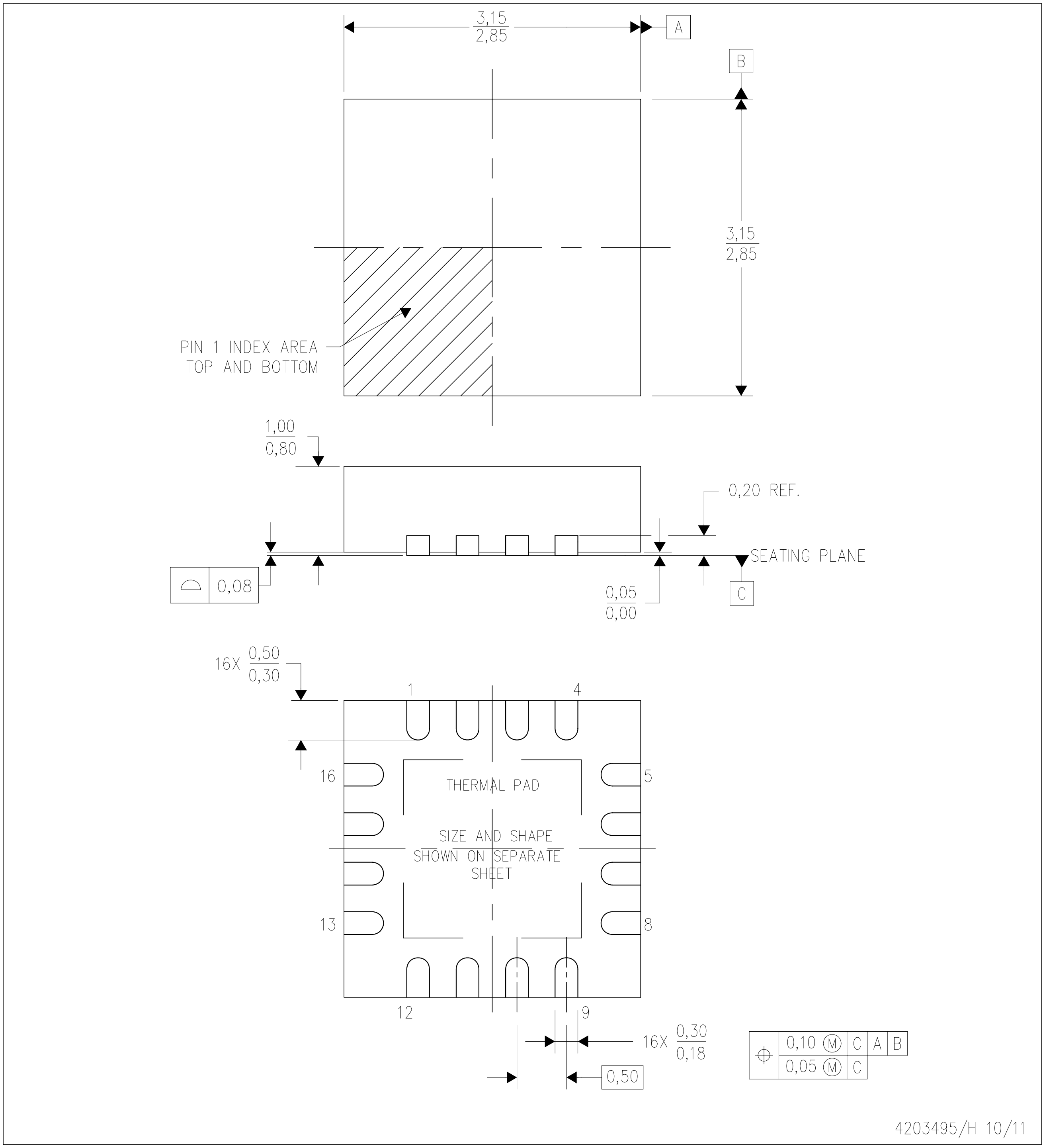
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGT (S-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO-220.

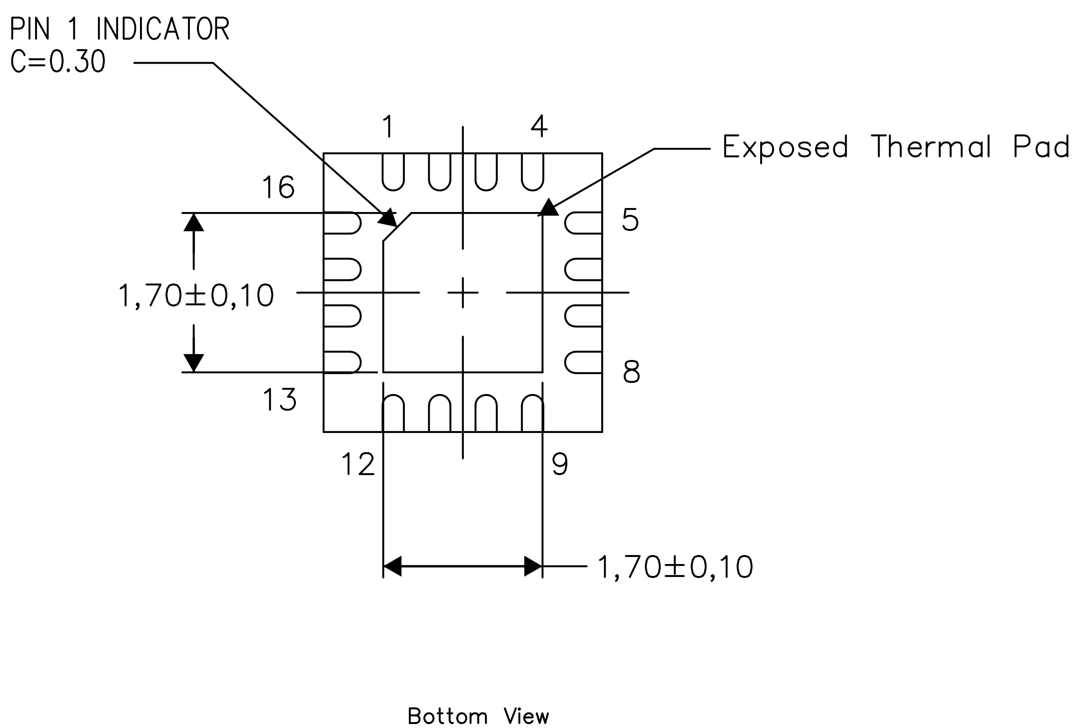
RGT (S-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

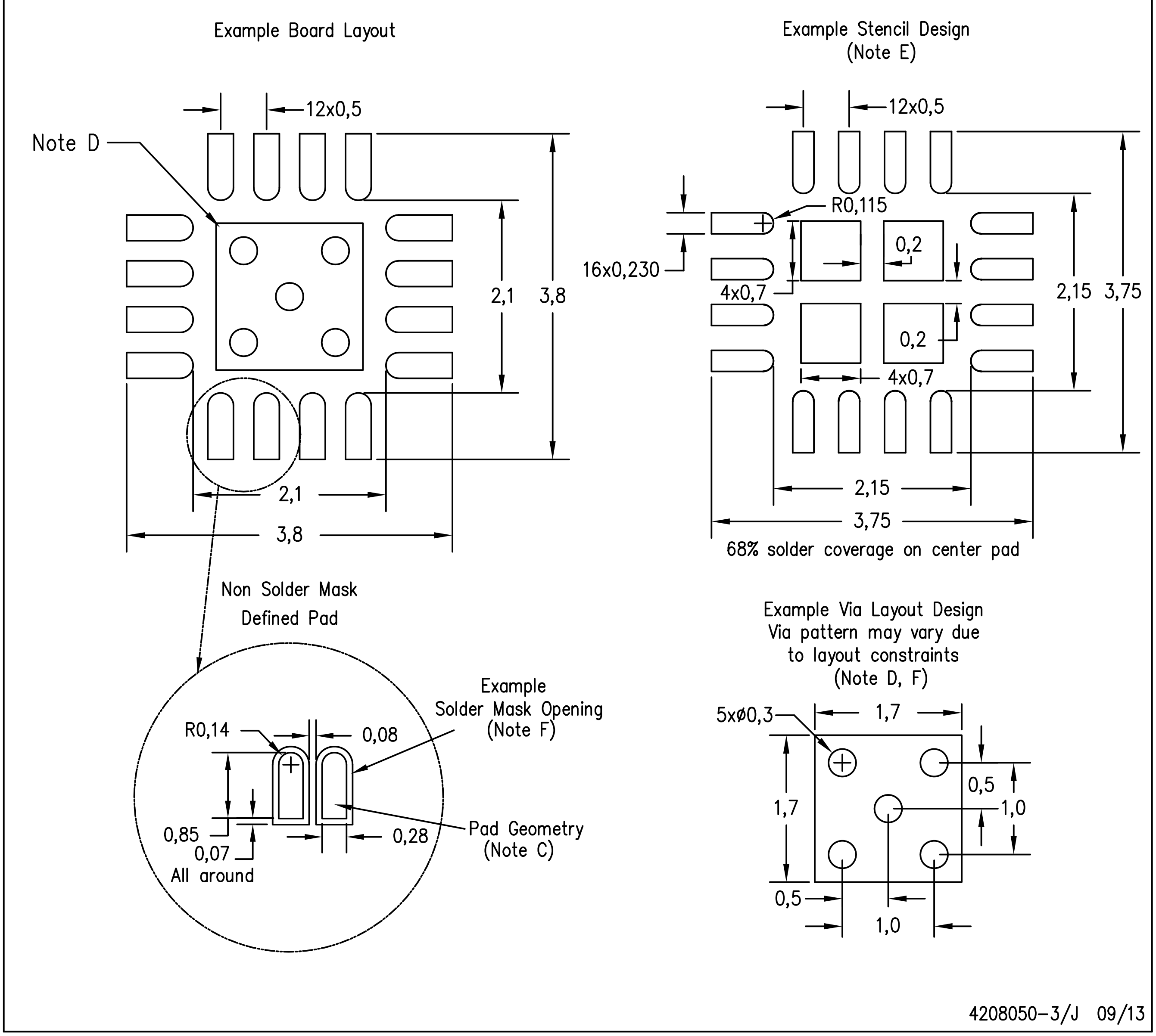


Exposed Thermal Pad Dimensions

4206349-4/U 09/13

NOTE: All linear dimensions are in millimeters

RGT (S-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.