4-CH Bidirectional Low Capacitance ESD Protection Device with 15kV Contact and Ultra Low Clamping Voltage

Check for Samples: TPD4E101

FEATURES

- **Provides System Level ESD Protection for Low-voltage IO Interface**
- **IEC 61000-4-2 Level 4**
  - **±15kV (Air discharge)**
  - **±15kV (Contact discharge)**
- **IEC 61000-4-5 (Surge): 3A (8/20 µs)**
- **IO Capacitance 4.8pF (Typ)**
- **$R_{DYNAMIC}$ 0.45Ω (Typ)**
- **DC Breakdown Voltage ±6V (Min)**
- **Ultra low Leakage Current 100nA (Max)**
- **10V Clamping Voltage (Max at Ipp = 1A)**
- **Industrial Temperature Range: –40°C to 125°C**
- **Space Saving DPW package (0.8mm x 0.8mm)**

APPLICATIONS

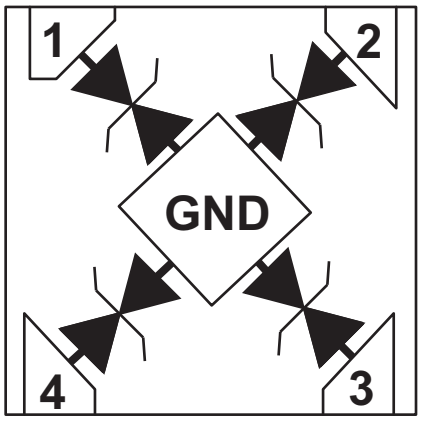
- **Cell Phones**
- **eBook**
- **Portable Media Players**
- **Digital Camera**
- **Tablet PC**
- **Set Top Box**

DESCRIPTION

The TPD4E101 is a four channel ESD protection device in an ultra small DPW package. It is the industry's smallest 4-ch ESD protection device with 0.48mm pitch. This larger pitch helps save on PCB manufacturing costs. The device provides IEC61000-4-2 compliance up to 15kV contact discharge. It has an ESD clamp circuit with back-to-back diodes for bipolar/bidirectional signal support. The 7pF line capacitance is suitable for a wide range of applications supporting data rate up to 700Mbps.Typical application areas in portable applications are:

- Audio lines (Microphone, Earphone and Speakerphone)
- SD interface
- SIM interface
- Keypad or other buttons

DEVICE CONFIGURATION



0.8 mm x 0.8mm DPW Package
(Bottom View)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating temperature range	–40	125	ºC
Storage temperature	–65	155	ºC
IEC 61000-4-2 Contact Discharge		±15	kV
IEC 61000-4-2 Air-gap Discharge		±15	kV
Peak Pulse Current (tp = 8/20 µs)		3	A
Peak Pulse Power (tp = 8/20 µs)		40	W

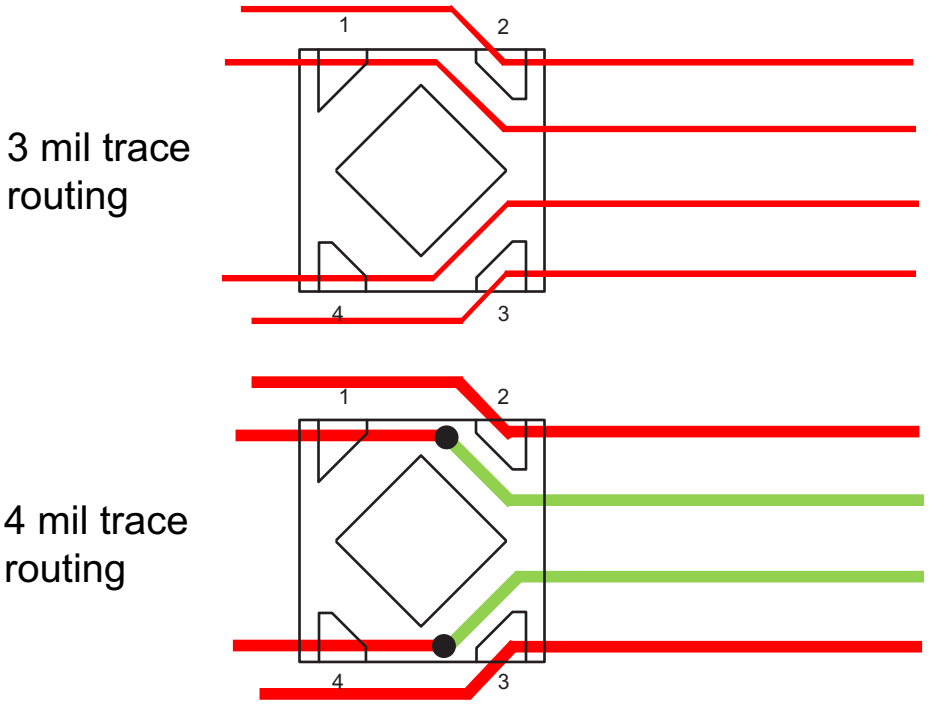
ELECTRICAL CHARACTERISTICS

T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage				±5.5	V
I_{LEAK}	Leakage current	Pins = 5 V, GND = 0 V			100	nA
VClamp1,2	Clamp voltage from data pin to ground pin	I_{PP} = 1 A, 8/20 µs(1)		10		V
		I_{PP} = 3 A, 8/20 µs(1)		13		V
VClamp2,1	Clamp voltage from ground pin to data pin	I_{PP} = 1 A, 8/20 µs(1)		9		V
		I_{PP} = 3 A, 8/20 µs(1)		13		V
R_{DYN}	Dynamic resistance	Pins to GND(2)		0.45		Ω
		GND to Pins(2)		0.42		Ω
C_{IO}	IO Capacitance	V_{IO} = 2.5 V		4.8	7	pF
V_{BRF}	Break-down voltage, pin 1, 2, 3, or 4 to GND	I_{IO} = 1 mA	6			V
V_{BRR}	Break-down voltage, GND to pin 1, 2, 3, or 4	I_{IO} = 1 mA	6			V

(1) Non-repetitive current pulse 8/20 us exponentially decaying waveform according to IEC61000-4-5
(2) Extraction of RDYN using least squares fit of TLP characteristics between I=10A AND I=20A

BOARD LAYOUT RECOMMENDATION



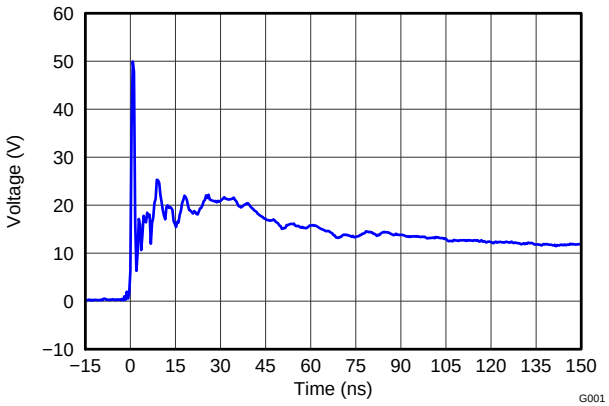


Figure 1. IEC 61000-4-2 Clamping Voltage, +8kV Contact

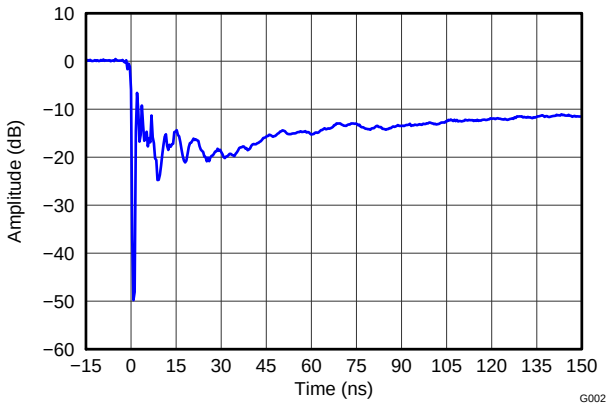


Figure 2. IEC 61000-4-2 Clamping Voltage, -8kV Contact

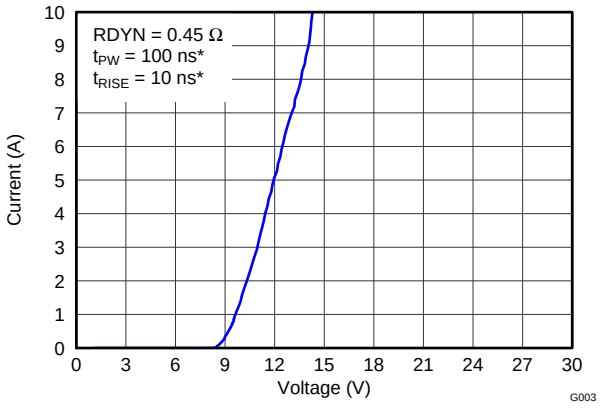


Figure 3. TLP, t_{PW} = 100nS, t_{RISE} = 10nS, Data to GND

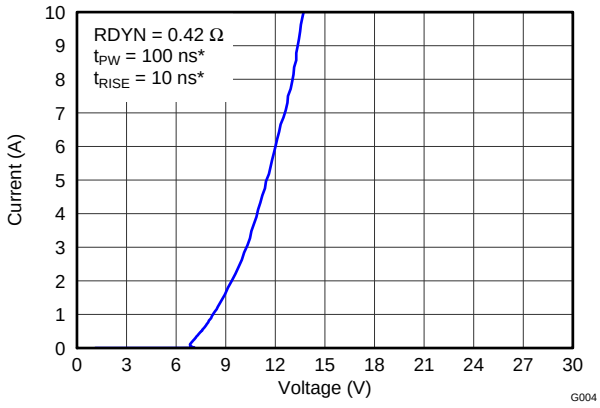


Figure 4. TLP, t_{PW} = 100nS, t_{RISE} = 10nS, GND to Data

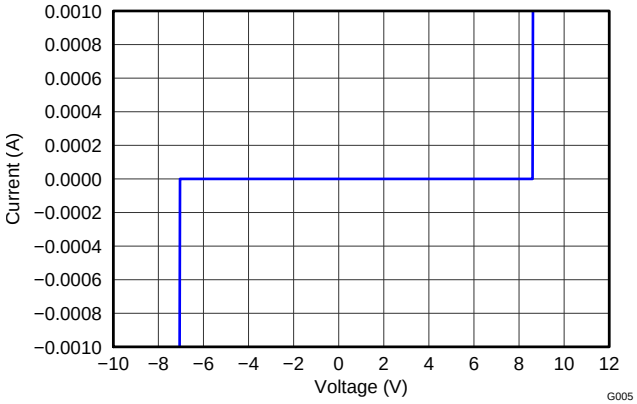


Figure 5. IV Curve

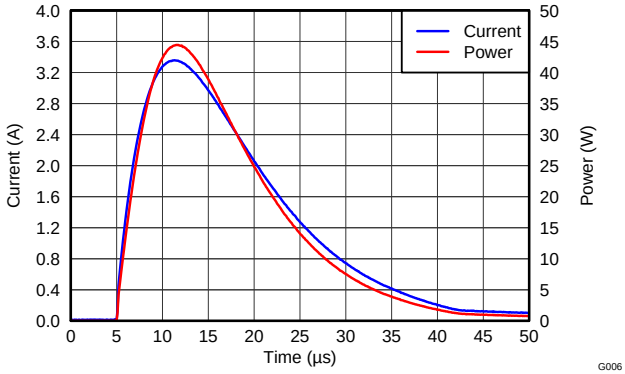


Figure 6. Surge Curves, Data to GND

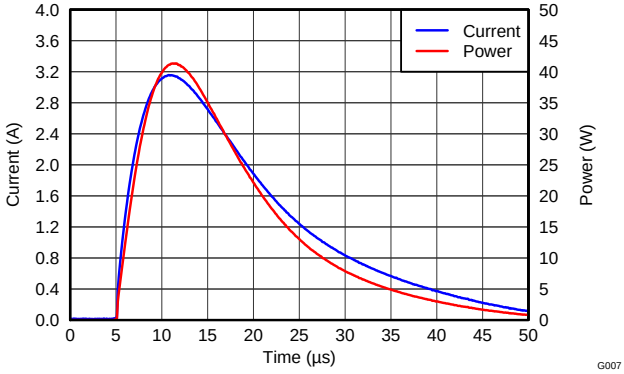


Figure 7. Surge Curves, GND to Data

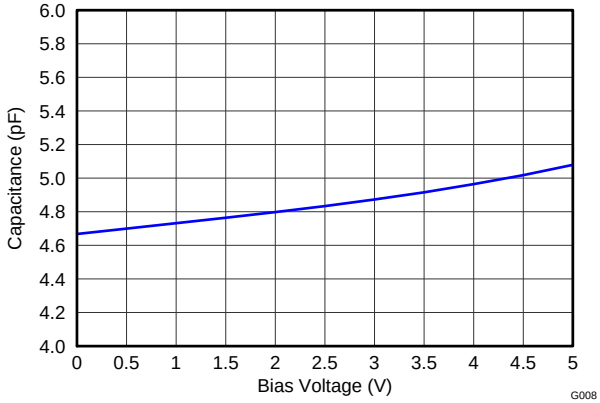


Figure 8. Capacitance

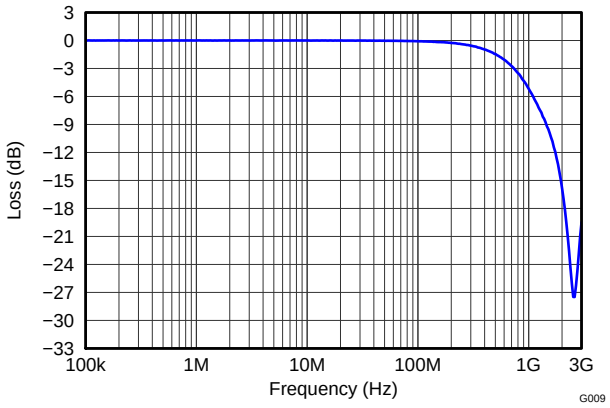


Figure 9. Insertion Loss

REVISION HISTORY

Changes from Original (August 2012) to Revision A **Page**

- Revised document to release full version of Datasheet. 1

Changes from Revision A (January 2013) to Revision B **Page**

- Updated PARAMETER wording for VClamp1,2 and VClamp2,1 2

Changes from Revision B (May 2013) to Revision C **Page**

- Updated first page formatting. 1
- Removed Ordering Information table 1
- Changed VClamp1,2 Test Condition From: I_{PP} = 5 A, 8/20 µs To: I_{PP} = 3 A, 8/20 µs 2
- Changed VClamp2,1 Test Condition From: I_{PP} = 5 A, 8/20 µs To: I_{PP} = 3 A, 8/20 µs 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD4E101DPWR	ACTIVE	X2SON	DPW	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	A1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

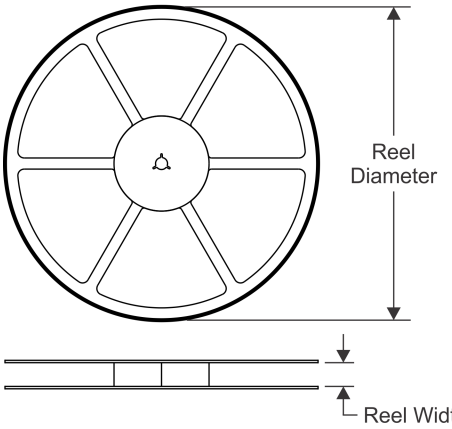
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

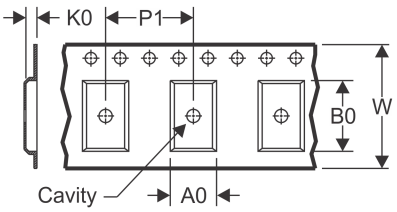
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

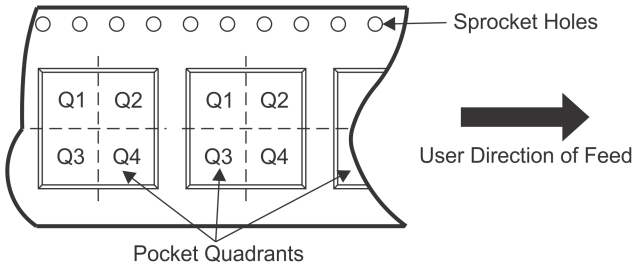


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

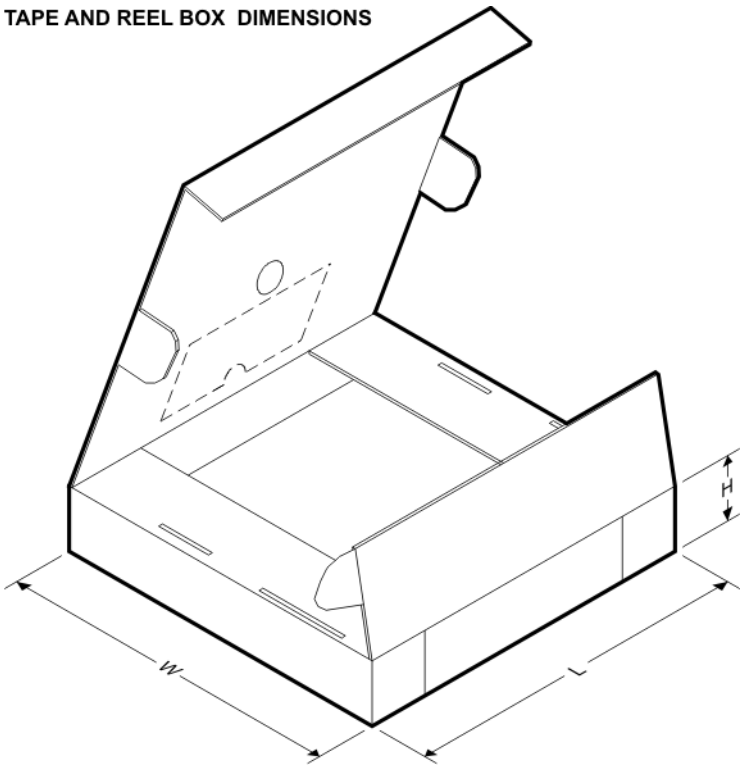
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E101DPWR	X2SON	DPW	4	3000	180.0	9.5	0.91	0.91	0.5	4.0	8.0	Q2

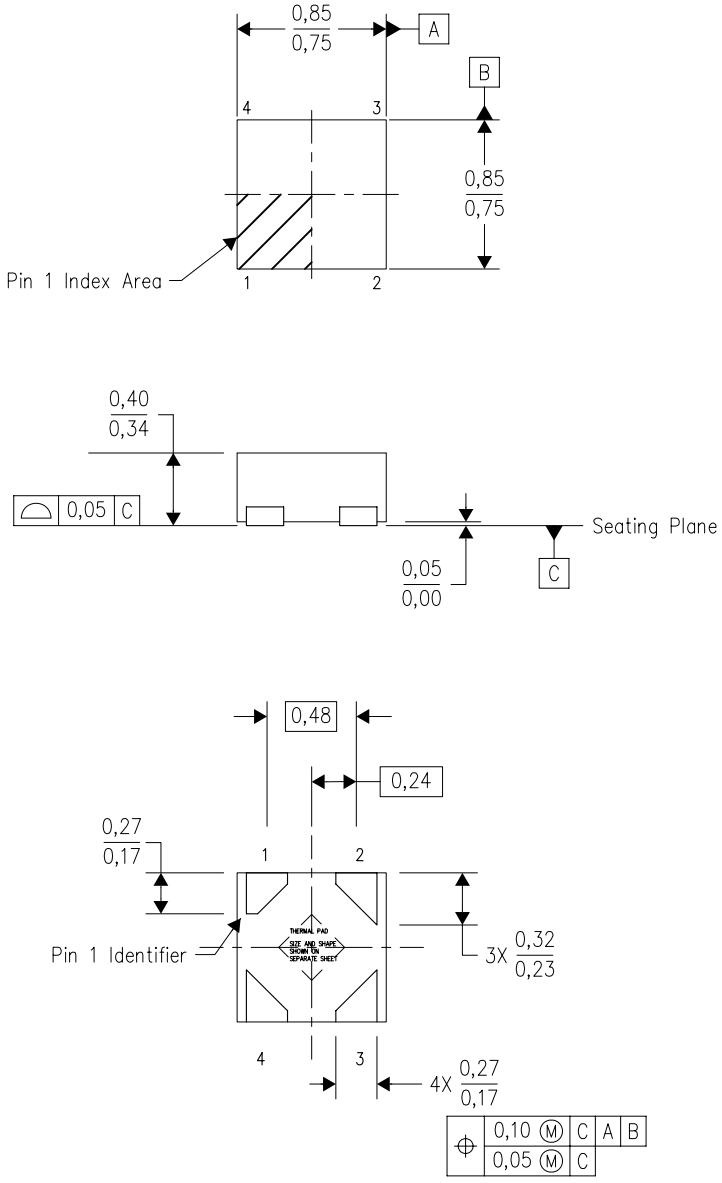
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E101DPWR	X2SON	DPW	4	3000	180.0	180.0	30.0

DPW (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD



4211218/C 05/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

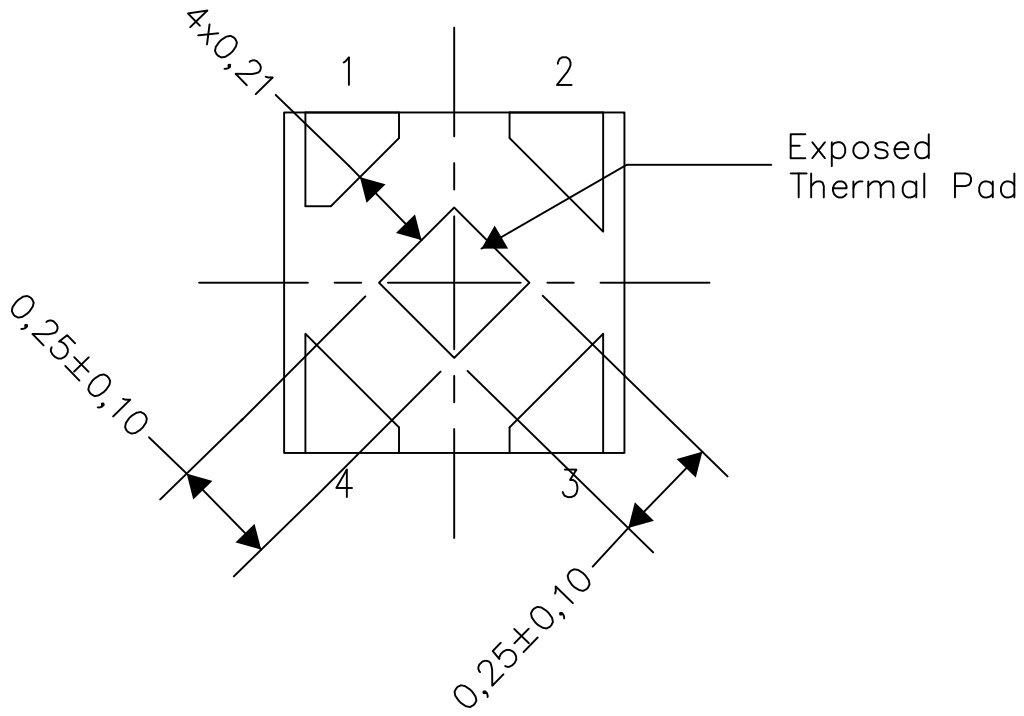
DPW (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



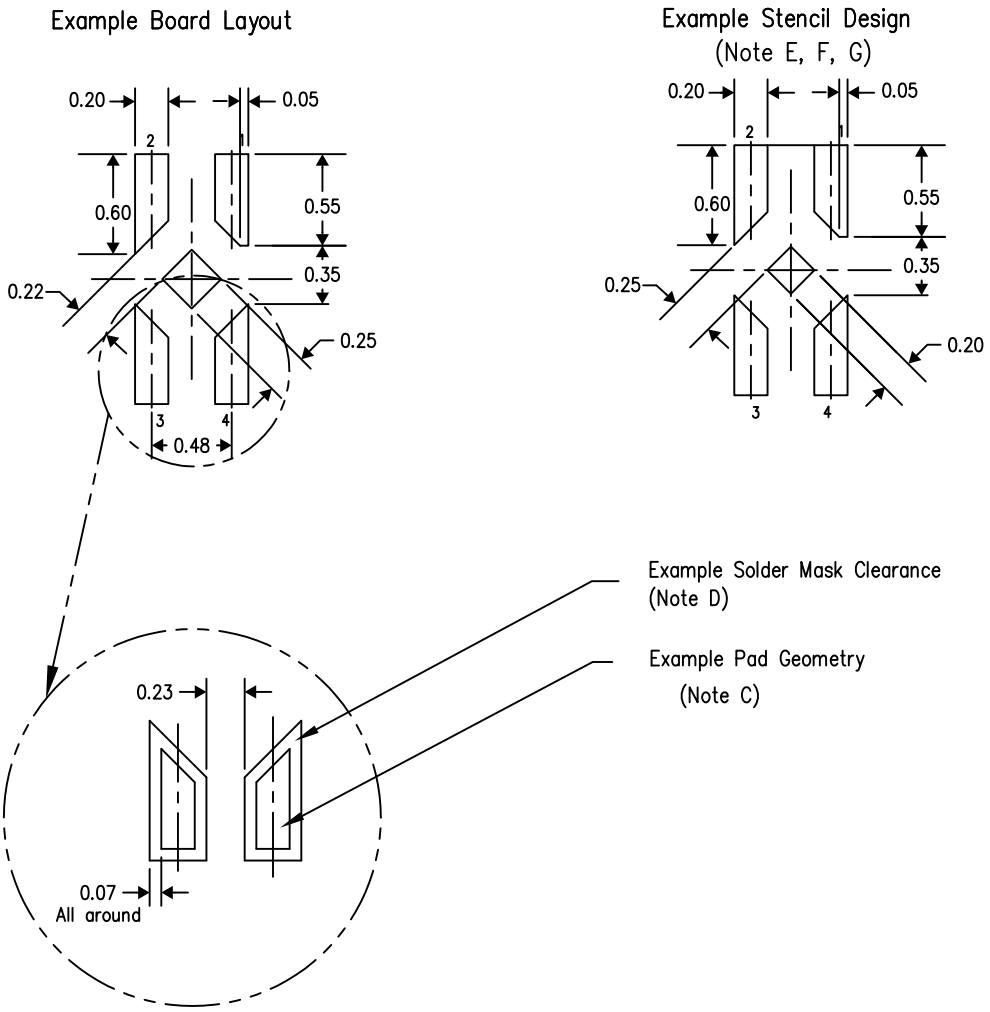
Bottom View

Exposed Thermal Pad Dimensions

4211578/G 07/13

NOTES: All linear dimensions are in millimeters

DPW (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD



4211735/F 07/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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