HDMI COMPANION CHIP WITH LEVEL SHIFTING BUFFER 5V LOAD SWITCH AND ESD PROTECTION

Check for Samples: TPD5S116

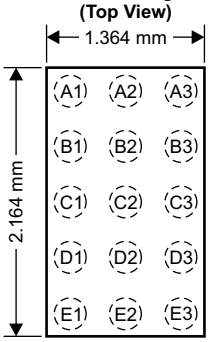
FEATURES

- **Conforms to HDMI Control and 5VOUT Compliance Tests Without External Components**
- **Supports HDMI1.3 and HDMI1.4 Standard**
- **Auto-direction Sensing I2C Level Shifter With One-Shot Circuit to Drive Long HDMI Cable (750-pF Load)**
- **Back Drive Protection**
- **55mA Load Switch With Short Circuit Protection**
- **Pb-free and RoHS Compliant (Dark Green Compliant)**
- **Hot Plug Detect Module With Pull Down Resistor**
- **Integrated Pull-up and Pull-down Resistors per HDMI Specification**
- **IEC61000-4-2 ±15kV Contact Rating**
- **IEC61000-4-2 ±15kV Air-gap Rating**
- **Utility Pin ESD Protection for Ethernet and Audio Return**

APPLICATIONS

- **Cell Phones**
- **eBook**
- **Portable Media Players**
- **Tablet**

YFF Package (Top View)



Pin Mapping (Top View)

	1	2	3
A	CEC_SYS	VCCA	CEC_CON
B	SCL_SYS	GND	SCL_CON
C	SDA_SYS	EN	SDA_CON
D	5V_SYS	GND	5V_CON
E	HPD_SYS	UTI_CON	HPD_CON

DESCRIPTION/ORDERING INFORMATION

TPD5S116 is a single-chip HDMI interface device with auto-direction sensing I2C voltage level shift buffers, 5V HDMI compliant current limited load switch, hot-plug-detect, and integrated ESD protection clamps for all connector side pins. The device pin mapping can be routed to either HDMI Type D or Type C connector. An internal 3.3V node powers the CEC pin, eliminating the need for a 3.3V supply on board.

TPD5S116 integrates all external termination resistors at the HPD, CEC, SCL, and SDA lines. There are three non-inverting bi-directional translation circuits for the SDA, SCL, and CEC lines. Each has a common power rail (VCCA) on system side from 1.1 V to 3.6V. A 55mA current limiting switch regulates current sent from 5V_SYS to 5V_CON. The SCL and SDA pins meet the I2C specification and can drive up to 750 pF capacitive loads, which exceeds HDMI1.4 specifications. The HPD_CON port has a glitch filter to avoid false detection due to plug bouncing during the HDMI connector insertion.

The TPD5S116 offers reverse current block at the 5V_CON pin. In fault conditions, such as when two HDMI transmitters are connected to the same HDMI cable, TPD5S116 ensures that the system is safe from powering up through external HDMI transmitter. The SCL_CON, SDA_CON, CEC_CON pins also feature reverse-current blocking, which ensures that the system sees no leakage if an HDMI receiver is connected while the system if powered off.

The EN pin enables the hot-plug detect and load switch. The level shifters are enabled after a valid HPD signal is detected.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	YFF	Tape and reel	TPD5S116YFFR	RE116

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

CIRCUIT SCHEMATIC DIAGRAM

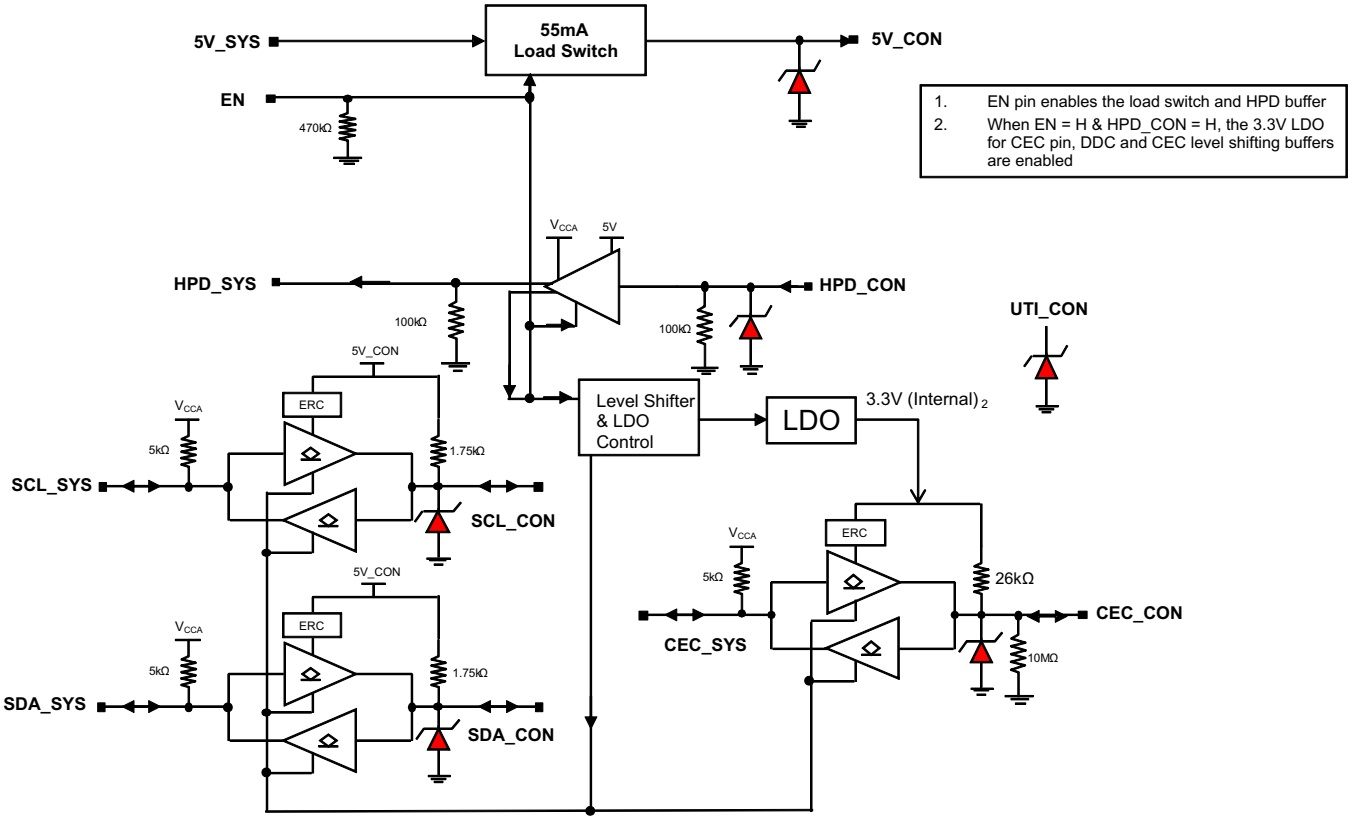


Figure 1. Circuit Schematics

APPLICATION INFORMATION

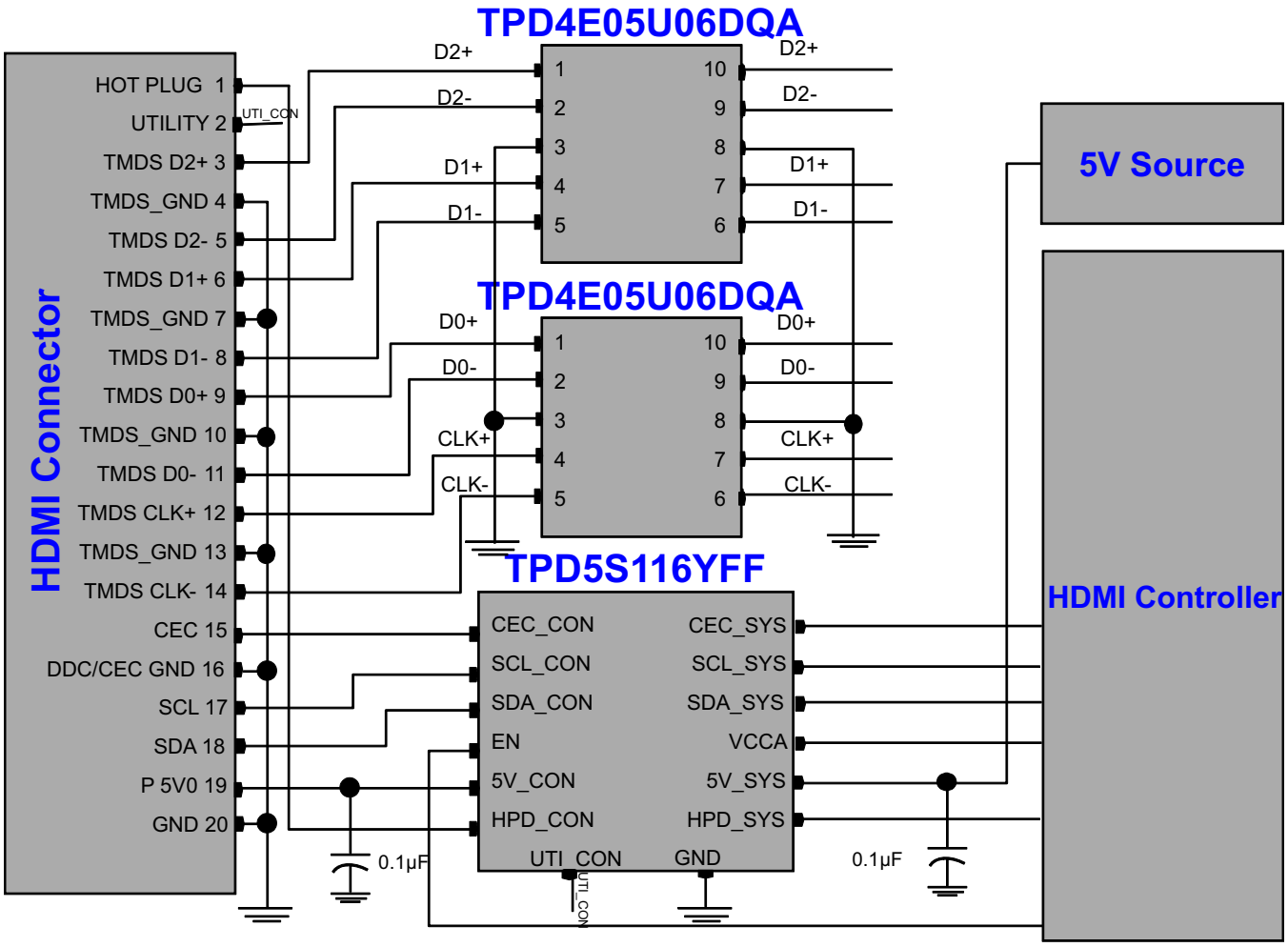


Figure 2. Application Schematics for HDMI Controllers with one GPIO for HDMI Interface Control

HDMI Driver Chip is controlling the TPD5S116 via only one control line (EN). The DDC and CEC level shifting buffers become active after HPD_CON receives a valid high signal and EN is high.

Table 1. FUNCTION TABLE – POWER SAVING OPTIONS

HPD_CON	EN	VCCA	5V_SYS	5V_CON	Dxx_SYS CEC_SYS Pull-ups	DCC_C ON Pull-ups	CEC_CON Pull-ups	CEC LDO	LOAD SW & HPD	DCC/CEC VLTs	ICCA Typ	ICC5V Typ	Comments
L	**L**	1.2V – 5.0V	5.0V	High-Z	Off	Off	Off	Off	Off	Off	1µA	2µA	Fully Disabled
L	**H**	1.2V – 5.0V	5.0V	5.0V	On	On	Off	Off	On	Off	1µA	30µA	Load Switch on
H	**L**	1.2V – 5.0V	5.0V	High-Z	Off	Off	Off	Off	Off	Off	1µA	2µA	Not Valid State
H	**H**	1.2V – 5.0V	5.0V	5.0V	On	On	On	On	On	On	24µA	125µA	Fully On
X	**X**	0V	0V	High-Z	High-Z	High-Z	High-Z	Off	Off	Off	0	0	Power Down
X	**X**	1.2V – 5.0V	0V	High-Z	High-Z	High-Z	High-Z	Off	Off	Off	1	0	Power Down
X	**X**	0V	5.0V	High-Z	High-Z	High-Z	High-Z	Off	Off	Off	0	1	Power Down

TERMINAL FUNCTIONS

PIN NAME	YFF	PIN TYPE	DESCRIPTION
HPD_SYS	E1	Output	HDMI system side: Hot plug detect Output referenced to VCCA. Connect to HDMI controller Hot plug detect input pin
HPD_CON	E3	Input	HDMI connector side: Hot plug detect Input. Connect directly to HDMI Connector Hot Plug Detect pin
CEC_SYS	A1	IO Port	HDMI system side CEC signal pin referenced to VCCA. Connect to HDMI controller.
CEC_CON	A3	IO Port	HDMI connector side CEC signal pin referenced to internal 3.3V supply. Connect to HDMI connector CEC pin.
SCL_SYS	B1	IO Port	HDMI system side SCL signal pin referenced to VCCA. Connect to HDMI controller.
SCL_CON	B3	IO Port	HDMI connector side SCL signal pin referenced to 5V_CON supply. Connect to HDMI connector SCL pin.
SDA_SYS	C1	IO Port	HDMI system side SDA signal pin referenced to VCCA. Connect to HDMI controller.
SDA_CON	C3	IO Port	HDMI connector side SDA signal pin referenced to 5V_CON supply. Connect to HDMI connector SDA pin.
EN	C2	Control Input	Disables the load switch and HPD when EN =L. The EN pin is referenced to VCCA
UTI_CON	E2	IO Port	Protects the HDMI connector's utility pin
5V_SYS	D1	Input Power	System side PCB 5V supply; input of load switch
VCCA	A2	Input Supply	Internal PCB Low Voltage Supply (Same as the HDMI Controller Chip Supply)
5V_CON	D3	Output Power	HDMI connector side external 5V Supply; output of load switch
GND	B2, D2	Ground	Connect to System Ground Plane

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		–0.3	6.0	V
5V_SYS	Supply voltage range		–0.3	6.0	V
V_I	Input voltage range(2)	SCL_SYS, SDA_SYS, CEC_SYS, EN	–0.3	6.0	V
		SCL_CON, SDA_CON, CEC_CON, HPD_CON	–0.3	6.0	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)(3)	SCL_SYS, SDA_SYS, CEC_SYS, HPD_SYS	–0.3	6.0	V
		SCL_CON, SDA_CON, CEC_CON, HPD_CON	–0.3	6.0	
V_O	Voltage range applied to any output in the high or low state(2)(3)	SCL_SYS, SDA_SYS, CEC_SYS,HPD_SYS	–0.3	V_{CCA} + 0.5	V
		SCL_CON, SDA_CON, CEC_CON	–0.3	5V_SYS + 0.5	
I_{IK}	Input clamp current	VI < 0		–50	mA
I_{OK}	Output clamp current	VO < 0		–50	mA
	Continuous current through 5V_SYS, or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CCA}	Supply Voltage			1.1		5.5	V
5V_SYS	Supply Voltage			4.5		5.5	V
V_{IH}	High-level input voltage	SCL_SYS, SDA_SYS,	V_{CCA} = 1.1 V to 5.5 V	0.7 × V_{CCA}		V_{CCA}	V
		CEC_SYS,	V_{CCA} = 1.1 V to 5.5 V	0.7 × V_{CCA}		V_{CCA}	V
		EN	V_{CCA} = 1.1 V to 5.5 V	1.0		V_{CCA}	V
		SCL_CON, SDA_CON,	5V_ SYS = 5.5 V	0.7 × 5V_SYS		5V_SYS	V
		CEC_CON	5V_ SYS = 5.5 V	0.7 ×V_{3P3}		V_{3P3}	
		HPD_CON	5V_ SYS = 5.5 V	2.0		5V_SYS	
V_{IL}	Low-level input voltage	SCL_SYS, SDA_SYS,	V_{CCA} = 1.1 V to 5.5 V	–0.5		0.082 × V_{CCA}	V
		CEC_SYS,	V_{CCA} = 1.1 V to 5.5 V	–0.5		0.082 × V_{CCA}	V
		EN	V_{CCA} = 1.1 V to 5.5 V	–0.5		0.4	V
		SCL_CON, SDA_CON,	5V_ SYS = 5.5 V	–0.5		0.3 × 5V_SYS	V
		CEC_CON	5V_ SYS = 5.5 V	–0.5		0.3 × V_{3P3}	V
		HPD_CON	5V_ SYS = 5.5 V	0		0.8	V
V_{ILC}	(contention) Low-level input voltage	SCL_SYS, SDA_SYS, CEC_SYS	V_{CCA} = 1.1 V to 5.5 V	–0.5		0.0524 × V_{CCA}	V
V_{OL} – V_{ILC}	Delta between VOL and VILC	SCL_SYS, SDA_SYS, CEC_SYS	V_{CCA} = 1.8 V		0.1 × V_{CCA}		mV
T_A	Operating free-air temperature			–40		85	°C

ESD TABLE

over operating free-air temperature range (unless otherwise noted)

PARAMETER	SIGNALS	TYP	UNIT
HBM ESD	SCL_SYS, SDA_SYS, CEC_SYS, HPD_SYS, 5V_SYS, V_{CCA}, EN	±2	kV
IEC 61000-4-2 Contact Discharge	SCL_CON, SDA_CON, CEC_CON, HPD_CON, 5V_CON, UTI_CON	±15	kV
IEC 61000-4-2 Air-gap ESD	SCL_CON, SDA_CON, CEC_CON, HPD_CON, 5V_CON, UTI_CON	±15	kV

ELECTRICAL CHARACTERISTICS

Max values measured across temp and VCCA=1.1V to 5.5V and 5V_SYS=5.5V. Typical values measured at VCCA=1.8V and 5V_SYS=5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current						
I_{CC5V}	Disabled	5V_SYS =5V, 5V_CON =Open EN = GND, HPD_CON=GND		2	10	µA
	Load Switch active	5V_SYS =5V, 5V_CON =Open EN = VCCA, HPD_CON=GND		30	50	µA
	Active	5V_SYS =5V, 5V_CON =Open EN = VCCA, HPD_CON=5V		125	200	µA
Load Switch						
V_{REV}	Reverse voltage comparator trip point	5V_SYS=4V, 5V_CON > 5V_SYS		100		mV
I_{OFF}	Leakage Current	5V_CON=0V, 5V_SYS=5V , EN=GND, HPD_CON=GND Measured at 5V_SYS pin.		1	5	µA
		5V_CON=0V, 5V_SYS=5V , EN=GND, HPD_CON=5V Measured at 5V_SYS pin		1	5	µA
		5V_CON =5V, 5V_SYS =0V , EN=GND, HPD_CON=GND Measured at 5V_CON pin.		1	5	µA
		5V_CON =5V, 5V_SYS =0V EN=GND, HPD_CON=5V Measured at 5V_CON pin.		1	5	µA
		5V_CON =5V, 5V_SYS =0V, EN=VCCA, HPD_CON=GND Measured at 5V_CON pin.		1	5	µA
		5V_CON =5V, 5V_SYS =0V, EN=VCCA, HPD_CON=5V Measured at 5V_CON pin.		1	5	µA
I_{SC}	Short circuit current at 5V_CON	5V_SYS=5V, 5V_CON = GND	110	140	170	mA
$T_{DEGLITCH}$	Deglitch time against false short	5V_SYS=5V , EN=VCCA, Short 5V_CON		3		µs
UVLO	Under voltage lockout rising	5V_SYS=0V to 5V, RL = 100 Ω, CL = 1uF		2.85		V
UVLO_HYS	Under voltage lockout falling hysteresis	5V_SYS=5V to 0V, RL = 100 Ω, CL = 1uF		200		mV
V_{DROP}	5V_OUT output voltage drop	5V_SYS =5V, I5V_OUT = 55 mA		38.5	55	mV
I_{RUSH}	Inrush Current	5V_SYS=5V, RL=100 Ω, Cin=10uF, C=1uF		140		mA
T_{ON}	Turn on Time, EN to 5V_CON	5V_SYS=5V, RL=100 Ω, Cin=10uF, C=1uF		92.3		µs
T_{OFF}	Turn off Time, EN to 5V_CON	5V_SYS=5V, RL=100 Ω, Cin=10uF, C=1uF		5		µs
T_{SHUT}	Thermal Shutdown	Shutdown threshold, TRIP(1)		166		°C
		HYST(2)		23		

(1) The TPD5S116 turns off after the device temperature reaches the TRIP temperature.
(2) Once the thermal shut-down circuit turns off the load switch, the switch turns on again after the device junction temperature cools down to a temperature equals to or less than TRIP-HYST.

Voltage Level Shifter - SCL, SDA Lines

PARAMETER		TEST CONDITIONS		V_{CCA}	–40°C to 85°C			UNIT
					MIN	TYP	MAX	
V_{OH_SYS}		I_{OH} = –10 µA	$V_I = V_{IH}$		0.8 × V_{CCA}		VCCA+0.02	V
V_{OL_SYS}		I_{OL} = 10 µA	$V_I = V_{IL}$				0.17 × V_{CCA}	V
V_{OH_CON}		I_{OH} = –10 µA	$V_I = V_{IH}$		0.8 x 5V_SYS		5V_SYS+0.02	V
V_{OL_CON}		I_{OH} = 3 mA	$V_I = V_{IL}$			0.3	0.4	V
ΔVT Hysteresis at the SDx_IN (VT+ - VT-)						40		mV
ΔVT Hysteresis at the SDx_OUT (VT+ - VT-)						400		mV
R_{PU} (Internal pull-up)		SCL_SYS, SDA_SYS	Pull-up connected to VCCA rail			5		kΩ
		SCL_CON, SDA_CON	Pull-up connected to 5V rail			1.75		
$I_{PULLUPAC}$ Transient Boosted Pull-up Current (rise-time accelerator)		SCL_CON, SDA_CON	Pull-up connected to 5V rail			13		mA
I_{off}	SYS Port	V_{CCA} = 0V, V_I or V_O = 0 to 3.6 V		0 V			±5	µA
	CON Port	5V_CON=0V, V_I or V_O = 0 to 5.5 V		0 V			±5	
I_{OZ}	SYS Port	$V_I = V_{CCI}$ or GND					±5	

Voltage Level Shifter - CEC Line

PARAMETER		TEST CONDITIONS		V_{CCA}	–40°C to 85°C			UNIT
					MIN	TYP	MAX	
V_{OH_SYS}		I_{OH} = –10 µA	$V_I = V_{IH}$		0.8 × V_{CCA}		VCCA+0.02	V
V_{OL_SYS}		I_{OL} = 10 µA	$V_I = V_{IL}$				0.17 × V_{CCA}	V
V_{OH_CON}		I_{OH} = –10 µA	$V_I = V_{IH}$		0.8 x V_{3P3}			V
V_{OL_CON}		I_{OH} = 3 mA	$V_I = V_{IL}$			0.3	0.4	V
ΔVT Hysteresis at the CEC_SYS (VT+ - VT-)						30		mV
ΔVT Hysteresis at the CEC_CON (VT+ - VT-)						283		mV
R_{PU} (Internal pull-up)		CEC_SYS	Pull-up connected to V_{CCA} rail			5		kΩ
		CEC_CON	Pull-up connected to 3.3V rail		22	26	30	kΩ
R_{PD} (Internal pull-down)		CEC_CON	Pull-down connected connector side			10		MΩ
I_{off}	SYS Port	V_{CCA} = 0V, V_I or V_O = 0 to 3.6 V		0 V			±5	µA
	CON Port	5V_CON=0V, V_I or V_O = 0 to 5.5 V		0 V			±1.8	
I_{OZ}	SYS Port	$V_I = V_{CCI}$ or GND					±5	

Voltage Level Shifter - HPD Line

PARAMETER		TEST CONDITIONS		V_{CCA}	–40°C to 85°C			UNIT
					MIN	TYP	MAX	
V_{OH_SYS}		I_{OH} = 1 mA	$V_I = V_{IH}$	1.2 V to 5.0 V	V_{CCA} × 0.7			V
$V_{OH\_SYS\_1P1}$		I_{OH} = 100 µA	$V_I = V_{IH}$	1.1V	V_{CCA} × 0.7			V
V_{OL_SYS}		I_{OL} = 3 µA	$V_I = V_{IL}$	1.2 V to 5.0 V			0.4	V
$V_{OL\_SYS\_1P1}$		I_{OL} = 3 mA	$V_I = V_{IL}$	1.1 V			0.68	V
ΔVT Hysteresis at the CEC_CON (VT+ - VT-)				1.2 V to 5.0 V		500		mV
R_{PD_IN} (Input internal pull-down resistor)			Pull-down connected to GND		60	100	140	kΩ
R_{PD_OUT} (Output internal pull-down resistor)			Pull-down connected to GND		60	100	140	kΩ
TFILT	Glitch Filter Duration	HPD_CON = 5 V, EN = V_{CCA}, Short HPD_SYS				10		µs

EN

PARAMETER	TEST CONDITIONS	V_{CCA}	–40°C to 85°C			UNIT
			MIN	TYP	MAX	
$R_{PD\ EN}$ (Internal pull-down resistor)	Pull-down connected to GND	1.8 V		470		kΩ

UTILITY PIN

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage				6	V
V_{CLAMP}	Clamp voltage with ESD strike	IPP = 1 A, tp = 8/20 µSec, from I/O to GND(1)		8		V
		IPP = 5 A, tp = 8/20 µSec, , from I/O to GND(1)		10		
R_{DYN}	Dynamic resistance	UTI pin to GND Pin(2)		033		Ω
C_{UTI}	Line capacitance	V_{IO}=0V, f=1GHz, I/O to GND		5.5		pF
V_{BR}	Break-down voltage	I_{IO} = 1mA	7			V
I_{LEAK}	Leakage current	V_{IO} = 3V		1	10	nA

(1) Non-repetitive current pulse 8/20us exponentially decaying waveform according to IEC61000-4-5
(2) Extraction of RDYN using least squares fit of TLP characteristics between I=10A and I=20A

I/O Capacitances

PARAMETER		TEST CONDITONS	SUPPLY & EN SIGNAL	–40°C to 85°C			UNIT
				MIN	TYP	MAX	
C_I	EN	V_{BIAS} = VCCA/2, f =1MHz, 30mV p-p ac signal			8	9	pF
C_I	HPD_CON	V_{BIAS} = 0V- 5V, f =1MHz, 30mV p-p ac signal			7	7.5	pF
C_{IO}	SYS port	V_{BIAS} = 1.8 V, f =1MHz, 30mV p-p ac signal			6.5	9.5	pF
	CON port	V_{BIAS} = 2.5 V, f =1MHz, 30mV p-p ac signal			15	20	pF
	SCL_CON, SDA_CON	V_{BIAS} = 2.5V, f =100KHz, 3.5V p-p ac signal	V_{CCA}= 3.6 V, 5V_SYS =5V, EN=HPD_CON=0 V		17		pF
	CEC_CON	V_{BIAS} = 1.65 V, f =100KHz, 2.5V p-p ac signal	V_{CCA}= 3.6 V, 5V_SYS =5V, EN=HPD_CON=0 V		13		pF
	CEC_CON	V_{BIAS} = 1.65 V, f =100KHz, 2.5V p-p ac signal	V_{CCA}= 0V 5V_SYS =0V EN=HPD_CON=0 V		12		pF

Dynamic Load Characteristics

Propagation delays measured from 50% threshold to 50% threshold

Rise time measured from 30% to 70% threshold

Fall time measured from 70% to 30% threshold

PARAMETER	DESCRIPTION	TEST CONDITION	MIN	TYP	Max	UNIT
CL	Bus Load Capacitance (Connector Side)				750	pF
	Bus Load Capacitance (System Side)				30	

Dynamic Characteristics - SCL, SDA Lines

5V_CON=5V; VCCA = 1.2V

PARAMETER	DESCRIPTION	PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	SYS to CON	DDC Channels Enabled		316		ns
		CON to SYS	DDC Channels Enabled		286		ns
T_{PLH}	Propagation Delay	SYS to CON	DDC Channels Enabled		489		ns
		CON to SYS	DDC Channels Enabled		199		ns
T_{FALL}	SYS Port Fall Time	SYS Port	DDC Channels Enabled		110		ns
T_{FALL}	CON Port Fall Time	CON Port	DDC Channels Enabled		82		ns
T_{RISE}	SYS Port Rise Time	SYS Port	DDC Channels Enabled		229		ns
T_{RISE}	CON Port Rise Time	CON Port	DDC Channels Enabled		86		ns
F_{MAX}	Maximum Switching Frequency		DDC Channels Enabled	400			kHz

Dynamic Characteristics - CEC Lines

5V_CON=5V; VCCA = 1.2V

PARAMETER	DESCRIPTION	PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	SYS to CON	CEC Channels Enabled		436		ns
		CON to SYS	CEC Channels Enabled		97		ns
T_{PLH}	Propagation Delay	SYS to CON	CEC Channels Enabled		13.8		µs
		CON to SYS	CEC Channels Enabled		319		ns
T_{FALL}	SYS Port Fall Time	SYS Port	CEC Channels Enabled		37		ns
T_{FALL}	CON Port Fall Time	CON Port	CEC Channels Enabled		114		ns
T_{RISE}	SYS Port Rise Time	SYS Port	CEC Channels Enabled		234		ns
T_{RISE}	CON Port Rise Time	CON Port	CEC Channels Enabled		16.6		µs

Dynamic Characteristics - HPD Lines

5V_CON=5V; VCCA = 1.2V

PARAMETER	DESCRIPTION	PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	CON to SYS	CEC Channels Enabled		10.1		µs
T_{PLH}	Propagation Delay	CON to SYS	CEC Channels Enabled		9.7		µs
T_{FALL}	SYS Port Fall Time	SYS Port	CEC Channels Enabled		14		ns
T_{RISE}	SYS Port Rise Time	SYS Port	CEC Channels Enabled		18		ns

Dynamic Characteristics - SCL, SDA Lines

5V_CON=5V; VCCA = 1.5V

PARAMETER	DESCRIPTION	PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	A to B	DDC Channels Enabled		297		ns
		B to A	DDC Channels Enabled		224		ns
T_{PLH}	Propagation Delay	A to B	DDC Channels Enabled		473		ns
		B to A	DDC Channels Enabled		193		ns
T_{FALL}	A Port Fall Time	A-Port	DDC Channels Enabled		87		ns
T_{FALL}	B Port Fall Time	B-Port	DDC Channels Enabled		82		ns
T_{RISE}	A Port Rise Time	A-Port	DDC Channels Enabled		226		ns
T_{RISE}	B Port Rise Time	B-Port	DDC Channels Enabled		86		ns
F_{MAX}	Maximum Switching Frequency		DDC Channels Enabled	400			kHz

Dynamic Characteristics - CEC Lines

5V_CON=5V; VCCA = 1.5V

PARAMETER	DESCRIPTION	PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	A to B	CEC Channels Enabled		419		ns
		B to A	CEC Channels Enabled		102		ns
T_{PLH}	Propagation Delay	A to B	CEC Channels Enabled		13.7		µs
		B to A	CEC Channels Enabled		314		ns
T_{FALL}	A Port Fall Time	A-Port	CEC Channels Enabled		39		ns
T_{FALL}	B Port Fall Time	B-Port	CEC Channels Enabled		115		ns
T_{RISE}	A Port Rise Time	A-Port	CEC Channels Enabled		230		ns
T_{RISE}	B Port Rise Time	B-Port	CEC Channels Enabled		16.6		µs

Dynamic Characteristics - HPD Lines

5V_CON=5V; VCCA = 1.5V

PARAMETER	DESCRIPTION	PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	B to A	CEC Channels Enabled		10.1		µs
T_{PLH}	Propagation Delay	B to A	CEC Channels Enabled		9.7		µs
T_{FALL}	A Port Fall Time	A-Port	CEC Channels Enabled		8		ns
T_{RISE}	A Port Rise Time	A-Port	CEC Channels Enabled		9.5		ns

Dynamic Characteristics - SCL, SDA Lines

5V_CON=5V; VCCA = 1.8V

PARAMETER	DESCRIPTION	PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	A to B	DDC Channels Enabled		292		ns
		B to A	DDC Channels Enabled		192		ns
T_{PLH}	Propagation Delay	A to B	DDC Channels Enabled		466		ns
		B to A	DDC Channels Enabled		190		ns
T_{FALL}	A Port Fall Time	A-Port	DDC Channels Enabled		75		ns
T_{FALL}	B Port Fall Time	B-Port	DDC Channels Enabled		82		ns
T_{RISE}	A Port Rise Time	A-Port	DDC Channels Enabled		224		ns
T_{RISE}	B Port Rise Time	B-Port	DDC Channels Enabled		86		ns
F_{MAX}	Maximum Switching Frequency		DDC Channels Enabled	400			kHz

Dynamic Characteristics - CEC Lines

5V_CON=5V; VCCA = 1.8V

PARAMETER	DESCRIPTION	PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	A to B	CEC Channels Enabled		417		ns
		B to A	CEC Channels Enabled		108		ns
T_{PLH}	Propagation Delay	A to B	CEC Channels Enabled		13.7		µs
		B to A	CEC Channels Enabled		312		ns
T_{FALL}	A Port Fall Time	A-Port	CEC Channels Enabled		41		ns
T_{FALL}	B Port Fall Time	B-Port	CEC Channels Enabled		114		ns
T_{RISE}	A Port Rise Time	A-Port	CEC Channels Enabled		228		ns
T_{RISE}	B Port Rise Time	B-Port	CEC Channels Enabled		16.6		µs

Dynamic Characteristics - HPD Lines

5V_CON=5V; VCCA = 1.8V

PARAMETER	DESCRIPTION	PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	B to A	CEC Channels Enabled		10.1		µs
T_{PLH}	Propagation Delay	B to A	CEC Channels Enabled		9.7		µs
T_{FALL}	A Port Fall Time	A-Port	CEC Channels Enabled		5.5		ns
T_{RISE}	A Port Rise Time	A-Port	CEC Channels Enabled		7		ns

Dynamic Characteristics - SCL, SDA Lines

5V_CON=5V; VCCA = 2.5V

PARAMETER	DESCRIPTION	PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	A to B	DDC Channels Enabled		291		ns
		B to A	DDC Channels Enabled		154		ns
T_{PLH}	Propagation Delay	A to B	DDC Channels Enabled		455		ns
		B to A	DDC Channels Enabled		186		ns
T_{FALL}	A Port Fall Time	A-Port	DDC Channels Enabled		64		ns
T_{FALL}	B Port Fall Time	B-Port	DDC Channels Enabled		82		ns
T_{RISE}	A Port Rise Time	A-Port	DDC Channels Enabled		221		ns
T_{RISE}	B Port Rise Time	B-Port	DDC Channels Enabled		86		ns
F_{MAX}	Maximum Switching Frequency		DDC Channels Enabled	400			kHz

Dynamic Characteristics - CEC Lines

5V_CON=5V; VCCA = 2.5V

PARAMETER	DESCRIPTION	PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	A to B	CEC Channels Enabled		421		ns
		B to A	CEC Channels Enabled		122		ns
T_{PLH}	Propagation Delay	A to B	CEC Channels Enabled		13.7		µs
		B to A	CEC Channels Enabled		311		ns
T_{FALL}	A Port Fall Time	A-Port	CEC Channels Enabled		49		ns
T_{FALL}	B Port Fall Time	B-Port	CEC Channels Enabled		114		ns
T_{RISE}	A Port Rise Time	A-Port	CEC Channels Enabled		225		ns
T_{RISE}	B Port Rise Time	B-Port	CEC Channels Enabled		16.6		µs

Dynamic Characteristics - HPD Lines

5V_CON=5V; VCCA = 2.5V

PARAMETER	DESCRIPTION	PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	B to A	CEC Channels Enabled		10.1		µs
T_{PLH}	Propagation Delay	B to A	CEC Channels Enabled		9.7		µs
T_{FALL}	A Port Fall Time	A-Port	CEC Channels Enabled		4		ns
T_{RISE}	A Port Rise Time	A-Port	CEC Channels Enabled		5		ns

Dynamic Characteristics - SCL, SDA Lines

5V_CON=5V; VCCA = 3.3V

PARAMETER	DESCRIPTION	PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	A to B	DDC Channels Enabled		292		ns
		B to A	DDC Channels Enabled		133		ns
T_{PLH}	Propagation Delay	A to B	DDC Channels Enabled		449		ns
		B to A	DDC Channels Enabled		184		ns
T_{FALL}	A Port Fall Time	A-Port	DDC Channels Enabled		57		ns
T_{FALL}	B Port Fall Time	B-Port	DDC Channels Enabled		82		ns
T_{RISE}	A Port Rise Time	A-Port	DDC Channels Enabled		218		ns
T_{RISE}	B Port Rise Time	B-Port	DDC Channels Enabled		86		ns
F_{MAX}	Maximum Switching Frequency		DDC Channels Enabled	400			kHz

Dynamic Characteristics - CEC Lines

5V_CON=5V; VCCA = 3.3V

PARAMETER	DESCRIPTION	PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	A to B	CEC Channels Enabled		428		ns
		B to A	CEC Channels Enabled		138		ns
T_{PLH}	Propagation Delay	A to B	CEC Channels Enabled		13.7		µs
		B to A	CEC Channels Enabled		309		ns
T_{FALL}	A Port Fall Time	A-Port	CEC Channels Enabled		59		ns
T_{FALL}	B Port Fall Time	B-Port	CEC Channels Enabled		114		ns
T_{RISE}	A Port Rise Time	A-Port	CEC Channels Enabled		223		ns
T_{RISE}	B Port Rise Time	B-Port	CEC Channels Enabled		16.6		µs

Dynamic Characteristics - HPD Lines

5V_CON=5V; VCCA = 3.3V

PARAMETER	DESCRIPTION	PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	B to A	CEC Channels Enabled		10.1		µs
T_{PLH}	Propagation Delay	B to A	CEC Channels Enabled		9.7		µs
T_{FALL}	A Port Fall Time	A-Port	CEC Channels Enabled		3		ns
T_{RISE}	A Port Rise Time	A-Port	CEC Channels Enabled		3.5		ns

Dynamic Characteristics - SCL, SDA Lines

5V_CON=5V; VCCA = 5V

PARAMETER	DESCRIPTION	PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	A to B	DDC Channels Enabled		298		ns
		B to A	DDC Channels Enabled		113		ns
T_{PLH}	Propagation Delay	A to B	DDC Channels Enabled		442		ns
		B to A	DDC Channels Enabled		182		ns
T_{FALL}	A Port Fall Time	A-Port	DDC Channels Enabled		52		ns
T_{FALL}	B Port Fall Time	B-Port	DDC Channels Enabled		82		ns
T_{RISE}	A Port Rise Time	A-Port	DDC Channels Enabled		217		ns
T_{RISE}	B Port Rise Time	B-Port	DDC Channels Enabled		86		ns
F_{MAX}	Maximum Switching Frequency		DDC Channels Enabled	400			kHz

Dynamic Characteristics - CEC Lines

5V_CON=5V; VCCA = 5V

PARAMETER	DESCRIPTION	PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	A to B	CEC Channels Enabled		446		ns
		B to A	CEC Channels Enabled		169		ns
T_{PLH}	Propagation Delay	A to B	CEC Channels Enabled		13.7		µs
		B to A	CEC Channels Enabled		306		ns
T_{FALL}	A Port Fall Time	A-Port	CEC Channels Enabled		82		ns
T_{FALL}	B Port Fall Time	B-Port	CEC Channels Enabled		114		ns
T_{RISE}	A Port Rise Time	A-Port	CEC Channels Enabled		221		ns
T_{RISE}	B Port Rise Time	B-Port	CEC Channels Enabled		16.6		µs

Dynamic Characteristics - HPD Lines

5V_CON=5V; VCCA = 5V

PARAMETER	DESCRIPTION	PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	B to A	CEC Channels Enabled		10.1		µs
T_{PLH}	Propagation Delay	B to A	CEC Channels Enabled		9.7		µs
T_{FALL}	A Port Fall Time	A-Port	CEC Channels Enabled		2.5		ns
T_{RISE}	A Port Rise Time	A-Port	CEC Channels Enabled		2.5		ns

TYPICAL CHARACTERISTICS

Conditions TBD

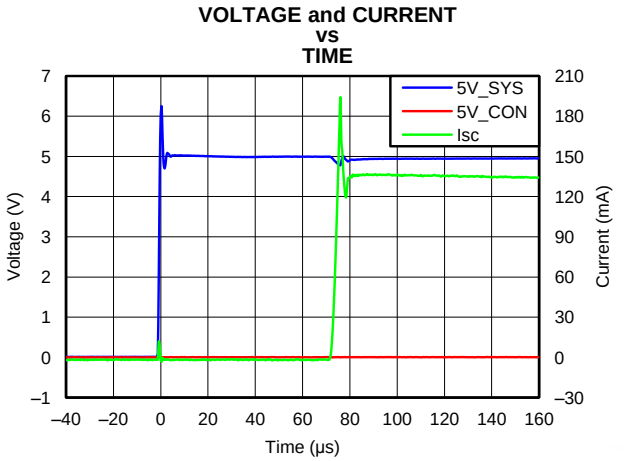


Figure 3. Powerup to Short Circuit

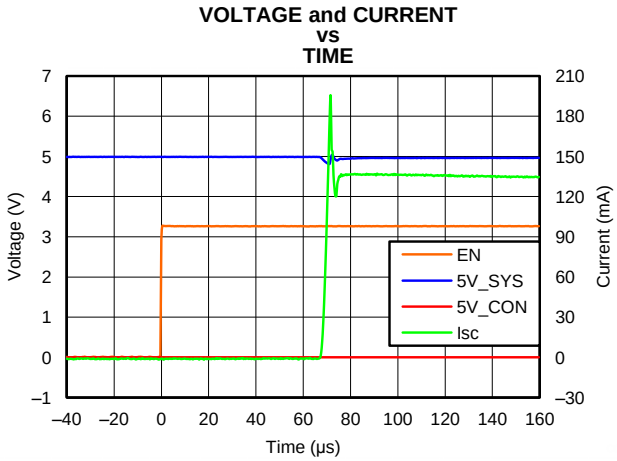


Figure 4. Enable to Short Circuit

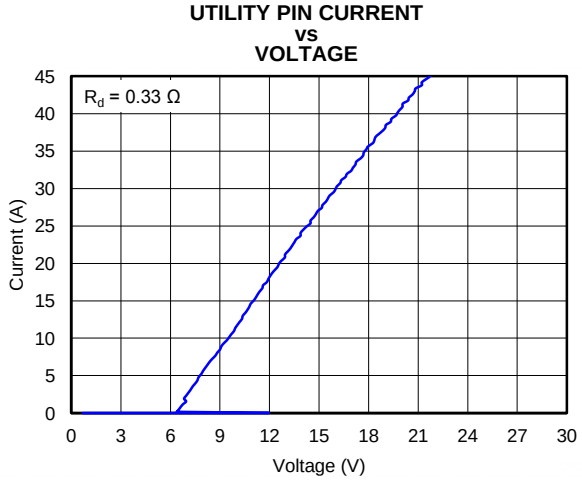


Figure 5. TLP Curve

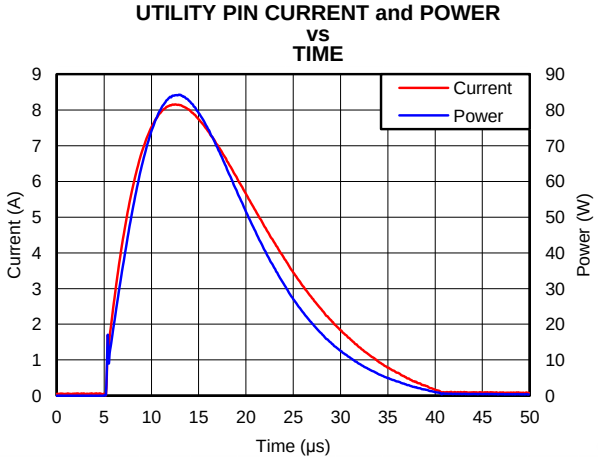


Figure 6. Surge Curves

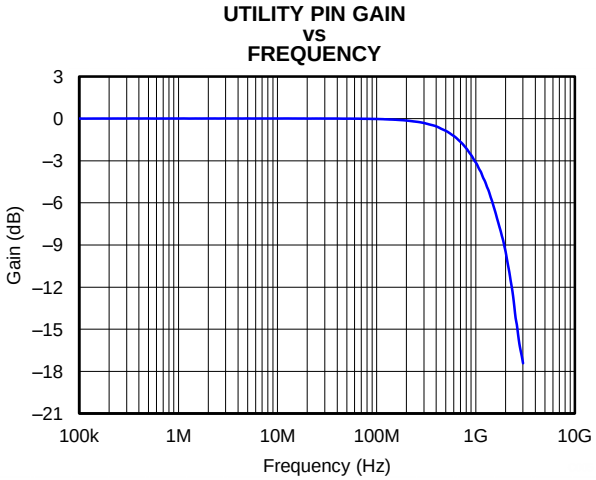


Figure 7. Insertion Loss Waveform Data

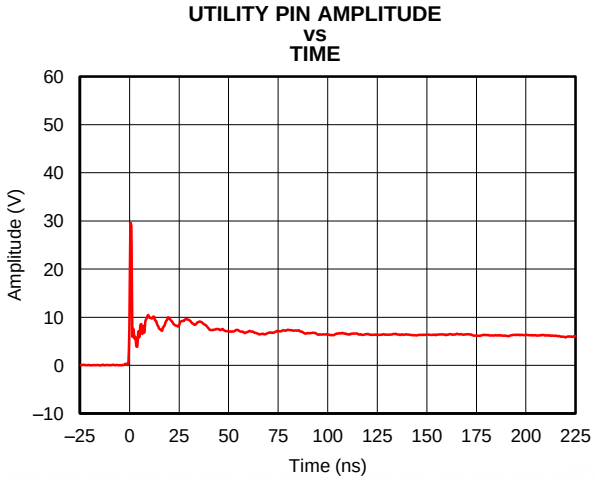


Figure 8. Keytek, +8kV IEC Voltage Clamp Waveform

TYPICAL CHARACTERISTICS (continued)

Conditions TBD

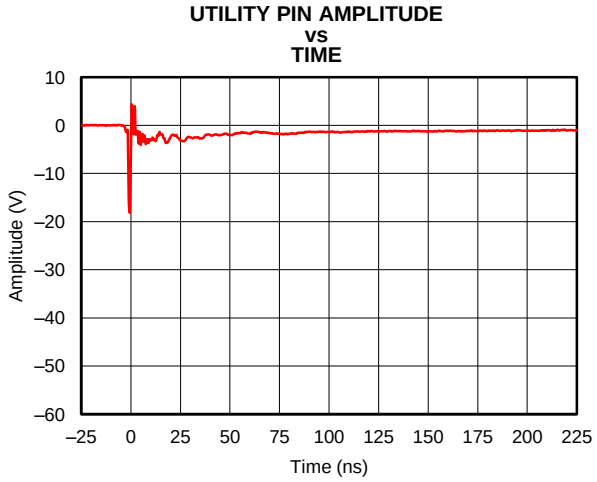


Figure 9. Keytek, -8kV IEC Voltage Clamp Waveform

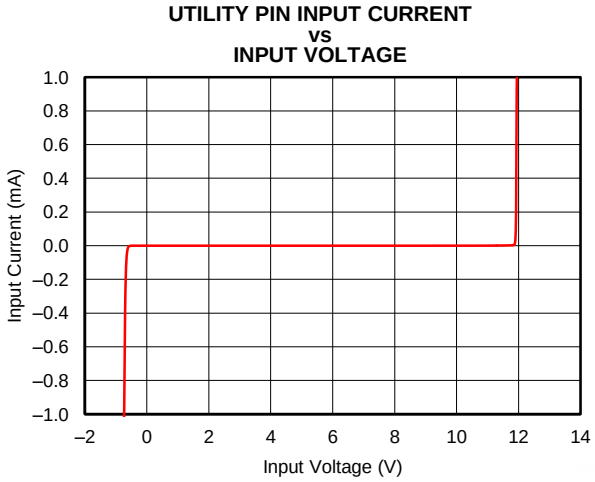


Figure 10. DC Curve Data

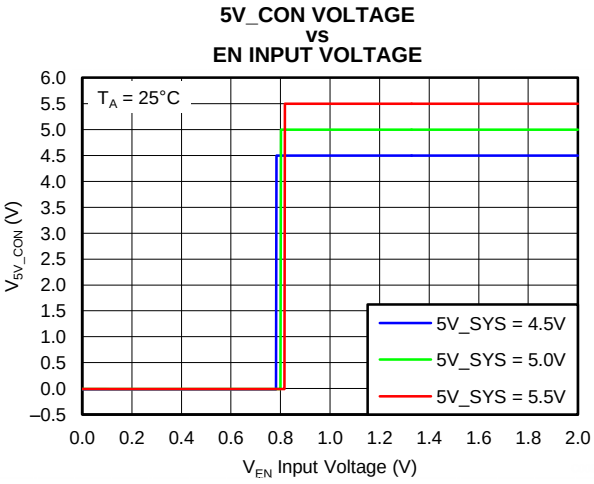


Figure 11. EN V_{TH}

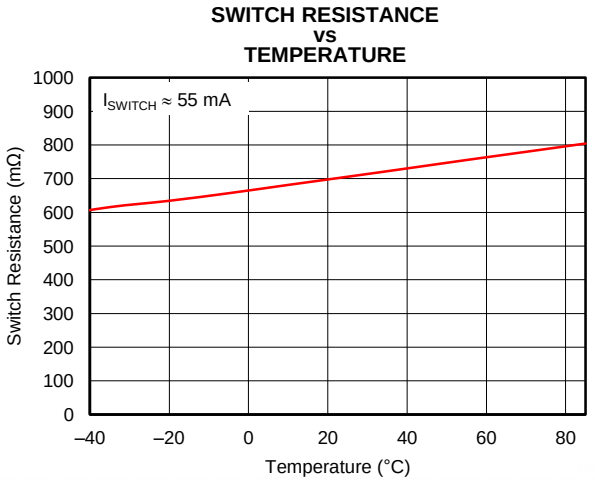


Figure 12. Rds Data

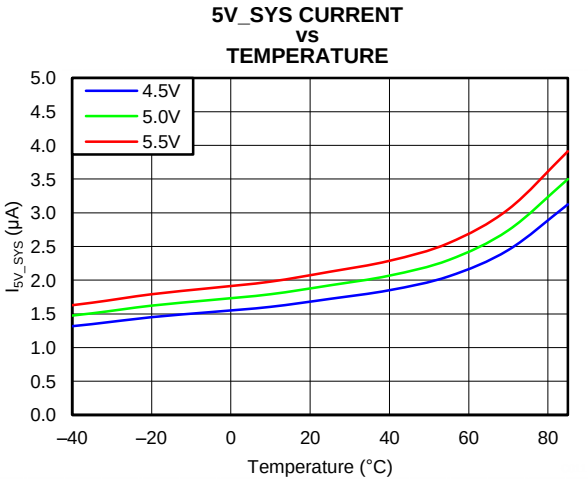


Figure 13. I_{5V_SYS} Data

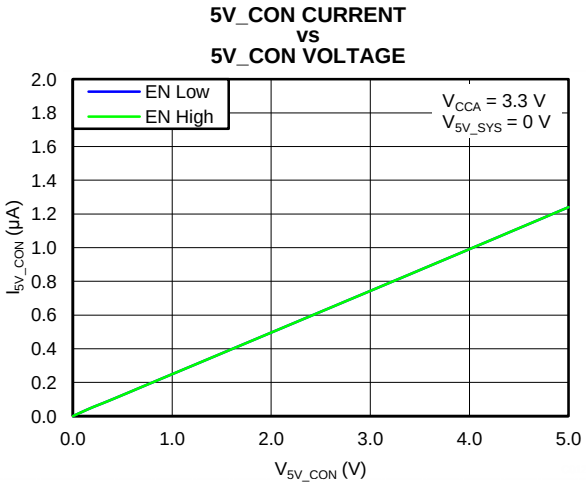


Figure 14. Reverse Switch Current Data

TYPICAL CHARACTERISTICS (continued)

Conditions TBD

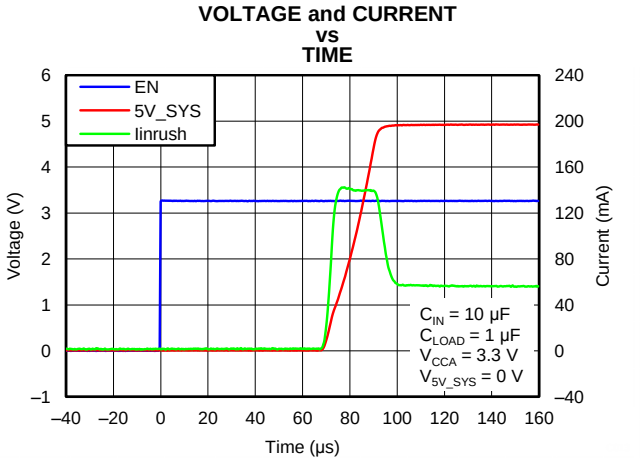


Figure 15. I_{INRUSH} Waveform Data

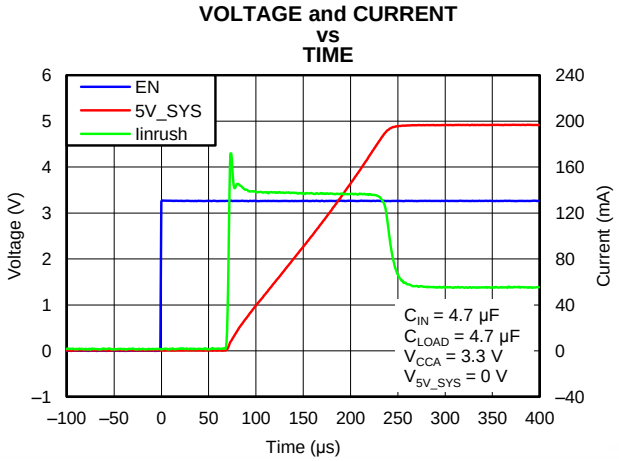


Figure 16. I_{INRUSH} Waveform Data

APPLICATION INFORMATION

DDC/CEC LEVEL SHIFT Circuit Operation

The TPD5S116 enables DDC translation from VCCA (system side) voltage levels to 5V_CON (HDMI connector side) voltage levels without degradation of system performance. The TPD5S116 contains 2 bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage, system side DDC-bus and the 5V connector side DDC-bus. The connector port I/Os are over-voltage tolerant to 5.5 V even when the device is un-powered. After power-up and with enable pin and HPD_CON pin HIGH, a LOW level on system port (below approximately VILC = 0.08 × VCCA V) turns the corresponding connector port driver (either SDA or SCL) on and drives it down to V_{OL_CON} V. When system port rises above approximately 0.10 × VCCA V, the connector port pull-down driver is turned off and the internal pull-up resistor pulls the pin HIGH. When connector port falls first and goes below 0.3 × 5V_CON, a CMOS hysteresis input buffer detects the falling edge, turns on the system port driver, and pulls it down to approximately V_{OLA} V. The connector port pull-down is not enabled unless the system port voltage goes below VILC, in which case the connector port pull-down driver is enabled until system port rises above (V_{ILC} + $\Delta V_{T\text{-}HYSTA}$). If the connector port is not externally driven LOW, its voltage will continue to rise due to the internal pull-up resistor.

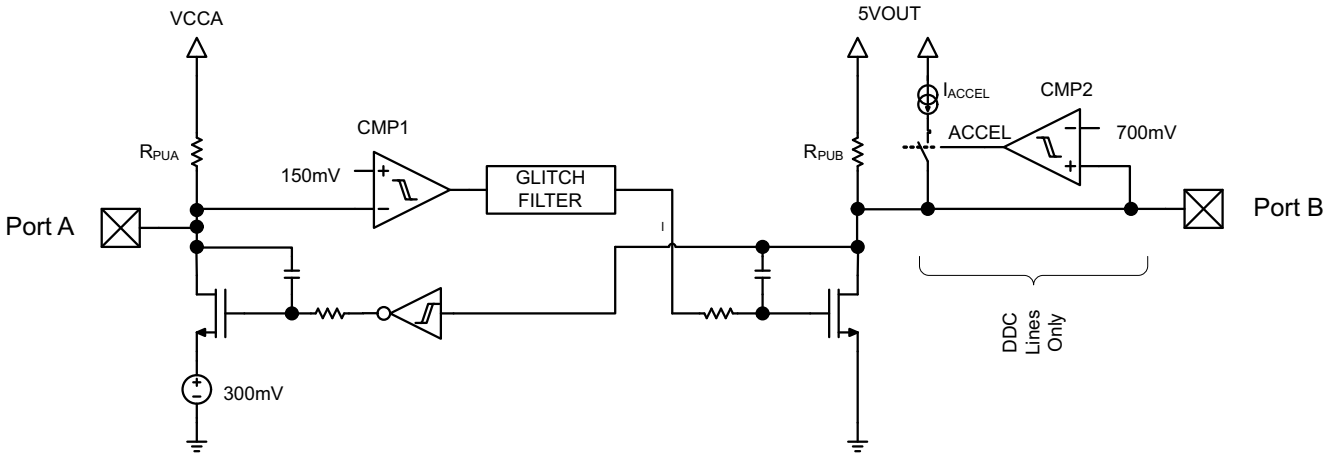


Figure 17. DDC/CEC Level Shifter Block Diagram

DDC/CEC Level Shifter Operational Notes for VCCA=1.8V

- The threshold of CMP1 is ~150mV +/- the 40mV of total hysteresis.
- The comparator will trip for a falling waveform at ~130mV
- The comparator will trip for a rising waveform at ~170mV
- To be recognized as a zero, the level at system port must first go below 130mV (V_{ILC} in spec) and then stay below 170mV (V_{IL_SYS} in spec)
- To be recognized as a one, the level at system port must first go above 170mV and then stay above 130mV
- V_{ILC} is set to 110mV in Electrical Characteristics Table to give some margin to the 130mV
- V_{IL_SYS} is set to 140mV in the Electrical Characteristics Table to give some margin to the 170mV
- V_{IH_SYS} is set to 70% of VCCA to be consistent with standard CMOS levels

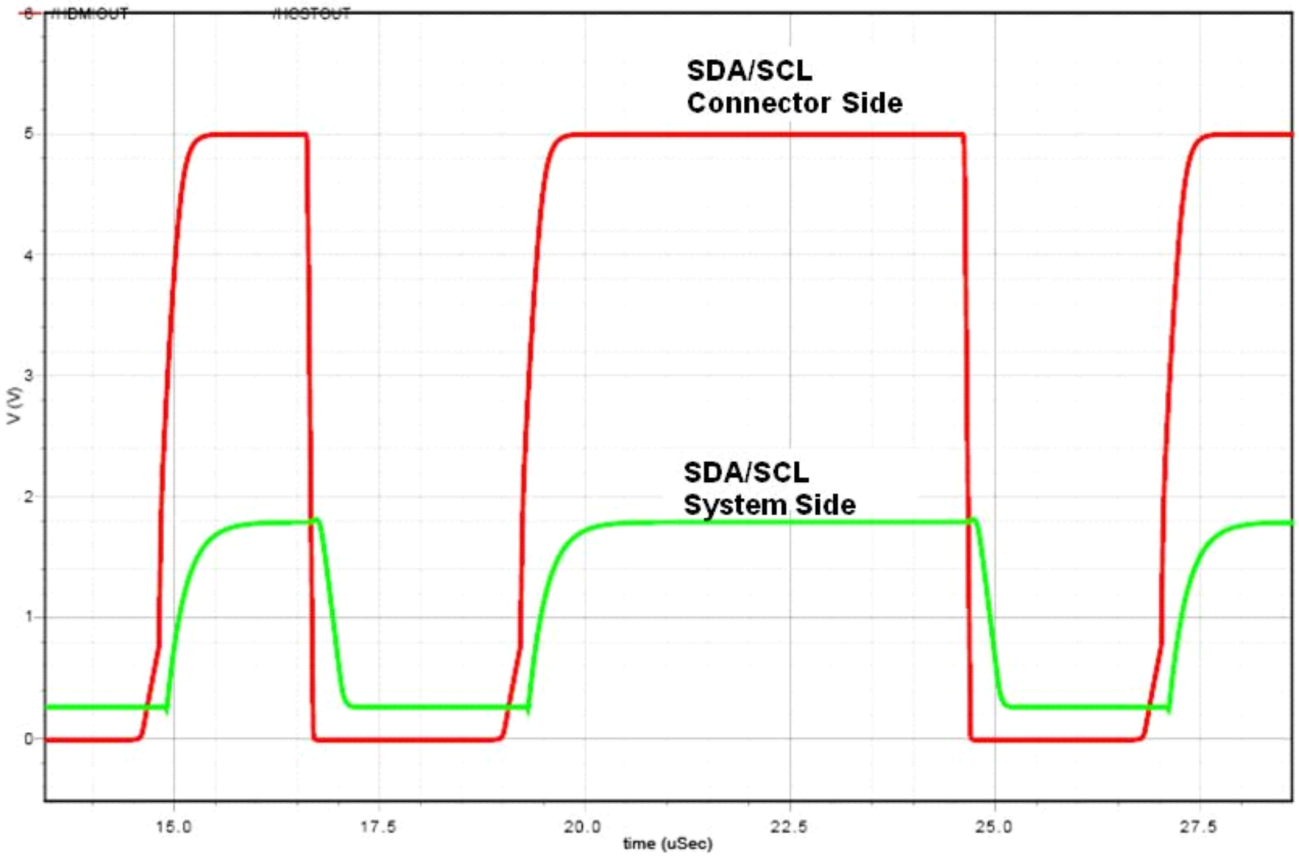


Figure 18. DDC Level Shifter Operation (Connector to System Direction)

Rise-Time Accelerators

The HDMI cable side of the DDC lines incorporates rise-time accelerators to support the high capacitive load on the HDMI cable side. The rise time accelerator boosts the cable side DDC signal independent of which side of the bus is releasing the signal.

Normal HDMI Transmit and Recieve Sequence

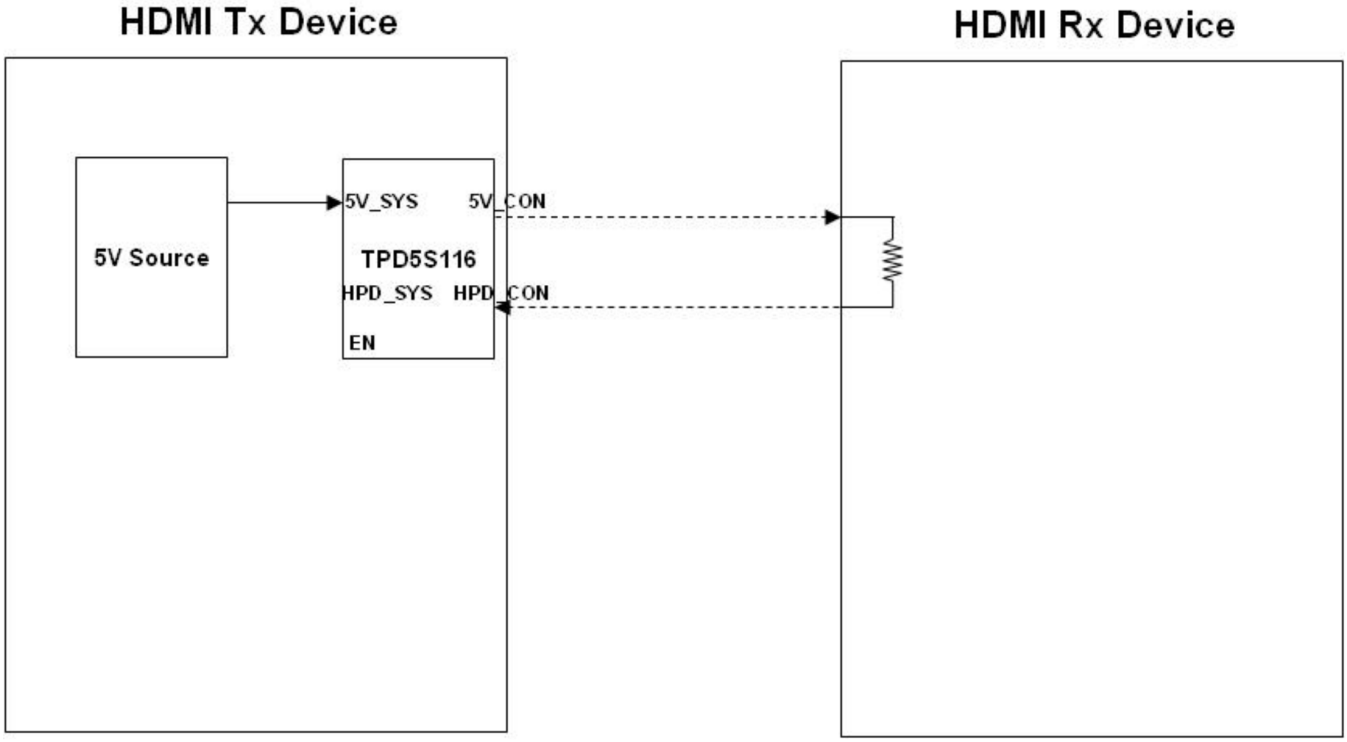


Figure 19. Tx Device Connecting with Rx Device

Hot Plug Detect

Once TPD5S116 is enabled and the system's 5V source is on, TPD5S116 is ready for continual HDMI receiver detection. When a HDMI cable connects receiving and transmitting device together, the 5V on the load switch (5V_CON) flows through the receiving device's internal resistor and into HPD's input (HPD_CON). The HPD buffer's output then goes high, indicating to the transmitter that a receiving device is connected. To save power, periodic detection can be done by turning on and off the TPD5S116 before a receiving device is connected.

Noise Considerations: Ground offset between the TPD5S116 ground and the ground of devices on system port of the TPD5S116 must be avoided. The reason for this cautionary remark is that a CMOS/NMOS open-drain capable of sinking 3 mA of current at 0.4 V will have an output resistance of 133Ω or less (R = E / I). Such a driver will share enough current with the system port output pull-down of the TPD5S116 to be seen as a LOW as long as the ground offset is zero. If the ground offset is greater than 0 V, then the driver resistance must be less. Since V_{ILC} can be as low as 90 mV at cold temperatures and the low end of the current distribution, the maximum ground offset should not exceed 50 mV. Bus repeaters that use an output offset are not interoperable with the system port of the TPD5S116 as their output LOW levels will not be recognized by the TPD5S116 as a LOW. If the TPD5S116 is placed in an application where the V_{IL_SYS} does not go below V_{ILC}, it will pull connector port LOW initially when system port input transitions LOW but the connector port will return HIGH, so it will not reproduce the system port input on connector port. Such applications should be avoided. Connector port is interoperable with all I2C-bus slaves, masters and repeaters.

Resistor Pull-Up Value Selection

The system is designed to work properly with no external pull-up resistors on the DDC, CEC, and HPD lines.

INPUT CAPACITOR (OPTIONAL)

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between 5V_SYS and GND. A 10-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of CIN can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

OUTPUT CAPACITOR (OPTIONAL)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_{LOAD} is highly recommended. A C_{LOAD} greater than C_{IN} can cause 5V_CON to exceed 5V_SYS when the system supply is removed. A C_{IN} to C_{LOAD} ratio of 10 to 1 is recommended for minimizing 5V_SYS dip caused by inrush currents during startup.

HDMI Compliance

The TPD5S116 is designed to be fully compliant to HDMI 7-13 capacitance specification. Both power on and power off capacitance measurements are done on the CEC, SDA, and SCL connector side pins using a Hioki 3522-50 meter. In power on setup, connect TPD5S116's EN and HPD_CON pins low and 5V_SYS and VCCA pins high. Use the Hioki meter to measure the test fixture with and without the TPD5S116 and subtract to obtain capacitance. In power off setup, connect TPD5S116's EN, HPD_CON, 5V_SYS, and VCCA pins low and conduct same test with the Hioki meter. Read the Cp result from the Hioki meter.

- SCL_CON, SDA_CON Test
  - Measure large signal capacitance at SCL_CON & SDA_CON pins either power-up or power down conditions:
    - VBIAS = 2.5 V
    - f = 100KHz
    - 3.5V p-p ac signal
- CEC Test
  - Measure large signal capacitance of the CEC_CON pin at both power-up and power down conditions:
    - VBIAS = 1.65 V,
    - f = 100KHz
    - 2.5V p-p ac signal

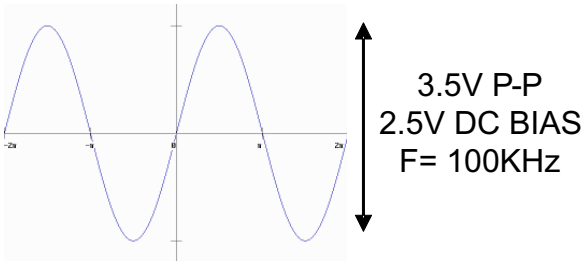


Figure 20. Hioki Meter Signal Set-up for SCL, SDA Cap Measurement

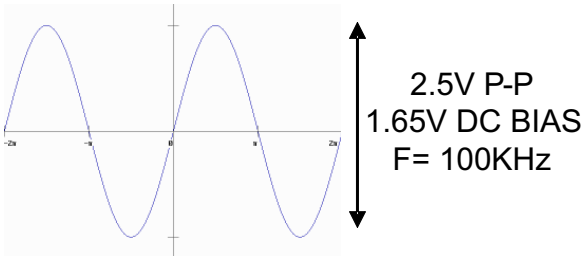


Figure 21. Hioki Meter Signal Set-up for CEC Cap Measurement

REVISION HISTORY

Changes from Original (December 2012) to Revision A	Page
• Changed the YFF package dimensions	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPD5S116YFFR	ACTIVE	DSBGA	YFF	15	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	RE116	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

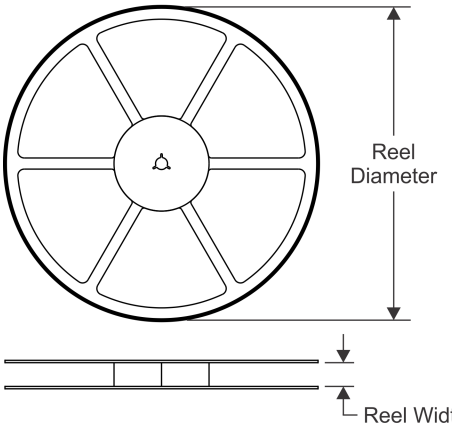
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

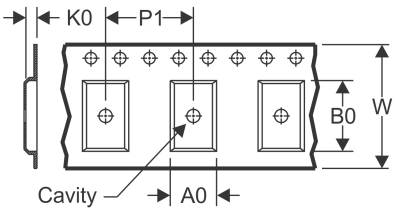
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

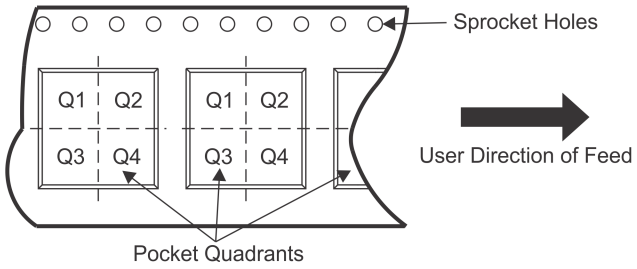


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

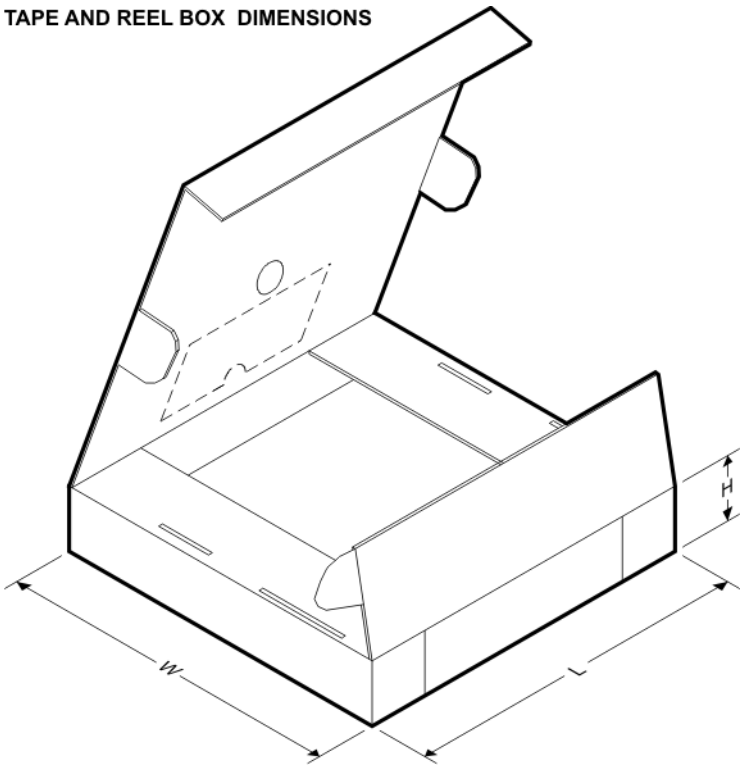
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD5S116YFFR	DSBGA	YFF	15	3000	180.0	8.4	1.46	2.28	0.71	4.0	8.0	Q1

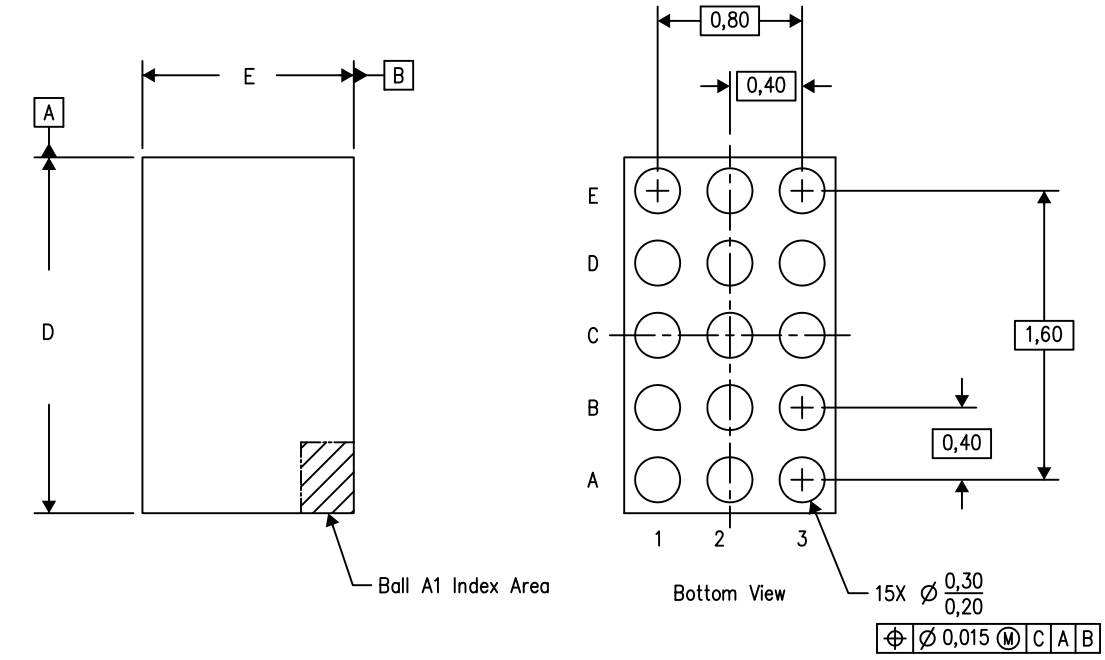
TAPE AND REEL BOX DIMENSIONS

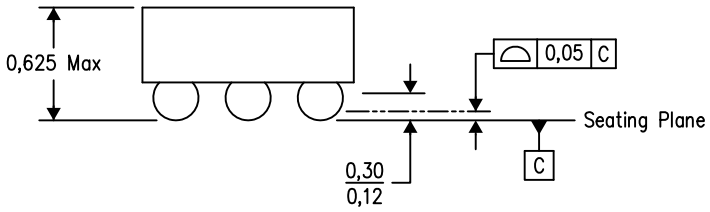


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD5S116YFFR	DSBGA	YFF	15	3000	182.0	182.0	17.0

YFF (R–XBGA–N15) DIE–SIZE BALL GRID ARRAY





D: Max = 2.164 mm, Min =2.104 mm

E: Max = 1.364 mm, Min =1.304 mm

4207625–30/AL 05/13

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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