ULTRA-SMALL, LOW-INPUT-VOLTAGE, LOW r_{ON} LOAD SWITCH

Check for Samples: TPS22924C

FEATURES

- **Integrated Single Load Switch**
- **Input Voltage: 0.75 V to 3.6 V**
- **Ultra-Low ON Resistance**
  - **r_{ON} = 18.3 mΩ at V_{IN} = 3.6 V**
  - **r_{ON} = 18.5 mΩ at V_{IN} = 2.5 V**
  - **r_{ON} = 19.6 mΩ at V_{IN} = 1.8 V**
  - **r_{ON} = 19.4 mΩ at V_{IN} = 1.2 V**
  - **r_{ON} = 20.3 mΩ at V_{IN} = 1.0 V**
  - **r_{ON} = 22.7 mΩ at V_{IN} = 0.75 V**
- **Ultra Small CSP-6 package 0.9 mm x 1.4 mm, 0.5-mm Pitch**
- **2-A Maximum Continuous Switch Current**
- **Low Shutdown Current**
- **Low Threshold Control Input**
- **Controlled Slew Rate to Avoid Inrush Currents**
- **Quick Output Discharge Transistor**
- **ESD Performance Tested Per JESD 22**
  - **5000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

APPLICATIONS

- **Battery Powered Equipment**
- **Portable Industrial Equipment**
- **Portable Medical Equipment**
- **Portable Media Players**
- **Point Of Sales Terminal**
- **GPS Devices**
- **Digital Cameras**
- **Netbooks / Notebooks**
- **Smartphones**

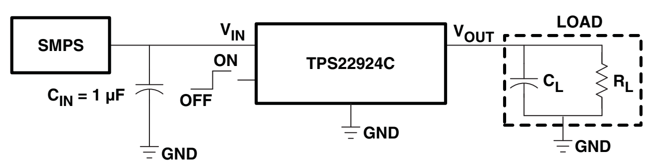
DESCRIPTION

The TPS22924C is a small, ultra-low r_{ON} load switch with controlled turn on. The devices contain N-channel MOSFETs that can operate over an input voltage range of 0.75 V to 3.6 V. An integrated charge pump biases the NMOS switch to achieve a minimum switch ON resistance. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals.

A 1250-Ω on-chip load resistor is added for output quick discharge when switch is turned off. The rise time of the device is internally controlled to avoid inrush current. The TPS22924C features a rise time of 800 µs at 3.6 V.

The TPS22924C is available in an ultra-small space-saving 6-pin CSP package and is characterized for operation over the free-air temperature range of –40ºC to 85ºC.

Figure 1. TYPICAL APPLICATION



NOTE: SMPS = Switched-mode power supply

Table 1. FEATURE LIST

	r_{ON} (TYP) AT 3.6 V	SLEW RATE (TYP) AT 3.6 V	QUICK OUTPUT DISCHARGE(1)	MAXIMUM OUTPUT CURRENT	ENABLE
TPS22924C	18.3 mΩ	800 µs	Yes	2 A	Active high

(1) This feature discharges the output of the switch to ground through a 1250-Ω resistor, preventing the output from floating. See the *Output Pulldown* section in Application Information.

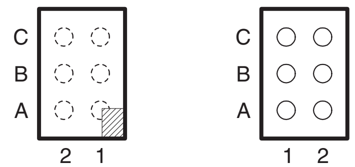
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION (1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
–40°C to 85°C	DSBGA – YZP (0.5-mm pitch)	Reel	TPS22924CYZPR (without back side coating)	_ _ _ 5L _
–40°C to 85°C	DSBGA – YZP (0.5-mm pitch)	Reel	TPS22924CYZPRB (with back side coating)	_ _ _ 5L _

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

YZP PACKAGE



Laser Marking View **Bump View**

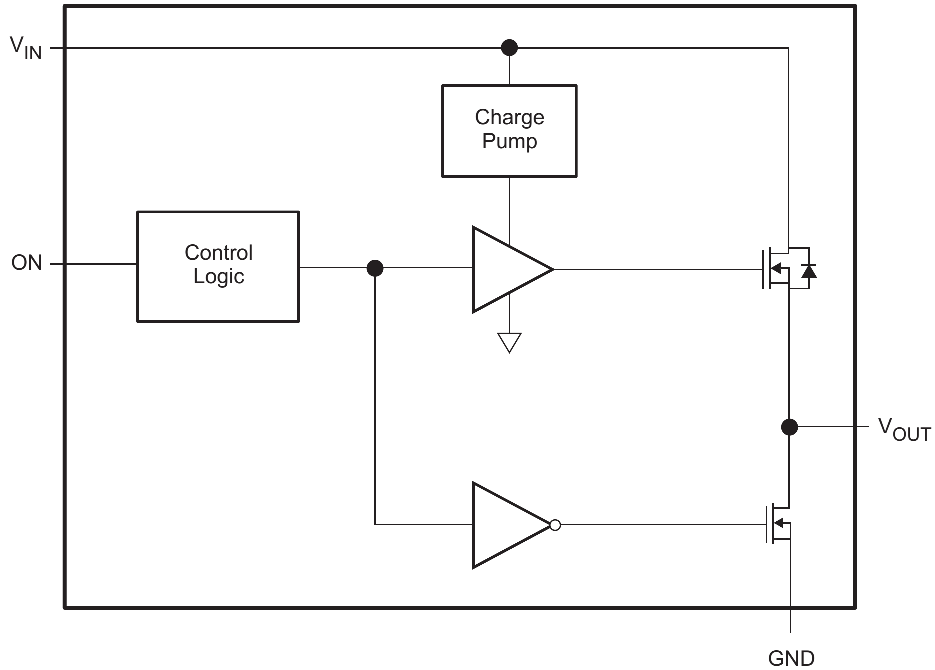
TERMINALS ASSIGNMENTS (YZP PACKAGE)

C	GND	ON
B	VOUT	VIN
A	VOUT	VIN
	1	2

TERMINAL FUNCTIONS

NO.	NAME	DESCRIPTION
C1	GND	Ground
C2	ON	Switch control input, active high. Do not leave floating
A1, B1	VOUT	Switch output
A2, B2	VIN	Switch input, bypass this input with a ceramic capacitor to ground

BLOCK DIAGRAM



FUNCTION TABLE

ON (Control Signal)	VIN to VOUT	VOUT to GND(1)
L	OFF	ON
H	ON	OFF

(1) See application section *Output Pulldown*.

ABSOLUTE MAXIMUM RATINGS[1]

			MIN	MAX	UNIT
V_{IN}	Input voltage range		–0.3	4	V
V_{OUT}	Output voltage range			V_{IN} + 0.3	V
V_{ON}	Input voltage range		–0.3	4	V
I_{MAX}	Maximum continuous switch current, T_A = -40°C to 85°C			2	A
I_{PLS}	Maximum pulsed switch current, 100-µs pulse, 2% duty cycle, T_A = -40°C to 85°C			4	A
T_A	Operating free-air temperature range		–40	85	°C
T_{stg}	Storage temperature range		–65	150	°C
ESD	Electrostatic discharge protection	Human-Body Model (HBM)		5000	V
		Charged-Device Model (CDM)		1000	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	T_A < 25°C	T_A = 70°C	T_A = 85°C
High-K[1]	YZP	17.6°C/W	123.36°C/W	- 8.1063 mW/°C	810.63 mW	445.84 mW	324.25 mW

(1) The JEDEC high-K (2s2p) board used to derive this data was a 3- × 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{IN}	Input voltage		0.75	3.6	V
V_{OUT}	Output voltage			V_{IN}	V
V_{IH}	High-level input voltage, ON	V_{IN} = 2.5 V to 3.6 V	1.2	3.6	V
		V_{IN} = 0.75 V to 2.5 V	0.9	3.6	
V_{IL}	Low-level input voltage, ON	V_{IN} = 2.5 V to 3.6 V		0.6	V
		V_{IN} = 0.75 V to 2.49 V		0.4	
C_{IN}	Input capacitance		1[1]		µF

(1) See the *Input Capacito*r section in Application Information.

ELECTRICAL CHARACTERISTICS

V_{IN} = 0.75 V to 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP(1)	MAX	UNIT
I_{IN}	Quiescent current	I_{OUT} = 0, V_{IN} = V_{ON}	V_{IN} = 3.6 V	Full		75	160	µA
			V_{IN} = 2.5 V			42	70	
			V_{IN} = 1.8 V			50	350	
			V_{IN} = 1.2 V			95	200	
			V_{IN} = 1.0 V			65	110	
			V_{IN} = 0.75 V			35	70	
$I_{IN(LEAK)}$	OFF-state supply current	V_{ON} = GND, OUT = 0V		Full			3.5	µA
r_{ON}	ON-state resistance	I_{OUT} = -200 mA	V_{IN} = 3.6 V	25°C		18.3	19.7	mΩ
				Full			26.0	
			V_{IN} = 2.5 V	25°C		18.5	19.5	
				Full			25.8	
			V_{IN} = 1.8 V	25°C		19.6	21.8	
				Full			27.4	
			V_{IN} = 1.2 V	25°C		19.4	21.8	
				Full			28.0	
			V_{IN} = 1.0 V	25°C		20.3	21.2	
				Full			28.6	
			V_{IN} = 0.75 V	25°C		22.7	25.3	
				Full			34.8	
r_{PD}	Output pulldown resistance(2)	V_{IN} = 3.3 V, V_{ON} = 0, I_{OUT} = 3 mA		25°C		1250	1500	Ω
I_{ON}	ON-state input leakage current	V_{ON} = 0.75 V to 3.6 V or GND		Full			0.1	µA

(1) Typical values are at V_{IN} = 3.3 V and T_A = 25°C.
(2) See Output Pulldown in *Application Information*.

SWITCHING CHARACTERISTICS

V_{IN} = 3.6 V, T_A = 25°C (unless otherwise noted)

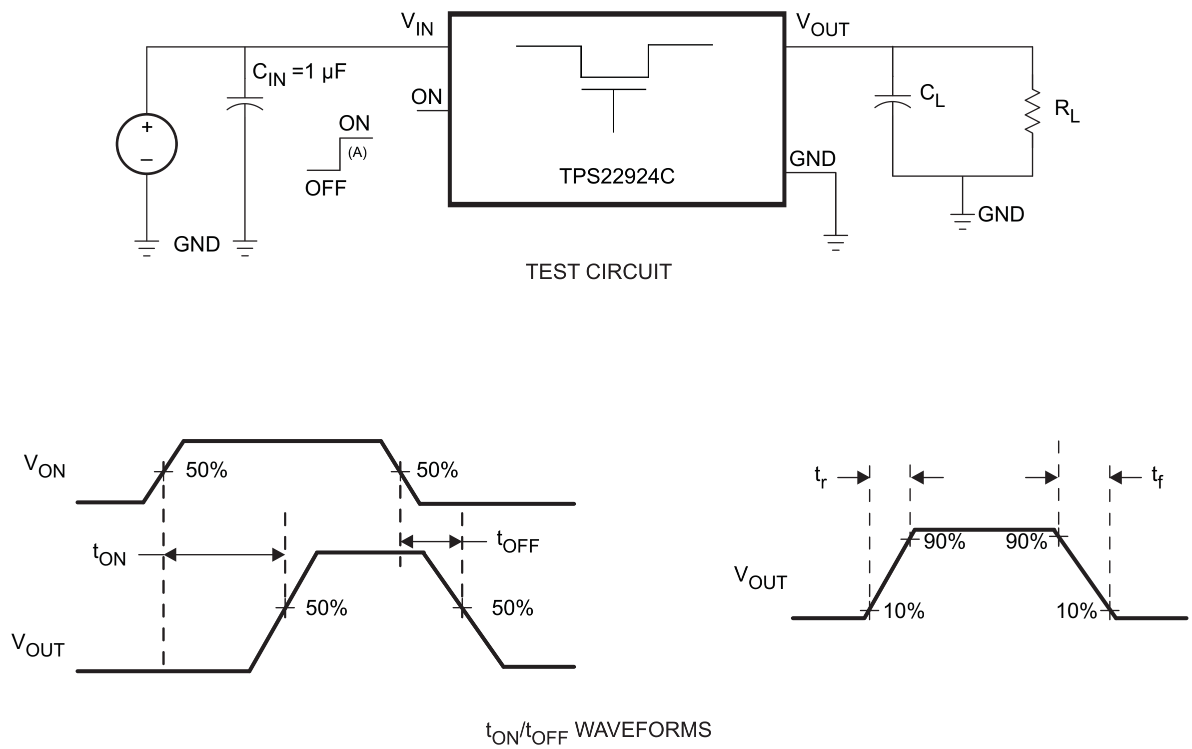
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turn-ON time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 3.6 V		800		µs
t_{OFF}	Turn-OFF time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 3.6 V		3		µs
t_r	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 3.6 V		800		µs
t_f	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 3.6 V		2.5		µs

SWITCHING CHARACTERISTICS

V_{IN} = 0.9 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turn-ON time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 0.9 V		865		µs
t_{OFF}	Turn-OFF time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 0.9 V		20		µs
t_r	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 0.9 V		500		µs
t_f	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 0.9 V		5		µs

PARAMETER MEASURMENT INFORMATION

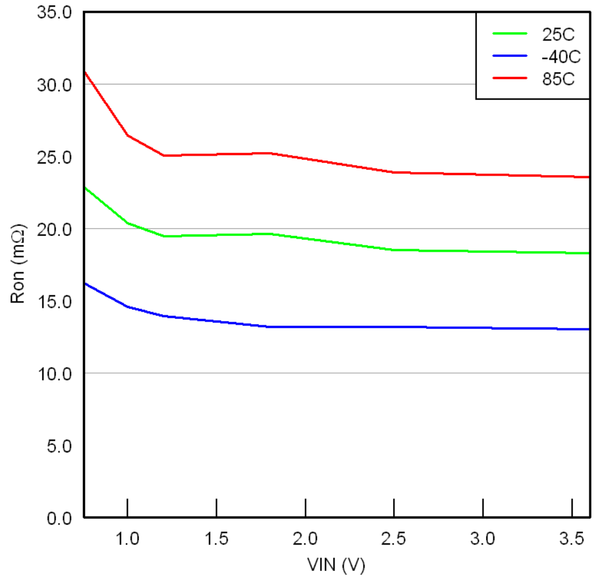


A. t_{rise} and t_{fall} of the control signal is 100 ns.

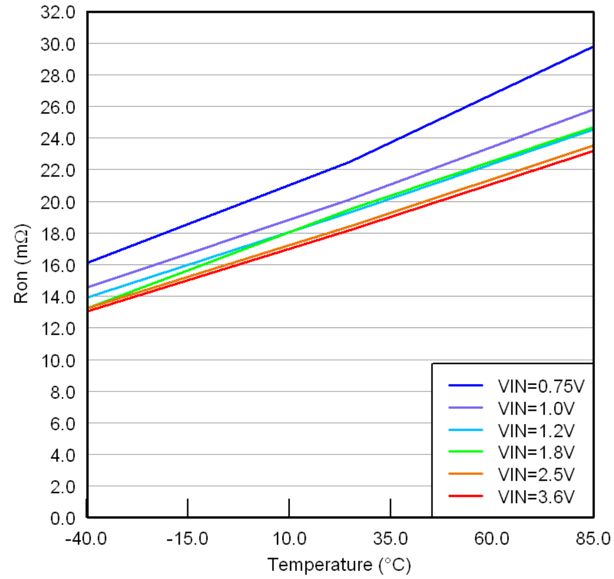
Figure 2. Test Circuit and t_{ON}/t_{OFF} Waveforms

TYPICAL CHARACTERISTICS

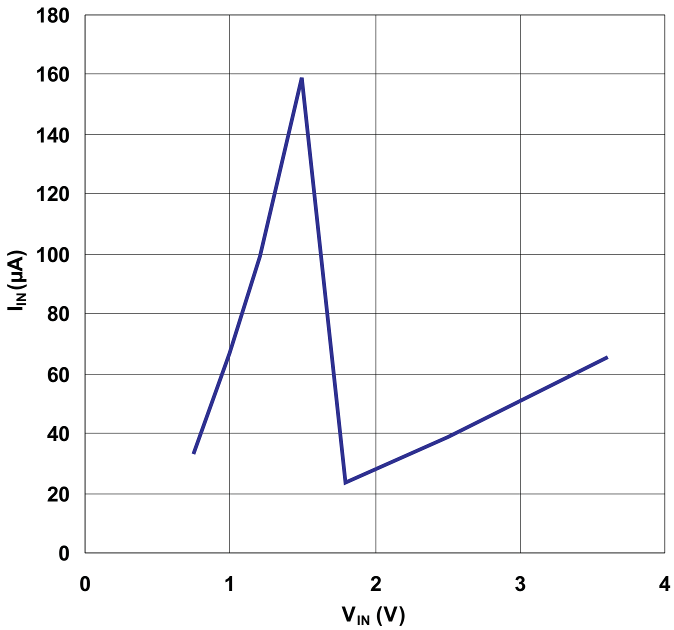
ON-STATE RESISTANCE vs INPUT VOLTAGE



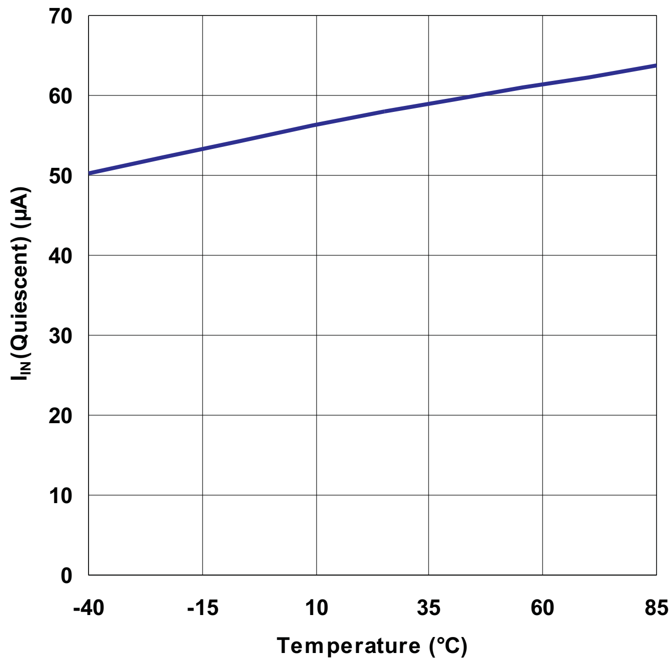
ON-STATE RESISTANCE vs TEMPERATURE



INPUT CURRENT, QUIESCENT vs INPUT VOLTAGE

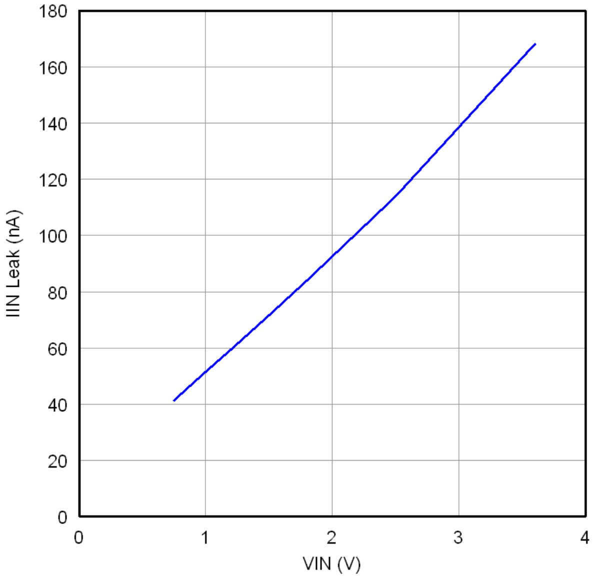


INPUT CURRENT, QUIESCENT vs TEMPERATURE

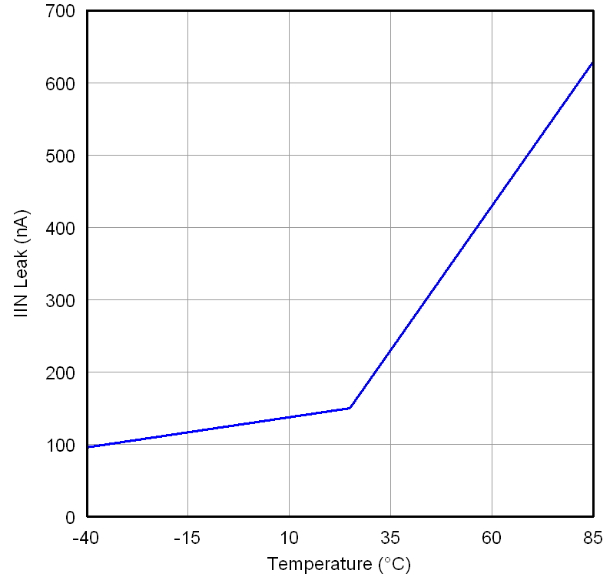


TYPICAL CHARACTERISTICS (continued)

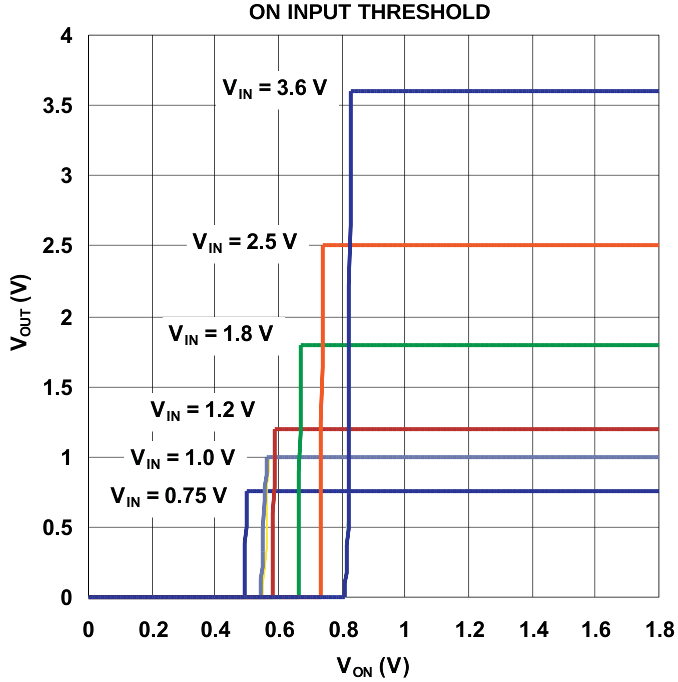
INPUT CURRENT, LEAK vs INPUT VOLTAGE



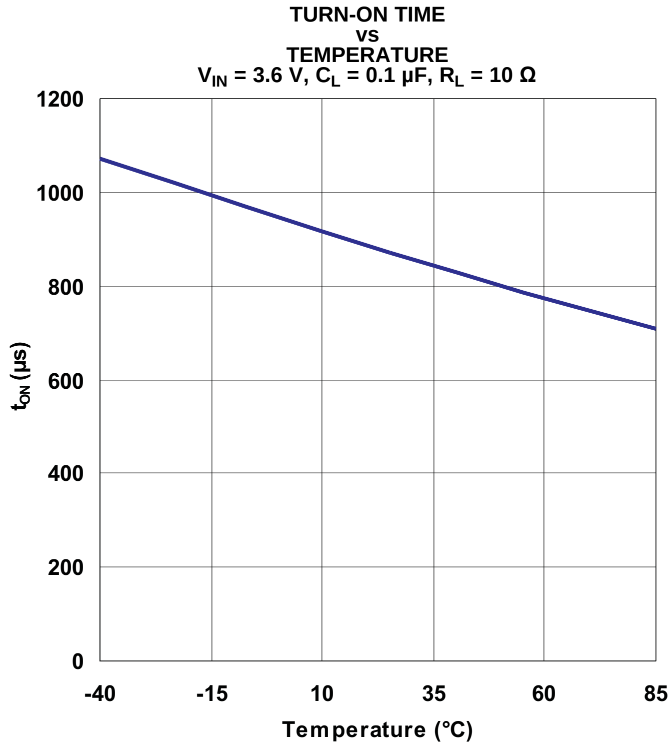
INPUT CURRENT, LEAK vs TEMPERATURE VIN = 3.6V

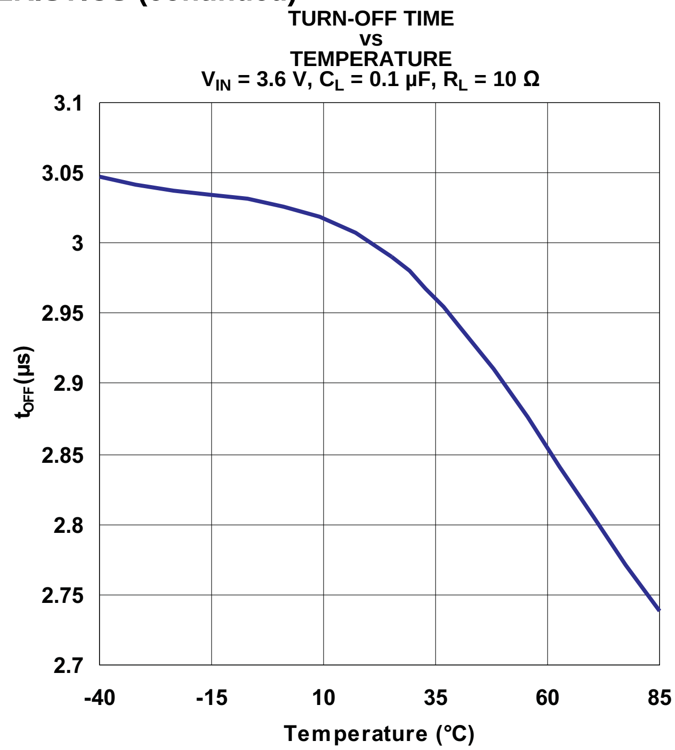


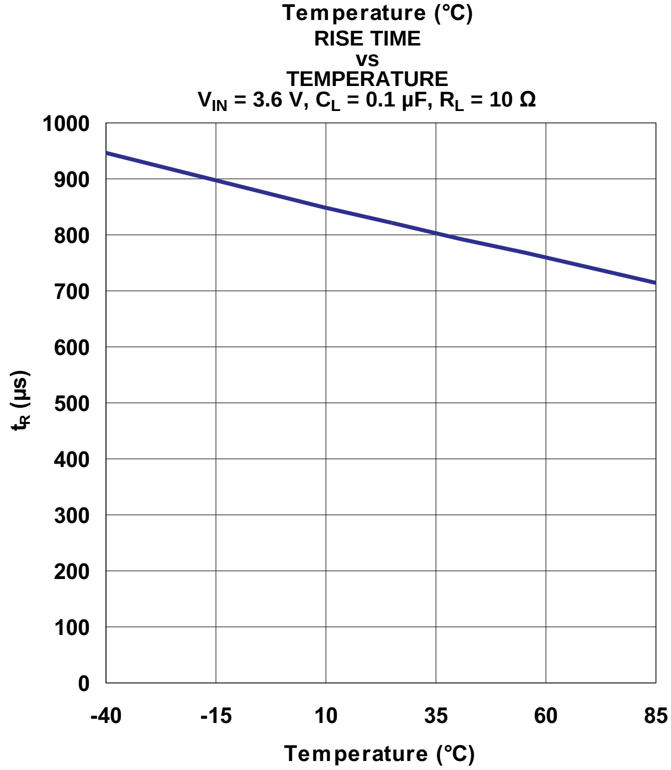
ON INPUT THRESHOLD

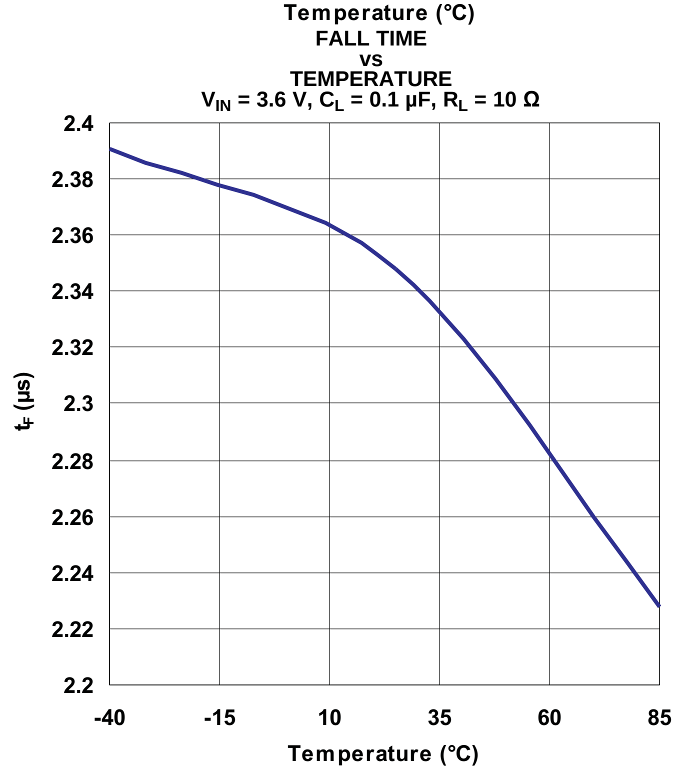


TYPICAL CHARACTERISTICS (continued)



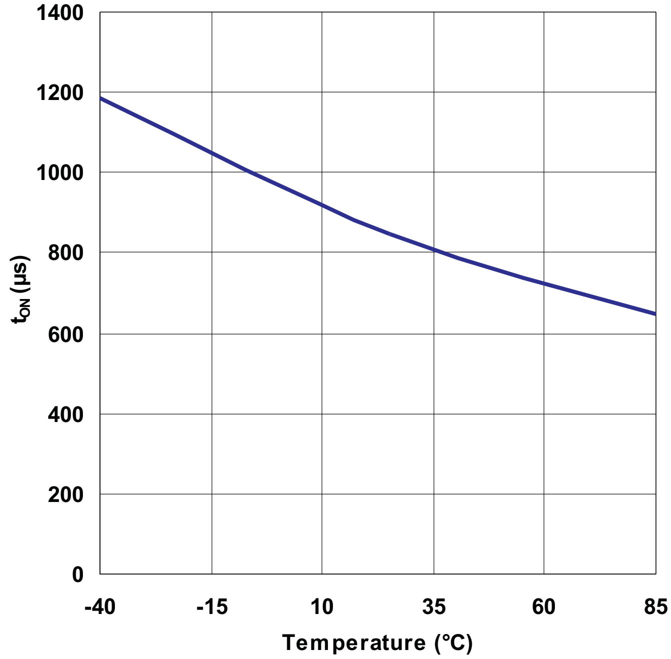




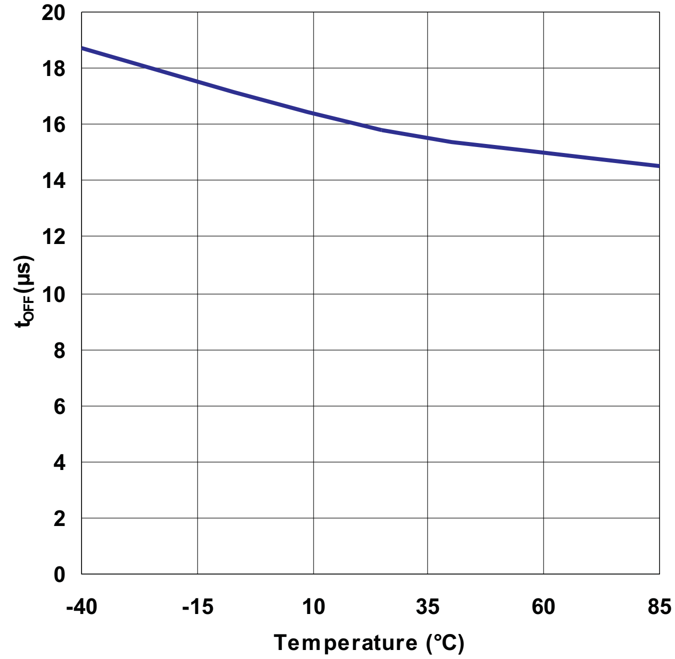


TYPICAL CHARACTERISTICS (continued)

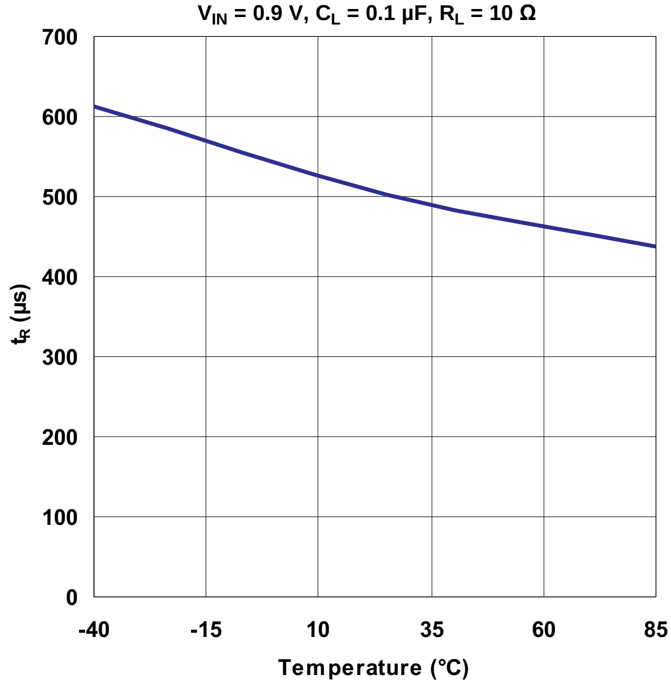
TURN-ON TIME vs TEMPERATURE
V_{IN} = 0.9 V, C_L = 0.1 µF, R_L = 10 Ω



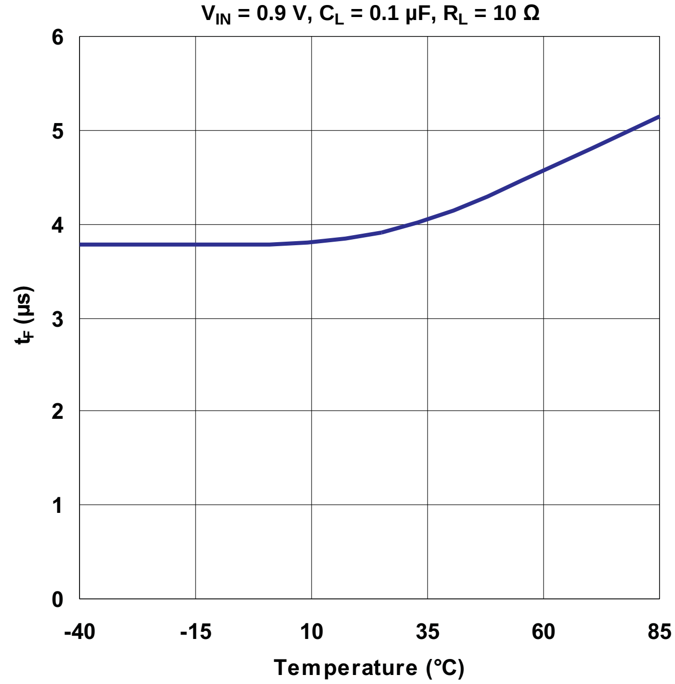
TURN-OFF TIME vs TEMPERATURE
V_{IN} = 0.9 V, C_L = 0.1 µF, R_L = 10 Ω



RISE TIME vs TEMPERATURE
V_{IN} = 0.9 V, C_L = 0.1 µF, R_L = 10 Ω

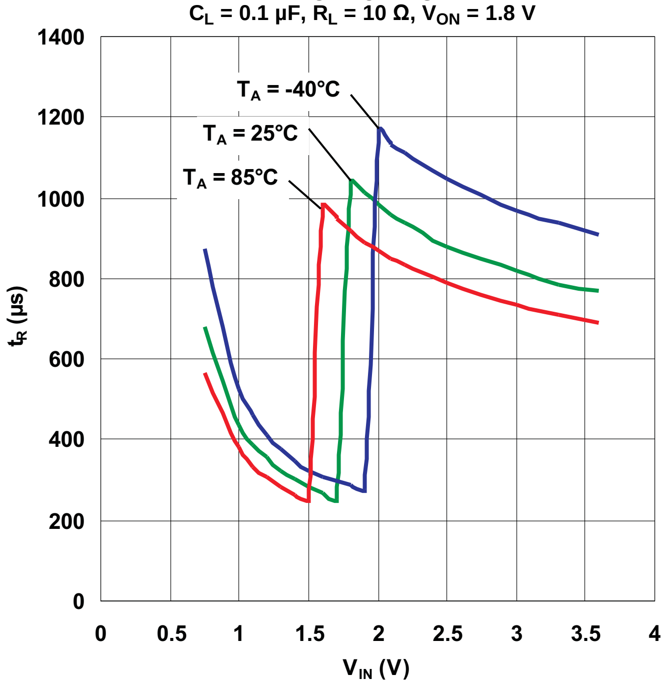


FALL TIME vs TEMPERATURE
V_{IN} = 0.9 V, C_L = 0.1 µF, R_L = 10 Ω

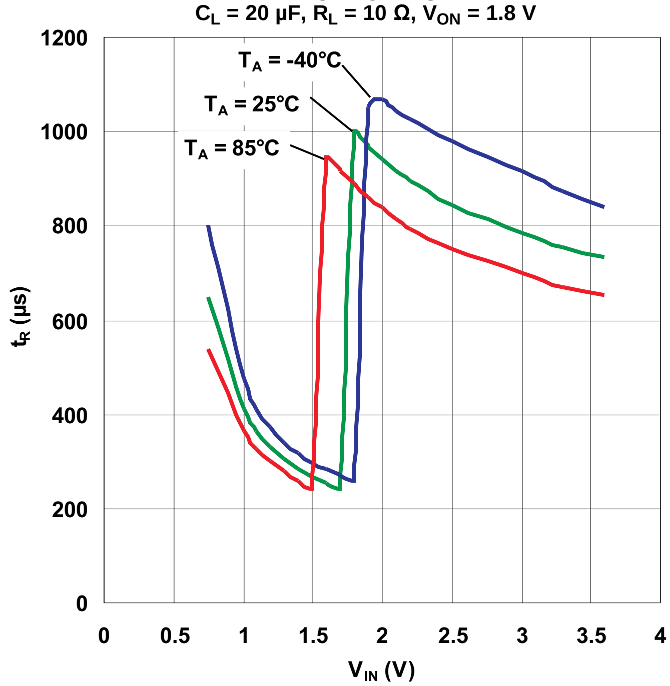


TYPICAL CHARACTERISTICS (continued)

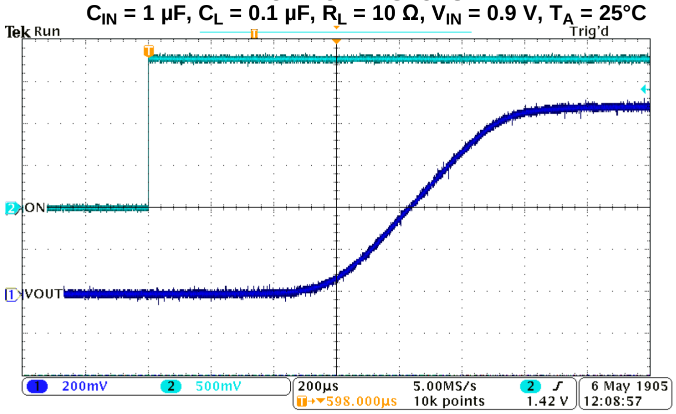
RISE TIME vs INPUT VOLTAGE
C_L = 0.1 µF, R_L = 10 Ω, V_{ON} = 1.8 V



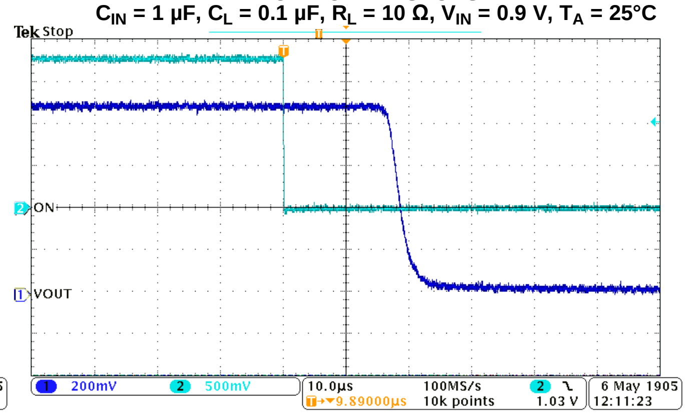
RISE TIME vs INPUT VOLTAGE
C_L = 20 µF, R_L = 10 Ω, V_{ON} = 1.8 V



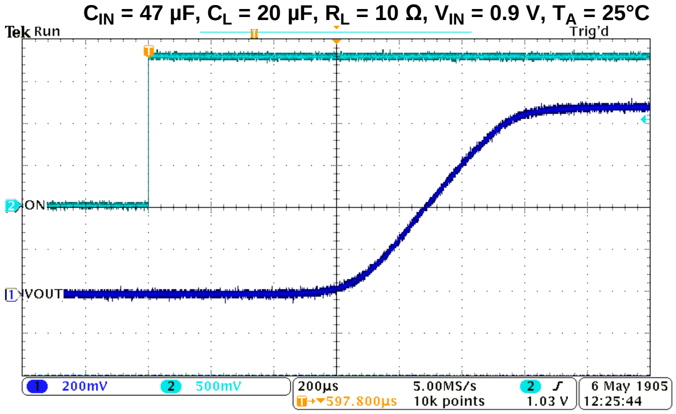
TURN-ON RESPONSE
C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, V_{IN} = 0.9 V, T_A = 25°C



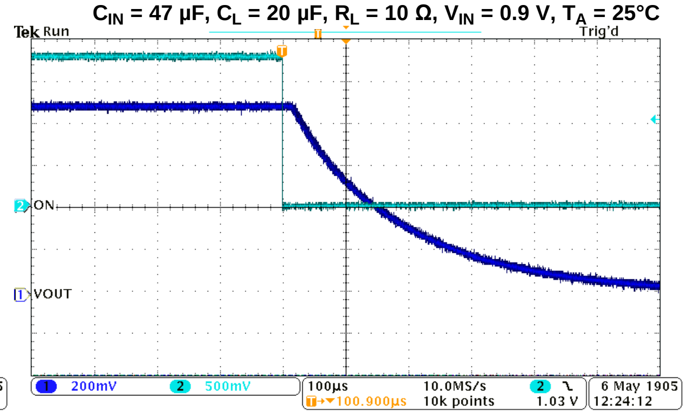
TURN-OFF RESPONSE
C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, V_{IN} = 0.9 V, T_A = 25°C



TURN-ON RESPONSE
C_{IN} = 47 µF, C_L = 20 µF, R_L = 10 Ω, V_{IN} = 0.9 V, T_A = 25°C

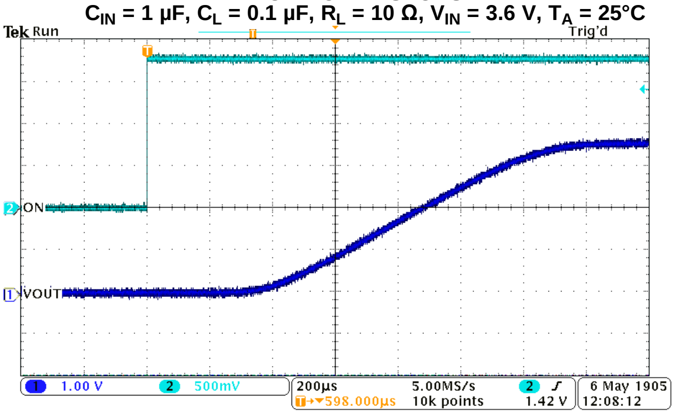


TURN-OFF RESPONSE
C_{IN} = 47 µF, C_L = 20 µF, R_L = 10 Ω, V_{IN} = 0.9 V, T_A = 25°C

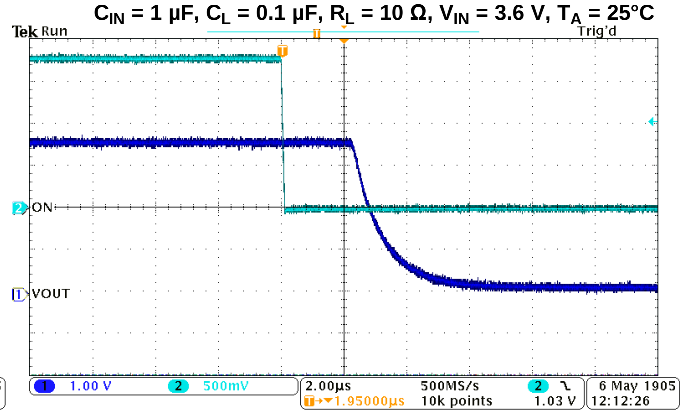


TYPICAL CHARACTERISTICS (continued)

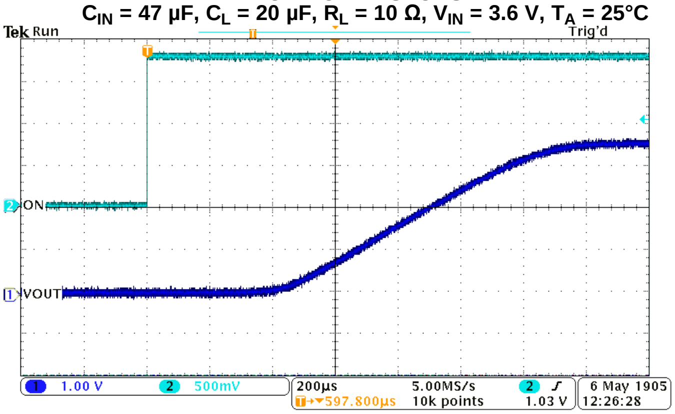
TURN-ON RESPONSE
C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, V_{IN} = 3.6 V, T_A = 25°C



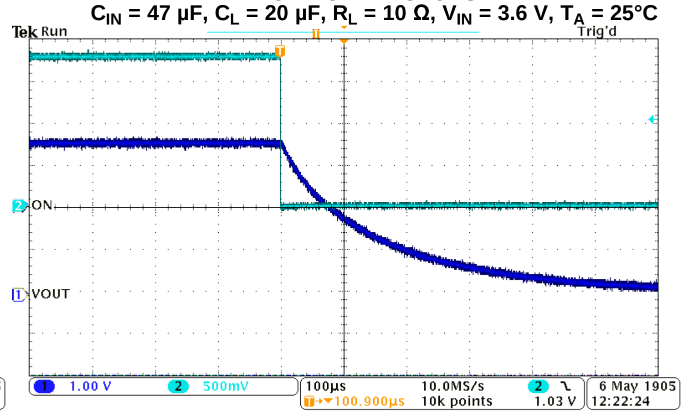
TURN-OFF RESPONSE
C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, V_{IN} = 3.6 V, T_A = 25°C



TURN-ON RESPONSE
C_{IN} = 47 µF, C_L = 20 µF, R_L = 10 Ω, V_{IN} = 3.6 V, T_A = 25°C



TURN-OFF RESPONSE
C_{IN} = 47 µF, C_L = 20 µF, R_L = 10 Ω, V_{IN} = 3.6 V, T_A = 25°C



APPLICATION INFORMATION

ON/OFF Control

The ON pin controls the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V or 3.3-V GPIOs.

Input Capacitor

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between V_{IN} and GND. A 1-μF ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop.

Output Capacitor

Due to the integral body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup.

Output Pulldown

The output pulldown is active when the user is turning off the main pass FET. The pulldown discharges the output rail to approximately 10% of the rail, then the output pulldown is automatically disconnected to optimize the shutdown current.

Board Layout

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for V_{IN}, V_{OUT}, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

REVISION HISTORY

Changes from Original (November 2009) to Revision A	Page
• Changed Ultra-Low ON Resistance list in Features	1
• Changed r_{ON} (TYP) in Feature List table from 5.7mΩ to 18.3mΩ.	1
• Changed block diagram to show a PMOS FET instead of an NMOS FET.	3
• Changed V_{IL} lower end V_{IN} value from (0.75 V to 2.5 V) to (0.75V to 2.49 V).	4
• Changed the way I_{IN} is specified.	5
• Changed the name of the parameter $I_{IN(OFF)}$ to $I_{IN(LEAK)}$. The test condition also changed from OUT = OPEN to OUT = 0V.	5
• Changed r_{ON} values.	5
• Changed Test Circuit diagram in the PARAMETER MEASURMENT INFORMATION section.	6
• Changed graphs in the TYPICAL CHARACTERISTICS section.	7

Changes from Revision A (May 2011) to Revision B	Page
• Changed parametric (MAX) values for I_{IN} Quiescent and $I_{IN(LEAK)}$.	5

Changes from Revision B (June 2011) to Revision C	Page
• Added new orderable part number to the ORDERING INFORMATION table.	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22924CYZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(5L ~ 5LG)	Samples
TPS22924CYZPRB	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5L	Samples
TPS22924CYZPT	ACTIVE	DSBGA	YZP	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(5LF ~ 5LG)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

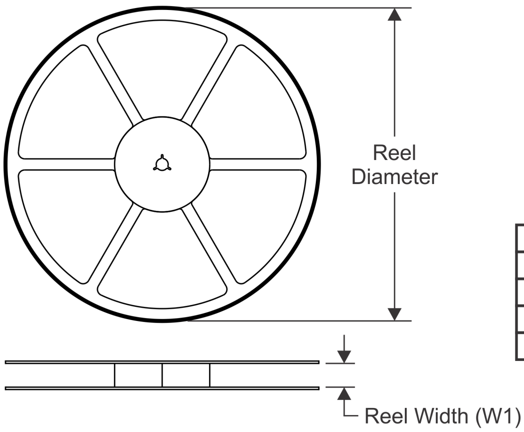
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

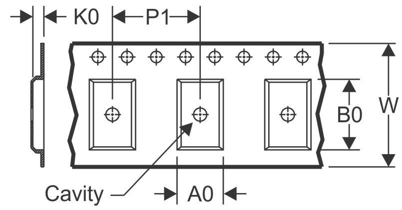
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

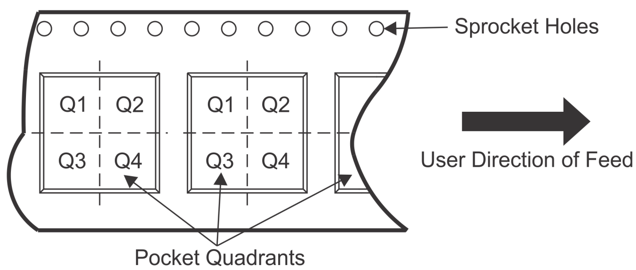


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

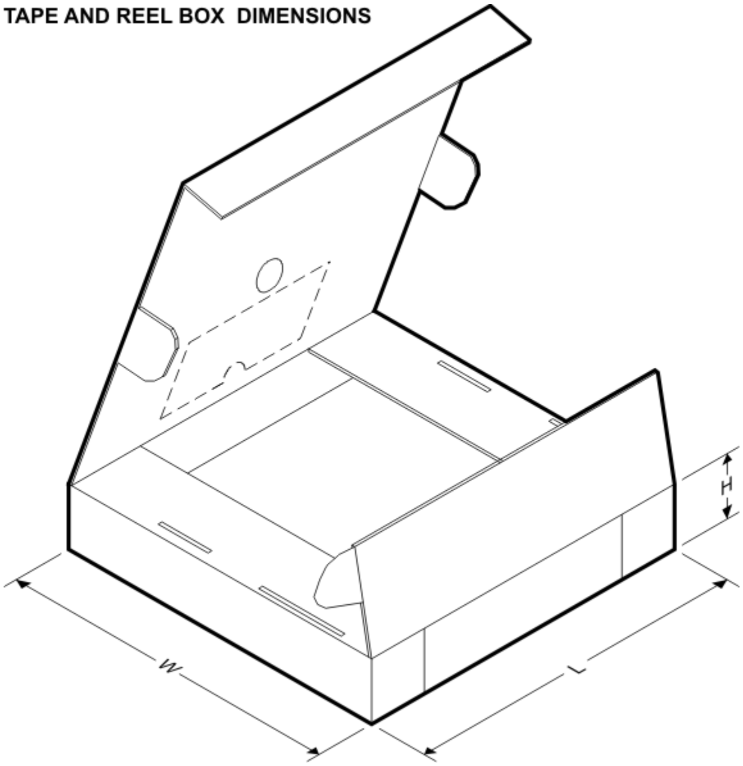
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22924CYZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
TPS22924CYZPRB	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
TPS22924CYZPT	DSBGA	YZP	6	250	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

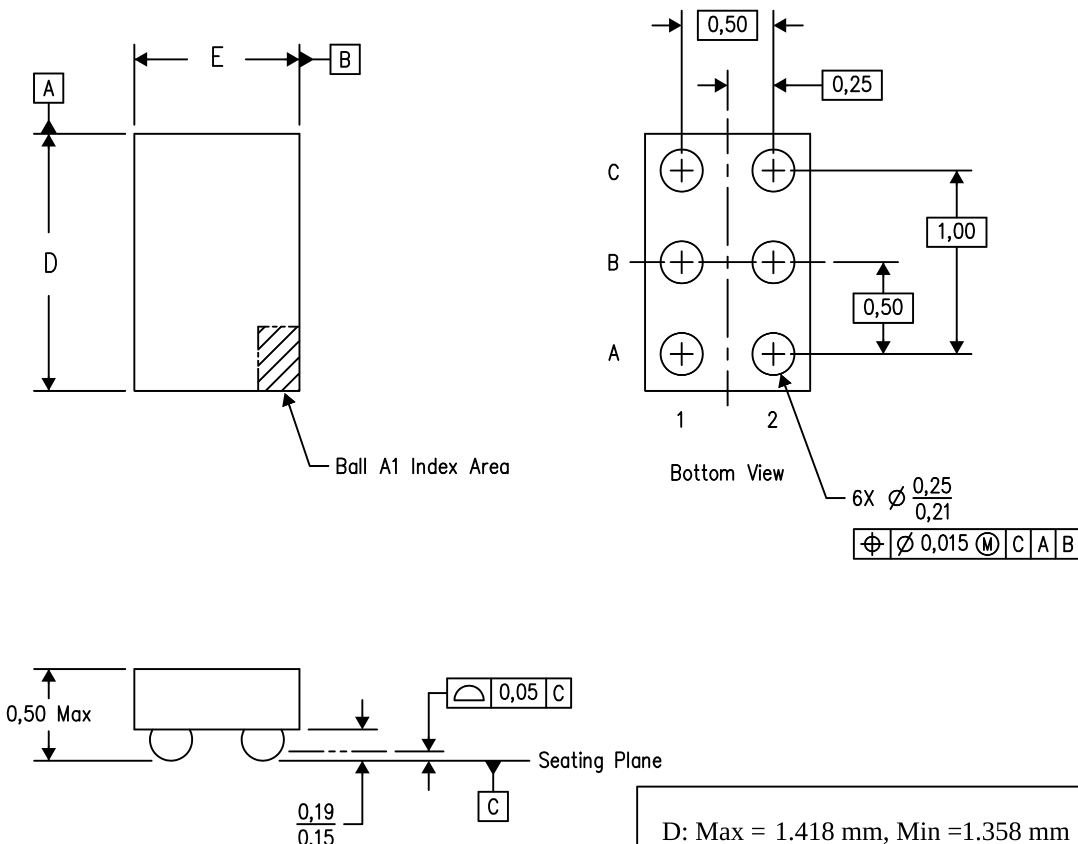
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22924CYZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0
TPS22924CYZPRB	DSBGA	YZP	6	3000	220.0	220.0	35.0
TPS22924CYZPT	DSBGA	YZP	6	250	220.0	220.0	35.0

YZP (R–XBGA–N6) DIE–SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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