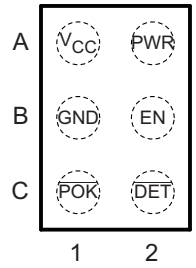
CURRENT-LIMITED 1-Ω SMART-LOAD SWITCH

Check for Samples: TPS22951

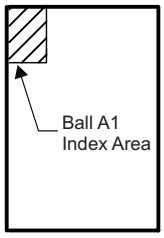
FEATURES

- **1-Ω P-Channel MOSFET**
- **300-mA Continuous Source Current**
- **Thermal and Short-Circuit Protection**
- **600-mA Current Limit**
- **Operating Range: V_{CC} = 2.8 V to 5.3 V**
- **41-µs Typical Rise Time**
- **10-µA Maximum Standby Supply Current**
- **Ambient Temperature Range: –40°C to 85°C**
- **ESD Performance Tested Per JESD 22**
  - **4000-V Human-Body Model (HBM)**
  - **400-V Machine Model (MM)**
  - **1000-V Charged-Device Model (CDM)**

YFP PACKAGE (TOP-THROUGH VIEW)



YFP PACKAGE (TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TPS22951 smart-load switch is intended for applications where heavy capacitive loads and short circuits are likely to be encountered. This device incorporates a 1-Ω P-channel MOSFET power switch for power distribution. The switch is controlled by a logic enable (EN) input and an accessory detect ($\overline{DET}$) pin. The switch is active when EN is high and $\overline{DET}$ is low. The switch is disabled if EN is low or $\overline{DET}$ is high. A low power state is achieved by driving EN high.

When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by increasing the on resistance of the power switch. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal-protection circuit shuts off the switch to prevent damage. The device recovers from a thermal shutdown once the device has cooled sufficiently, but the switch remains OFF until EN is toggled. This smart-load switch is designed to set current limit at 600-mA maximum.

TERMINAL FUNCTIONS

BALL		DESCRIPTION
NO.	NAME	
A1	V_{CC}	Supply voltage
A2	PWR	Power switch output
B1	GND	Ground
B2	EN	Enable input(1)
C1	$\overline{POK}$	Power OK switch status open-drain output, active low
C2	$\overline{DET}$	Accessory detect, active low

(1) $\overline{DET}$ must be low for a minimum of 2 µs before EN is pulled high (see Timing Requirements).

ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	WCSP – YFP	Tape and reel	TPS22951YFPR	_ _2W_(3)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) The actual top-side marking has two preceding characters to denote year, month, and one following character to designate the wafer fab/assembly site.

LOGIC DIAGRAM

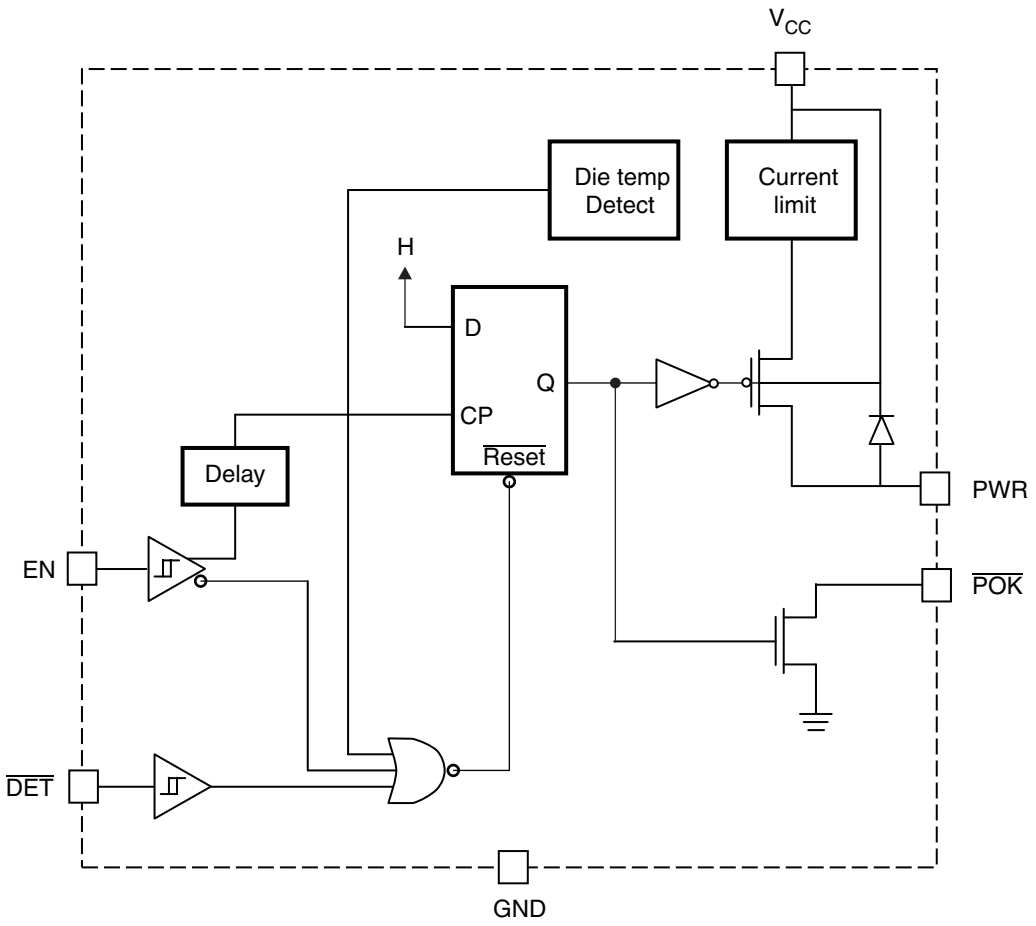


Table 1. FUNCTION TABLE

EN	$\overline{DET}$	CURRENT LIMIT	THERMAL LIMIT	POWER SWITCH (V_{CC} TO PWR)	$\overline{POK}$ (OPEN DRAIN)
0	X	Not exceeded	Not exceeded	OFF	Z
X	1	Not exceeded	Not exceeded	OFF	Z
1	0	Not exceeded	Not exceeded	ON	L
1	0	Exceeded	Not exceeded	ON – current limited	L
X	X	X	Exceeded(1)	OFF	Z

(1) In order to recover from a thermal event, the die temperature must first drop below the specified limit. EN must then be toggled in order to latch in the proper state of the flip-flop.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (2)		–0.3 V to 6 V
Output voltage range, $V_{O(PWR)}$ (2)		–0.3 V to V_{CC} + 0.3 V
Input voltage range, $V_{I(EN)}$, $V_{I(\overline{DET})}$		–0.3 V to 6 V
Voltage range, $V_{O(\overline{POK})}$		–0.3 V to 6 V
Continuous output current, $I_{O(PWR)}$		Internally limited
Continuous total power dissipation		See Dissipation Ratings
Operating virtual junction temperature range, T_J		–40°C to 85°C
Storage temperature range, T_{stg}		–65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 in) from case for 10 s		–0.3 V to 6 V
Electrostatic discharge (ESD) protection	Human-Body Model (HBM)	4000 V
	Machine Model (MM)	400 V
	Charged-Device Model (CDM)	1000 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.

DISSIPATION RATINGS

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
YFP-6	810 mW	–8.3 mW/°C	440 mW	310 mW

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
Supply voltage, V_{CC}	2.2	5.3	V
Input voltage, $V_{I(EN)}$, $V_{I(\overline{DET})}$	0	V_{CC}	V
Continuous output current, $I_{O(PWR)}$	0	–600	mA
Operating virtual junction temperature, T_J	–40	85	°C

ELECTRICAL CHARACTERISTICS

over operating –40°C ≤ T_J ≤ 85°C range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]			MIN	TYP	MAX	UNIT
Power Switch								
$r_{DS(on)}$	Static drain-source on-state resistance, 3-V operation	V_{CC} = 3 V, I_O = 0.3 A					1	Ω
t_r [2]	Rise time, output	V_{CC} = 5.3 V	C_L = 1 µF, R_L = 20 Ω	T_J = 25°C		41		µs
		V_{CC} = 2.8 V				6		
t_f [2]	Fall time, output	V_{CC} = 5.3 V	C_L = 1 µF, R_L = 20 Ω	T_J = 25°C		43		µs
		V_{CC} = 2.8 V				43		
	Leakage current	PWR connected to GND, $V_{I(EN)}$ = 0 V				1		µA
EN and $\overline{DET}$								
V_{IH}	High-level input voltage	2.8 V ≤ V_{CC} ≤ 5.3 V			1.35			V
V_{IL}	Low-level input voltage	2.8 V ≤ V_{CC} ≤ 5.3 V					0.45	V
I_I	Input current	$V_{I(EN)}$ or $V_{I(\overline{DET})}$ = 0 V or 5.3 V					1	µA
t_{on} [2]	Turn-on time (EN to PWR)	V_{CC} = 5.3 V	C_L = 1 µF, R_L = 20 Ω			42		µs
	Turn-on time (EN to $\overline{POK}$)		C_P = 15 pF, R_P = 10 kΩ			9.5		
t_{off} [2]	Turn-off time (EN to PWR)	V_{CC} = 5.3 V	C_L = 1 µF, R_L = 20 Ω			48		µs
	Turn-off time (EN to $\overline{POK}$)		C_P = 15 pF, R_P = 10 kΩ			47		
Current Limit								
I_{OS}	Short-circuit output current	V_{CC} = 2.8 V or 5.3 V, PWR connected to GND, Device enabled into short circuit			–0.3		–0.6	A
Supply Current								
	Supply current, enabled	No load on PWR, V_{CC} = 5.3 V, $V_{I(EN)}$ = V_{CC}, $V_{I(\overline{DET})}$ = V_{CC} or 0 V					100	µA
	Supply current, disabled	No load on PWR, V_{CC} = 5.3 V, $V_{I(EN)}$ = 0 V, $V_{I(\overline{DET})}$ = V_{CC} or 0 V					10	µA
$\overline{POK}$								
$V_{OL(\overline{POK})}$	Power OK output low voltage	$I_{(POK)}$ = 1 mA					0.4	V
	Off-state current	$V_{(POK)}$ = 5.3 V					1	µA
Thermal Shutdown								
	Thermal shutdown threshold[2]				135			°C
	Recovery from thermal shutdown[2]				125			°C
	Hysteresis[2]					25		°C

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) Not tested in production, specified by design

TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
t_{su}	Setup time, $\overline{DET}$ low before EN high	2		µs

TYPICAL CHARACTERISTICS

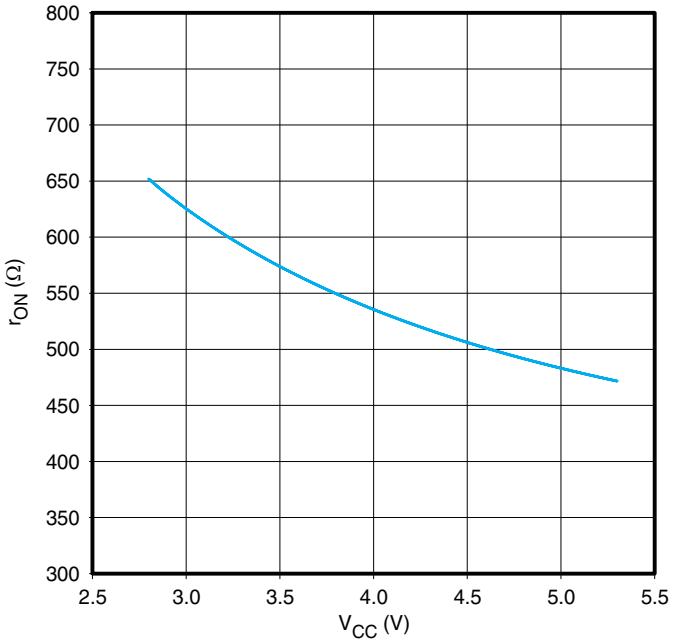


Figure 1. ON-State Resistance vs V_{CC}

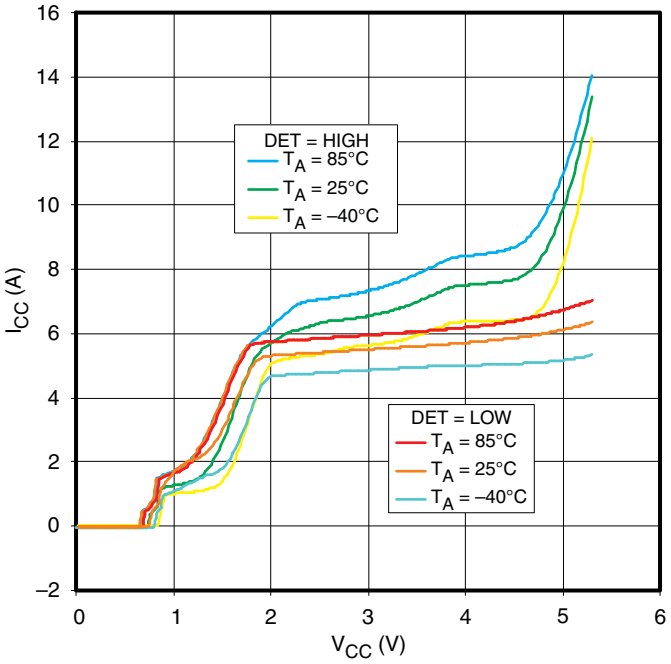


Figure 2. I_{CC} vs V_{CC}, EN = V_{CC}

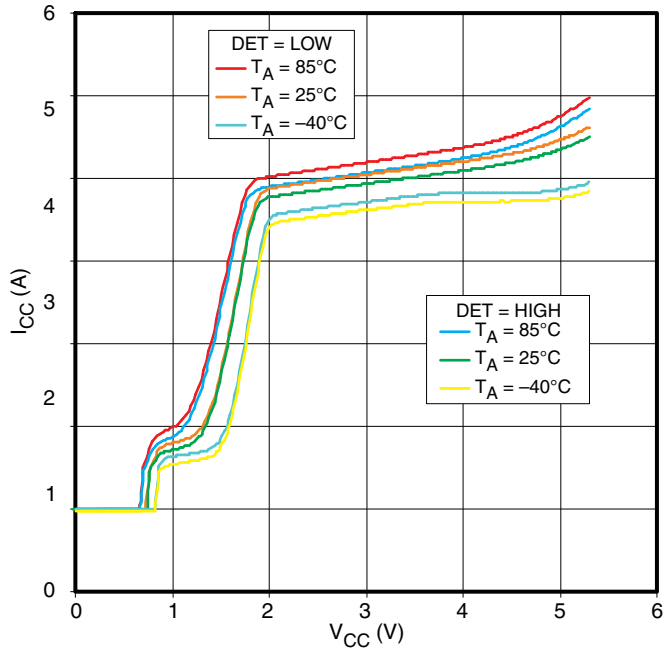


Figure 3. I_{CC} vs V_{CC}, EN = GND

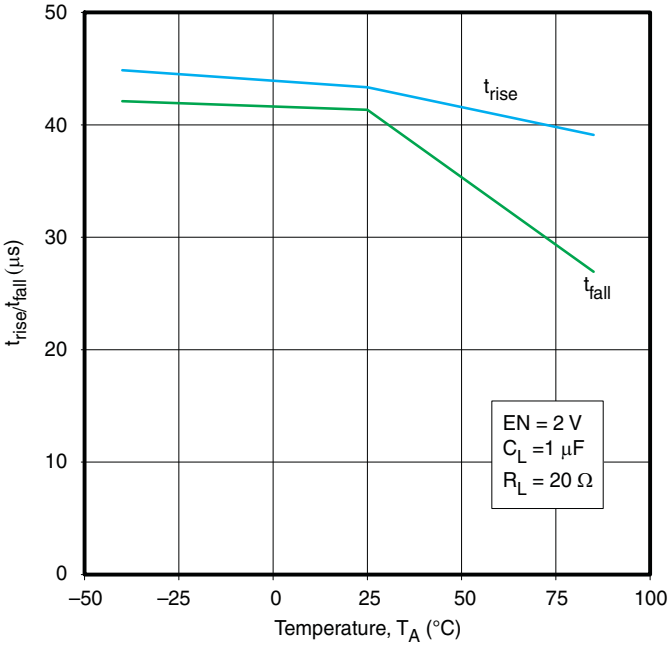


Figure 4. t_{rise}/t_{fall} vs Temperature, V_{CC} = 5.3 V

TYPICAL CHARACTERISTICS (continued)

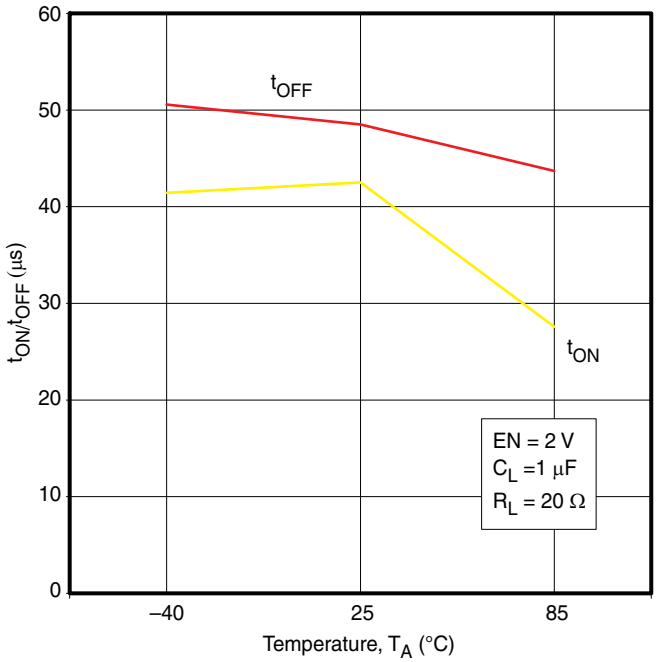


Figure 5. t_{ON}/t_{OFF} vs Temperature, V_{CC} = 5.3 V

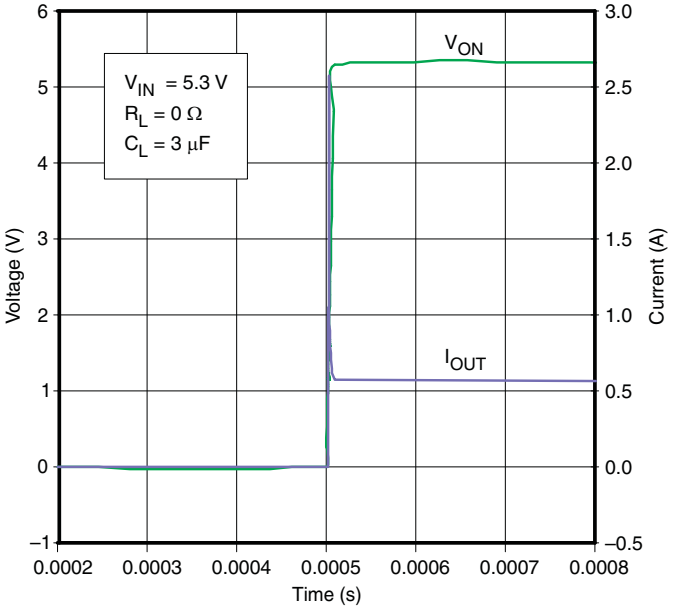


Figure 6. Device Enabled into Short Circuit

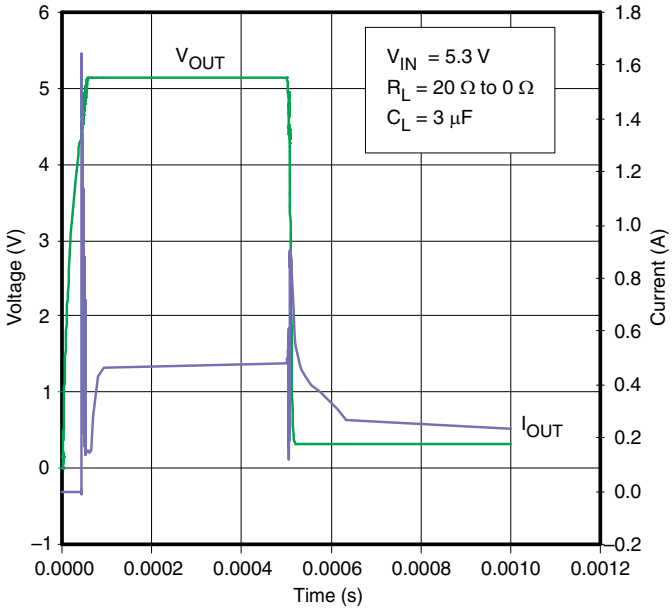


Figure 7. Full Load to Short-Circuit Transient Response

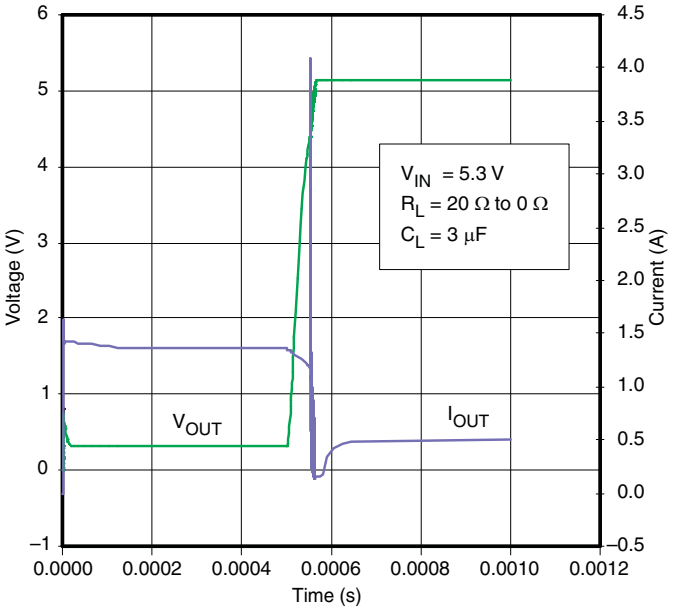


Figure 8. Short Circuit to Full-Load Recovery Response

TYPICAL CHARACTERISTICS (continued)

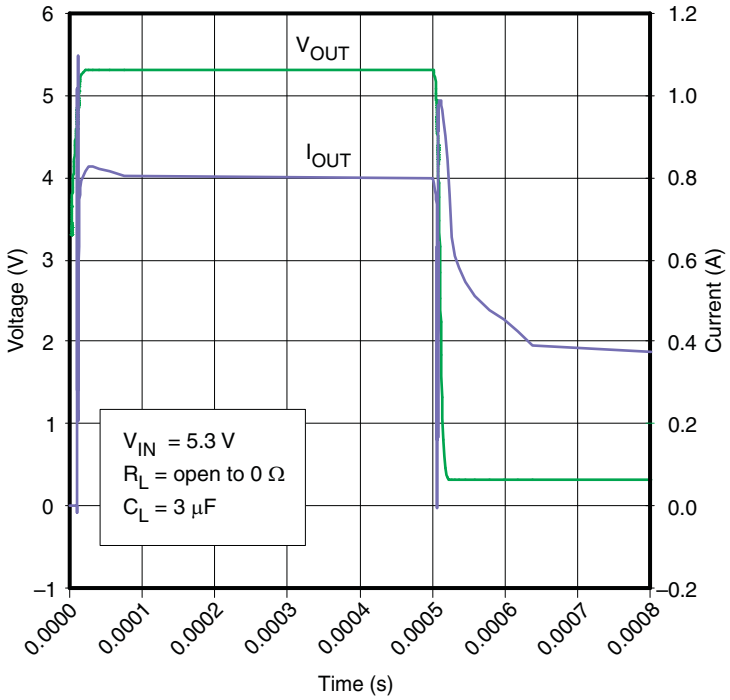


Figure 9. No Load to Short-Circuit Transient Response

PARAMETER MEASUREMENT INFORMATION

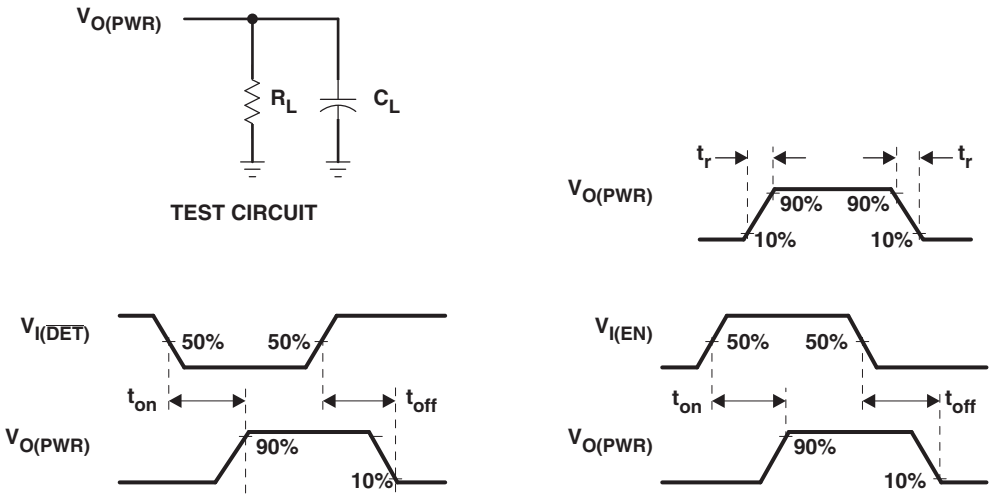


Figure 10. Test Circuit and Voltage Waveforms

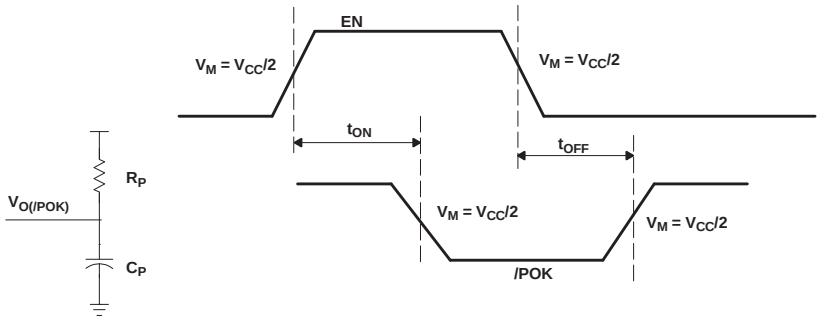


Figure 11. EN to $\overline{\text{POK}}$ Test Point

REVISION HISTORY

Changes from Revision A (March 2009) to Revision B	Page
• Updated TOP-SIDE MARKING in the ORDERING INFORMATION table.	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS22951YFPR	ACTIVE	DSBGA	YFP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(2W ~ 2W7)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

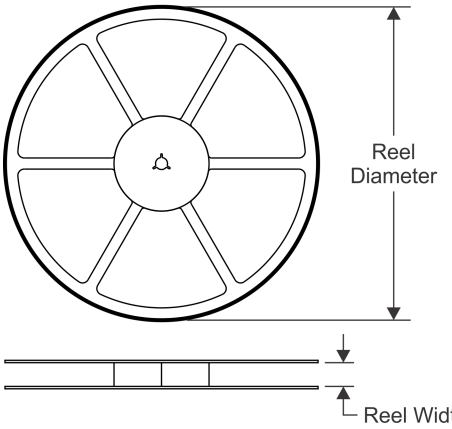
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

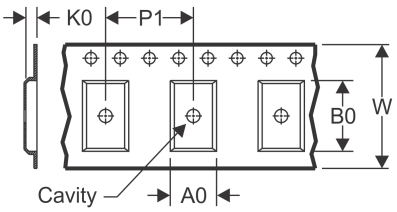
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

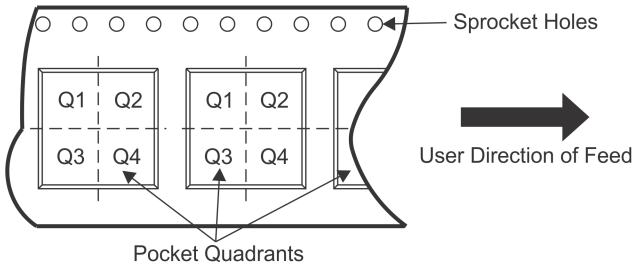


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

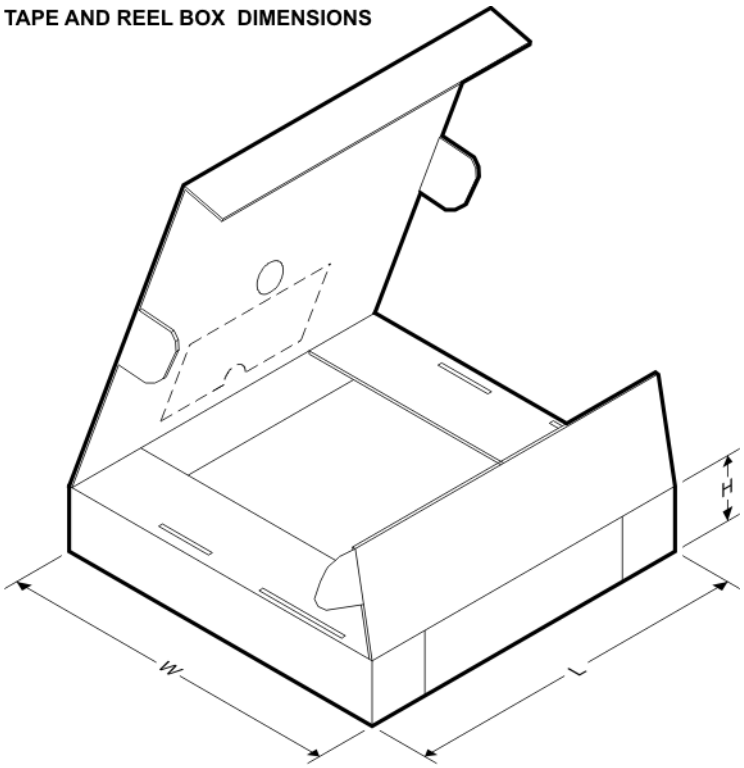
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22951YFPR	DSBGA	YFP	6	3000	180.0	8.4	0.9	1.3	0.6	4.0	8.0	Q1

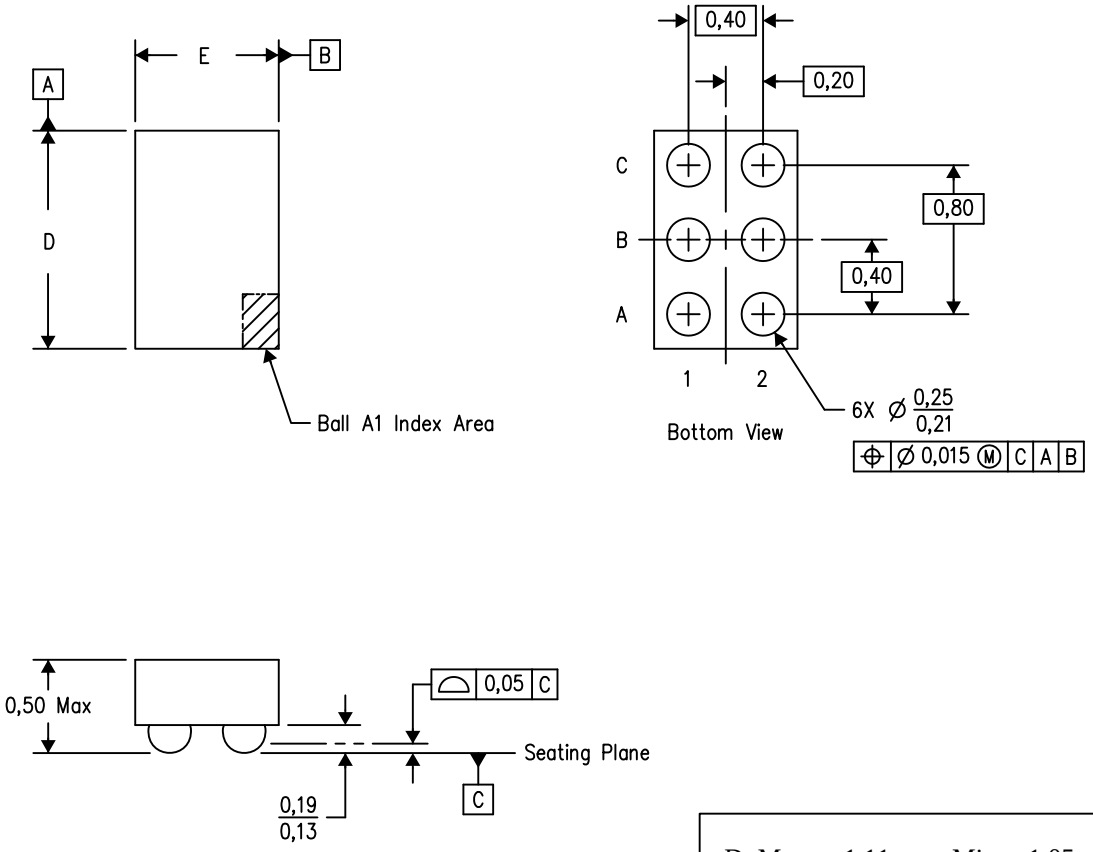
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22951YFPR	DSBGA	YFP	6	3000	220.0	220.0	34.0

YFP (R–XBGA–N6) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments

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